NOTE: This disposition is nonprecedential.

United States Court of Appeals for the Federal Circuit

SYNOPSYS, INC.,
Appellant

v.

ATOPTECH, INC.,
Appellee

2016-1956, 2016-1957

Appeals from the United States Patent and Trademark Office, Patent Trial and Appeal Board in Nos. IPR2014-01150, IPR2014-01159.

Decided: April 24, 2017

MATTHEW J. SILVEIRA, Jones Day, San Francisco, CA, argued for appellant. Also represented by KRISTA SCHWARTZ; GREGORY A. CASTANIAS, Washington, DC; DAVID B. COCHRAN, JOSEPH M. SAUER, Cleveland, OH; JOSHUA R. NIGHTINGALE, Pittsburgh, PA.

PHILIP WILLIAM MARSH, Arnold & Porter, LLP, Palo Alto, CA, argued for appellee. Also represented by PAUL ALEXANDER; SEAN MICHAEL CALLAGY, WILLOW WHITE NOONAN, San Francisco, CA.

Before LOURIE, MOORE, and HUGHES, *Circuit Judges.*

MOORE, *Circuit Judge*.

The present appeal arises from an inter partes review ("IPR") involving ATopTech, Inc. ("ATopTech") and Synopsys, Inc. ("Synopsys"). ATopTech petitioned for IPR of independent claims 1 and 32 of Synopsys' U.S. Patent No. 6,567,967 (the "'967 patent"). The Patent Trial and Appeal Board (the "Board") instituted IPR and held that claim 1 would have been obvious in light of the combination of Carol A. Fields, *Creating Hierarchy in HDL-Based High Density FGPA* [sic] *Design*, Euro-DAC '95, 594–99 (Sep. 18–22, 1995) ("Fields") and Hsiao-Pin Su, et al., *Performance-Driven Soft-Macro Clustering and Placement by Preserving HDL Design Hierarchy*, Proceedings, 1998 International Symposium on Physical Design: ISPD-98, 12–17 (April 8, 1998) ("Su").[1] The Board also found that Su anticipated claim 32. Synopsys appeals to our court. Because the Board's decision is not supported by substantial evidence, we *reverse*.

BACKGROUND

The '967 patent discloses a method for designing the layout of a large integrated circuit. There are two types of components relevant to this appeal—hard blocks and soft blocks (sometimes referred to as hard or soft "macros"). A hard block has predefined physical characteristics, such as shape, size, layout, and timing. '967 patent at 5:58–60. A soft block has an arbitrary shape, and its size is deter-

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[1] The Board also held that dependent claims 4, 8, 9, 12, 16, and 19–22 would have been obvious in light of the combination of Fields and Su. The challenged dependent claims rise or fall with independent claim 1.

mined by the number and size of smaller cells within it. *Id.* at 6:58–60.

The claimed method aims to improve circuit performance by splitting large components into smaller sub-components that can be designed individually, then optimizing the connections between sub-components. *Id.* at 2:44–49. One disclosed method is to remove levels of hierarchy in a logic tree. The bottom level of a tree is referred to as the "leaf level." *Id.* at 6:38. "Atomic blocks" sit above the leaf level. *Id.* at 6:35–39.

Claim 1 requires "flattening each of said plurality of hierarchically arranged branches by eliminating superfluous levels of hierarchy above said atomic blocks." The Board held that it was "persuaded based on the figures and accompanying text in both references, that one of ordinary skill in the art would have understood Fields and Su to teach or suggest the elimination of a level of hierarchy above the atomic blocks." J.A. 22. Claim 32 requires "determining optimal placement of each of the hard blocks, if any, within the predefined area." The Board found that Su expressly disclosed this limitation. J.A. 27. Synopsys appeals. We have jurisdiction pursuant to 28 U.S.C. § 1295(a)(4)(A).

DISCUSSION

We review the Board's legal conclusions de novo and its factual findings for substantial evidence. *Meiresonne v. Google, Inc.*, 849 F.3d 1379, 1382 (Fed. Cir. 2017). Anticipation is a question of fact we review for substantial evidence. *REG Synthetic Fuels, LLC v. Neste Oil Oyj*, 841 F.3d 954, 958 (Fed. Cir. 2016). Obviousness is a question of law based on underlying findings of fact. *Apple Inc v. Samsung Elecs. Co.*, 839 F.3d 1034, 1047 (Fed. Cir. 2016).

A. Claim 1

The Board concluded that "we are persuaded based on the figures and accompanying text in both references, that

one of ordinary skill in the art would have understood Fields and Su to teach or suggest the elimination of a level of hierarchy above the atomic blocks." J.A. 22. This determination is not supported by substantial evidence.

Fields discloses a method for organizing the hierarchical design structure of a FPGA. Figure 1 illustrates an example hierarchy:

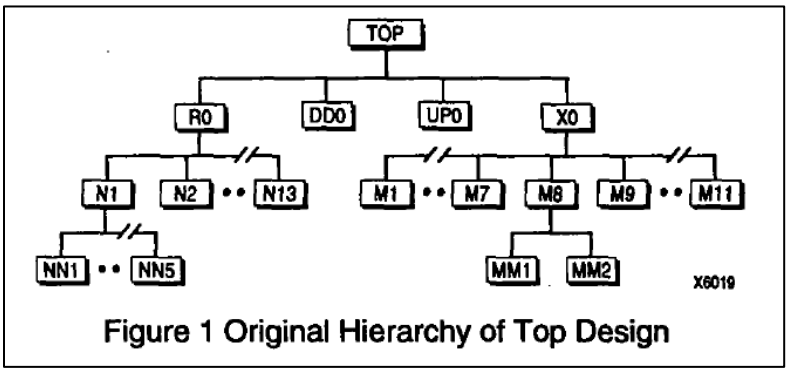

Figure 1 Original Hierarchy of Top Design

J.A. 1013. Fields teaches that blocks R0 and X0 contain a large number of nested blocks, so both should be divided into smaller groupings. It describes a reallocation process where R0 is transformed into four blocks R1–R4, and X0 is transformed into blocks X1 and X2. The nested blocks are divided among the new blocks. Figure 4 illustrates the resulting hierarchy:

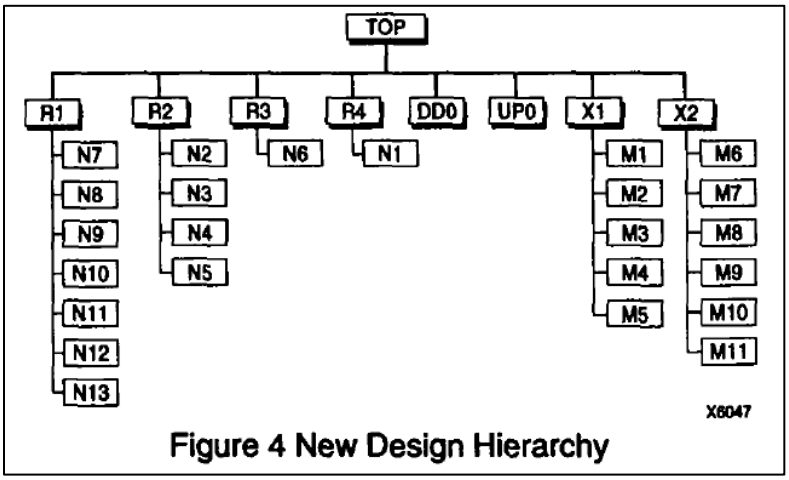

Figure 4 New Design Hierarchy

J.A. 1015.

Fields does not provide substantial evidence to support the Board's determination that Fields taught or suggested eliminating a superfluous level of hierarchy. ATopTech argues the removal of R0 and X0 discloses "flattening each of said plurality of hierarchically arranged branches by eliminating superfluous levels of hierarchy above said atomic blocks." Appellee's Br. 32–34. Not only does Fields fail to teach "flattening" and "eliminating superfluous levels of hierarchy," it teaches *expanding* the level ATopTech contends is removed. Fields teaches that blocks R0 and X0 are transformed into six new blocks: R1–R4, X1, and X2. The six new blocks remain on the same hierarchical level as the two original blocks. No levels are eliminated. Fields even teaches that a flatter design would be "difficult or impossible to route." J.A. 1013.

Su discloses a method for organizing soft macros on a circuit board. The Board cited two figures from the reference (Figures 2(b) and 3(a), reproduced below) as disclosing the elimination of superfluous levels:

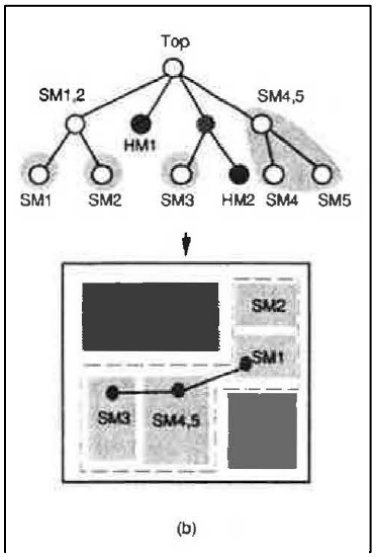

Figure 2(b)

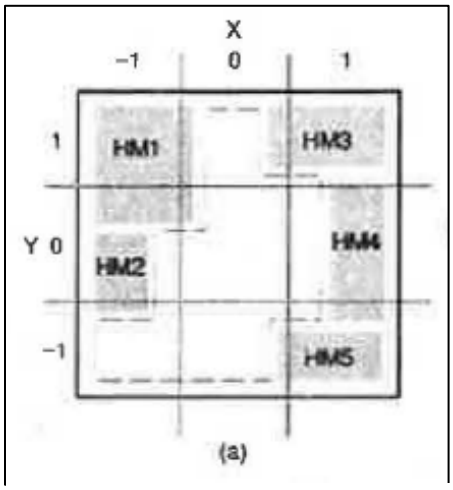

Figure 3(a)

J.A. 1019, 1021. The Board reasoned that "[i]n Figure 2(b) of Su, the two hard macros HM1 and HM2 are first shown at two different levels of the structural tree of the design, and then are depicted after soft macro formation [in Figure 3(a)] in the same layout plane, where each hard macro is assigned into its corresponding region." J.A. 22 (internal quotations omitted).

The cited disclosures from Su do not provide substantial evidence to support the Board's determination that Su teaches or suggests elimination of a level of hierarchy above the atomic blocks. Su provides no indication that Figure 3(a) illustrates the hard macro layout of the tree disclosed in Figure 2(b), nor does the Board articulate any. *See* J.A. 21–22. Su describes Figure 2(b) as "an example." J.A. 1019. When it later describes Figure 3(a), it does not refer to the prior example or structural tree illustrated in Figure 2(b). The figures themselves appear to be unrelated. Figure 2(b) only contains two hard macros (HM1 and HM2), while Figure 3(a) contains five

(HM1–5). There is no teaching that any superfluous levels are removed from Figure 2(b), nor is there any teaching that the disclosed tree structure is flattened.

Moreover, even if Su disclosed the elimination of hierarchical branch HM2, it still would not disclose the "flattening" required by claim 1. Claim 1 requires eliminating "superfluous levels of hierarchy above said atomic blocks." The claim requires atomic blocks to be "one or more hierarchy levels above the bottom" of a hierarchical tree. Because HM2 is located at the bottom level of the tree, it is not an atomic block. The atomic blocks must be at least one level higher. Therefore, it does not disclose eliminating levels of hierarchy *above* the atomic level.

Neither Fields nor Su nor the combination of both discloses or suggests flattening or eliminating a level of hierarchy. We reverse the Board's conclusion that claim 1 of the '967 patent would have been obvious in light of Fields and Su.

B. Claim 32

Claim 32 requires "determining optimal placement of each of the hard blocks." The Board found that Su expressly disclosed this limitation. It reasoned that Su teaches using a commercial floorplanner to place hard blocks, and Su teaches that its overall layout determination method is "performance-driven," so therefore Su teaches optimal placement of hard blocks. *See* J.A. 27. This finding is not supported by substantial evidence.

Su is focused entirely on the placement of soft blocks. This is reflected in its title ("Performance-Driven Soft-Macro Clustering . . .), abstract (referencing "soft-macros" three times in three sentences), conclusion ("We have presented a performance-driven soft-macro clustering . . .), and analysis throughout. Su discloses a method for creating and arranging soft blocks and testing chip performance based on the chosen soft-block layout. It

teaches a specific algorithm for determining the optimal size of a soft block, and it teaches a series of equations for determining the location of each soft block. It then describes the results of testing "without/with our proposed soft-macro clustering and placement method." J.A. 1022.

Su discloses very little about the placement of hard blocks. It only refers to hard blocks in teaching that "we use a commercial floorplanner to perform macro floorplanning to determine the locations of hard macros . . . ." and that "each hard-macro is assigned into its corresponding region according to the floorplanning result." J.A. 1019–20. ATopTech's expert, Dr. Ghiasi, testified that a skilled artisan would understand these teachings to disclose "determining optimal placement" of hard blocks because floorplanning is the process of determining the optimal placement of components in a circuit. The Board cited Dr. Ghiasi's testimony and found that "[o]ptimal hard block placement is consistent with the explicitly stated goals of Su's methodology." J.A. 27.

The Board's finding, that Su expressly discloses optimal hard block placement, is not supported by substantial evidence. Although Su discloses determining the optimal placement of soft blocks, it never discloses determining the optimal placement of hard blocks. The Board cites three disclosures where Su purportedly discloses optimal placement of hard blocks. *See* J.A. 27. Each of these disclosures, however, is limited to optimal placement of soft blocks. Su's title is "Performance-Driven *Soft-Macro* Clustering and Placement by Preserving HDL Design Hierarchy." J.A. 1018 (emphasis added). Its abstract teaches "a performance-driven *soft-macro* clustering and placement method with preserves HDL design hierarchy to guide the *soft-macro* placement process." *Id*. (emphasis added). The "effectiveness of the proposed method" refers to "a *soft-macro* clustering and placement technique." *Id*. (emphasis added). Finally, the Board's reference to the "quality of soft macro placement" says nothing about the

placement of hard blocks. Every reference in Su to improved performance attributes that improved performance to its placement of soft blocks. We fail to see how a disclosure which repeatedly touts the value of optimizing the placement of soft blocks *expressly* discloses the claimed "optimal placement" of hard blocks.

ATopTech argues that because Su teaches a "performance-driven" method, the commercial floorplanner used to place hard blocks *must* place those blocks in their optimal location. This argument is inconsistent with the Board's findings. The Board found that although Su expressly anticipated claim 32, it did not inherently anticipate the claim. J.A. 27 n.2. This distinction is fatal to ATopTech's argument. A reference inherently anticipates a limitation only when it "must *necessarily* include the unstated limitation." *King Pharm., Inc. v. Eon Labs, Inc.*, 616 F.3d 1267, 1274 (Fed. Cir. 2010) (emphasis in original).

We reverse the Board's finding that Su anticipates claim 32 of the '967 patent.

CONCLUSION

The Board's decision that claims 1, 4, 8, 9, 12, 16, and 19–22 would have been obvious in light of Fields and Su and that Su anticipates claim 32 is *reversed*.

REVERSED

COSTS

Costs to Synopsys.