NOTE: This disposition is nonprecedential.

United States Court of Appeals for the Federal Circuit

ELBRUS INTERNATIONAL LIMITED,
Appellant

v.

SAMSUNG ELECTRONICS CO., LTD.,
Appellee

2017-1855

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2015-01524.

Decided: June 27, 2018

PHILIP P. MANN, Mann Law Group, Seattle, WA, for appellant.

NAVEEN MODI, Paul Hastings LLP, Washington, DC, for appellee. Also represented by STEPHEN BLAKE KINNAIRD, JOSEPH PALYS; JOSEPH JOHN RUMPLER, II, Palo Alto, CA.

Before REYNA, BRYSON, and HUGHES, *Circuit Judges*.

PER CURIAM.

Elbrus International Ltd. appeals from the final written decision in an inter partes review proceeding in which the Patent Trial and Appeal Board found claims 1, 2, 5, 6, and 9 of U.S. Patent No. 6,366,130 ("the '130 patent") to be invalid. *Samsung Elecs. Co., Ltd. v. Elbrus Int'l Ltd.*, No. IPR2015-01524, 2017 WL 379208 (P.T.A.B. Jan. 17, 2017). We affirm.

BACKGROUND

The '130 patent, entitled "High Speed Low Power Data Transfer Scheme," relates to a "high speed and lower power" complementary metal-oxide semiconductor ("CMOS") data transfer arrangement. The arrangement "includes two active pull up/pull down bus drivers, a differential bus that precharges to a specific voltage level and a latched differential sense amplifier that serves as a bus receiver." '130 patent, col. 1, ll. 24–28.

Claim 1 is the only independent claim. It recites:

> 1. A data transfer arrangement comprising:
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> two bus drivers;
>
> a voltage precharge source;
>
> a differential bus coupled to the bus drivers and to the voltage precharge source; a[n]d
>
> a latching sense amplifier coupled to the differential bus;
>
> wherein the latching sense amplifier comprises:
>
> a first stage including a cross-coupled latch coupled to a differential data bus; and
>
> an output stage coupled to an output of said first stage;

> wherein the output of the first stage is coupled to an input of the output stage; [and]
>
> wherein the differential bus and the differential data bus are precharge[d] to a voltage Vpr between Vdd and ground, where Vpr=K*Vdd, and K is a precharging voltage factor.

DISCUSSION

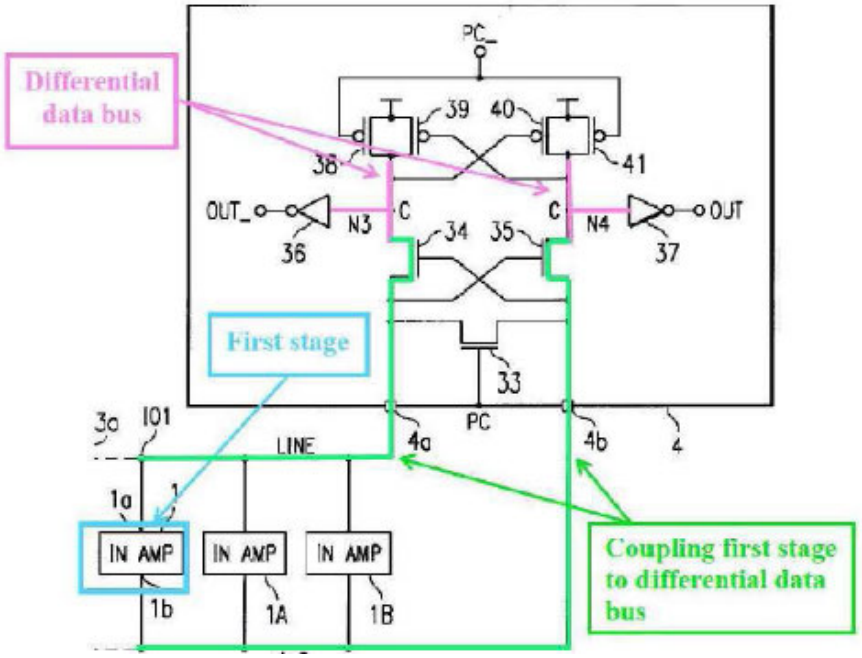
I

Elbrus argues that the Board adopted an erroneous construction of the claim term "bus." Adopting Samsung's proposal, the Board construed "bus" as "one or more conductors that are used for the transmission of signals, data, or power." *Samsung Elecs. Co.*, 2017 WL 379208, at *3. Elbrus contends that the Board should have adopted its proposed construction, i.e., "a common path along which power or signals travel from one or several sources to one or several destinations." *Id.* The meaning of the term "bus" bears on whether Samsung's lead prior art reference, U.S. Patent No. 5,828,241 ("Sukegawa"), discloses a "differential data bus," as recited in claim 1.

Although the Board adopted Samsung's construction, it concluded that Sukegawa discloses a "differential data bus" under both Samsung's and Elbrus's proposed constructions. *Id.* at *6–7. Because we find no error in the Board's conclusion, we need not address Elbus's arguments regarding the proper construction of "bus."

Sukegawa is entitled "Signal Transmission Circuit Providing Amplified Output from Positive Feedback of Intermediate Amplifier Circuit." It concerns "a type of signal transmission circuit wherein the signal is amplified and transmitted by means of the positive feedback of an intermediate amplifier circuit having input/output shared terminals." Sukegawa, col. 1, ll. 11–15.

As part of its petition, Samsung provided the following annotated excerpt of figure 1 of Sukegawa:



In the diagram, Samsung identified the differential data bus as the lines associated with nodes N3 and N4 (also labeled C), which connect the transistors 38–41 to the transistors 34 and 35 as well as to CMOS inverters 36 and 37. *See* Sukegawa, col. 8, ll. 49–53.

The Board found that those lines disclosed a differential data bus under both Samsung's and Elbrus's proposed constructions. The Board noted that Sukegawa "discloses a 'signal transmission circuit,' wherein a signal is transmitted to receiver circuit 4 containing output terminals OUT and OUT_." *Samsung Elecs. Co.*, 2017 WL 379208, at *6 (citing Sukegawa, col. 9, ll. 4–24). Those lines carry electrical signals from the transistors to the inverters, a function that satisfies Samsung's construction of bus as "one or more conductors that are used for the transmission of signals, data, or power." *Id.* (citing Sukegawa, col. 8, ll. 59–64; col. 9, ll. 4–7; col. 9, ll. 14–24).

The Board also found that the portion of figure 1 identified by Samsung satisfies Elbrus's construction of "bus." Citing the figure and expert testimony, the Board found that figure 1 shows "a finite, non-zero distance between transistors 34 and 35 and inverters 36 and 37, respectively, and discloses transmitting from one portion of the circuit to another portion." *Id.* at *7. From this, the Board concluded that Sukegawa discloses a "bus" even under Elbrus's construction of "a common path along which power or signals travel from one or several sources to one or several destinations." *Id.*

We find no error in the Board's analysis. On appeal, Elbrus argues that Sukegawa's nodes have "no non-trivial distance" and that there is no "transmission of signals, data, or power" over those lines. Neither argument is persuasive. As to the first, the Board cited testimony from both Samsung's and Elbrus's experts that a wire of some length would be needed to connect the transistors and the inverters, even if a person of ordinary skill would have been motivated to minimize the length of the wire. *Id.* at *6–7. Elbrus's argument that a "bus" must span a "non-trivial distance" is new on appeal; in any event, it is unpersuasive, as there is nothing in the patent to suggest that the claim language is limited to a bus of a certain minimum length. As to the second argument, Sukegawa's circuit 4, of which those identified lines are part, is a receiver that plays a role in signal transmission, *see* Sukegawa, col. 8, l. 49 to col. 9, l. 29, and that those lines therefore carry "signals, data, or power."

In sum, because Sukegawa discloses a "bus" under either Samsung's or Elbrus's construction, we affirm the Board's conclusion and need not reach Elbrus's other claim construction arguments.

II

Elbrus next challenges the Board's conclusion that claim 1's limitation of buses that are "precharge[d] to a

voltage Vpr between Vdd and ground" would have been obvious in light of Sukegawa and a 1984 article in the *IEEE Journal of Solid State Circuits* by Nicky Chau-Chun Lu & Hu H. Chao ("Lu"). The article, entitled "Half-V_{DD} Bit-Line Sensing Scheme in CMOS DRAM's," describes a sensing scheme in which the bit line is pre-charged to half V_{DD}. The article teaches that "the half-V_{DD} bit-line sensing scheme has several unique advantages, especially for high-performance high-density" CMOS Dynamic Random Access Memory ("DRAM"), "compared to the full-V_{DD} bit-line sensing scheme used for" N-type metal-oxide-semiconductor ("NMOS") memory arrays or "the grounded bit-line sensing scheme for" P-type metal-oxide-semiconductor ("PMOS") arrays in CMOS DRAM's.

Elbrus raises two arguments on appeal. First, Elbrus argues that Sukegawa teaches away from precharging the bus to half of the supply voltage, as taught in Lu. Elbrus argues that because Sukegawa used Vdd/2 precharging on a portion of his circuit but not on the differential data bus, this "strongly taught away from Vdd/2 precharging of the 'differential data bus.'"

The Board found that Sukegawa does not teach away from precharging the differential data bus to Vdd/2. *Samsung Elecs. Co.*, 2017 WL 379208, at *9. The Board noted that Elbrus "does not direct us to anything in Sukegawa that can be said to discourage a person of ordinary skill in the art from pre-charging to Vdd/2," and, to the contrary, "the record is replete with evidence demonstrating the advantages of precharging to a value below Vdd, as set forth in Lu, and those advantages would apply equally in the context of precharging the differential data bus." *Id.*

Whether a reference teaches away from the claimed invention is a question of fact, which is reviewed for substantial evidence. *Meiresonne v. Google, Inc.*, 849 F.3d 1379, 1382 (Fed. Cir. 2017). A reference "that 'merely

expresses a general preference for an alternative invention but does not criticize, discredit, or otherwise discourage investigation into' the claimed invention does not teach away." *Id.* (quoting *Galderma Labs., L.P. v. Tolmar, Inc.*, 737 F.3d 731, 738 (Fed. Cir. 2013)).

We conclude that substantial evidence supports the Board's factfinding that Sukegawa does not teach away from applying the teachings of Lu. As the Board found, nothing in Sukegawa discourages precharging a differential data bus to Vdd/2. At the oral hearing before the Board, when asked "is there anything in the disclosure of Sukegawa that we can look to to determine why he charged to Vdd as opposed to some intermediate charge," Elbrus's counsel responded, "I have not found anything that says exactly why he did that." Counsel then elaborated, saying that Sukegawa "doesn't say exactly why he's doing it. So we can only infer that he must have had a reason . . . . But it's not in Sukegawa. I admit that." Given that "a particular reference's mere silence about a particular feature does not tend to teach away from it," *In re Haase*, 542 F. App'x 962, 967 (Fed. Cir. 2013), the Board's conclusion that Sukegawa does not teach away from precharging a differential data bus to Vdd/2 is supported by substantial evidence.[1]

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[1] Elbrus's reliance on *In re Urbanski*, 809 F.3d 1237 (Fed. Cir. 2016), and *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339 (Fed. Cir. 2001), is misplaced. As stated in *Urbanski*, "[i]f references taken in combination would produce a seemingly inoperative device, . . . such references teach away from the combination and thus cannot serve as predicates for a prima facie case of obviousness." 809 F.3d at 1243 (quoting *McGinley*, 262 F.3d at 1354). However, the Board rejected Elbrus's argument that combining Sukegawa and Lu would lead to an unworkable circuit. Instead, the Board credited Samsung's ex-

Second, Elbrus argues that combining Lu with Sukegawa would lead to an inoperable circuit absent significant additional design work. However, "it is not necessary that [Sukegawa and Lu] be physically combinable to render [a claim] obvious." *Allied Erecting & Dismantling Co. v. Genesis Attachments, LLC*, 825 F.3d 1373, 1381 (Fed. Cir. 2016) (quoting *In re Sneed*, 710 F.2d 1544, 1550 (Fed. Cir. 1983)). That is so because "'[t]he test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference,' but rather whether 'a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention.'" *Id.* (quoting *In re Keller*, 642 F.2d 413, 425 (CCPA 1981), and *Pfizer, Inc. v. Apotex, Inc.*, 480 F.3d 1348, 1361 (Fed. Cir. 2007)). Therefore, Elbrus's argument that combining Sukegawa and Lu could lead to an unworkable circuit is "basically irrelevant." *In re Etter*, 756 F.2d 852, 859 (Fed. Cir. 1985) (en banc).

In any event, the Board's conclusion that any operability hurdles in modifying Sukegawa's circuit in view of Lu's teachings would be overcome by a person of ordinary skill is supported by substantial evidence. The Board, crediting Samsung's expert and discounting the testimony of Elbrus's expert, found that operability issues would arise only if "the modified Sukegawa system was designed poorly," and that a person of ordinary skill would have been able to make "simple adjustments" to the circuit to

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pert's testimony that only "simple adjustments" were necessary to ensure that "the circuit worked and didn't fail." *Samsung Elecs. Co.,* 2017 WL 379208, at *10. As discussed below, substantial evidence supports the Board's conclusion. Inoperability therefore is not a basis for finding that Sukegawa teaches away from applying Lu to obtain the claimed invention.

make it work.[2] *Samsung Elecs. Co.*, 2017 WL 379208, at *10. Elbrus's arguments on appeal do not provide a basis to disturb the Board's weighing of the expert evidence on that point, and we therefore affirm.

III

Finally, Elbrus argues that the Board erred in finding that claim 7 would have been obvious in light of the combination of Sukegawa with Lu and U.S. Patent No. 6,249,469 B1 ("Hardee"). Claim 7 depends from claims 1 and 2. Claim 2 adds to claim 1 that "the bus drivers comprise active pull-up and active pull-down bus drivers." Claim 7 then adds that "the active pull up and pull down bus drivers are NMOS transistors." According to the petition, Sukegawa discloses active pull down drivers that are NMOS transistors, but discloses PMOS transistors for the pull up drivers. As a result, Samsung relies on Hardee to show NMOS transistors as pull up and pull down drivers.

The Hardee patent, entitled "Sense Amplifier with Local Sense Drivers and Local Read Amplifiers," is directed to "a CMOS sense amplifier with local write driver transistors to eliminate the pattern sensitivities and delays of the prior art." Hardee, col. 4, ll. 58–60. The

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[2] Elbrus complains that the Board misapprehended the testimony of its expert, Dr. Huber, when the Board stated: "We have considered Dr. Huber's testimony that modifying Sukegawa in view of Lu *may* lead to 'power-wasting current paths.'" *Samsung Elecs. Co.*, 2017 WL 379208, at *10. Elbrus argues that Dr. Huber testified that the modification *would* lead to power-wasting current paths. In light of the fact that the Board credited Samsung's expert's opinion that simple modifications avoid this issue, any imprecision in the Board's paraphrase of Dr. Huber's testimony is inconsequential.

parties do not dispute that Hardee discloses NMOS pull up and pull down transistors. *See id.* at col. 6, ll. 28–46; *id.* at fig. 5.

The Board credited Samsung's argument that a person of ordinary skill would have been motivated to combine the teachings of Hardee with those of Sukegawa. *Samsung Elecs. Co.*, 2017 WL 379208, at *14–16. The Board agreed with Samsung that "substituting Hardee's NMOS pull up transistors for Sukegawa's PMOS pull up transistors would result in some area savings" on the circuit. *Id.* at *15. The Board noted that the parties disputed the magnitude of the space savings—Elbrus argued that the savings would be only 0.8%; Samsung argued that it would be 9%—but because it was "undisputed that modifying Sukegawa in view of Hardee would result in some reduction in layout size," the space-saving feature would have been a motivation to combine the two references. *Id.* In addition, the Board was persuaded by Samsung's argument that the combination would avoid latch-up, which is a type of short circuit. *Id.* at *16. Although Elbrus argued that "latch-up would not be a problem in Sukegawa's circuits" because the transistors "do not receive or drive off-chip signals," the Board credited Samsung's evidence that latch-up is "not limited to transistor circuits that drive external circuits." *Id.*

Elbrus makes three arguments on appeal. First, Elbrus argues that the space savings offered by combining Hardee with Sukegawa would be "trivial at best" and would "not provide a meaningful incentive to make the combination." The Board's conclusion that the space savings—whether 0.8% or 9%—would motivate a person of ordinary skill to combine the references is supported by substantial evidence. In particular, the Board found persuasive Samsung's expert's testimony that a reduction in layout size can be an important consideration in circuit design. *Id.* at *15.

Second, Elbrus contends that Sukegawa does not actually exhibit latch-up, so the asserted motivation to combine is illusory. Elbrus argues, as it did before the Board, that Sukegawa does not have a latch-up problem because all of the signals and transistors are on-chip. However, the Board found credible the testimony of Samsung's expert testimony and Samsung's other evidence that latch-up can occur in transistor circuits that drive internal circuits. That evidence included a 1998 article entitled "Understanding Latch-up in Advanced CMOS Logic," which explained that "[t]he cause of the latch-up exists in all junction-isolated or bulk CMOS processes." The Board's conclusion is therefore supported by substantial evidence.

Finally, Elbrus argues that the Board relied on a misapprehension of Dr. Huber's testimony. The "misapprehension" appears to have originated in Elbrus's own patent owner's response brief, in which Elbrus stated: "It would not have been obvious to combine Hardee with Sukegawa, since the alleged advantages are non-existent, and such a substitution *could* require boosting voltages above Vdd." The Board quoted that sentence in its opinion but concluded that it agreed with Samsung that "the mere possibility of having to boost voltages above Vdd does not detract from the aforementioned advantages associated with modifying Sukegawa in view of Hardee's teachings." *Samsung Elecs. Co.*, 2017 WL 379208, at *16. Elbrus now complains that the Board misunderstood the evidence because Elbrus's expert had stated that the signals "*would have to be* boosted above VDD to pull the driver outputs all the way to VDD." However, Elbrus's expert explained that the voltage boost would have to occur only if needed to achieve the "desirable (for both speed and noise immunity)" condition that the outputs "swing all the way to VDD or all the way to ground when activated." The Board therefore did not err in referring to

Elbrus's response that boosting voltage above Vdd could occur, but is not required to.

Because substantial evidence supports the Board's finding that a person of ordinary skill would have been motivated to combine Sukegawa with Hardee, we affirm the Board's conclusion that claim 7 would have been obvious.

AFFIRMED