United States Court of Appeals for the Federal Circuit

VLSI TECHNOLOGY LLC,
Appellant

v.

INTEL CORPORATION,
Appellee

2021-1826, 2021-1827, 2021-1828

Appeals from the United States Patent and Trademark Office, Patent Trial and Appeal Board in Nos. IPR2019-01198, IPR2019-01199, IPR2019-01200.

Decided: November 15, 2022

NATHAN NOBU LOWENSTEIN, Lowenstein & Weatherwax LLP, Santa Monica, CA, argued for appellant. Also represented by KENNETH J. WEATHERWAX.

S. CALVIN WALDEN, Wilmer Cutler Pickering Hale and Dorr LLP, New York, NY, argued for appellee. Also represented by JEFFREY ANDREW DENNHARDT; MARK CHRISTOPHER FLEMING, JOHN V. HOBGOOD, STEPHANIE LIN, Boston, MA; RONALD GREGORY ISRAELSEN, Washington, DC.

Before CHEN, BRYSON, and HUGHES, *Circuit Judges*.

BRYSON, *Circuit Judge*.

Appellee Intel Corporation filed three petitions for *inter partes* review ("IPR") of U.S. Patent No. 7,247,552 ("the '552 patent"), which is owned by appellant VLSI Technology LLC. The Patent Trial and Appeal Board instituted the IPR proceedings, and in a combined Final Written Decision, the Board found all of the challenged claims of the '552 patent to be unpatentable. For the reasons set forth below, we affirm in part, reverse in part, and remand.

I

A

The '552 patent is directed to "[a] technique for alleviating the problems of defects caused by stress applied to bond pads" of an integrated circuit. '552 patent, Abstract.

An integrated circuit, sometimes referred to as a "chip" or "die," contains numerous electronic circuits that are integrated on a flat piece of semiconductor called a "substrate." The specification of the '552 patent discloses an integrated circuit that includes several metal "interconnect layers" positioned above the substrate and frequently surrounded by "dielectric" or insulating material. *See id.* at col. 3, ll. 1–10 & Fig. 1. The integrated circuits described in the '552 patent also include one or more "bond pads" that sit above the interconnect layers and are used to attach the chip to another electronic component, such as a computer motherboard. *See id.* at col. 3, ll. 22–25.

When a chip is attached to another electronic component, forces are exerted on the chip's bond pad. *Id.* at Abstract & col. 5, ll. 53–57. Those forces can result in damage to the interconnect layers and to the dielectric material that surrounds those layers. *See id.* at Abstract & col. 1, ll. 39–42. As such, dedicated support structures made of metal layers and vias are connected to and provide support

for the bond pad. *See id.* at col. 1, ll. 53–61. In the prior art, these metal support layers were linked to the bond pad, and thus were not "functionally independent," i.e., they could not be "used for wiring or interconnects unrelated to the pad." *Id.* at col. 1, ll. 58–64.

The '552 patent discloses improvements to the structures of an integrated circuit that reduce the potential for damage to the interconnect layers and dielectric material when the chip is attached to another electronic component while also "permit[ing] each of the interconnect layers underlying [the pad] to be functionally independent in the circuit if desired." *See id.* at col. 3, line 64 through col. 4, line 7. Specifically, the '552 patent discloses that only "a predetermined minimum amount of metal or a minimum density" is needed to "adequately support" the bond pad. *See id.* at col. 3, line 64 through col. 4, line 4. If the functionally independent interconnect layers underneath the pad are insufficient to reach a predetermined minimum density, "dummy metal lines"—i.e., metal lines that do not serve any electrical purpose—may be added to increase the metal density of the interconnect layers. *See id.* at col. 4, ll. 13–56; *see also id.* at Fig. 3.

Claim 1 is the only independent apparatus claim of the '552 patent and is representative of the claimed invention. It recites as follows:

> 1. An integrated circuit, comprising:
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> a substrate having active circuitry;
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> a bond pad over the substrate;
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> a force region at least under the bond pad characterized by being susceptible to defects due to stress applied to the bond pad;
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> a stack of interconnect layers, wherein each interconnect layer has a portion in the force region; and

> a plurality of interlayer dielectrics separating the interconnect layers of the stack of interconnect layers and having at least one via for interconnecting two of the interconnect layers of the stack of interconnect layers;
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> wherein at least one interconnect layer of the stack of interconnect layers comprises a functional metal line underlying the bond pad that is not electrically connected to the bond pad and is used for wiring or interconnect to the active circuitry, the at least one interconnect layer of the stack of interconnect layers further comprising dummy metal lines in the portion that is in the force region to obtain a predetermined metal density in the portion that is in the force region.

'552 patent, claim 1. Claim 2 depends from claim 1, and claim 11 is a method claim generally similar to claim 1.

Claim 20 also plays a role in this appeal. It recites as follows:

> 20. A method of making an integrated circuit having a plurality of bond pads, comprising:
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> developing a circuit design of the integrated circuit;
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> developing a layout of the integrated circuit according to the circuit design, wherein the layout comprises a plurality of metal-containing interconnect layers that extend under a first bond pad of the plurality of bond pads, at least a portion of the plurality of metal-containing interconnect layers underlying the first bond pad and not electrically connected to the bond pad as a result of being used for electrical interconnection not directly connected to the bond pad;

> modifying the layout by adding dummy metal lines to the plurality of metal-containing interconnect layers to achieve a metal density of at least forty percent for each of the plurality of metal-containing interconnect layers; and
>
> forming the integrated circuit comprising the dummy metal lines.

'552 patent, claim 20.

B

In 2018, VLSI brought suit in the United States District Court for the District of Delaware, charging Intel with infringing the '552 patent. The district court subsequently conducted a claim construction hearing. In the course of the hearing, the court construed the term "force region," which appears in independent claims 1 and 11 of the '552 patent. Citing a passage from the '552 patent, the district court construed "force region" to mean a "region within the integrated circuit in which forces are exerted on the interconnect structure when a die attach is performed." J.A. 6017, 6356; *see also* '552 patent, col. 3, ll. 49–52.

In June 2019, after the district court action was filed but before the claim construction proceedings in that action, Intel filed its petitions for IPR, challenging the validity of claims 1, 2, 11, and 20 of the '552 patent. In the petition directed to claims 1 and 2, Intel proposed a construction of "force region" that was consistent with the claim construction that Intel subsequently offered to the district court and that the district court adopted, i.e., a "region within the integrated circuit in which forces are exerted on the interconnect structure when a die attach is performed." J.A. 6588–89.

VLSI did not oppose Intel's proposed construction before the Board. It soon became evident, however, that although the parties purported to agree on the construction to be given to the term "force region," their agreement was

merely apparent, because they disagreed as to the meaning of the term "die attach."

Intel argued that the term "die attach" refers to any method of attaching the chip to another electronic component, and that the term "die attach" therefore includes attachment by a method known as wire bonding. J.A. 6594 (Petition in IPR2019-1198); J.A. 6789–93 (Petitioner's Reply to Patent Owner's Preliminary Response); J.A. 7063–70 (Petitioner's Reply); J.A. 7286–87 (Oral Hearing before the Board). VLSI, on the other hand, argued that the term "die attach" refers to a method of attachment known as "flip chip" bonding, and does not include wire bonding. *See* J.A. 6720–29 (Patent Owner's Preliminary Response); J.A. 7005–14 (Patent Owner's Response); J.A. 7100–05 (Patent Owner's Sur-Reply to Petitioner's Reply to the Patent Owner's Response); *see also* J.A. 7299–7300 (Oral Hearing before the Board in which counsel for Intel noted that although the parties agreed on the construction of "force region," they disagreed on the meaning of the term "die attach").

Applying its proposed restrictive definition of "die attach," VLSI distinguished Intel's principal prior art reference for the "force region" limitation, U.S. Patent Publication No. 2004/0150112 ("Oda"). That reference discloses attaching a chip to another component using wire bonding. Based on its contention that the term "die attach" does not encompass attachment by wire bonding, VLSI argued that Oda does not disclose a "force region" within the meaning of the claims of the '552 patent as construed by the district court.

In its Institution Decisions, the Board stated that "based on the current record," it disagreed with VLSI that the method of performing a "die attach" cannot include the method of wire bonding. J.A. 6846, 20006. The Board pointed out that Intel had provided argument and evidence that wire bonding is a type of die attach, and that Oda

therefore disclosed a "force region" under Intel's claim construction, i.e., a region within the integrated circuit in which forces are exerted on the interconnect structure when a die attach is performed. J.A. 6846–47, 20006–07. In addition, the Board noted that Intel asserted that the "force region" includes regions directly under the bond pad, and that VLSI's proposed construction during the district court proceeding also included regions directly under the bond pad. J.A. 6845, 20005–06. The Board then stated that a construction of "force region" that includes regions at least under the bond pad "is consistent with the plain language of claim[s] 1" and 11. *See* J.A. 6845, 20005.

In its Final Written Decision, unlike in the Institution Decisions, the Board did not resolve the parties' dispute regarding the meaning of the term "die attach." Instead, the Board construed the term "force region" as "including at least the area directly under the bond pad." *Intel Corp. v. VLSI Tech. LLC*, Nos. IPR2019-01198, IPR2019-01199, IPR2019-01200, 2021 WL 388740, at *6 (P.T.A.B. Feb. 3, 2021). The Board also found that the '552 patent specification made clear in several places that the term "force region" was not limited to flip chip bonding, but could include wire bonding as well. *Id.* at *7. Based on that finding, the Board concluded that Oda disclosed the "force region" element of claims 1, 2, and 11, and that those claims were unpatentable for obviousness. *Id.* at *12–13.

With respect to claim 20 of the '552 patent, the parties disagreed over the construction of the limitation providing that the "metal-containing interconnect layers" are "used for electrical interconnection not directly connected to the bond pad." VLSI argued that the phrase requires a connection to active circuitry or the capability to carry electricity. *Id.* at *8. Intel argued that the claim does not require that the interconnection actually carry electricity. *See id.* The Board sided with Intel; it found that "[c]laim 20 does not recite 'active circuitry'" and declined "to import [that] limitation into claim 20." *Id.* at *9. The Board therefore

construed the phrase to encompass interconnect layers that are "electrically connected to each other but not electrically connected to the bond pad." *Id.* at *10.

Intel relied principally upon U.S. Patent No. 7,102,223 ("Kanaoka") as teaching the "used for electrical interconnection" limitation in claim 20 as construed by the Board. Figure 45 of Kanaoka discloses a die that has a series of interconnect layers, some of which are connected to each other by vertical metal structures called "vias." J.A. 7655; *see also* Appellee's Br. 6–7. Because the interconnect layers disclosed in Kanaoka were electrically connected to one another but not to the bond pad, the Board found that Kanaoka disclosed the "used for electrical interconnection" limitation of claim 20. *Intel*, 2021 WL 388740, at *28.

Based on its analysis, the Board concluded that all the challenged claims (claims 1, 2, 11, and 20) of the '552 patent were unpatentable. *Id.* at *29. VLSI appealed.

II

VLSI raises two principal issues on appeal. First, VLSI argues that the Board erred in its treatment of the "force region" limitation of claims 1, 2, and 11. Second, VLSI argues that the Board erred in construing the phrase "used for electrical interconnection" in claim 20 to encompass a metallic structure that is not connected to active circuitry. We affirm with respect to the first issue, and we reverse and remand with respect to the second.

A

1

With regard to the "force region" limitation, VLSI argues that the Board erred in declining to adopt the construction of "force region" that was proposed by Intel and adopted by the district court. Specifically, VLSI argues that the Board failed to acknowledge and give appropriate weight to the district court's claim construction. VLSI

bases its argument principally on the Patent and Trademark Office procedures that require the Board to "consider" prior claim construction determinations by a district court and give such prior constructions appropriate weight. *See* 37 C.F.R. § 42.100(b); *see also Power Integrations, Inc. v. Lee*, 797 F.3d 1318, 1326–27 (Fed. Cir. 2015); Patent Trial and Appeal Board, Consolidated Trial Practice Guide 46–47 (Nov. 2019); Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340, 51,354 (Oct. 11, 2018).

We reject VLSI's argument regarding the asserted regulatory violation for several reasons. First, while it is true that the Board did not specifically mention the district court's claim construction in its Final Written Decision, the Board was clearly well aware of that construction, as the district court's construction was the subject of repeated and extensive discussion in the briefing and in the oral hearing before the Board. *See* J.A. 6720 (Patent Owner's Preliminary Response); J.A. 6954, 7001 (Patent Owner's Response); J.A. 7099–7100 (Patent Owner's Sur-reply); J.A. 7328, 7333–35 (Oral Hearing).

Second, the Board did not reject the district court's construction. Instead, in light of the arguments made by the parties before the Board, it was clear that the apparent agreement as to the district court's construction concealed a fundamental disagreement between the parties as to the proper construction of "force region." The Board recognized that simply adopting Intel's proposed construction would not resolve the true dispute between the parties, which turned on whether the term "force region," as used in the '552 patent, was limited to flip chip bonding or covered wire bonding as well. *See* J.A. 6838, 6846–47. Although the district court defined the term "force region" with reference to "die attach" processes, the district court did not decide—and was not asked to decide—whether the term "die attach," as used in the patent, included wire bonding or was

limited to flip chip bonding. *See generally VLSI Tech. LLC v. Intel Corp.*, No. 18-cv-966, Dkt. No. 228 (D. Del. Aug. 19, 2019) (Joint Claim Construction Brief). Thus, the Board addressed an argument not made to the district court, and it reached a conclusion not at odds with the conclusion reached by the district court. *See* Consolidated Trial Practice Guide 47 (noting that the "facts and circumstances of each case will be analyzed as appropriate").

Finally, we conclude that the Board's treatment of the term "force region" was not erroneous, for the reasons we address below. Because the parties' positions before the Board made it clear that the Board needed to go beyond the district court's claim construction in order to resolve the parties' dispute, it was unnecessary for the Board to advert to the district court's claim construction. Therefore, even if it might have been useful for the Board to begin by expressly acknowledging the district court's claim construction, the Board was not required to do so, and any failure to do so was at most harmless error.

2

As to the merits of the Board's claim construction, we conclude that the Board's claim construction of "force region" and its application of that construction to the Oda reference were not inconsistent with the proper construction of "force region."

Both Intel and the district court relied on a passage from column 3 of the '552 patent as providing support for Intel's proposed construction of the term "force region." That passage explains that "[t]he force region 64 is a region within the integrated circuit 10 in which forces are exerted on the interconnect structure when a die attach is performed." '552 patent, col. 3, ll. 49–52. Like the Board, we conclude that the passage in column 3 is directed to the embodiment disclosed in Figures 1 and 2 of the '552 patent. *See Intel*, 2021 WL 388740, at *7. Thus, even if the term "die attach," as used in the '552 patent, were construed to

include only flip chip bonding, that would not affect the construction of the term "force region." As we have repeatedly cautioned, claims should not be limited "to preferred embodiments or specific examples in the specification." *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1328 (Fed. Cir. 2002) (quoting *Comark Commc'ns, Inc. v. Harris Corp.*, 156 F.3d 1182, 1186 (Fed. Cir. 1998)). It was therefore unnecessary for the Board to determine whether the term "die attach," as used in column 3 of the '552 patent, excludes wire bonding.

Even if the term "die attach," as used in column 3 of the '552 patent, is understood to refer to flip chip bonding in particular and not to other forms of attachment such as wire bonding, other portions of the specification make clear that the invention is not limited to flip chip bonding. The specification specifically calls out wire bonding mechanisms, stating that examples of an interconnect pad within the scope of the invention "include, but are not limited to, a wire bond pad, a probe pad, a flip-chip bump pad, a test point or other packaging or test pad structures that may require underlying structural support." '552 patent, col. 2, ll. 42–45.

In addition, as the Board noted, other language in the specification indicates that the claimed "force region" is not limited to attachment processes that use flip chip bonding. *See Intel*, 2021 WL 388740, at *7. For example, with respect to another embodiment of the invention, the specification states that "[i]n another form the force region is a region in which the interconnect layers . . . are susceptible to stress from the bond pad *due to assembly or other processes*." '552 patent, col. 6, ll. 25–29 (emphasis added). Likewise, the specification elsewhere states that a force region "is identified around and under the bond pad characterized by being susceptible to defects due to contacts to the bond pad." *Id.* at col 5, ll. 55–57. Based on those portions of the specification, the Board found that the Oda reference reads on the "force region" limitation.

We conclude that the correct construction of the term "force region" is the definition provided in column 6 of the '552 patent. That is, "force region" is construed to mean "a region in which the interconnect layers are susceptible to stress from the bond pad due to assembly or other processes." *See* '552 patent, col. 6, ll. 25–29. Under that construction, stresses on the interconnect layers resulting from any assembly process, including wire bonding, would fall within the scope of the term "force region." The Board's treatment of that limitation is not inconsistent with our construction. In fact, the Board relied on the same language from column 6 of the '552 patent in concluding that the Oda reference discloses the "force region" of claim 1. *Intel*, 2021 WL 388740, at *13.

The Board was able to resolve the case by construing the term "force region" to include at least the area directly under the bond pad and by not limiting the term to situations in which the flip chip bonding method is used. That construction is not inconsistent with our construction. The Board therefore properly found that the Oda reference, in combination with other references cited to the Board, made claims 1, 2, and 11 unpatentable.

3

VLSI raises two other challenges to the Board's construction of the term "force region." First, it contends that defining "force region" to mean a region at least directly under the bond pad is legally flawed because the definition restates a requirement that is already in the claims, which refer in the case of claim 1 to a "force region at least under the bond pad" and in the case of claim 11 to "a force region at least under the first bond pad of the plurality of bond pads." That construction, according to VLSI, would violate the principle that construing claims to include features of the term that are already recited in the claims "would make those expressly recited features redundant," and that

"[i]deally" such constructions should be avoided. *Apple, Inc. v. Ameranth*, 842 F.3d 1229, 1237 (Fed. Cir. 2016).

While a construction that introduces redundancy into a claim is disfavored, it is not foreclosed. *See SimpleAir, Inc. v. Sony Ericsson Mobile Commc'ns AB*, 820 F.3d 419, 429 (Fed. Cir. 2016). That is particularly true where, as in this case, intrinsic evidence makes it clear that the "redundant" construction is correct. To be sure, the claim language in question could have been drafted more precisely. But the meaning of the claim limitation referring to the force region is clear: The claim identifies a region that is "at least under the bond pad" and is "characterized by being susceptible to defects due [to] stress applied to the bond pad," and it refers to that region as the "force region." Thus, the "force region" limitation is best understood as containing a definition of the force region, just as would be the case if the language of the limitation had read "a region, *referred to as a force region,* at least under the bond pad . . ." or "a force region, *i.e., a region* at least under the bond pad . . . ." As such, that language from the claims is best viewed not as redundant, but merely as clumsily drafted.

VLSI's second argument is that when the parties to an IPR proceeding agree to a particular construction of a claim term, the Board is bound by that construction, regardless of whether the construction to which the parties agree is actually the proper construction of that term. *See* Oral Argument at 14:22–22:04; *see also* Appellant's Reply Br. 12–14. In support of its argument regarding that prohibition, VLSI cites the Supreme Court's decision in *SAS Institute v. Iancu*, 138 S. Ct. 1348 (2018), and our decisions in *Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330 (Fed. Cir. 2020), and *In re Magnum Oil Tools International, Ltd.*, 829 F.3d 1364 (Fed. Cir. 2016).

We disagree with VLSI's reading of those cases. In *SAS*, the Court held that the petition "guide[s] the life of

the litigation" in an IPR proceeding. *SAS*, 138 S. Ct. at 1356. In *Koninklijke*, we reaffirmed the principle that "it is the petition, not the Board's discretion, that defines the metes and bounds of an [IPR]." *Koninklijke*, 948 F.3d at 1336. And in *Magnum Oil*, we held that "the Board must base its decision on arguments that were advanced by a party, and to which the opposing party was given a chance to respond." *Magnum Oil*, 829 F.3d at 1381. Each of those cases stands for the proposition that the petition defines the scope of the IPR proceeding and that the Board must base its decision on arguments that were advanced by a party and to which the opposing party was given a chance to respond. None of those cases prohibits the Board from construing claims in accordance with its own analysis. To the contrary, we have held that the Board is not limited to the claim constructions proffered by the parties, but may adopt its own claim construction of a disputed claim term. *See, e.g.*, *WesternGeco LLC v. ION Geophysical Corp.*, 889 F.3d 1308, 1328–29 (Fed. Cir. 2018); *Uniloc 2017 LLC v. Facebook Inc.*, 989 F.3d 1018, 1032–33 (Fed. Cir. 2021).

Although the parties may have agreed to apply the language of the district court's construction of "force region," this was not a case in which the parties actually agreed on the proper claim construction. As we explained above, it is true that Intel proposed to construe "force region" as "a region within the integrated circuit in which forces are exerted on the interconnect structure when a die attach is performed," and that VLSI did not oppose that construction. But the parties' purported agreement concealed a fundamental disagreement about the meaning of that construction. Because of the parties' very different understandings of the meaning of the term "die attach," it was clear in the Board proceedings that there was no real agreement on the proper claim construction. In that

situation, it was proper for the Board to adopt its own construction of a disputed claim term.[1]

For the foregoing reasons, we conclude that the Board's analysis of the "force region" limitation was not erroneous. Because VLSI raises no other challenges to the Board's decision that claims 1, 2, and 11 are unpatentable,[2] we affirm the Board's decision with respect to those claims.

B

VLSI next argues that the Board erred in construing the phrase "used for electrical interconnection not directly connected to the bond pad," which appears in claim 20 of the '552 patent. The Board held that this phrase encompasses interconnect layers that are "electrically connected to each other but not electrically connected to the bond pad" or to any other active circuitry. *Id.* at *10. VLSI argues that the Board should have construed the phrase to require

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[1] In its reply brief, VLSI argues that judicial estoppel and waiver preclude Intel from advocating for the Board's claim construction. Given that the proceedings before the Board revealed that the parties disagreed as to the meaning of the term "die attach," it was appropriate for the Board to adopt, and Intel to advocate for, a construction that captured the essence of Intel's position, i.e., that the term "force region" referred to a region at least under the bond pad that was susceptible to defects due to stress applied to the bond pad, regardless of the type of bonding that was responsible for causing that stress.

[2] We note that VLSI has expressly waived any due process challenge to the Board's construction of "force region." *See* Oral Argument at 18:47–18:53. In particular, VLSI has not suggested that it lacked notice of the Board's construction of that term or an opportunity to contest that construction.

that the interconnect layers be connected to active circuitry or have the capability to carry electricity.

VLSI argues that under its proposed construction, the Kanaoka reference does not disclose the "used for electrical interconnection" limitation of claim 20, because the metallic layers are connected by the vias only to one another; they do not carry electricity and are not electrically connected to any other components.

We agree with VLSI that the Board's construction of the phrase "used for electrical interconnection not directly connected to the bond pad" was too broad. Two aspects of the claims make this point clear. First, the use of the words "being used for" in the claim imply that some sort of actual use of the metal interconnect layers to carry electricity is required. Second, the recitation of "dummy metal lines" elsewhere in claim 20 implies that the claimed "metal-containing interconnect layers" are capable of carrying electricity; otherwise, there would be no distinction between the dummy metal lines and the rest of the interconnect layer.

The file history of the '552 patent provides further support for that conclusion. The phrase "used for electrical interconnection not directly connected to the bond pad" was added to claim 20 during prosecution of the '552 patent. The underlined language below was added to claim 20 at that time:

> 20. A method of making an integrated circuit having a plurality of bond pads, comprising:
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> developing a circuit design of the integrated circuit;
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> developing a layout of the integrated circuit according to the circuit design, wherein the layout comprises a plurality of metal-containing interconnect layers that extend under a first bond pad of the plurality of bond pads, at least a portion of the

> plurality of metal-containing interconnect layers underlying the first bond pad and not electrically connected to the first bond pad as a result of being used for electrical interconnection not directly connected to the bond pad;
>
> modifying the layout by adding dummy metal lines to the plurality of metal-containing interconnect layers to achieve a metal density of at least forty percent for each of the plurality of metal-containing interconnect layers; and
>
> forming the integrated circuit comprising the dummy metal lines.

J.A. 272–73 (emphasis added). The Board observed that the amendment to claim 20 appeared to address what "the metal interconnect layers could *not* be attached to (i.e., the bond pad), rather than limiting what [they] *must be* connected to." *Intel*, 2021 WL 388740, at *9.

The problem with that observation is that it does not explain the addition of the phrase "as a result of being used for electrical interconnection not directly to the bond pad." That phrase could be eliminated from the inventor's proposed amendment and the claim would still require that the interconnect layers not be electrically connected to the bond pad. Presumably, that phrase was meant to serve some purpose and should be construed to have some independent meaning. *See Merck & Co. v. Teva Pharms. USA, Inc.*, 395 F.3d 1364, 1372 (Fed. Cir. 2005) ("A claim construction that gives meaning to all the terms of the claim is preferred over one that does not do so."). Indeed, the applicant argued in the context of claim 1 that "none of the area under the [prior art] bond pad may be used for wiring or interconnect[ion] unrelated to the pad," J.A. 8176, and argued that claim 20 was allowable for the same reason,

J.A. 8178.[3] In context, that independent meaning of "as a result of being used for electrical interconnection not directly to the bond pad" would seem to require that the interconnect layers be used for conducting electricity to components other than the bond pad.

In support of the Board's construction, Intel points out that VLSI's expert admitted that two interconnect layers can be "electrically connected" even if they do not carry electricity and even if they are not connected to any structure other than each other. *See* J.A. 8555–56. The problem with that argument is that the claim does not use the words "electrically connected." Instead, it recites the phrase "being used for electrical interconnection." And, as noted, the words "being used for" imply that the interconnect layers are at least capable of carrying electricity.

We therefore adopt VLSI's proposed construction of "used for electrical interconnection." That is, the phrase requires the interconnect layers to be capable of carrying electricity or be connected to active circuitry. The Board's construction of that phrase must therefore be reversed. We remand the patentability determination of claim 20 to the Board to assess Intel's obviousness arguments regarding that claim in light of our construction of the "used for electrical interconnection" limitation.

III

In summary, the Board's treatment of the term "force region" was not erroneous, and its decision that claims 1, 2, and 11 are unpatentable is therefore affirmed. Because the Board erred in construing the phrase "used for electrical interconnection," we reverse the Board's construction of

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[3] Claim 1 was amended, in part, to recite: "a functional metal line underlying the bond pad that is not electrically connected to the bond pad and is used for wiring or interconnect to active circuitry." J.A. 8171.

that phrase and remand for further proceedings regarding claim 20.

No costs.

AFFIRMED-IN-PART, REVERSED-IN-PART, AND REMANDED