IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

INNOVATIVE MEMORY SYSTEMS, INC., Plaintiff, v. MICRON TECHNOLOGY, INC., Defendant.	Civil Action No. 14-1480-RGA

MEMORANDUM OPINION

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November 23, 2020

/s/ Richard G. Andrews
ANDREWS, UNITED STATES DISTRICT JUDGE:

Before me is the issue of claim construction of multiple terms in U.S. Patent Nos. 7,000,063 ("the '063 patent") and 6,901,498 ("the '498 patent"). I have considered the Parties' Joint Claim Construction Brief. (D.I. 133). I held oral argument via Skype on November 3, 2020. (D.I. 147).

I. LEGAL STANDARD

"It is a bedrock principle of patent law that the claims of a patent define the invention to which the patentee is entitled the right to exclude." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal quotation marks omitted). "'[T]here is no magic formula or catechism for conducting claim construction.' Instead, the court is free to attach the appropriate weight to appropriate sources 'in light of the statutes and policies that inform patent law.'" *SoftView LLC v. Apple Inc.*, 2013 WL 4758195, at *1 (D. Del. Sept. 4, 2013) (quoting *Phillips*, 415 F.3d at 1324) (alteration in original). When construing patent claims, a court considers the literal language of the claim, the patent specification, and the prosecution history. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 977–80 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996). Of these sources, "the specification is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term." *Phillips*, 415 F.3d at 1315 (internal quotation marks omitted).

"[T]he words of a claim are generally given their ordinary and customary meaning. . . . [Which is] the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id.* at 1312–13 (citations and internal quotation marks omitted). "[T]he ordinary meaning of a claim term is its meaning to [an] ordinary artisan after reading the entire patent." *Id.* at 1321

(internal quotation marks omitted). "In some cases, the ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words." *Id.* at 1314.

When a court relies solely upon the intrinsic evidence—the patent claims, the specification, and the prosecution history—the court's construction is a determination of law. *See Teva Pharm. USA, Inc. v. Sandoz, Inc.*, 574 U.S. 318, 331 (2015). The court may also make factual findings based upon consideration of extrinsic evidence, which "consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises." *Phillips*, 415 F.3d at 1317–19 (internal quotation marks omitted). Extrinsic evidence may assist the court in understanding the underlying technology, the meaning of terms to one skilled in the art, and how the invention works. *Id.* Extrinsic evidence, however, is less reliable and less useful in claim construction than the patent and its prosecution history. *Id*.

"A claim construction is persuasive, not because it follows a certain rule, but because it defines terms in the context of the whole patent." *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998). It follows that "a claim interpretation that would exclude the inventor's device is rarely the correct interpretation." *Osram GMBH v. Int'l Trade Comm'n*, 505 F.3d 1351, 1358 (Fed. Cir. 2007) (citation and internal quotation marks omitted).

II. BACKGROUND

This case is about electronic memory devices. Memory devices are data storage systems composed of memory cells, to which data can be written. Memory cells can be re-written a variable number of times. The number of writes or re-writes to a memory cell varies based on

user need and physical limitations of the cell and can be accordingly restricted. A memory cell used for non-volatile data storage allows data storage without requiring power to retain the data stored. Because the cell retains the data stored, however, the cell must be erased before it can take on a different value; cells can be reliably erased and re-written a limited number of times. Those that can be re-written more than once are called write-many memory cells. Memory cells restricted to only one additional write, on the other hand, are called write-once memory cells.

Memory devices contain many memory cells. Common data architecture for non-volatile data storage includes organization of memory cells into "blocks," which constitute the smallest number of cells that can be simultaneously erased. Blocks are then assigned to logical zones. Defective blocks can arise during manufacture or regular use and can result in memory device failure if there are too many defective blocks in any one zone. Boundaries of logical zones can be adjusted to avoid memory failure by ensuring there is a sufficient number of good blocks in each zone. Zone adjustment can be done, as is relevant here, with firmware shortly after manufacture or by using a "controller" that can "dynamically" adjust zone boundaries in response to block defects that arise during operation of the memory device.

The disputed terms here come from a patent covering limitation of the number of writes to cells in a write-many device (the '063 Patent) and a patent covering adjustment of logical zone boundaries of assigned blocks in a memory device (the '498 Patent). The two patents have different inventors and specifications.

The following representative claims show the use of the disputed terms.

Claim 42 of the '063 Patent

1. A method for creating a write-once memory device from a write-many memory device, the method comprising:

(a) providing a memory device comprising a memory array comprising a plurality of write-many memory cell; and

(b) *rendering at least some of the write-many memory cells in the memory array as write-once memory cells by preventing more than one write to said at least some of the write-many memory cells*.

(D.I. 138-2, Exh. B (the "'063 Patent"), claim 42) (emphasis added).

Claim 1 of the '498 Patent

1. A memory system circuit, comprising:

a memory comprising a plurality of blocks of non-volatile storage elements wherein the storage elements within individual ones of the blocks are simultaneously erasable, and

a controller that controls programming of data into addressed blocks, reading data from addressed blocks and erasing data from one or more of addressed blocks at a time, wherein the memory is organized into logical zones each comprised of one or more blocks for address translation, and *wherein the correspondence of blocks to zones is adjustable by controller*.

(D.I. 138-3, Exh. C ("'498 Patent"), claim 1) (emphasis added).

Claim 11 of the '498 Patent

11. A memory system circuit, comprising:

a memory comprising a plurality of blocks of non-volatile storage elements wherein the storage elements within individual ones of the blocks are simultaneously erasable, and

a controller that controls programming of data into addressed blocks, reading data from addressed blocks and erasing data from one or more of addressed blocks at a time, wherein the memory is organized into logical zones each comprised of one or more blocks for address translation, and *wherein the correspondence of blocks to zones is dynamically adjustable by controller*.

(D.I. 138-3, Exh. C ("'498 Patent"), claim 11) (emphasis added).

Claim 43 of the '498 Patent

43. A memory system circuit, comprising:

a memory comprising a plurality-of [sic] blocks of non-volatile storage elements wherein the storage elements within individual ones of the blocks are simultaneously erasable,

a controller that controls programming of data into addressed blocks, reading data from addressed blocks and erasing data from one or more of addressed blocks at a time, wherein the non-volatile is organized into logical address sections as seen by the controller, *wherein the correspondence between physical blocks and logical address sections is adaptable by the controller in response to defects in the memory*.

(D.I. 138-3, Exh. C ("'498 Patent"), claim 43) (emphasis added).

III. CONSTRUCTION OF AGREED-UPON TERMS

I adopt the following agreed-upon constructions:

Claim Term	**Construction**
"write-many device" ('063 Patent)	"an electronic storage device to which data can be written more than once"
"write-many memory cell" ('063 Patent)	"a memory cell to which data can be written more than once"
"write-once memory cells" ('063 Patent)	"memory cells that cannot be written to more than once"
"manufacturer" ('063 Patent)	"any party who handles the memory device before it is sold or distributed to an end user, including a party involved in the manufacturing, assembly, packaging, sale or distribution of the memory device"
"block" ('498 Patent)	"the smallest grouping of nonvolatile memory cells (unit of erase) that are erasable at one time"
"logical zone" ('498 Patent)	"a logical subdivision of the total capacity of the nonvolatile memory die"
"planes" ('498 Patent)	"physical subdivisions of the memory on a single die"
"multi-state storage units" ('498 Patent)	"memory cells that each simultaneously store two or more bits of data per storage element"

IV. CONSTRUCTION OF DISPUTED TERMS

1. Term 1: "rendering at least some of the write-many memory cells in the memory array as write-once memory cells by preventing more than one write to said at least some of the write-many memory cells" ('063/42)

a. *Plaintiff's proposed construction*: "causing at least some of the write-many memory cells in the memory array to become memory cells that thereafter cannot be written to more than once"

b. *Defendant's proposed construction*: "converting at least some of the write-many memory cells in the memory array to write-once memory cells by setting a maximum write count of one"

c. *Court's construction*: "causing at least some of the write-many memory cells in the memory array to become write-once memory cells"

The parties agree that a write-many memory cell can be written more than once, and a write-once memory cell cannot be written more than once. (D.I. 133 at 2). They also agree that a write-many memory cell can be "rendered" into a write-once memory cell. (*Id.* at 4, 11). They dispute, however, whether the claimed invention must "render" write-many memory cells into write-once memory cells by setting a maximum write count, N, equal to one (i.e. N=1) for the memory cell. (*Id.* at 5, 11).

Defendant makes two primary arguments.

First, Defendant argues that Plaintiff distinguished the claimed invention from prior art during IPR proceedings by defining the "'rendering' limitation to require use of a maximum write count." (*Id.* at 5). At IPR, Defendant asserted a prior art reference, Kasa, that used a "write protect step" to render write-many memory cells into read-only memory cells, which can no longer be written. (*Id.* at 6; D.I. 138-6, Ex. F, IPR2016-00325, Preliminary Response at 17). Defendant claims Kasa's write-protect step "prevents more than one write" to the memory cells and would therefore meet the requirement for a write-once memory cell. (D.I. 133 at 6). Defendant maintains that in order to distinguish Kasa during IPR, Plaintiff indicated that "rendering" required setting a "maximum write count" of N=1, which would exclude a read-only memory cell because it cannot be written to at all. (D.I. 138-6, Ex. F, IPR2016-00325, Preliminary Response at 16–17).

Second, Defendant argues that the "rendering" term is a results-based limitation and therefore should be restricted to the process of achieving the result disclosed in the specification. (D.I. 133 at 8) (citing *Medicines Co. v. Mylan, Inc.*, 853 F.3d 1296, 1304 (Fed. Cir. 2017)). In *Medicines Co.*, the claimed invention involved "efficient mixing" of a solution to ensure the concentration of a chemical impurity remained below a specified threshold. 853 F.3d at 1306. Although the claims did not define any one process for "efficient mixing," the Federal Circuit noted that construing the claim to mean "any way of mixing" that results in an appropriate impurity concentration would allow the claim to cover "all solutions to the identified 'impurities' problem, without describing the entire range of solutions to that problem." *Id.* at 1307. Because such an interpretation "would cause the claim to have a potential scope of protection beyond that which is justified by the specification disclosure," the Federal Circuit held that the method for "efficient mixing" should be restricted to the mixing method described in the specification. *Id.* at 1306–07. Defendant argues that "rendering" similarly seeks a result—converting write-many memory cells into write-once memory cells—and should therefore also be limited to the method described in the specification, which achieves the result by setting a maximum write count of one. (D.I. 133 at 9).

Plaintiff contests both arguments.

First, Plaintiff asserts that its arguments during IPR to distinguish the prior art reference, Kasa, from the claimed invention do not limit the "rendering" step to a maximum write count. (*Id.* at 12–13). Kasa discloses a memory device with a one-time programmable (OTP) sector that, when using a write-protect step, can prevent further writes to memory cells in the OTP sector. (D.I. 138-6, Ex. F, IPR2016-00325, Preliminary Response at 11). Plaintiff argues that this write-protect step "renders" write-many memory cells in the OTP sector into read-only memory

cells, which cannot be written to at all, rather than write-once memory cells, which cannot be written to more than once. (D.I. 133 at 12–13).

Second, Plaintiff argues that "rendering" should not be restricted to "use of a maximum write count" described in exemplary embodiments of the claimed invention. (*Id.* at 14). Plaintiff asserts at the outset that "rendering" has a "plain and ordinary meaning" (i.e. "causes to become") and does not need contextualization from the specification or prosecution history. (*Id.* at 13–15; D.I. 147 at 22:19–23:6). Nothing in the claim language, moreover, requires that the method of "rendering" involve setting a maximum write count. (D.I. 147 at 22:16–20). Plaintiff also argues that the PTAB's reference to exemplary embodiments that use a maximum write count does not constitute prosecution history disclaimer because the PTAB did not exclude other methods of rendering from the claim scope. (D.I. 133 at 17) (citing *Continental Circuits LLC v. Intel Corporation*, 915 F.3d 788, 797 (Fed. Cir. 2019)). Finally, Plaintiff distinguishes *Medicines Co.* because in that case, the term at issue carried no accepted meaning to someone of ordinary skill in the art and was not adequately disclosed in the specification. (*Id.* at 18).

I agree with Plaintiff on both disputes.

First, "rendering" does not need to be limited to a "maximum write count" in order to distinguish the claimed invention from the prior art. The prior art reference, Kasa, that Micron asserted during IPR proceedings "renders" write-many memory cells directly into read-only memory cells. (D.I. 138-6, Ex. F, IPR2016-00325, Preliminary Response at 16–17). Read-only memory cells cannot be written at all—and therefore certainly cannot be written once. While I understand Micron's objection that memory cells that can be written to at least once (write-once memory cells) also include those that cannot be written to at all (read-only memory cells) (D.I. 147 at 11:1–13:1), it is the converse that is dispositive. Read-only memory cells *cannot*

encompass memory cells that can be written to once (i.e. write-once memory cells); Kasa therefore does not disclose "rendering" write-many memory cells into write-once memory cells. Limiting the method by which write-once memory cells are made is not necessary for this distinction because limiting the number of writes was not "technologically difficult," making it something that a person of ordinary skill in the art at the time of invention likely knew how to do. (*Id.* at 13:20–14:2, 33:24–34:7).

Second, "rendering" is not restricted to the use of a "maximum write count" described in exemplary embodiments in the specification. (*See, e.g.*, D.I. 138-2, Exh. B, Fig.1, 4A–D). Disclosure of "only one method for making the invention . . . does not automatically lead to finding a clear disavowal of claim scope," *Continental Circuits LLC v. Intel Corp.*, 915 F.3d 788, 797 (Fed. Cir. 2019), especially in light of the Federal Circuit's statement in *Phillips* that "although the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments." 415 F.3d at 1323. Indeed, "[a]bsent a clear disavowal in the specification or the prosecution history, the patentee is entitled to the full scope of its claim language." *Home Diagnostics, Inc. v. LifeScan, Inc.*, 381 F.3d 1352, 1358 (Fed. Cir. 2004).

There is no such "clear disavowal" of claim scope here. The representative claim covers the concept of "rendering" a write-many cell into a write-once cell; the claim neither relies on nor recites any one method of "rendering." Although Defendant asserts that, under *Medicines Co.*, "rendering" of write-many cells should be restricted to the use of a "maximum write count" described in exemplary embodiments (D.I. 133 at 8), that case is inapplicable here. In *Medicines Co.*, the Federal Circuit did limit the claim term "efficient mixing" to the process described in a specific embodiment, but it did so because a person of ordinary skill in the art would have had to

rely on the embodiment's description of "efficient mixing" to practice the claimed invention. 853 F.3d at 1308–09. Here, both sides agree that the claimed invention does not recite something technologically difficult. (D.I. 147 at 13:20–14:2, 33:24–34:7). It stands to reason, then, that a person of ordinary skill in the art would not have had any issue limiting the number of writes to a memory cell, obviating the need for limitation of the method of "rendering" to use of a "maximum write count" of one.

Nothing in the prosecution history indicates that Plaintiff's arguments during IPR proceedings disclaim the scope of the claim at issue here. Nor does the use of a "maximum write count" by exemplary embodiments support limitation of "rendering" to that particular method. Given the absence of a "clear disavowal" of claim scope, the term "rendering" need not be limited. I therefore adopt a modified version of Plaintiff's construction that replaces "memory cells that thereafter cannot be written to more than once" with the more concise "write-once memory cells" because both parties have already agreed they mean the same thing. (D.I. 138-1, Exh. A at A-1).

2. **Term 2: "wherein the correspondence of blocks to zones is adjustable by controller" ('498/1)**

    a. *Plaintiff's proposed construction*: "the controller can adjust zone boundaries such that blocks from one logical zone are shifted to another logical zone"

    b. *Defendant's proposed construction*: "wherein a controller is configured to adjust boundaries between zones of assigned blocks such that blocks from one logical zone are shifted to another logical zone to balance the number of good blocks across the zones"

    c. *Court's construction*: "wherein the controller can adjust zone boundaries such that assigned blocks from one logical zone are shifted to another logical zone"

The ’498 patent discloses the grouping of blocks of memory cells into logical zones. (D.I. 138-3, Exh. C at 6:24–39). The parties agree that the claimed memory system includes a controller that can adjust the number of good blocks across logical zones. (D.I. 133 at 24, 31–32). The parties disagree whether the construction must specify that blocks were “assigned” to logical addresses in the zones. (*Id.* at 26, 32–33). The parties also disagree whether adjusting the “correspondence of blocks to zones” must be limited to balancing the number of good blocks across logical zones. (*Id.* at 27, 34).

A. *Assigned Blocks*

Defendant asserts that blocks in the claimed memory system require logical addresses (i.e. assignment to logical zones) before any adjustment of zone boundaries. (*Id.* at 26). For support, Defendant cites to the Federal Circuit’s review of the IPR decision, in which the court concluded that the claim language “requires a controller that can adjust boundaries between zones of assigned blocks.” (*Id.*) (citing *Innovative Memory Sys., Inc. v. Micron Tech., Inc.*, 781 F. App’x. 1013, 1018 (Fed. Cir. 2019)). Plaintiff agreed at oral argument with Defendant’s position that “blocks within those logical zones had to have logical addresses assigned to them.” (D.I. 147 at 56:17–24). I therefore adopt “assigned blocks” instead of “blocks” for this construction.

B. *Balancing the Number of Good Blocks Across Logical Zones*

Defendant argues that the specification and prosecution history confirm that adjusting the “correspondence of blocks to zones” means balancing the number of good blocks across logical zones. (D.I. 133 at 27). The specification states that adjusting zone boundaries after “the number of good blocks becomes unbalanced” across logical zones is a “princip[al] aspect of the invention.” (D.I. 138-3, Exh. C at 8:20–34). Defendant also points to Plaintiff’s statements

during IPR that the invention claims adjustment of logical zone boundaries to ensure "enough 'good' blocks . . . remain functional," and that the adjustment "results in a more uniform distribution of good blocks across the zones." (D.I. 138-12, Exh. L, IPR2016-00330, Preliminary Response at 8; D.I. 138-13, Exh. M, IPR2016-00330, Response at 10). Zone shifting of good blocks, Defendant argues, was also one of Plaintiff's bases for distinguishing prior art during IPR. (D.I. 138-12, Exh. L, IPR2016-00330, Preliminary Response at 26).

Plaintiff, on the other hand, maintains the Federal Circuit equated adjusting boundaries with the "correspondence" between blocks and logical zones to "assist zones with defective blocks." (D.I. 133 at 34) (citing *Innovative Memory Sys.*, 781 F. App'x. at 1016–17). In doing so, Plaintiff argues, the Federal Circuit made clear that "adjusting" correspondence of blocks to zones is not limited to any narrower purpose than shifting blocks from one logical zone to another. (*Id.* at 34–35; *see* D.I. 147 at 53:3–54:24). Limiting the adjustment of logical zones for the purpose of balancing the number of good blocks across logical zones, Plaintiff asserts, also is not supported by the specification. (D.I. 133 at 35). Plaintiff notes that embodiments describing adjustment of good blocks across logical zones, such as Figures 4 and 6, do not describe equal distribution of those good blocks. (*Id.* at 36).

I agree with Plaintiff. The Federal Circuit made clear that the claim language "requires a controller that can adjust boundaries between zones of assigned blocks 'such that blocks from one logical zone are shifted to another logical zone.'" *Innovative Memory Sys.*, 781 F. App'x. at 1018. The Court acknowledged that the claim teaches adjustment of "the correspondence of blocks to zones" when blocks become defective in a zone (*id.* at 1016), but the Court did not read onto the claim any further limitation related to the purpose of adjustment, such as equal distribution of good blocks across logical zones. Defendant's argument of prosecution history

disclaimer is similarly unwarranted. The Federal Circuit made clear that this claim has a "narrow scope" as shown "by the plain text of the claim[] itself"; because "the specification is not being used to narrow the claim," the disavowal doctrine does not apply. *Id.* at 1017.

I therefore adopt Plaintiff's proposed construction with the modification of "blocks" to "assigned blocks" and the addition of "wherein" at the beginning of the construction, to match the claim language.

3. **Term 3: "wherein the correspondence of blocks to zones is dynamically adjustable by controller" ('498/11)**

    a. *Plaintiff's proposed construction*: "the controller can adjust zone boundaries during use such that blocks from one logical zone are shifted to another logical zone"

    b. *Defendant's proposed construction*: "wherein a controller is configured to detect imbalances in the distribution of good blocks across zones during use and adjust zone boundaries between zones such that blocks from one logical zone are shifted to another logical zone to balance the number of good blocks across the zones"

    c. *Court's construction*: "wherein the controller can adjust zone boundaries during operating conditions as the need arises such that assigned blocks from one logical zone are shifted to another logical zone"

The parties agreed at oral argument that "dynamically" generally means the controller is adjusting the correspondence of blocks to zones during normal use of the device. (D.I. 147 at 48:17–49:7, 59:13–60:7). The parties dispute whether, as with claim 1 of the '498 Patent, the claim language should be limited to adjusting zone boundaries for the purpose of balancing the number of good blocks across zones. (D.I. 133 at 42, 43). Because the language of claim 1 and claim 11 of the '498 patent are identical except for the word "dynamically," I come to the same conclusions for the rest of the term language: "blocks" should be modified to "assigned blocks,"

"wherein" should be included at the beginning of the construction, and no limitation of purpose is necessary when "blocks from one logical zone are shifted to another logical zone."

With regards to the definition of "dynamically," I requested both parties to submit definitions of the term from technical dictionaries. (D.I. 145, 146). Both parties presented definitions that indicated "dynamic" refers to adjustment during operation in response to a change in needs. (D.I. 145, 146). I therefore adopt the following construction: "wherein the controller can adjust zone boundaries during operating conditions as the need arises such that assigned blocks from one logical zone are shifted to another logical zone."

4. **Term 4: "wherein the correspondence between physical blocks and logical address sections is adaptable by the controller in response to defects in the memory" ('498/43)**

    a. *Plaintiff's proposed construction*: "the controller can adjust zone boundaries such that blocks from one logical zone are shifted to another logical zone in response to defects occurring in the memory"

    b. *Defendant's proposed construction*: "wherein the controller can detect defects and adjust zone boundaries between zones such that blocks from one logical zone are shifted to another logical zone to balance the number of good blocks across the zones"

    c. *Court's construction*: "wherein the controller can adjust zone boundaries such that assigned blocks from one logical zone are shifted to another logical zone in response to defects occurring in the memory"

The parties dispute whether, as with claim 1 of the '498 Patent, the claim language should be limited to adjusting zone boundaries for the purpose of balancing the number of good blocks across zones. (D.I. 133 at 43, 45). The language of claim 1 and claim 43 of the '498 patent is identical except for the words "in response to defects in the memory."

The Federal Circuit clearly indicated that the construction "blocks from one logical zone are shifted to another logical zone" also "holds true for claim 43." *Innovative Memory Sys.*, 781 F. App'x. at 1016. I therefore come to the same conclusions for the rest of the term language as I did for claim 1: "blocks" should be modified to "assigned blocks," "wherein" should be included at the beginning of the construction, and no limitation of purpose is necessary when "blocks from one logical zone are shifted to another logical zone."

I accordingly adopt the following modified version of Plaintiff's construction: "wherein the controller can adjust zone boundaries such that assigned blocks from one logical zone are shifted to another logical zone in response to defects occurring in the memory."

V. CONCLUSION

Within five days the parties shall submit a proposed order consistent with this Memorandum Opinion suitable for submission to the jury.