**UNITED STATES DISTRICT COURT**

**DISTRICT OF OREGON**

**PORTLAND DIVISION**

**MENTOR GRAPHICS CORPORATION**, an Oregon Corporation,

Plaintiff/Counter-defendant,

v.

**EVE-USA, INC.**, a Delaware corporation; and **SYNOPSYS EMULATION AND VERIFICATION S.A.,** formed under the laws of France,

Defendants/Counter-claimants.

**SYNOPSYS, INC.**, a Delaware corporation; **EVE-USA, INC.**, a Delaware corporation; and **SYNOPSYS EMULATION AND VERIFICATION S.A.**, formed under the laws of France,

Plaintiffs/Counter-defendants

v.

**MENTOR GRAPHICS CORPORATION**, an Oregon corporation,

Defendant/Counter-claimant.

Case No. 3:10-cv-954-MO (lead)
Case No. 3:12-cv-1500-MO
Case No. 3:13-cv-579-MO

OPINION AND ORDER

**MOSMAN, J.**,

On February 24, 2014, I held a claim construction hearing in the above-entitled patent actions. At issue were claim terms appearing in U.S. Patent Nos. 7,069,526 ("'526 patent"), 6,240,376 ("'376 patent"), 5,649,176 ("'176 patent"), 6,009,531 ("'531 patent), and 6,947,882 ("'882 patent"). In this Order, I announce my constructions of the following terms:

| Claim Term | Construction |
|---|---|
| *'526 Patent* | |
| design visibility | "monitoring the entire or partial state of the DUT at, and relative to, predetermined events" |
| design patching | "altering the behavior of the DUT to a predetermined particular desired state at predetermined events" |
| design control | "methods to specify the events that control design visibility and design patching" |
| instrumentation circuitry | "additional circuitry to facilitate debugging" |
| aspect | "portion" |
| integrated circuit product | "one or more manufactured or configured chips that implement a design in the target technology" |
| *'376 Patent* | |
| gate-level netlist | "a list of gates and their inputs, outputs, and interconnects" |
| gate-level design | "a list of gates and their inputs, outputs, and interconnects" |
| instrumentation signal | "output signal added or preserved during logic synthesis that indicates whether a corresponding RTL source code statement is active" |
| simulating a gate-level design | "modeling the operation of a gate level design using software and/or hardware" |
| sensitivity list | "a list of signals to which a process is responsive" |
| process | "a description of the behavior of some portion of a circuit design" |
| generating logic | "generating gates" |
| *'176 and '531 Patents* | |
| logic system | "a system including one or more configurable logic devices into which the circuit design under test is configured" |
| configurable logic system | "a system including one or more configurable logic devices into which the circuit design under test is configured" |
| environment | "a real or simulated system or circuit, external to the configurable logic system, in which the circuit design under test is intended to operate" |

| | |
|---|---|
| environmental timing signal | "a timing signal, originating from the environment and received by the logic system, with a frequency that is lower than the internal clock frequency" |
| internal clock signal | "a signal existing within the configurable logic system and invisible to the environment that provides a time base for scheduling the operation of the resynthesized circuit" |
| *'882 Patent* | |
| reconfigurable logic device | "chip that includes a plurality of reconfigurable logic elements and input/output circuitry" |
| first plurality of reconfigurable logic devices | "two or more reconfigurable logic devices, none of which are included in the second plurality of reconfigurable logic devices or the third plurality of reconfigurable logic devices" |
| second plurality of reconfigurable logic devices | "two or more reconfigurable logic devices, none of which are included in the first plurality of reconfigurable logic devices or the third plurality of reconfigurable logic devices" |
| third plurality of reconfigurable logic devices | "two or more reconfigurable logic devices, none of which are included in the first plurality of reconfigurable logic devices or the second plurality of reconfigurable logic devices" |
| interconnect device | This term no longer appears in any patent claim at issue. |
| time multiplexed interconnection | "structure capable of receiving data from each reconfigurable logic device in one plurality and transmitting the data to each reconfigurable logic device in another plurality" |
| "independent" clocking | "wherein there is no required timing relationship between clock edges"[1] |
| circuit design | "a design for an integrated circuit" |
| emulation system | "a system capable of reproducing the operation of a circuit design through steps including mapping the circuit design onto hardware" |
| emulator | "a system capable of reproducing the operation of a circuit design through steps including mapping the circuit design onto hardware" |

IT IS SO ORDERED.

DATED this 6th day of March, 2014.

/s/ Michael W. Mosman
MICHAEL W. MOSMAN
United States District Judge

[1] I remain uncertain as to whether the construction of this term should include further language referring specifically to the structures recited in claims 1 and 5 of the '882 patent. I invite the parties to submit any comments on this question by way of an email to my courtroom deputy clerk before the end of business on Friday, March 14, 2014.