**IN THE UNITED STATES DISTRICT COURT**
**FOR THE EASTERN DISTRICT OF TEXAS**
**MARSHALL DIVISION**

SEMCON IP INC.,
*Plaintiff,*

v.

AMAZON.COM, INC.,
*Defendant.*

Case No. 2:18-cv-00192-JRG

**CLAIM CONSTRUCTION MEMORANDUM OPINION AND ORDER**

Before the Court is the opening claim construction brief of Semcon IP Inc. ("Plaintiff") (Dkt. No. 48, filed on March 20, 2019),[1] the response of Amazon.com, Inc. ("Defendant") (Dkt. No. 50, filed on April 3, 2019), and Plaintiff's reply (Dkt. No. 53, filed on April 10, 2019). The Court held a hearing on the issues of claim construction and claim definiteness on May 2, 2019. Having considered the arguments and evidence presented by the parties at the hearing and in their briefing, the Court issues this Order.

[1] Citations to the parties' filings are to the filing's number in the docket (Dkt. No.) and pin cites are to the page numbers assigned through ECF.

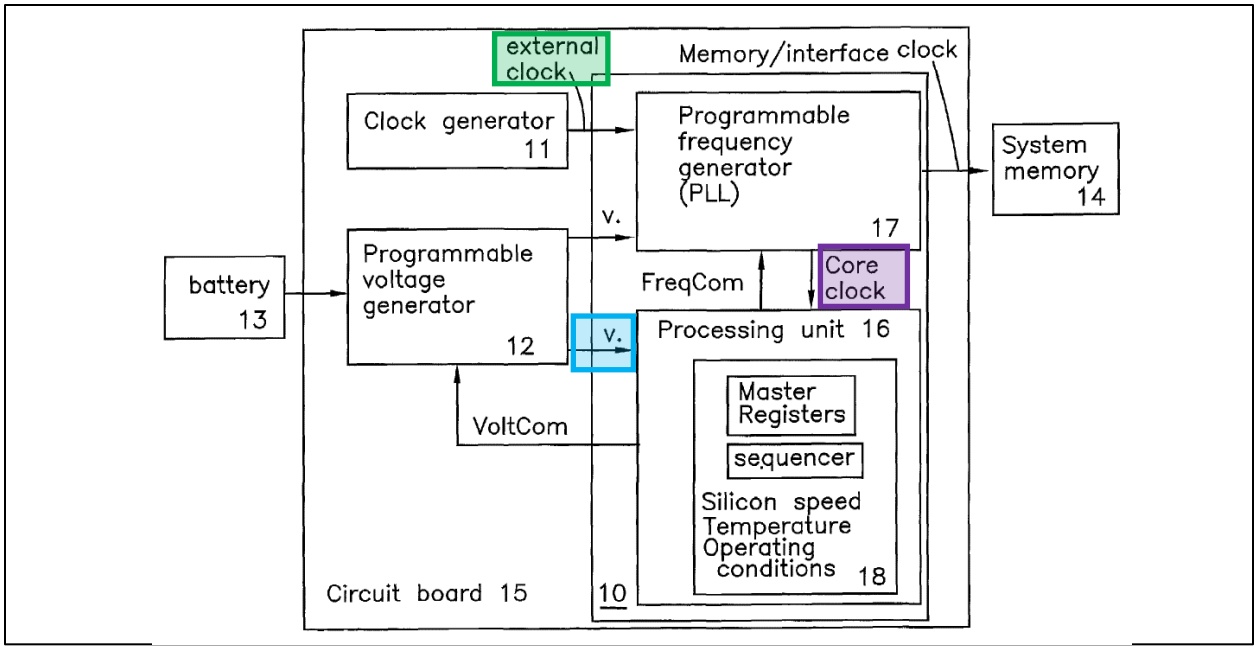
## Table of Contents

## I. BACKGROUND

Plaintiff alleges infringement of four U.S. Patents: No. 7,100,061 (the "'061 Patent"), No. 7,596,708 (the "'708 Patent"), No. 8,566,627 (the "'627 Patent"), and No. 8,806,247 (the "'247 Patent") (collectively, the "Asserted Patents"). These patents are related through a series of continuation applications and all ultimately claim priority to the application that issued as the '061 Patent, which was filed on January 18, 2000. The '061 Patent was subject to an inter partes reexamination requested on June 13, 2007 and from which a certificate issued on August 4, 2009.

The Court previously construed terms of the Asserted Patents in *Semcon IP Inc. v. Huawei Device USA Inc. et al.*, No. 2:16-cv-00437-JRG-RSP, 2017 U.S. Dist. LEXIS 108040 (E.D. Tex. July 12, 2017) ("*Huawei*"). Several of the terms now before the Court were construed in *Huawei*.

The Asserted Patents are generally directed to technology for managing a computer system's power consumption by dynamically adjusting the processor's operating frequency and voltage. The technology of the patents may be generally understood with reference to Figure 1 of the '061 Patent, produced here and annotated by the Court. A frequency generator (17) receives an external or "slow" clock (green) and from that generates a processor or "core" clock (purple) for operating



the processor's processing unit (16). The generator (17) also provides other clocks for various system-memory and other components. '061 Patent col.3 ll.18–26. As shown in the figure, a voltage generator (12) that is connected to a power supply (13) provides a voltage (blue) to the processor's processing unit 16. *See id*. at col.2 ll.46–57. The processor's power consumption and operability are related to the voltage and core-clock frequency. *See, e.g., id*. at col.1 ll.39–47, col.7 ll.39–60.

The abstracts of the Asserted Patents are identical and provide as follows:

> A method for controlling the power used by a computer including the steps of measuring the operating characteristics of a central processor of the computer, determining when the operating characteristics of the central processor are significantly different than required by the operations being conducted, and changing the operating characteristics of the central processor to a level commensurate with the operations being conducted.

Claims 1 and 17 of the '247 Patent, exemplary method and system claims respectively, provide:

> **1.** A method, comprising:
> determining a level of permitted power consumption by a processing device from a set of operating conditions of the processing device, with the determining the level of permitted power consumption not based upon instructions to be executed by the processing device;
> determining a highest allowable frequency of operation of the processing device that would result in power consumption not exceeding the level of permitted power consumption;
> determining a lowest allowable level of voltage to apply to the processing device that would allow execution of the instructions by the processing device at the highest allowable frequency; and
> changing power consumption of the processing device during execution of the instructions by reducing a magnitude of a difference between an operating frequency of the processing device and the highest allowable frequency of operation of the processing device and reducing a magnitude of a difference between a voltage applied to the processing device and the lowest allowable level of voltage.
>
> **17.** An apparatus, comprising:
> a frequency generator configured to generate a first clock signal at a first frequency; and
> a processing device configured to receive the first clock signal and a first

> voltage provided by a voltage source, the processing device operable to monitor operating parameters of the processing device, the processing device operable to determine a second frequency of the first clock signal and a second voltage for operation of the processing device at lower power than operation at the first frequency and the first voltage, with the processing device operable to determine the second frequency and the second voltage not based on instructions to be executed by the processing device, the processing device operable to control the frequency generator to change from generating the first clock signal at the first frequency to generating the first clock signal at a second frequency, and the processing device operable to control the voltage source to change from providing the first voltage to providing the second voltage during execution of the instructions by the processing device.

## II. LEGAL PRINCIPLES

### A. Claim Construction

"It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (quoting *Innova/Pure Water Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). To determine the meaning of the claims, courts start by considering the intrinsic evidence. *Id.* at 1313; *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 861 (Fed. Cir. 2004); *Bell Atl. Network Servs., Inc. v. Covad Commc'ns Group, Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001). The intrinsic evidence includes the claims themselves, the specification, and the prosecution history. *Phillips*, 415 F.3d at 1314; *C.R. Bard, Inc.*, 388 F.3d at 861. The general rule—subject to certain specific exceptions discussed *infra*—is that each claim term is construed according to its ordinary and accustomed meaning as understood by one of ordinary skill in the art at the time of the invention in the context of the patent. *Phillips*, 415 F.3d at 1312–13; *Alloc, Inc. v. Int'l Trade Comm'n*, 342 F.3d 1361, 1368 (Fed. Cir. 2003); *Azure Networks, LLC v. CSR PLC*, 771 F.3d 1336, 1347 (Fed. Cir. 2014) ("There is a heavy presumption that claim terms carry their accustomed meaning in the relevant community at the relevant time.") (vacated on other grounds).

"The claim construction inquiry … begins and ends in all cases with the actual words of the claim." *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1248 (Fed. Cir. 1998). "[I]n all aspects of claim construction, 'the name of the game is the claim.'" *Apple Inc. v. Motorola, Inc.*, 757 F.3d 1286, 1298 (Fed. Cir. 2014) (quoting *In re Hiniker Co.*, 150 F.3d 1362, 1369 (Fed. Cir. 1998)). First, a term's context in the asserted claim can be instructive. *Phillips*, 415 F.3d at 1314. Other asserted or non-asserted claims can also aid in determining the claim's meaning because claim terms are typically used consistently throughout the patent. *Id.* Differences among the claim terms can also assist in understanding a term's meaning. *Id*. For example, when a dependent claim adds a limitation to an independent claim, it is presumed that the independent claim does not include the limitation. *Id*. at 1314–15.

"[C]laims 'must be read in view of the specification, of which they are a part.'" *Id*. (quoting *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc)). "[T]he specification 'is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.'" *Id*. (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)); *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1325 (Fed. Cir. 2002). "'Although the specification may aid the court in interpreting the meaning of disputed claim language, particular embodiments and examples appearing in the specification will not generally be read into the claims.'" *Comark Commc'ns, Inc. v. Harris Corp.*, 156 F.3d 1182, 1187 (Fed. Cir. 1998) (quoting *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1571 (Fed. Cir. 1988)); *see also Phillips*, 415 F.3d at 1323. "[I]t is improper to read limitations from a preferred embodiment described in the specification—even if it is the only embodiment—into the claims absent a clear indication in the intrinsic record that the

patentee intended the claims to be so limited." *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004).

The prosecution history is another tool to supply the proper context for claim construction because, like the specification, the prosecution history provides evidence of how the U.S. Patent and Trademark Office ("PTO") and the inventor understood the patent. *Phillips*, 415 F.3d at 1317. However, "because the prosecution history represents an ongoing negotiation between the PTO and the applicant, rather than the final product of that negotiation, it often lacks the clarity of the specification and thus is less useful for claim construction purposes." *Id.* at 1318; *see also Athletic Alternatives, Inc. v. Prince Mfg.*, 73 F.3d 1573, 1580 (Fed. Cir. 1996) (ambiguous prosecution history may be "unhelpful as an interpretive resource").

Although extrinsic evidence can also be useful, it is "'less significant than the intrinsic record in determining the legally operative meaning of claim language.'" *Phillips*, 415 F.3d at 1317 (quoting *C.R. Bard, Inc.*, 388 F.3d at 862). Technical dictionaries and treatises may help a court understand the underlying technology and the manner in which one skilled in the art might use claim terms, but technical dictionaries and treatises may provide definitions that are too broad or may not be indicative of how the term is used in the patent. *Id*. at 1318. Similarly, expert testimony may aid a court in understanding the underlying technology and determining the particular meaning of a term in the pertinent field, but an expert's conclusory, unsupported assertions as to a term's definition are not helpful to a court. *Id*. Extrinsic evidence is "less reliable than the patent and its prosecution history in determining how to read claim terms." *Id*. The Supreme Court recently explained the role of extrinsic evidence in claim construction:

> In some cases, however, the district court will need to look beyond the patent's intrinsic evidence and to consult extrinsic evidence in order to understand, for example, the background science or the meaning of a term in the relevant art during the relevant time period. *See, e.g., Seymour v. Osborne*, 11 Wall. 516, 546 (1871)

> (a patent may be "so interspersed with technical terms and terms of art that the testimony of scientific witnesses is indispensable to a correct understanding of its meaning"). In cases where those subsidiary facts are in dispute, courts will need to make subsidiary factual findings about that extrinsic evidence. These are the "evidentiary underpinnings" of claim construction that we discussed in *Markman*, and this subsidiary factfinding must be reviewed for clear error on appeal.

*Teva Pharm. USA, Inc. v. Sandoz, Inc.*, 135 S. Ct. 831, 841 (2015).

### B. Departing from the Ordinary Meaning of a Claim Term

There are "only two exceptions to [the] general rule" that claim terms are construed according to their plain and ordinary meaning: "1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of the claim term either in the specification or during prosecution."[2] *Golden Bridge Tech., Inc. v. Apple Inc.*, 758 F.3d 1362, 1365 (Fed. Cir. 2014) (quoting *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012)); *see also GE Lighting Solutions, LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014) ("[T]he specification and prosecution history only compel departure from the plain meaning in two instances: lexicography and disavowal."). The standards for finding lexicography or disavowal are "exacting." *GE Lighting Solutions*, 750 F.3d at 1309.

To act as his own lexicographer, the patentee must "clearly set forth a definition of the disputed claim term," and "clearly express an intent to define the term." *Id.* (quoting *Thorner*, 669 F.3d at 1365); *see also Renishaw*, 158 F.3d at 1249. The patentee's lexicography must appear "with reasonable clarity, deliberateness, and precision." *Renishaw*, 158 F.3d at 1249.

To disavow or disclaim the full scope of a claim term, the patentee's statements in the specification or prosecution history must amount to a "clear and unmistakable" surrender. *Cordis*

[2] Some cases have characterized other principles of claim construction as "exceptions" to the general rule, such as the statutory requirement that a means-plus-function term is construed to cover the corresponding structure disclosed in the specification. *See, e.g., CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1367 (Fed. Cir. 2002).

*Corp. v. Boston Sci. Corp.*, 561 F.3d 1319, 1329 (Fed. Cir. 2009); *see also Thorner*, 669 F.3d at 1366 ("The patentee may demonstrate intent to deviate from the ordinary and accustomed meaning of a claim term by including in the specification expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope."). "Where an applicant's statements are amenable to multiple reasonable interpretations, they cannot be deemed clear and unmistakable." *3M Innovative Props. Co. v. Tredegar Corp.*, 725 F.3d 1315, 1326 (Fed. Cir. 2013).

### C. Functional Claiming and 35 U.S.C. § 112, ¶ 6 (pre-AIA) / § 112(f) (AIA)[3]

A patent claim may be expressed using functional language. *See* 35 U.S.C. § 112, ¶ 6; *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1347–49 & n.3 (Fed. Cir. 2015) (en banc in relevant portion). Section 112, Paragraph 6, provides that a structure may be claimed as a "means … for performing a specified function" and that an act may be claimed as a "step for performing a specified function." *Masco Corp. v. United States*, 303 F.3d 1316, 1326 (Fed. Cir. 2002).

However, § 112, ¶ 6 does not apply to all functional claim language. There is a rebuttable presumption that § 112, ¶ 6 applies when the claim language includes "means" or "step for" terms, and that it does not apply in the absence of those terms. *Masco Corp.*, 303 F.3d at 1326; *Williamson*, 792 F.3d at 1348. The presumption stands or falls according to whether one of ordinary skill in the art would understand the claim with the functional language, in the context of the entire specification, to denote sufficiently definite structure or acts for performing the function. *See Media Rights Techs., Inc. v. Capital One Fin. Corp.*, 800 F.3d 1366, 1372 (Fed. Cir. 2015) (§ 112, ¶ 6 does not apply when "the claim language, read in light of the specification, recites sufficiently definite structure" (quotation marks omitted) (citing *Williamson*, 792 F.3d at 1349;

[3] The Court refers to the pre-AIA version of § 112 but understands that there is no substantial difference between functional claiming under the pre-AIA version and under the AIA version of the statute.

*Robert Bosch, LLC v. Snap-On Inc.*, 769 F.3d 1094, 1099 (Fed. Cir. 2014))); *Williamson*, 792 F.3d at 1349 (§ 112, ¶ 6 does not apply when "the words of the claim are understood by persons of ordinary skill in the art to have sufficiently definite meaning as the name for structure"); *Masco Corp.*, 303 F.3d at 1326 (§ 112, ¶ 6 does not apply when the claim includes an "act" corresponding to "how the function is performed"); *Personalized Media Communications, L.L.C. v. International Trade Commission*, 161 F.3d 696, 704 (Fed. Cir. 1998) (§ 112, ¶ 6 does not apply when the claim includes "sufficient structure, material, or acts within the claim itself to perform entirely the recited function … even if the claim uses the term 'means.'" (quotation marks and citation omitted)).

When it applies, § 112, ¶ 6 limits the scope of the functional term "to only the structure, materials, or acts described in the specification as corresponding to the claimed function and equivalents thereof." *Williamson*, 792 F.3d at 1347. Construing a means-plus-function limitation involves multiple steps. "The first step … is a determination of the function of the means-plus-function limitation." *Medtronic, Inc. v. Advanced Cardiovascular Sys., Inc.*, 248 F.3d 1303, 1311 (Fed. Cir. 2001). "[T]he next step is to determine the corresponding structure disclosed in the specification and equivalents thereof." *Id.* A "structure disclosed in the specification is 'corresponding' structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim." *Id.* The focus of the "corresponding structure" inquiry is not merely whether a structure is capable of performing the recited function, but rather whether the corresponding structure is "clearly linked or associated with the [recited] function." *Id.* The corresponding structure "must include all structure that actually performs the recited function." *Default Proof Credit Card Sys. v. Home Depot U.S.A., Inc.*, 412 F.3d 1291, 1298 (Fed. Cir. 2005). However, § 112 does not permit "incorporation of structure from the written

description beyond that necessary to perform the claimed function." *Micro Chem., Inc. v. Great Plains Chem. Co.*, 194 F.3d 1250, 1258 (Fed. Cir. 1999).

For § 112, ¶ 6 limitations that are implemented by a programmed general purpose computer or microprocessor, the corresponding structure described in the patent specification must include an algorithm for performing the function. *WMS Gaming Inc. v. Int'l Game Tech.*, 184 F.3d 1339, 1349 (Fed. Cir. 1999). The corresponding structure is not a general purpose computer but rather the special purpose computer programmed to perform the disclosed algorithm. *Aristocrat Techs. Austl. Pty Ltd. v. Int'l Game Tech.*, 521 F.3d 1328, 1333 (Fed. Cir. 2008).

### D. Definiteness Under 35 U.S.C. § 112, ¶ 2 (pre-AIA) / § 112(b) (AIA)[4]

Patent claims must particularly point out and distinctly claim the subject matter regarded as the invention. 35 U.S.C. § 112, ¶ 2. A claim, when viewed in light of the intrinsic evidence, must "inform those skilled in the art about the scope of the invention with reasonable certainty." *Nautilus Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 910 (2014). If it does not, the claim fails § 112, ¶ 2 and is therefore invalid as indefinite. *Id.* at 901. Whether a claim is indefinite is determined from the perspective of one of ordinary skill in the art as of the time the application for the patent was filed. *Id.* at 911. As it is a challenge to the validity of a patent, the failure of any claim in suit to comply with § 112 must be shown by clear and convincing evidence. *BASF Corp. v. Johnson Matthey Inc.*, 875 F.3d 1360, 1365 (Fed. Cir. 2017). "[I]ndefiniteness is a question of law and in effect part of claim construction." *ePlus, Inc. v. Lawson Software, Inc.*, 700 F.3d 509, 517 (Fed. Cir. 2012).

[4] The Court refers to the pre-AIA version of § 112 but understands that there is no substantial difference between definiteness under the pre-AIA version and under the AIA version of the statute.

When a term of degree is used in a claim, "the court must determine whether the patent provides some standard for measuring that degree." *Biosig Instruments, Inc. v. Nautilus, Inc.*, 783 F.3d 1374, 1378 (Fed. Cir. 2015) (quotation marks omitted). Likewise, when a subjective term is used in a claim, "the court must determine whether the patent's specification supplies some standard for measuring the scope of the [term]." *Datamize, LLC v. Plumtree Software, Inc.*, 417 F.3d 1342, 1351 (Fed. Cir. 2005). The standard "must provide objective boundaries for those of skill in the art." *Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1371 (Fed. Cir. 2014).

In the context of a claim governed by 35 U.S.C. § 112, ¶ 6, the claim is invalid as indefinite if the claim fails to disclose adequate corresponding structure to perform the claimed function. *Williamson*, 792 F.3d at 1351–52. The disclosure is inadequate when one of ordinary skill in the art "would be unable to recognize the structure in the specification and associate it with the corresponding function in the claim." *Id*. at 1352.

## III. AGREED CONSTRUCTIONS

The parties have agreed to the following constructions set forth in their Joint Claim Construction Chart (Dkt. No. 54).

| Term[5] | Agreed Construction |
|---|---|
| "means for executing instructions … where said means for executing instructions cannot function at said first frequency and said second voltage"<br><br>• Dkt. No. 54-1 at 16, Agreed No. 1 | This claim is governed by 35 U.S.C. § 112(6).<br><br>**function**: executing instructions ... where said means for executing instructions cannot function at said first frequency and said second voltage.<br><br>**structure:** Processing unit 16. |

[5] For all term charts in this order, the terms in dispute are identified by reference to the appendix to the Parties' Joint Claim Construction Chart (Dkt. No. 54-1).

| Term[5] | Agreed Construction |
|---|---|
| "programmable power supply" / "programmable voltage supply"<br><br>• Dkt. No. 54-1 at 17, Agreed No. 2 | power supply configured to provide one of a plurality of distinct voltage levels specified by an input |
| "a selectable voltage"<br><br>• Dkt. No. 54-1 at 17, Agreed No. 3 | one of a plurality of distinct voltage levels specified by an input |
| "voltage source includes a programmable voltage supply"<br><br>• Dkt. No. 54-1 at 17, Agreed No. 4 | voltage source includes a power supply configured to provide one of a plurality of distinct voltage levels specified by an input |
| "power supply furnishing selectable output voltages" / "power supply … configured to furnish a selectable voltage"<br><br>• Dkt. No. 54-1 at 18, Agreed No. 5 | power supply providing one of a plurality of distinct voltage levels corresponding to an input / a power supply configured to provide one of a plurality of distinct voltage levels specified by an input |
| "idle time"<br><br>• Dkt. No. 54-1 at 18, Agreed No. 6 | time spent in an idle state |
| "idle state(s)" / "idle states of said computer processor" / "plurality of idle states of said computer processor"<br><br>• Dkt. No. 54-1 at 18, Agreed No. 7 | state in which various components of the system are quiescent |
| "halt time"<br><br>• Dkt. No. 54-1 at 18, Agreed No. 8 | state in which the core clock has been stopped but the processor responds to most interrupts |
| "reducing [a/the] magnitude of a difference …"<br><br>• Dkt. No. 54-1 at 19, Agreed No. 9 | reducing the absolute value of the difference … |
| "monitoring idle time of said computer processor/monitoring [internal data of said computer processor relating to] the amount of time spent in a plurality of idle states"<br><br>• Dkt. No. 54-1 at 19, Agreed No. 10 | plain and ordinary meaning |
| "monitoring a halt state"<br><br>• Dkt. No. 54-1 at 19, Agreed No. 11 | plain and ordinary meaning |

| Term[5] | Agreed Construction |
|---|---|
| "monitoring idle states of said computer processor"<br><br>• Dkt. No. 54-1 at 19, Agreed No. 12 | plain and ordinary meaning |
| "[monitoring/monitors/monitor] a temperature"<br><br>• Dkt. No. 54-1 at 19, Agreed No. 13 | plain and ordinary meaning |
| "monitoring a thermal condition operating characteristic"<br><br>• Dkt. No. 54-1 at 20, Agreed No. 14 | plain and ordinary meaning |
| "monitoring internal conditions of a computer processor"<br><br>• Dkt. No. 54-1 at 20, Agreed No. 15 | plain and ordinary meaning |
| "computer processor monitoring operating conditions internal to said computer processor"<br><br>• Dkt. No. 54-1 at 20, Agreed No. 16 | plain and ordinary meaning |
| "monitoring [an] operating characteristic[s] of said [computer] processor /monitors [one or more] operating characteristics of said [processor/apparatus]"<br><br>• Dkt. No. 54-1 at 20, Agreed No. 17 | plain and ordinary meaning |
| "monitoring operating conditions of [a/said] processing unit"<br><br>• Dkt. No. 54-1 at 20, Agreed No. 18 | plain and ordinary meaning |
| "[monitoring/monitor] operating parameters of the processing device"<br><br>• Dkt. No. 54-1 at 21, Agreed No. 19 | plain and ordinary meaning |

Having reviewed the intrinsic and extrinsic evidence of record, the Court hereby adopts the parties' agreed constructions.

## IV. CONSTRUCTION OF DISPUTED TERMS

### A. "computer processor," "processor," "central processor," "processing unit," and "processing device"

| Disputed Term | Plaintiff's Proposed Construction | Defendant's Proposed Construction |
|---|---|---|
| "computer processor" / "processor" / "central processor"<br><br>• Dkt. No. 54-1 at 3, No. 2 | CPU | CPU. Each core of a multi-core processor is a CPU. |
| "processing unit" / "processing device"<br><br>• Dkt. No. 54 1 at 3, No. 3 | computing portion of CPU | Computing portion of CPU. Each core of a multi-core processor is a CPU. |

Since the parties' arguments and proposed constructions with respect to these terms are related, the Court addresses the terms together.

**The Parties' Positions**

Plaintiff submits: Its proposed constructions are those issued by the Court in *Huawei*[6]. The issue of whether the core of a multi-core processor satisfies the limitations as previously construed is an issue of infringement, not of claim construction. Dkt. No. 48 at 11–13.

In addition to the claims themselves, Plaintiff cites the following **extrinsic evidence** to support its position: Thornton Decl.[7] ¶¶ 39–40, 42–44 (Plaintiff's Ex. F, Dkt. No. 48-7 at 14–17).

Defendant responds: These terms need to be construed to clarify that the CPU that experiences the claimed voltage or frequency change is the CPU that experiences the claimed clock or

[6] *Semcon IP Inc.* v. *Huawei Device USA Inc.*, No. 2:16-cv-00437-JRG-RSP, 2017 U.S. Dist. LEXIS 108040 (E.D. Tex. July 12, 2017).

[7] Expert Declaration of Mitchell A. Thornton, Ph.D., P.E. Regarding the Proposed Constructions and/or Indefiniteness of the Asserted Claims of U.S. Patent Nos. 7,100,061, 7,596,708, 8,566,627, and 8,806,247.

instruction state (stopped or not stopped). This matters because multicore processors have multiple CPUs—each core is a CPU. Dkt. No. 50 at 8–12.

In addition to the claims themselves, Defendant cites the following **extrinsic evidence** to support its position: Thornton Decl. ¶¶ 42–44 (Defendant's Ex. H, Dkt. No. 50-9 at 15–17); Diefendorff, *Power4 Focuses on Memory Bandwidth: IBM Confronts IA-64, Says ISA Not Important*, Microdesign Resources: Microprocessor Report (Oct. 6, 1999) (Defendant's Ex. I, Dkt. No. 50-10); L. Hammond, *The Stanford Hydra CMP*, IEEE MICRO (2000) (Defendant's Ex. J, Dkt. No. 50-11).

Plaintiff replies: The issue of whether each core in a multi-core processor is a CPU is not an issue of claim construction. Rather, Defendant's proposed construction is simply an attempt to improperly resolve infringement at the claim-construction stage. Dkt. No. 53 at 4–5.

**Analysis**

The issue in dispute distills to whether the Court should construe "multi-core processor." Given that "multi-core processor" is not a term in the Asserted Patents, the Court declines at this stage to rule on whether any claim reads on a multi-core processor.

To begin, the construction in *Huawei* was directed to resolving the dispute over whether the processor and processing-unit terms of the claims necessarily exclude an operating system because of statements made during prosecution of the '061 Patent. *Huawei*, 2017 U.S. Dist. LEXIS 108040, at *20–21. There was not a substantial dispute regarding whether the processor terms of the claims referred to a "CPU" and whether the processing-unit terms referred to the "computing portion of CPU." *Id*. at *17–26. Specifically, *Huawei* did not construe the processor terms in the context of any dispute over whether the scope of the terms includes or excludes multi-core processors.

The Court understands that the processor and processing-unit terms in the claims refer to a CPU and the computing portion of a CPU, respectively. The Court further understands that recitals of "the" or "said" processor or processing unit/device in a claim plainly refer to the same processor or processing unit/device, respectively. That said, the Court declines to rule as an issue of claim construction whether every multi-core processor is necessarily comprised of multiple processors. Whether a particular accused processor or processing unit satisfies the processor / processing-unit limitations is a factual issue of infringement, not an issue of claim construction.

Accordingly, and as explained in *Huawei*,[8] the Court hereby construes the terms as follows:

- **"computer processor"** means **"CPU"**;
- **"processor"** means **"CPU"**;
- **"central processor"** means **"CPU"**;
- **"processing unit"** means **"computing portion of CPU"**; and
- **"processing device"** means **"computing portion of CPU."**

### B. The Changing-the-Voltage-While-Executing-Instructions Terms

| Disputed Term | Plaintiff's Proposed Construction | Defendant's Proposed Construction |
|---|---|---|
| • Dkt. No. 54-1 at 10–11, No. 37 | plain and ordinary meaning | the [processor/processing unit] does not stop the core clock to the [processor/processing unit] and continues execution of instructions in the period of time that the voltage is changing |

Since the parties' arguments and proposed constructions with respect to these terms are related, the Court addresses the terms together.

[8] *Huawei*, 2017 U.S. Dist. LEXIS 108040, at *17–26.

**The Parties' Positions**

Plaintiff submits: The meaning of these terms is clear without construction. As the Court held in *Huawei*, changing the voltage while instructions are being executed does not require that the clock remain "operational at all times during the voltage change." Dkt. No. 48 at 15.

In addition to the claims themselves, Plaintiff cites the following intrinsic and extrinsic evidence to support its position: **Intrinsic evidence**: '061 Patent col.6 ll.16–29. **Extrinsic evidence**: Carbonell Decl.[9] ¶¶ 42–46 (Plaintiff's Ex. E, Dkt. No. 48-6 at 18–19); Thornton Decl. ¶¶ 58–60 (Plaintiff's Ex. F, Dkt. No. 48-7 at 24–25).

Defendant responds: These terms need to be construed to clarify that the core clock of the processor is not stopped and instructions are executed "at least during some point in the period of time that the voltage is changing between a first and a second voltage." This is the rationale underlying the Court's holding in *Huawei*. This is distinct from a situation in which the clock is active and instructions are executed after the command to change the voltage and before the voltage actually begins to change, but the clock is not active and instructions are not executed while the voltage is actually changing. During prosecution of the '061 Patent, the patentee distinguished the prior art on this point—the clock is active or instructions are executed at some point during an actual change in voltage. Dkt. No. 50 at 12–14.

In addition to the claims themselves, Defendant cites the following intrinsic and extrinsic evidence to support its position: **Intrinsic evidence**: '061 Patent File Wrapper August 3, 2004 Amendment and Response at 16–17 (Defendant's Ex. K, Dkt. No. 50-12 at 17–18), September 15, 2005 Reasons for Allowance at 2 (Defendant's Ex. C, Dkt. No. 50-4 at 6), March 6, 2006 Reasons

[9] Declaration of Jaime G. Carbonell, Ph.D. Regarding Proposed Constructions and Definiteness of the Asserted Claims of U.S. Patent Nos. 7,100,061, 7,596,708, 8,566,627, and 8,806,247.

for Allowance at 2 (Defendant's Ex. A, Dkt. No. 50-2 at 6); '708 Patent File Wrapper August 2, 2007 Reasons for Allowance at 2 (Defendant's Ex. B, Dkt. No. 50-3 at 6). **Extrinsic evidence**: Thornton Decl. ¶ 59 (Defendant's Ex. H, Dkt. No. 50-9 at 24–25).

Plaintiff replies: The Court did not hold in *Huawei* that the "core clock" must be functional at some point during a voltage change. This is important because while execution of instructions may require operation of a clock, it does not necessarily require operation of the ***core*** clock. Further, the patents do not distinguish between the point at which the voltage change is caused and the point at which the voltage actually changes. Dkt. No. 53 at 7–8.

**Analysis**

The main issue in dispute is whether the claimed execution of instructions during a voltage change necessarily requires operation of the "core clock." It does.

To begin, the construction in *Huawei* was directed to resolving the dispute over whether the clock must run at all times during a voltage change. *Huawei*, 2017 U.S. Dist. LEXIS 108040, at *37. The Court there held that while "the clock is necessarily operational at least at some point during the voltage change" it is not "not necessarily … operational at all times during the voltage change." *Id*. at *37–40. That is, in order to execute instructions, or to be able to execute instructions,[10] during the voltage change the clock must be operational at some point during the voltage change. *Id*. The Court held that this is the plain meaning of the terms. The Court reiterates that holding here and further clarifies that the plain meaning of "changing the … voltage" and similar constructs is that the voltage change is actual, not simply requested or initiated or otherwise

[10] For example, Claim 1 of the '061 Patent recites "executing instructions in said computer processor while changing the voltage." Claim 26 of the '708 Patent recites "changing the operating voltage from a first voltage to a second voltage while the processing unit is enabled to execute instructions."

desired but not realized. The issue of which clock is used for executing instructions was not before the Court in *Huawei*.

In the Asserted Patents, the "core clock" must be enabled for a processor to be capable of executing instructions during the voltage change. For example, the patents provide:

> The [frequency] ***generator*** 17 responds to values furnished by control software executing on the processor to produce from the slow clock ***a core clock for operation of the processing unit 16***, one or more clocks for operation of the various system memory components shown as system memory 14 in the figure, the system bus, and any other components which might utilize[] a separate clock.

'061 Patent col.3 ll.20–23 (emphasis added). From this, the Court understands that the processor/processing-unit clock is the core clock. The patents further provide ways in which the processor voltage change will not disrupt the frequency generator so the instructions may be executed while the voltage is changing:

> For example, if increases of approximately 50 millivolts are enabled, then the ***frequency generator will remain stable*** during the voltage increase and a system reset will not occur. This ***offers the advantage*** that the processor may continue to execute commands during the period in which the voltage change is taking place.

*Id*. at col.6 ll.24–29. From this, the Court understands that the processor is able to execute instructions during a voltage change because the core clock continues to operate during a voltage change. In contrast, the processor is shut down by shutting down the core clock for a frequency change. *Id*. at col.6 ll.32 – col.7 l.5 ("operations of the processor are prepared for shut down," and the "sequencer … shut[s] down the core clock"). If the processor is able to execute commands during the voltage change based on other clocks, like the slow clock used by the generator to produce the core clock, the "***advantage***" of proceeding with a voltage change so as to not disrupt the frequency generator is illusory and the need to shut down operations of the processor for a frequency change is nonsensical. Further, the patents provide using an external clock for purposes

other than continued execution of instructions during the voltage change but describe execution of instructions solely with respect to the core clock. *See, e.g.*, *id*. at col.6 l.61–63.

The continued operation of the core clock to enable execution of instructions during the voltage change is ostensibly a point of novelty for the Asserted Patents. During prosecution of the '061 Patent, the patentee explained that "executing instructions …while changing voltage …" means "instructions … are clocked through a computer processor while changing the voltage." '061 Patent File Wrapper, August 3, 2004 Response at 16, Dkt. No. 50-12 at 17. This was a distinction over the prior art because the prior art disclosed that the "voltage change … occur[s] when the processor clock … is not running" and "[t]he ***processor cannot execute instructions while the processor clock is not running***." *Id*. at 17 (emphasis added), Dkt. No. 50-12 at 18. The patent examiner noted this distinction over the prior art in granting the '061 and '708 Patents. '061 Patent File Wrapper March 6, 2006 Reasons for Allowance at 2 ("the processor does not stop the clock"), Dkt. No. 50-2 at 6; '708 Patent Filer Wrapper August 2, 2007 Reasons for Allowance at 2 ("the processor is not suspended from executing instructions … meaning that the processor does not stop the clock"), Dkt. No. 50-3 at 6. Ultimately, the Court understands "executing instructions" during a voltage change refers to using the core clock to clock instructions through the processor. The processor of the claims is able to execute instructions during a voltage change because the core clock is enabled.

The Court rejects Defendant's proposed construction, however. First, the proposed construction requires the processor to "not stop the core clock … and continue[] execution of instructions in the period of time that the voltage is changing." While the Court understands that Defendant is not advocating that the clock is enabled at all times during a voltage change, Dkt. No. 50 at 13–14, its proposed construction seems to say just that. Second, some claims require

only the ability to execute instructions while others require actual execution of instructions. For example, Claim 1 of the '061 Patent recites "executing instructions in said computer processor while changing the voltage" and Claim 26 of the '708 Patent recites "changing the operating voltage from a first voltage to a second voltage while the processing unit is enabled to execute instructions."

Accordingly, the Court hereby construes these voltage-change terms by construing "executing instructions" and variants in those terms in the claims at issue as follows:

- **"executing … instructions"** means **"executing … instructions using the core clock"**;
- **"execution of … instructions"** means **"execution of … instructions using the core clock";**
- **"execute instructions"** means **"execute instructions using the core clock"**; and
- **"executes … instructions" means "executes … instructions using the core clock."**

### C. The Changing-the-Frequency-While-Execution-of-Instructions-is-Stopped Terms

| Disputed Term | Plaintiff's Proposed Construction | Defendant's Proposed Construction |
|---|---|---|
| • Dkt. No. 54-1 at 14, No. 47 | plain and ordinary meaning | the [processor/processing unit] stops the core clock to the [processor/processing unit] and does not execute instructions for the time that the frequency is changing |

Since the parties' arguments and proposed constructions with respect to these terms are related, the Court addresses the terms together.

**The Parties' Positions**

Plaintiff submits: These terms are not limited to require either stopping the core clock or cessation of execution of instructions at all times while the frequency is changing. With respect to stopping the core clock, dependent Claim 6 of the '708 Patent expressly requires "shutting down said clock." This means that the frequency change recited in Claim 1, from which Claim 6 depends, does not require shutting down the clock. With respect to whether the claims allow for a frequency change while executing instructions, the claims are open ended and it would be improper to read such a negative limitation into a positive requirement for frequency change while execution is stopped. Dkt. No. 48 at 21–22.

In addition to the claims themselves, Plaintiff cites the following **extrinsic evidence** to support its position: Carbonell Decl. ¶¶ 61–65 (Plaintiff's Ex. E, Dkt. No. 48-6 at 24–25).

Defendant responds: The intrinsic record is clear that the core clock and execution of instructions are both stopped for a frequency change. As explained in the Asserted Patents, the clock is shut down so that instructions cannot be executed. There is no support in the specification for allowing the clock to continue to run during a frequency change. Dkt. No. 50 at 14–16.

In addition to the claims themselves, Defendant cites the following intrinsic and extrinsic evidence to support its position: **Intrinsic evidence**: '708 Patent col.6 ll.26–67; '708 Patent File Wrapper June 29, 2007 Amendment and Response at 12 (Defendant's Ex. F, Dkt. No. 50-7 at 13); '627 Patent File Wrapper November 7, 2012 Response at 11 (Defendant's Ex. E, Dkt. No. 50-6 at 12). **Extrinsic evidence**: Thornton Decl. ¶ 87 (Defendant's Ex. H, Dkt. No. 50-9 at 34–35).

Plaintiff replies: These terms are distinct from the Shutting-Down-the-Clocks-in-Response to-a-Frequency-Change-Initiation terms. In these terms, there is no support for limiting the "clocks"

to "core clocks" or requiring the cessation of execution of instructions for the entire time the frequency changes. Dkt. No. 53 at 11–12.

Plaintiff cites further **intrinsic evidence** to support its position: '708 Patent File Wrapper June 29, 2007 Amendment and Response (Defendant's Ex. F, Dkt. No. 50-7).

**Analysis**

There are three issues in dispute. First, whether stopping execution of instructions during a frequency change necessarily means stopping the core clock. It does not. Second, whether the "clock" that is expressly stopped according to the claims is necessarily the core clock. It is. Third, whether the clock / execution of instructions is necessarily stopped for the entire time the frequency is changed. It is not.

Stopping execution of instructions does not necessarily require stopping the processor clock. Each of these terms fall into one of two general categories. The first category recites stopping execution of instructions for a frequency change. For example, Claim 23 recites: "processing unit that operates at [] a frequency responsive to a clock signal … stopping execution of instructions in said processing unit … [and] while instruction execution is stopped, adjusting said programmable frequency generator to change the frequency." The second category recites stopping the processor clock in order to stop execution of instructions. For example, Claim 25 of the '708 Patent recites: "The method of claim 23 wherein said stopping comprises stopping said clock signal." Thus, under the plain meaning of the claims, stopping execution of the instructions is distinct from stopping the clock. There is nothing in the intrinsic record to mandate that stopping execution necessarily requires stopping the processor clock. This is different from the execution of instructions during a voltage change discussed above, which the intrinsic record established requires operation of the processor clock. That executing instructions during a voltage change requires an operational

processor clock does not mean that not executing instructions requires stopping the clock. While the embodiments described in the patents do in fact stop the clock for the frequency change, this is not enough to read a stopping-the-clock limitation into all claims directed to changing the frequency—especially considering that some claims express stopping the clock and others do not. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1323 (Fed. Cir. 2005) (en banc) ("we have expressly rejected the contention that if a patent describes only a single embodiment, the claims of the patent must be construed as being limited to that embodiment"); *Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1366 (Fed. Cir. 2012) ("It is likewise not enough that the only embodiments, or all of the embodiments, contain a particular limitation. We do not read limitations from the specification into claims; we do not redefine words. Only the patentee can do that."); *SRI Int'l v. Matsushita Elec. Corp.*, 775 F.2d 1107, 1122 (Fed. Cir. 1985) (en banc) ("It is settled law that when a patent claim does not contain a certain limitation and another claim does, that limitation cannot be read into the former claim in determining either validity or infringement.").

The "clock" expressly stopped in the claims is the "core clock." The Court understands that the issues here are related to asserted Claims 6, 13, 19, and 22 of the '708 Patent which each expressly require stopping the "clock." Claim 6 states: "wherein the processor includes a clock and said changing said operating frequency further comprises: shutting down said clock." Claim 13 states: "wherein said processor includes a clock and said changing the frequency of operation further comprises: shutting down said clock." Claim 19, which depends from Claim 14, states: "wherein said causing adjustment comprises shutting down said clock." Claim 22, which depends from Claim 20, states: "wherein said adjusting said programmable frequency generator comprises stopping said clock signal." The clock or clock signal of Claims 6, 13, and 22 each expressly are the processor or processing-unit clock. For Claim 14, the clock is that provided to the 'means for

executing instructions" which the parties agree is the "processing unit 16" described in the patents. Dkt. No. 54-1 at 16–17, Agreed No. 1. Thus, as plainly stated, each clock of the claims at issue is the processor or processing-unit clock. As described above, this "processor clock" is the core clock. *See also*, '061 Patent col.3 ll.20–26; '061 Patent File Wrapper, August 3, 2004 Response at 16–17, Dkt. No. 50 12 at 17–18.

Neither the clock nor the execution of instructions is necessarily stopped for all frequency changes. The terms at issue are found in open-ended claims. Open-ended claims allow for unrecited structure or steps. *See, e.g.*, *In re Affinity Labs of Tex., LLC*, 856 F.3d 902, 907 (Fed. Cir. 2017). Thus, while the claims require changing the frequency while execution of instructions is stopped (which may or may not mean the clock is stopped), the claims do not thereby necessarily preclude also changing the frequency while execution of instructions is not stopped.

Accordingly, the Court rejects Defendant's proposals to limit the claims to require stopping the core clock in order to stop execution of instructions and to require that the execution and clock are stopped for all frequency changes. For the **terms that do not include the term "clock,"** the Court holds those terms to have their **plain and ordinary meaning** without the need for further construction. For the **clock terms at issue in Claims 6, 13, 19, and 22 of the '708 Patent**, the Court hereby construes **"clock"** to mean **"core clock"** and holds that the **terms otherwise have their plain and ordinary meaning** without the need for further construction.

### D. The Shutting-Down-the-Clocks-in-Response-to-a-Frequency-Change-Initiation Terms

| Disputed Term | Plaintiff's Proposed Construction | Defendant's Proposed Construction |
|---|---|---|
| • Dkt. No. 54-1 at 15, No. 48 | plain and ordinary meaning | the [processor/processing unit] stops the core clock to the [processor/processing unit] and does not execute instructions for the time that the frequency is changing |

Since the parties' arguments and proposed constructions with respect to these terms are related, the Court addresses the terms together.

**The Parties' Positions**

Plaintiff submits: The plain meanings of these terms do not require that execution of instructions be stopped. Such a limitation is expressed in other claims and should not be read into Claims 1, 10, or 16 of the '627 Patent. Further, while the terms require that clocks to the processing unit be "shut down," other clocks may still operate and be received by the processing unit. Dkt. No. 48 at 22–23.

In addition to the claims themselves, Plaintiff cites the following **extrinsic evidence** to support its position: Carbonell Decl. ¶ 63 (Plaintiff's Ex. E, Dkt. No. 48-6 at 24–25); Thornton Decl. ¶¶ 87–88 (Plaintiff's Ex. F, Dkt. No. 48-7 at 34–36).

Defendant responds: See the Changing-the-Frequency-While-Execution-of-Instructions-is-Stopped Terms addressed above.

Plaintiff replies: Neither the '627 Patent nor the prosecution history justify requiring shutting down the "core clock" or ceasing the execution of instructions. Dkt. No. 53 at 12.

**Analysis**

There are three issues in dispute. First, whether the processor "clocks" shut down in the claims necessarily include the "core clock." They do. Second, whether shutting down the processor clock

necessarily means that there are no instructions executed. It does not. Third, whether the clock is necessarily stopped for the entire time the frequency is changed. It is not.

The "clocks" of the claims at issue, Claims 1, 10, and 16 of the '627 Patent, include the core clock. Claim 1 of the '627 Patent recites:

> a frequency generator configured to receive a first clock signal from a clock generator and to adjust a frequency of said first clock signal to ***furnish clock signals*** at different frequencies ***to said processing unit*** and said second component … wherein, ***in response to initiating a change in frequency*** for said processing unit, said processing unit is configured to start a counter and to ***shut down clocks to said processing unit*** and said second component.

Claim 10 similarly recites:

> said frequency generator configured to adjust said frequency of said first clock signal to concurrently ***furnish clock signals*** at different frequencies ***to said processing unit*** and said second component … wherein, in response to initiating said change in frequency, said processing unit is configured to start a counter and ***to shut down clocks to said processing unit*** and said second component.

Claim 16 similarly recites:

> a first clock signal at a first frequency to ***provide a second clock signal at a second frequency to a processing unit*** … in response to initiation of a change in frequency for said processing unit, starting a counter and ***stopping said first and second clock signals***.

That is, the "clocks" or "clock signals" of the claims expressly include the processing-unit clock. As explained above, the processing-unit clock is the core clock. *See also,* '061 Patent col.3 ll.20–26; '061 Patent File Wrapper, August 3, 2004 Response at 16–17, Dkt. No. 50-12 at 17–18.

While, as set forth above, the Court understands that execution of instructions during a voltage change requires operation of the core clock, it does not understand the claims at issue here to preclude instructions based on other clocks. As set forth above, the patentee explained during prosecution of the '061 Patent that execution of instructions during the voltage change means clocking instructions through the processor and that this is not possible when the processor clock is not running. '061 Patent File Wrapper, August 3, 2004 Response at 16–17, Dkt. No. 50 12 at

17–18. Thus, claimed execution of instructions during the voltage change requires operation of the core clock. The claims at issue here, however, do not refer to either continuing to execute instructions or stopping the execution of instructions, during a voltage change or otherwise. Nor do the claims, which are open-ended, preclude the use or presence of unrecited clocks. Ultimately, the Court finds nothing in the intrinsic record to require that any and all instructions be executed only through use of the core clock. While the Court also finds no intrinsic-record disclosure of using any clock other than the core clock to execute instructions, whether such is technically possible is an issue of fact outside the patents and whether a claim to such undisclosed clock is supported by the disclosure of the Asserted Patents is an issue of invalidity under the enablement or written-description requirements, not an issue of claim construction. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1327 (Fed. Cir. 2005) (en banc) ("we have certainly not endorsed a regime in which validity analysis is a regular component of claim construction").

The terms at issue do not require that the clocks are necessarily shut down for the entire frequency-change operation. The claims themselves recite when the shut-down clocks are reenabled. For instance, Claim 10 recites:

> processing unit configured to register ***a value*** corresponding to an amount of time allowed for phase-locked-loop (PLL) circuitry to lock in response to a change in frequency of said first clock signal … a frequency generator coupled to said clock generator and comprising said PLL circuitry, said frequency generator configured to adjust said frequency of said first clock signal to concurrently furnish clock signals at different frequencies to said processing unit and said second component … in response to initiating said change in frequency, said processing unit is configured to start a counter and to shut down clocks to said processing unit and second component … ***in response to said counter reaching said value***, said processing unit is configured to tum on said clocks.

The claim expressly recites that the clocks are shut down for a sufficient period of time to allow the phase-locked-loop circuitry to lock in in response to a change in frequency. Claims 1 and 16 are different. Claim 1 recites: "in response to said counter reaching a ***specified value***, said

processing unit is configured to turn on said clocks." Claim 16 recites: "in response to said counter reaching a ***specified value***, restarting said first and second clock signals." Unlike Claim 10, Claims 1 and 16 are silent on how or whether the "specified value" is related to the duration of the frequency change. While the Court finds no intrinsic-record disclosure of a specified value other than one "used to measure the time allowed for the phase-lock-loop circuitry to lock to the new frequency," '061 Patent col.6 ll.63–66, whether the disclosure of the Asserted Patents supports a claim to such is an issue of invalidity under the enablement or written-description requirements, not an issue of claim construction. Ultimately, the Court finds nothing in the intrinsic record that mandates the clocks be shut down for the entirety of the frequency change.

Accordingly, the Court rejects Defendant's proposals to limit the claims to prohibit execution of instructions other than those enabled by the core clock and to limit the claims to prohibit an enabled core clock at any point during a frequency-change operation. The Court hereby construes the "clock signal" terms as set forth below, and holds that the **shutting-down-the-clocks-in-response-to-a-frequency-change-initiation terms otherwise** have their **plain and ordinary meaning** without the need for further construction:

- In Claims 1 and 10 of the '627 Patent, **"in response to initiating [a/said] change in frequency … shut down clocks to said processing unit and said second component"** means **"in response to initiating [a/said] change in frequency … shut down clocks, including the core clock, to said processing unit and said second component"**; and
- In Claim 16 of the '627 Patent, **"in response to initiation of a change in frequency for said processing unit … stopping said first and second clock signals"** means **"in response to initiation of a change in frequency for said**

**processing unit … stopping said first and second clock signals, including the core clock."**

### E. The Operating-Conditions Terms

| Disputed Term | Plaintiff's Proposed Construction | Defendant's Proposed Construction |
|---|---|---|
| • Dkt. No. 54-1 at 11–12, No. 38 | plain and ordinary meaning | the present frequency and voltage of operation of the processor, the temperature of operation of the processor, or the amount of time the processor spends in one of what may be a number of idle states |

Since the parties' arguments and proposed constructions with respect to these terms are related, the Court addresses the terms together.

**The Parties' Positions**

Plaintiff submits: The specific operating conditions listed in Defendant's proposed construction are exemplary conditions described in the Asserted Patents. As exemplary embodiments, they should not be read into the claims. Dkt. No. 48 at 16.

In addition to the claims themselves, Plaintiff cites the following intrinsic and extrinsic evidence to support its position: **Intrinsic evidence**: '061 Patent col.5 ll.21–29. **Extrinsic evidence**: Carbonell Decl. ¶¶ 47–50 (Plaintiff's Ex. E, Dkt. No. 48-6 at 19–20).

Defendant responds: The operating conditions or characteristics of the claims are limited to those described in the Asserted Patents: operating frequency, operating voltage, operating temperature, and time the processor spends in an idle state. Specifically, the conditions do not include "instructions to be executed by the processor." Such instructions were disclaimed as operating conditions during prosecution of the '061 Patent. A "plain meaning" construction

threatens to improperly allow operating conditions or characteristics to encompass instructions to be executed. Dkt. No. 50 at 16–18.

In addition to the claims themselves, Defendant cites the following **intrinsic evidence** to support its position: '061 Patent col.2 l.67 – col.3 l.12; '061 Patent File Wrapper September 8, 2008 Reply to Action Closing Prosecution in Inter Partes Reexamination at 2 (Defendant's Ex. D, Dkt. No. 50-5 at 7).

Plaintiff replies: The patentee did not disclaim instructions to be executed from the scope of operating conditions. Rather, the patentee amended certain claims to include that a determination is made "independently of instructions to be executed by the processor." This means that "instructions to be executed" are actually within the scope of "operating conditions," else there would have been no need to amend the claims. Dkt. No. 53 at 8.

**Analysis**

There are two issues in dispute. First, whether the recited operating "conditions," "characteristics," and "parameters" of the processor are limited to those listed in the Asserted Patents. They are not. Second, whether the recited operating "conditions," "characteristics," and "parameters" of the processor necessarily excludes "instructions to be executed by the processor." They do not.

The Asserted Patents' list of operating conditions, namely, "the present frequency and voltage of operation, the temperature of operation, the amount of time the processor spends in one of what may be a number of idle states in which various components of the system are quiescent," '061 Patent col.5 ll.23–28, is not exhaustive. "[V]oltage and frequency monitoring" is expressly exemplary, *id*. at col.3 ll.2–5 (using "such as" to introduce voltage and frequency monitoring), as is monitoring of "temperature data." *Id*. at col.3 ll.5–9 (using "e.g." to introduce temperature data).

Other exemplary condition monitoring includes "detecting other operations of the system including commands to be executed from which a particular type of operation to be executed may be determined." *Id*. at col.3 ll.9–12 (using "including" to introduce a list of other operations detected). The patents also refer to "various operating characteristics" with reference to U.S. Patent App. No. 09/417,930. *Id*. at col.3 ll.12–15. Further, the patents disclose monitoring "various conditions of the processor that relate to power expenditure by the processor" which "may include …the amount of time the processor spends in one of what may be a number of idle states in which various components of the system are quiescent." *Id*. at col.5 ll.21–28. Relatedly, the patents mention ramping up the frequency and voltage for a "short time," suggesting the time of overclocking may also be an operating condition that is monitored. *See id*. at col.7 ll.45–58; Carbonell Decl. ¶ 49, Dkt. No. 48-6 at 20. Ultimately, the listed operating conditions/characteristics/parameters are not exhaustive as Defendant suggests.

Except as expressly provided in the claims, the "instructions to be executed by the" processor/processing device condition is not excluded from the claimed operating conditions/characteristics/parameters. Claim 1 of the '247 Patent recites: "determining a level of permitted power consumption by a processing device from a set of operating conditions of the processing device, with the determining the level of permitted power consumption not based upon instructions to be executed by the processing device." This expressly states that the "instructions to be executed by the processing device" are not part of the "operating conditions" used in "the determining [a] level of permitted power." This suggests that "operating conditions" does not inherently exclude "instructions to be executed by the processing device." Further, amending Claim 1 during prosecution of the '061 Patent reexamination to expressly remove "instructions to be executed by the processor" from the conditions used in determining a reduced maximum power

consumption level is not a broad disclaimer of "instructions to be executed by the" processor/processing device from the scope of "operating conditions" regardless of the role of those conditions in a claim.

Accordingly, the Court rejects Defendant's proposal to limit the terms to "the present frequency and voltage of operation of the processor, the temperature of operation of the processor, or the amount of time the processor spends in one of what may be a number of idle states" and to necessarily exclude "instructions to be executed by the processor." The Court hereby holds that the **Operating-Conditions terms** have their **plain and ordinary meanings** without the need for further construction.

### F. "a counter"

| Disputed Term | Plaintiff's Proposed Construction | Defendant's Proposed Construction |
|---|---|---|
| "a counter"<br>• Dkt. No. 54-1 at 12, No. 39 | plain and ordinary meaning | a device that counts to a predetermined time |

**The Parties' Positions**

Plaintiff submits: As the Court held in *Huawei*, the meaning of "counter" is understandable without construction. A "counter" is not necessarily a "device" nor does it necessarily "count[] to a predetermined time." The fact that an exemplary embodiment of a counter described in the Asserted Patents counts to a predetermined time does not justify limiting "counter" in the claims to one that "counts to a predetermined time." Dkt. No. 48 at 16–17.

In addition to the claims themselves, Plaintiff cites the following **extrinsic evidence** to support its position: Carbonell Decl. ¶¶ 52–53 (Plaintiff's Ex. E, Dkt. No. 48-6 at 21); Thornton Decl. ¶¶ 68–70 (Plaintiff's Ex. F, Dkt. No. 48-7 at 27–29).

Defendant responds: As the Court explained in *Huawei*, the counter is used to control how long the clocks are disabled for a frequency change. This means the counter must count to a time. This is expressed in the claims in that the counter is started when the clocks are shut down and the clocks are restarted after the counter reaches a "specified value." Further, this is how the described embodiments work—the counter measures a predetermined time to allow the frequency change to be effected. Finally, the "counter" limitation was added during prosecution and was recognized as a distinction over the prior art in that it counted to a predetermined time in order to restart the clocks. In contrast, a "plain and ordinary meaning" construction of "counter" could encompass things as diverse as a person who counts and a mechanical turnstile counter. Dkt. No. 50 at 18–20.

In addition to the claims themselves, Defendant cites the following **intrinsic evidence** to support its position: '627 Patent figs.2, 4, col.5 ll.6–8, col.6 l.63 – col.7 l.2; '627 Patent File Wrapper November 7, 2012 Response at 2–8 (Defendant's Ex. E, Dkt. No. 50-6 at 3–9), November 23, 2012 Reasons for Allowance at 2 (Defendant's Ex. G, Dkt. No. 50-8 at 7).

Plaintiff replies: Under its plain meaning in the context of the claims and the patents' disclosure, a "counter" is neither a person who counts nor necessarily a device that counts to a predetermined time. Dkt. No. 53 at 8–9.

**Analysis**

The main issue in dispute is whether the counter of the Asserted Patents necessarily counts to a predetermined time. It does not.

In *Huawei*, the Court held that the "counter" of Claims 1, 10, and 16 of the '627 Patent was not limited to one that "counts to time the phase-lock-loop relock process." *Huawei*, 2017 U.S. Dist. LEXIS 108040, at *26–31. The Court there held that while the exemplary embodiment of a counter described in the '627 Patent "is utilized to measure the time allowed for the PLL circuitry

to lock to the new frequency," the counter of the invention was not defined as one that necessarily "counts to time the phase-lock-loop relock process." *Id*. at *28 (quoting '627 Patent at col.6 ll.63–66). The Court reiterates that holding here.

The counter counts, but it does not necessarily count to a predetermined time. As described above with respect to the shutting-down-the-clocks-in-response-to-a-frequency-change-initiation terms, Claims 1, 10, and 16 recite that the shut-down clocks are "turned on" or "restarted" when a counter reaches a specified value. In Claims 1 and 10, the "processing unit" reenables the clocks "in response to the counter reaching a certain value." Claim 16 states simply, "in response to said counter reaching a specified value, restarting said first and second clock signals." While the restart of the clocks in each of these claims is tied to the counter reaching some predetermined value, the counter does not necessarily count to this predetermined value nor is the predetermined value necessarily a "time." The counter of Claim 10 is expressly tied to a time: the "value" that triggers turning on the clocks is "a value corresponding to an amount of time allowed for phase-locked-loop (PLL) circuitry to lock in response to a change in frequency of said first clock signal." The clock-restart values of Claims 1 and 16 are not expressly tied to a time. That the restart value is expressly tied to a time in one claim and not others suggests that it is not inherently a time. None of the claims require that the counter count to the value, only that once it reaches the value, the clocks are restarted. Not even the counter of the described embodiment is limited to counting to a predetermined time. Rather, it is simply "utilized to measure the time." '061 Patent col.6 l.61 – col.7 l.5. In fact, the patents describe that the "relock time" is stored in the "master register" and the "sequencer" restarts that clock once this period has "passed." *Id*. This suggests that the clock-restart counter may count higher than the relock time and that something other than the counter may determine if the counter has reached the predetermined value. The patents also describe

another counter, the "time stamp counter," which "keep[s] track of world clock values," suggesting that a "counter" is not inherently a device that counts to a predetermined time. *Id*. at col.7 ll.6–25. Ultimately, the counter of the claims does not necessarily count to a predetermined time.

While the Court does not perceive any real risk that a party or an expert may present a person or a mechanical turnstile counter as a counter of the claims, or that a jury might misunderstand the counter of the claims to encompass a person or a mechanical turnstile counter and thereby reach an incorrect conclusion on infringement or invalidity, Defendant has raised this as a dispute. The "counter" of the Asserted Patents and of the claims of the '627 Patent is not a person or a mechanical turnstile counter. In the context of the patents, the plain meaning of "counter" is a unit, whether hardware or software, that counts.

Accordingly, the Court hereby construes **"counter"** to mean **"hardware or software that counts."**

### G. The Frequency-Generator and Clock-Generator Terms

| Disputed Term | Plaintiff's Proposed Construction | Defendant's Proposed Construction |
|---|---|---|
| "clock frequency source"<br><br>• Dkt. No. 54-1 at 12, No. 40 | plain and ordinary meaning | a unit that provides an external clock signal to the processor |
| "clock generator"<br><br>• Dkt. No. 54-1 at 12, No. 41 | plain and ordinary meaning | a unit that provides an external clock signal to the processor |
| "clock frequency generator"<br><br>• Dkt. No. 54-1 at 12, No. 42 | plain and ordinary meaning | a unit within the processor that generates clock frequencies |
| "programmable frequency generator"<br><br>• Dkt. No. 54-1 at 13, No. 43 | plain and ordinary meaning | a unit within the processor that generates clock frequencies |

| Disputed Term | Plaintiff's Proposed Construction | Defendant's Proposed Construction |
|---|---|---|
| "frequency generator"<br><br>• Dkt. No. 54-1 at 13, No. 44 | plain and ordinary meaning | a unit within the processor that generates clock frequencies |

Since the parties' arguments and proposed constructions with respect to these terms are related, the Court addresses the terms together.

**The Parties' Positions**

Plaintiff submits: The generator or source recited in these terms is not necessarily located either within or outside the processor, as Defendant proposes. In fact, some claims expressly recite the location of the generator or source while others do not. Thus, it would be improper to import location limitations from the described embodiments into the claims. Dkt. No. 48 at 18–19.

In addition to the claims themselves, Plaintiff cites the following **extrinsic evidence** to support its position: Carbonell Decl. ¶ 57 (Plaintiff's Ex. E, Dkt. No. 48-6 at 22–23); Thornton Decl. ¶¶ 74–79 (Plaintiff's Ex. F, Dkt. No. 48-7 at 30–32).

Defendant responds: The Asserted Patents' technical disclosure and the patentee's positions in prosecution of the '061 Patent make clear that the clock source and clock generator are external to the processor and the frequency generator is internal to the processor. During prosecution, the patentee disparaged prior-art frequency generators that are "external to and separate from the processor" as they "slowed processing," among other things. In the technical disclosure of the patents, an external clock generator provides a signal to an internal frequency generator to generate the processor's core clock. Thus, frequency generator is on the same chip as the processor and the clock generator is not. Dkt. No. 50 at 20–22.

In addition to the claims themselves, Defendant cites the following **intrinsic evidence** to support its position: ’061 Patent fig.1, col.2 ll.58–60, col.3 ll.18–23; ’061 Patent File Wrapper May 7, 2002 Preliminary Amendment at 6 (Defendant’s Ex. L, Dkt. No. 50-13 at 7).

Plaintiff replies: The prosecution-history statements regarding the advantages of having a generator internal to the processor were made in the context of a claim amendment requiring a clock generator on the same chip as the processor. This is not paramount to a disclaimer of frequency generators that are not on the same chip for claims that do not express the “on the same chip” limitation. Nor is it a disclaimer of clock generators that are on the same chip. Dkt. No. 53 at 9–10.

Plaintiff cites further **intrinsic evidence** to support its position: ’061 Patent File Wrapper May 7, 2002 Preliminary Amendment (Defendant’s Ex. L, Dkt. No. 50-13 at 6–7, 9).

**Analysis**

There are two main issues in dispute, both related to the location of the particular source/generator. First, whether the frequency generator of the claims is necessarily on the same chip as the processor. It is. Second, whether the clock generator of the claims is necessarily external to the processor. It is not.

The Asserted Patents repeatedly distinguish the invention from the prior art based on the processor frequency generator being located on the same chip as the processor. For example, in describing the exemplary embodiment, the patents provide: “The processor 10 includes ***on the same semiconductor chip*** a number of components including a processing unit 16 and a programmable ***frequency generator*** 17.” ’061 Patent col.2 ll.58–60 (emphasis added). Placing the generator on the same chip addressed some of the failings of the off-chip generators of the prior art:

> It should be specifically noted that contrasted to prior art systems, the programmable frequency generator is able to provide individual frequencies selectable for each of these components. Thus, ***prior art arrangements utilize an external clock generator to provide all of the different frequencies utilized by the system***. This has a number of effects which are less than desirable. Since the clocks are generated ***off-chip***, the time needed to change frequency is long. Since in an integrated processor all clocks are created from a single slow clock ***off chip***, if the core frequency changes all of the frequencies change with it. Thus, a frequency furnished a single component cannot be changed without affecting a change in other frequencies. The voltage furnished by the ***external*** clock generator does not change even though reduced frequencies adapted to provide reduced levels of operations are furnished for various components of the system. A number of other factors slow the response of the system to changes in the various clocks when an ***external*** clock is used to generate the various operating frequencies for a system.

*Id*. at col.3 ll.27–46 (emphasis added). The patents again explain how placing the frequency generator on the same chip as the processor benefits the prior-art failings:

> Thus, by utilizing the phase-lock-loop generator 17 to determine a core clock frequency and dividing that frequency by a plurality of different values determined by the control software, the operating frequencies for the different components of the system may be individually controlled and furnished to other components of the processor ***without the necessity of crossing chip boundaries*** with the consequent slowing caused by negotiating the boundaries.

*Id*. at col.4 ll.21–28 (emphasis added). The patentee reiterated this on-chip/off-chip distinction during prosecution of the ’061 Patent:

> As explained at page 2, line 22, through page 3, line 12, prior to the invention, this had been accomplished by one or more ***frequency generators***, state machines or power management units, and power supplies all of which are ***external to and separate from the processor itself***. Frequency generators which are external to the processor cause delays in crossing various interfaces, eliminated the ability to provide frequencies which may be changed in different ratios for different components, and generally slowed processing
>
> …
>
> ***The present invention improves on the prior art by providing a frequency generator on the same silicon chip as the processor***. This eliminates the various interfaces which slow operation, allows direct control of the frequency by the processor itself, and facilitates the maintenance of a plurality of optimum frequencies for different components associated with the processor under control of the processor. None of these are possible utilizing prior art knowledge including that of Horden.

’061 Patent File Wrapper May 7, 2002 Preliminary Amendment at 6–7, Dkt. No. 50-13 at 7–8 (emphasis added). Taken together, the repeated description of the invention as having an on-chip frequency generator, the repeated extolling of the virtues of an on-chip generator, and the repeated criticism of off-chip generators clearly point to the conclusion that the frequency generators of the claims are limited to on-chip generators. *See UltimatePointer, L.L.C. v. Nintendo Co.*, 816 F.3d 816, 823–24 (Fed. Cir. 2016).

The frequency generating aspects of the claimed frequency generators are clearly expressed in the claims and do not need to be clarified in a construction. For example, Claim 56 of the ’061 Patent (reexam) states: “the clock frequency generator to furnish … an output clock frequency for the central processor.” Claim 14 of the ’708 Patent similarly provides: “a programmable frequency generator providing a clock signal with an operating frequency at a first frequency; means for executing instructions, said means coupled to said clock signal.” Claim 1 of the ’627 Patent provides: “a frequency generator configured to receive a first clock signal from a clock generator and to adjust a frequency of said first clock signal to furnish clock signals at different frequencies to said processing unit and said second component.” Claim 2 of the ’247 Patent provides: “controlling a frequency generator, using the processing device, to provide the operating frequency to the processing device.” Simply, there is no need to construe the frequency-generator terms to clarify what it provides and to what component it provides it.

The Court understands that even though the frequency generator of the claimed invention is on the same chip as the processor that does not mean the clock source/generator utilized by the frequency generator is necessarily external to that chip. While the described embodiment provides an “external” clock, there is not sufficient language to read this as key to the invention and import “external” into the claims. Unlike the above-cited description of the on-chip nature of the

frequency generator as key to the invention, the description of the clock source/generator does not suggest the off-chip nature is key to the invention. Further, the relationship between the "clock frequency source"/"clock generator" and the frequency generator is clearly expressed in the claims and does not need to be clarified in a construction. For example, Claim 56 of the '061 Patent (reexam) provides: "a clock frequency generator receiving a clock frequency from the clock frequency source." Claim 1 of the '627 Patent provides: "a frequency generator configured to receive a first clock signal from a clock generator." Claim 3 of the '247 Patent provides: "supplying a clock signal to the frequency generator using a clock generator."

Accordingly, the Court rejects Defendant's "external" construction for "clock frequency source" and "clock generator." The Court hereby holds that the terms **"clock frequency source"** and **"clock generator"** have their **plain and ordinary meaning** without the need for construction. The Court also construes the **Frequency-Generator Terms** as follows:

- **"clock frequency generator"** means **"clock frequency generator on the same chip as the processor"**;
- **"programmable frequency generator"** means **"programmable frequency generator on the same chip as the processor"**; and
- **"frequency generator"** means **"frequency generator on the same chip as the processor."**

### H. "a voltage source"

| Disputed Term | Plaintiff's Proposed Construction | Defendant's Proposed Construction |
|---|---|---|
| "a voltage source"<br><br>• Dkt. No 54-1 at 13, No. 45 | plain and ordinary meaning | power supply configured to provide one of a plurality of distinct voltage levels specified by an input |

**The Parties' Positions**

Plaintiff submits: As the Court held in *Huawei*, a "voltage source" may include a power supply but is not necessarily a power supply nor does it necessarily include a power supply. In fact, a claim limitation construed by the Court in *Huawei* expressly recited a "voltage source includes a programmable power supply." There would be no need to recite this if a voltage source inherently was a power supply. Thus, a "voltage source" is not necessarily a power supply that provides distinct voltage levels specified by an input. Dkt. No. 48 at 19–20.

Defendant responds: As the Court held for similar terms in *Huawei*, the "voltage source" necessarily is a power supply that provides different voltage outputs. As recited in the claims (Claim 10 and 17 of the '247 Patent), the "voltage source" is used to change the processor supply voltage. As described in the Asserted Patents, the voltage source that does this is a "programmable voltage generator" that provides selectable and distinct voltage levels to the processor. Ultimately, the "voltage source" of the claims must be able to provide different voltages to the processor. Dkt. No. 50 at 22–23.

In addition to the claims themselves, Defendant cites the following **intrinsic evidence** to support its position: '247 Patent col.2 ll.63–65, col.6 ll.12–16.

Plaintiff replies: Defendant's proposed construction is not clear because it is "unclear what makes a voltage level 'distinct.'" Further, it imports limitations from "programmable" and "selectable" sources expressed in different claims. Dkt. No. 53 at 10.

Plaintiff cites further **intrinsic evidence** to support its position: ’247 Patent col.6 ll.9–11.

**Analysis**

There are two issues in dispute. First, whether a “voltage source” is necessarily a “power supply.” It is not. Second, whether the voltage source is necessarily “configured to provide one of a plurality of distinct voltage levels specified by an input.” It is not.

To begin, the Court’s construction of various “programmable”/“selectable” “power supply” and “voltage” terms in *Huawei* was directed to resolving the dispute over whether “programmable” and “selectable” means that the voltage supplied was “one of several possible voltage outputs [provided] in response to an input.” *Huawei*, 2017 U.S. Dist. LEXIS 108040, at *42. Neither the issue of whether the voltage source of the claims inherently is (or includes) a power supply nor the issue of whether the voltage source of the claims inherently is configured to provide a plurality of distinct voltage levels specified by an input was raised or addressed in *Huawei*. *Id.* at *40–43. The “voltage source” terms here, from Claims 10 and 17 of the ’247 Patent, were not before the Court in *Huawei*. *Id.*

The claims at issue, Claims 10 and 17 of the ’247 Patent, both expressly provide that the “voltage source” is capable of providing at least two different voltage levels, but do not limit how that capability is used or implemented as Defendant advocates. For example, Claim 10 recites: “using the processing device, controlling a voltage source to change a voltage supplied to the processing device from the first voltage to the second voltage.” Claim 17 similarly provides, “the processing device operable to control the voltage source to change from providing the first voltage to providing the second voltage.” It is plain without construction that the two voltage levels supplied or provided by the “voltage source” in these claims are distinct—the voltage is ***changed*** therefore the levels are different. Claim 10 further provides that the “second voltage, [has] a

magnitude less than a magnitude of the first voltage." The claims also require that the processing device implement the change. That said, there is no requirement that the output of the voltage source be "specified by an input." In *Huawei*, the "specified by an input" limitation was a function of the expressed "selectable" or "programmable" limitations, not of the "voltage source" limitations. *Huawei*, 2017 U.S. Dist. LEXIS 108040, at *40–43. Lacking the "selectable" or "programmable" limitation expressed in other claims, the Court rejects Defendant's proposal to limit the output of the voltage source in Claims 10 or 17 to that "specified by an input."

The Court also rejects Defendant's invitation to rewrite "voltage source" to "power supply." In the exemplary embodiments, a "power supply" and a "voltage generator" are distinct concepts. *See, e.g.*, '061 Patent col.2 ll.49–52 ("The hardware includes a processor 10, a clock generator 11, a programmable ***voltage generator*** 12, system memory (DRAM) 14, and an external ***battery (or other power supply)*** 13."). In Figure 1, the voltage generator, not the power supply, provides the voltage to the processing unit. From this, the Court understands that a voltage source may be distinct from a power supply. Indeed, it is not clear that the Figure 1 embodiment has anything that satisfies the "voltage source" terms under Defendant's proposed construction. The power source is a battery and there is no suggestion that the battery is configurable to provide different voltage outputs in response to an input. That function is performed by the voltage generator, which is distinct from the power supply.

Accordingly, the Court rejects Defendant's proposal to limit a voltage source to a "power supply configured to provide one of a plurality of distinct voltage levels specified by an input." The Court holds that the term **"voltage source"** has is **plain and ordinary meaning** without the need for further construction.

## I. The Causing-a-Change-in-Voltage Terms

| Disputed Term | Plaintiff's Proposed Construction | Defendant's Proposed Construction |
|---|---|---|
| • Dkt. No. 54-1 at 13, No. 46 | plain and ordinary meaning | the voltage generator changes the voltage furnished by the voltage generator to the determined voltage level as a result of a specified input |

Since the parties' arguments and proposed constructions with respect to these terms are related, the Court addresses the terms together.

**The Parties' Positions**

Plaintiff submits: "Voltage generator" and "changes … to the predetermined voltage level as a result of a specific input" limitations should not be imported into claims that simply recite causing a voltage change. Dkt. No. 48 at 20–21.

In addition to the claims themselves, Plaintiff cites the following **extrinsic evidence** to support its position: Carbonell Decl. ¶¶ 58–59 (Plaintiff's Ex. E, Dkt. No. 48-6 at 23).

Defendant responds: As set forth by the Court in *Huawei*, the voltage output of the power supply is a function of input to the power supply. As described in the Asserted Patents, the voltage generator is external to the processor and thus requires a command or request to cause a voltage change to a predetermined value. This is distinct from random voltage fluctuations. Dkt. No. 50 at 23–25.

In addition to the claims themselves, Defendant cites the following **intrinsic evidence** to support its position: '061 Patent fig.1, col.2 ll.46–60, col.6 ll.2–15, col.6 ll.30–36, col.7 ll.32–34.

Plaintiff replies: As the Court held in *Huawei*, the meanings of these terms are readily understandable in the context of the claims. There is nothing in the patents that mandates that

"causing" a voltage change necessarily requires a "voltage generator" or a "determined" voltage. Dkt. No. 53 at 10–11.

**Analysis**

There are two issues in dispute. First, whether causing a voltage change necessarily requires changing the voltage to a determined level as a result of a specified input. It does not. Second, whether causing a voltage change necessarily requires a voltage generator. It does not.

As set forth in the section of "voltage source," the patents use a variety of language in regard to providing voltages. For example, the patents provide a "voltage source," a "programmable power supply," a "programmable voltage supply," and "voltage generator." *See, e.g.*, '247 Patent Claims 10 and 16; '061 Patent col.2 l.53, Claim 10. In light of this, the Court will not read a "voltage generator" limitation into the terms at issue here.

Also as set forth above, the Court's *Huawei* construction regarding the output voltage level being "specified by an input" relate to programmable and selectable voltage sources and power supplies, not to every source of voltage. The Court rejects Defendant's proposal to inject this limitation into each of the Causing-a-Change-in-Voltage Terms.

As to whether "causing" a voltage change according to the claims includes within its scope random voltage changes, whatever their cause, the Court holds it does not. In the context of the Asserted Patents, the plain meaning of causing a voltage change requires a controlled and purposeful, rather than accidental, change. *See, e.g.*, '061 Patent col.6 ll.9–13, col.7 ll.32–35. Indeed, at oral argument Plaintiff indicated that a random voltage change is not "caused" as claimed.

Accordingly, the Court rejects Defendant's request to read in the limitations of "voltage generator changes the voltage furnished by the voltage generator to the determined voltage level

as a result of a specified input." The Court holds that the **Causing-a-Change-in-Voltage Terms** have their **plain and ordinary meaning** without the need for further construction.

### J. The Determining Terms

| Disputed Term | Plaintiff's Proposed Construction | Defendant's Proposed Construction |
|---|---|---|
| "determining …" / "determines …" / "determination …"<br><br>• Dkt. No. 54-1 at 3–10, Nos. 4–36 | plain and ordinary meaning | indefinite |

Since the parties' arguments and proposed constructions with respect to these terms are related, the Court addresses the terms together.

**The Parties' Positions**

Plaintiff submits: Defendant's indefiniteness position is premised on the Asserted Patents having to provide how the recited determinations are made. This is an issue of enablement, not definiteness. Dkt. No. 48 at 13–14.

In addition to the claims themselves, Plaintiff cites the following intrinsic and extrinsic evidence to support its position: **Intrinsic evidence**: '061 Patent col.1 ll.42–45, col.5 ll.63–66. **Extrinsic evidence**: Thornton Decl. ¶¶ 46–48 (Plaintiff's Ex. F, Dkt. No. 48-7 at 18–19); Carbonell Decl. ¶¶ 37–41 (Plaintiff's Ex. E, Dkt. No. 48-6 at 15–18).

Defendant responds: "Determining" the parameters stated in the claims may cover "a variety of activities" and neither the claims nor the rest of the specification of the Asserted Patents provide guidance regarding what activities are within the scope of determining in the claims. For the meanings of the Determining Terms to be clear, the claims or the technical disclosure must provide either an input or output and also "the process or algorithm for how the actual determining is made." The patents, however, "fail to disclose any techniques for determining" the recited

parameters. Thus, the meanings of the Determining Terms are not reasonably clear. Dkt. No. 50 at 25–28.

In addition to the claims themselves, Defendant cites the following intrinsic and extrinsic evidence to support its position: **Intrinsic evidence**: '061 Patent col.3 ll.49–52, col.4 ll.12–20. **Extrinsic evidence**: Thornton Decl. ¶¶ 46–56 (Defendant's Ex. H, Dkt. No. 50-9 at 18–23).

Plaintiff replies: The issue of whether the Asserted Patents disclose any techniques for determining a recited parameter is not an issue of claim construction. Rather, this is an issue of enablement. In any event, the patents disclose using a look-up table to determine frequency. Dkt. No. 53 at 5–6.

Plaintiff cites further **intrinsic evidence** to support its position: '061 Patent col.5 ll.23–28, col.5 ll.63–67.

**Analysis**

The issue is whether the Asserted Patents must provide algorithms for the various "determining" functions recited in the claims for the claims to be definite. They do not.

The Court is not persuaded by Defendant's argument that for a claim including functional language to be definite, the functional language must be supported by descriptions of algorithms for how the function is performed. While this may be true when 35 U.S.C. § 112, ¶ 6 applies, Defendant provides no legal support for this as a rule separate from § 112, ¶ 6 and does not directly argue that § 112, ¶ 6 applies to the Determining Terms. Thus, whether the "determining" language is supported by the written description is determined under the enablement or written-description statutory requirements, it is not an issue of claim construction.

Accordingly, the Court holds that Defendant has not proven any claim indefinite by reason of including "determining" in the claim language and holds that the **Determining Terms** have their **plain and ordinary meaning** without the need for further construction.

### K. "safe level"

| Disputed Term | Plaintiff's Proposed Construction | Defendant's Proposed Construction |
|---|---|---|
| "safe level"<br><br>• Dkt. No. 54-1 at 15, No. 49 | plain and ordinary meaning | indefinite |

**The Parties' Positions**

Plaintiff submits: The term "safe level," in the context of the processor temperature, plainly means the maximum temperature level provided in published standards and specifications sheets for a processor. Dkt. No. 48 at 23–24.

In addition to the claims themselves, Plaintiff cites the following intrinsic and extrinsic evidence to support its position: **Intrinsic evidence**: '708 Patent col.7 ll.37–41. **Extrinsic evidence**: Carbonell Decl. ¶ 67 (Plaintiff's Ex. E, Dkt. No. 48-6 at 26–27).

Defendant responds: The Asserted Patents provide no guidance regarding what makes a particular level safe and "safe level" is not a term of art with definite meaning. Further, there is no indication in the patents that the operating levels specified in a product data sheet establishes what is or is not a "safe level." Rather, the patents teach that it is possible to run the processor outside the specified levels, so long as the temperature stays below a "safe level." Thus, there is no way to determine whether any particular level is a "safe level." Dkt. No. 50 at 28–30.

In addition to the claims themselves, Defendant cites the following intrinsic and extrinsic evidence to support its position: **Intrinsic evidence**: '708 Patent col.7 ll.32–52. **Extrinsic evidence**: Thornton Decl. ¶ 91 (Defendant's Ex. H, Dkt. No. 50-9 at 36–37).

Plaintiff replies: Defendant's position fails to account for the information available to persons of ordinary skill in the art; namely, product data sheets. In the context of this information, what constitutes a "safe level" is reasonably certain. Dkt. No. 53 at 12–13.

Plaintiff cites further **extrinsic evidence** to support its position: Carbonell Decl. ¶¶ 66–68 (Plaintiff's Ex. E, Dkt. No. 48-6 at 25–27).

**Analysis**

The issue is whether the meaning of "safe level" for a processor's temperature is reasonably certain to one of ordinary skill in the art. It is.

The meaning of the "safe level" of Claims 30, 32, 42, 44, 48, and 50 of the '708 Patent is reasonably certain. The Asserted Patents provide:

> It should be noted that at some point during the monitoring operation it may be found that the processor is functioning at a normal frequency and voltage, that the temperature of operation is below some preselected value, and that a series of processor-intensive commands have been furnished to be executed by the processor. In such a case, these characteristics suggest that it may be desirable to increase the voltage and frequency of operation in order to handle these commands for a period less than would raise operating temperatures beyond a safe level. In such a case, the control software may compute higher frequency and voltage values and a temperature (or a time within which temperature will not increase beyond a selected level) in order to cause the hardware to move to this higher frequency state of operation. In such a case, the processor executing the process illustrated effectively ramps up the frequency and voltage so that the processor "sprints" for a short time to accomplish the desired operations. This has the effect of allowing a processor which nominally runs at a lower frequency to attain operational rates reached by more powerful processors during those times when such rates are advantageous.

'061 Patent col.7 ll.40–61. It is possible to clear a back-log of commands by increasing the processor's operating frequency (its core clock) for a period of time. It is important, however, to keep the temperature of operation at a "safe level." One of ordinary skill in the art would read this disclosure with the knowledge that processors are designed to be functional below a certain temperature. *See* Carbonell Decl. ¶ 67, Dkt. No. 48-6 at 26–27. Processor manufacturers provide

the temperature beyond which the processor may no longer be operable. *Id*. With this context, it is reasonably certain that "safe level" refers to the temperature beyond which the processor may not function properly. Going beyond that level poses a risk that the processor will not function properly and defeat the purpose of increasing the frequency.

The claims involving a "safe level" of temperature parallel and are informed by the above-quoted overclocking description from the patent. For example, Claim 30 of the '708 Patent depends from a series of claims related to increasing the processor frequency and voltage (Claim 27) for a period of time (Claim 28) less than required for temperature to increase beyond a "safe level" (Claims 29, 30). This closely parallels the overclocking disclosure in the patent. "Safe level" should be interpreted in the context of this disclosure and with the knowledge of one of ordinary skill in the art, and thus its meaning is reasonably certain.

Accordingly, Defendant has not proven any claim is indefinite for inclusion of the term "safe level." The Court hereby construes **"safe level"** to mean **"maximum operable temperature."**

### L. "level of permitted power"

| Disputed Term | Plaintiff's Proposed Construction | Defendant's Proposed Construction |
|---|---|---|
| "level of permitted power"<br><br>• Dkt. No. 54-1 at 15, No. 50 | plain and ordinary meaning | indefinite |

**The Parties' Positions**

Plaintiff submits: The Court in *Huawei* held that the meaning of "permitted power consumption" of "determining a level of permitted power consumption" was reasonably certain. The issue here is the same as that before the Court in *Huawei*. The permitted power consumption level, the level of permitted power consumption, is known to those of skill in the art to be a function of device parameters and operational circumstances. Dkt. No. 48 at 24–25.

In addition to the claims themselves, Plaintiff cites the following **extrinsic evidence** to support its position: Carbonell Decl. ¶¶ 70–71 (Plaintiff's Ex. E, Dkt. No. 48-6 at 27–28).

Defendant responds: The Asserted Patents provide no guidance regarding what makes a particular power level permitted or not and "level of permitted power" is not a term of art with definite meaning. Further, there is no indication in the patents that the operating levels specified in a product data sheet establishes what is or is not a "level or permitted power." Rather, the patents teach that it is possible to run the processor outside the specified levels. Thus, there is no way to determine whether any particular level is a "level of permitted power." Dkt. No. 50 at 30–31.

In addition to the claims themselves, Defendant cites the following intrinsic and extrinsic evidence to support its position: **Intrinsic evidence**: '708 Patent col.7 ll.32–52. **Extrinsic evidence**: Thornton Decl. ¶¶ 93–94 (Defendant's Ex. H, Dkt. No. 50-9 at 37).

Plaintiff replies: Defendant's position fails to account for the information available to persons of ordinary skill in the art; namely, product data sheets. In the context of this information, what constitutes a "level of permitted power" is reasonably certain. Dkt. No. 53 at 13.

Plaintiff cites further **extrinsic evidence** to support its position: Carbonell Decl. ¶¶ 69–72 (Plaintiff's Ex. E, Dkt. No. 48-6 at 27–28).

**Analysis**

The issue is whether the meaning of "level of permitted power" of a processor is reasonably certain to one of ordinary skill in the art. It is.

This is substantially the same issue as addressed by the Court in *Huawei*. There, the Court held that the meaning of "determining the level of permitted power consumption" in Claim 1 of the '247 Patent is reasonably certain. *Huawei*, 2017 U.S. Dist. LEXIS 108040, at *31–34. For the

reasons set forth in *Huawei*, the Court reiterates that the meaning of this term in the context of Claim 1 of the '247 Patent is reasonably certain.

Accordingly, Defendant has failed to prove that any claim is indefinite for including "level of permitted power." The Court hereby holds that the term **"level of permitted power"** has its **plain and ordinary meaning** without the need for further construction.

### M. "is not capable of functioning" and "can not function"

| Disputed Term | Plaintiff's Proposed Construction | Defendant's Proposed Construction |
|---|---|---|
| "where said [processor/means for executing instructions/processing unit] [is not capable of functioning/can not function] at said [first frequency/first frequency of operation] and said [second voltage/second operating voltage]"<br><br>• Dkt. No. 54-1 at 15, No. 51 | plain and ordinary meaning | indefinite |
| "where said [processor/processing unit] [is not capable of functioning/can not function] at said [second frequency/second frequency of operation] and said [first voltage/first operating voltage]"<br><br>• Dkt. No. 54-1 at 16, No. 52 | plain and ordinary meaning | indefinite |
| "wherein said processor can not function at the frequency of operation greater than said nominal operating frequency and said corresponding operating voltage"<br><br>• Dkt. No. 54-1 at 16, No. 53 | plain and ordinary meaning | indefinite |

Since the parties' arguments and proposed constructions with respect to these terms are related, the Court addresses the terms together.

**The Parties' Positions**

Plaintiff submits: Processors are operable at certain frequency and voltage settings, as published in product data sheets. Outside of these settings, the processor cannot function. Further, the "nominal" setting is the normal setting for the operating conditions, as stated on the product data sheets. This is known to the person of ordinary skill in the art. Dkt. No. 48 at 25–26.

In addition to the claims themselves, Plaintiff cites the following intrinsic and extrinsic evidence to support its position: **Intrinsic evidence**: '708 Patent col.5 ll.26–29, col.5 ll.36–39. **Extrinsic evidence**: Carbonell Decl. ¶¶ 67, 73–75 (Plaintiff's Ex. E, Dkt. No. 48-6 at 26–29).

Defendant responds: The Asserted Patents provide no guidance regarding what makes a processor not capable of functioning or even what level of dysfunction rises to not functioning. Further, there is no indication in the patents that a processor product data sheet specifies parameters at which the processor is not able to function. Rather, the patents teach that it is possible to run the processor outside the recommended levels. Thus, there is no way to determine what is means for a processor to be unable to function. Dkt. No. 50 at 31–32.

In addition to the claims themselves, Defendant cites the following intrinsic and extrinsic evidence to support its position: **Intrinsic evidence**: '708 Patent figs.2, 4 col.4 l.58 – col.5 l.18, col.5 l.42 – col.7 l.24, col.7 ll.32–52. **Extrinsic evidence**: Thornton Decl. ¶ 97 (Defendant's Ex. H, Dkt. No. 50-9 at 38).

Plaintiff replies: Defendant's position fails to account for the information available to persons of ordinary skill in the art; namely, product data sheets. In the context of this information, whether a processor can function at specified frequency and voltage pairings is reasonably certain. Dkt. No. 53 at 13.

**Analysis**

The issue is whether what it means that a processor is not capable of functioning or cannot function is reasonably certain to one of ordinary skill in the art. It is.

These terms are related to the frequency and voltage pairings for operating a processor. For example, Claim 1 of the '708 Patent provides that the "processor is not capable of functioning at said first frequency and said second voltage." Claim 26 of the patent provides that the "processing unit can not function at said second frequency and said first voltage." The Asserted Patents describe:

> The power consumed by a CMOS integrated circuit is given approximately by $P=CV^2f$, where C is the active switching capacitance, V is the supply voltage, and f is the frequency of operation. ***The maximum allowable frequency is described by $f_{max}=kV$***, where k is a constant.
>
> It is desirable to operate the processor at the lowest possible voltage at a frequency that provides the computing power desired by the user at any given moment.

'061 Patent col.1 ll.42–50. That is, the patents explain that there is a maximum frequency allowable for a given processor voltage. "If the frequency is to be increased, it is first necessary that the voltage be increased to allow the processor to function at a higher frequency. In such a case, it is first necessary to increase the voltage level of operation." *Id*. at col.6 ll.2–6. That is, if the frequency is increased beyond that allowed by the voltage, the processor will be unable to function—it is not capable of functioning, it can not function. In the context of the patents, this is shown by the relationship between maximum allowable frequency and voltage: $f_{max}=kV$. Ultimately, whether a particular processor is unable to function at a particular voltage-frequency pairing is a factual issue.

Accordingly, Defendant has not proven any claim is indefinite for including the "is not capable of functioning" or "can not function." The Court holds that the **"Is Not Capable of Functioning"**

**and "Can Not Function" Terms** have their **plain and ordinary meaning** without the need for further construction.

### N. "means for causing adjustment in consumption of power by said apparatus, by …"

The parties indicated at oral argument that Claim 14 of the '708 Patent is no longer asserted in the litigation and that, therefore, there is no need to address this term in claim construction.

## V. CONCLUSION

The Court adopts the constructions set forth above, as summarized in the following table. The parties are **ORDERED** that they may not refer, directly or indirectly, to each other's claim-construction positions in the presence of the jury. Likewise, the parties are **ORDERED** to refrain from mentioning any portion of this opinion, other than the actual definitions adopted by the Court, in the presence of the jury. Any reference to claim-construction proceedings is limited to informing the jury of the definitions adopted by the Court.

Within thirty (30) days of the issuance of this Memorandum Opinion and Order, the parties are hereby **ORDERED**, in good faith, to mediate this case with the designated mediator in this case. As a part of such mediation, each party shall appear by counsel (with lead and local counsel present and participating) and by at least one corporate officer possessing sufficient authority and control to unilaterally make binding decisions for the corporation adequate to address any good faith offer or counteroffer of settlement that might arise during such mediation. Failure to do so shall be deemed by the Court as a failure to mediate in good faith and may subject that party to such sanctions as the Court deems appropriate.

| Group | Term[11] | Construction |
|---|---|---|
| A | computer processor / processor / central processor<br><br>• ’061 Patent, all asserted claims<br>• ’708 Patent, all asserted claims<br>• ’627 Patent, all asserted claims<br>• ’247 Patent, all asserted claims | CPU |
| | processing unit / processing device<br><br>• ’061 Patent, all asserted claims<br>• ’708 Patent, all asserted claims<br>• ’627 Patent, all asserted claims<br>• ’247 Patent, all asserted claims | computing portion of CPU |
| B | executing [said] instructions in said [central/computer] processor while [changing/lowering] voltage at which said [central/computer] processor is operated<br><br>• ’061 Patent Claims 1, 4, 5, 26, 29, 36, 38, 42 | executing [said] instructions using the core clock in said [central/computer] processor while [changing/lowering] voltage at which said [central/computer] processor is operated |
| | executing instructions in said computer processor during said [change in voltage/voltage change]<br><br>• ’061 Patent Claims 15, 23, 30, 39 | executing instructions using the core clock in said computer processor during said [change in voltage/voltage change] |
| | execution of instructions in said central processor while changing voltage at which said central processor is operated | execution of instructions using the core clock in said central processor while changing voltage at which said central processor is operated |
| | cause voltage furnished to the central processor to change while the central processor is executing instructions<br><br>• ’061 Patent Claim 56 | cause voltage furnished to the central processor to change while the central processor is executing instructions using the core clock |
| | changing a voltage … while said processor executes instructions<br><br>• ’708 Patent Claim 1 | changing a voltage … while said processor executes instructions using the core clock |

[11] The Court lists and construes only that claim language which is found in a claim identified by the parties in their Patent Rule 4-5(d) Joint Claim Construction Chart, Dkt. No. 54-1.

| Group | Term[11] | Construction |
|---|---|---|
| | changes the voltage at which said processing unit is operated … while said processing unit executes instructions<br><br>• '708 Patent Claims 36, 39, 59 | changes the voltage at which said processing unit is operated … while said processing unit executes instructions using the core clock |
| | changing a voltage … at which said processor is operated while allowing said processor to execute instructions<br><br>• '708 Patent Claim 7 | changing a voltage … at which said processor is operated while allowing said processor to execute instructions using the core clock |
| | changing a voltage at which said processor is operated … while said processor executes instructions<br><br>• '708 Patent Claim 51 | changing a voltage at which said processor is operated … while said processor executes instructions using the core clock |
| | changing said first voltage … while said means for executing instruction executes instructions<br><br>• '708 Patent Claim 14 | changing said first voltage … while said means for executing instruction executes instructions using the core clock |
| | changing the operating voltage from a first voltage to a second voltage while the processing unit is enabled to execute instructions<br><br>• '708 Patent Claim 26 | changing the operating voltage from a first voltage to a second voltage while the processing unit is enabled to execute instructions using the core clock |
| | changing the operating voltage of said processing unit … while execution of instructions by said processing unit proceeds<br><br>• '708 Patent Claim 20 | changing the operating voltage of said processing unit … while execution of instructions using the core clock by said processing unit proceeds |
| | changing the operating voltage while allowing the processing unit to execute instructions<br><br>• '708 Patent Claim 23 | changing the operating voltage while allowing the processing unit to execute instructions using the core clock |
| | changes the first operating voltage to a second operating voltage [corresponding to said second frequency of operation] while said processing unit executes instructions<br><br>• '708 Patent Claims 33, 55 | changes the first operating voltage to a second operating voltage [corresponding to said second frequency of operation] while said processing unit executes instructions using the core clock |

| Group | Term[11] | Construction |
|---|---|---|
| | changing power consumption of the processing device during execution of the instructions by … reducing a magnitude of a difference between a voltage applied to the processing device and the lowest allowable level of voltage<br><br>• '247 Patent Claim 1 | changing power consumption of the processing device during execution of the instructions using the core clock by … reducing a magnitude of a difference between a voltage applied to the processing device and the lowest allowable level of voltage |
| | change a voltage supplied to the processing device from the first voltage to the second voltage while the processing device executes the instructions<br><br>• '247 Patent Claim 10 | change a voltage supplied to the processing device from the first voltage to the second voltage while the processing device executes the instructions using the core clock |
| | change from providing the first voltage to providing the second voltage during execution of the instructions by the processing device<br><br>• '247 Patent Claim 17 | change from providing the first voltage to providing the second voltage during execution of the instructions using the core clock by the processing device |
| **C** | changing an operating frequency at which said processor is operated … while execution of instructions by said processor is stopped<br><br>• '708 Patent Claim 1 | plain and ordinary meaning |
| | change said operating frequency to a second frequency while execution of said instructions is stopped<br><br>• '708 Patent Claim 14 | plain and ordinary meaning |
| | changing a frequency of operation of the processor … while execution of instructions is stopped<br><br>• '708 Patent Claim 7 | plain and ordinary meaning |
| | changes [the/the first] frequency of operation of the processing unit … while execution of instructions by the processing unit is stopped<br><br>• '708 Patent Claim 33, 36, 39, 55, 59 | plain and ordinary meaning |

| Group | Term[11] | Construction |
|---|---|---|
| | changing an operating frequency at which said processor is operated … while execution of instructions by said processor is stopped<br><br>• '708 Patent Claim 51 | plain and ordinary meaning |
| | adjusting said programmable frequency generator while instruction execution is stopped to change the frequency of said processing unit<br><br>• '708 Patent Claim 20 | plain and ordinary meaning |
| | adjusting said programmable frequency generator comprises stopping said clock signal<br><br>• '708 Patent Claim 22 | adjusting said programmable frequency generator comprises stopping the core clock signal |
| | changing [said operating/the] frequency further comprises: shutting down said clock<br><br>• '708 Patent Claims 6, 13 | changing [said operating/the] frequency further comprises: shutting down the core clock |
| | said causing adjustment comprises shutting down said clock to said means for executing instructions<br><br>• '708 Patent Claim 19 | said causing adjustment comprises shutting down the core clock to said means for executing instructions |
| | while instruction execution is stopped, adjusting said programmable frequency generator to change the frequency of said processing unit<br><br>• '708 Patent Claim 23 | plain and ordinary meaning |
| | while instruction execution is disabled, adjusting said programmable frequency generator to change the frequency of said processing unit<br><br>• '708 Patent Claim 26 | plain and ordinary meaning |
| **D** | in response to initiating [a/said] change in frequency … shut down clocks to said processing unit and said second component<br><br>• '627 Patent Claims 1, 10 | in response to initiating [a/said] change in frequency … shut down clocks, including the core clock, to said processing unit and said second component |

| Group | Term[11] | Construction |
|---|---|---|
| | in response to initiation of a change in frequency for said processing unit … stopping said first and second clock signals<br><br>• '627 Patent Claim 16 | in response to initiation of a change in frequency for said processing unit … stopping said first and second clock signals, including the core clock |
| **E** | operating [conditions/characteristic/characteristics/parameters] [of the/internal to said/internal to the/of said/of a] [processor/central processor/computer processor/apparatus/processing unit/processing device]<br><br>• '061 Patent Claims 1, 7, 15, 56<br>• '708 Patent Claims 2, 3, 8, 9, 33, 34, 52, 53, 55, 56<br>• '627 Patent Claims 4, 12, 16, 18, 19 | plain and ordinary meaning |
| | internal [operating] conditions [of a computer processor]<br><br>• '061 Patent Claims 15, 39 | plain and ordinary meaning |
| **F** | a counter<br><br>• '627 Patent Claims 1, 10, 16 | hardware or software that counts |
| **G** | clock frequency source<br><br>• '061 Patent Claim 56 | plain and ordinary meaning |
| | clock generator<br><br>• '627 Patent Claims, 10<br>• '247 Patent Claims 3, 4, 14, 15, 21, 22 | plain and ordinary meaning |
| | clock frequency generator<br><br>• '061 Patent Claims 56, 57, 58, 59 | clock frequency generator on the same chip as the processor |
| | programmable frequency generator<br><br>• '708 Patent Claims 14, 18, 20, 21, 22, 23, 24, 26 | programmable frequency generator on the same chip as the processor |

| Group | Term[11] | Construction |
|---|---|---|
| | frequency generator<br><br>• ’627 Patent Claims 1, 2, 4, 10, 11, 12<br>• ’247 Patent Claims, 2, 3, 4, 10, 14, 15, 17, 21, 22 | frequency generator on the same chip as the processor |
| **H** | a voltage source<br><br>• ’247 Patent Claims 10, 17 | plain and ordinary meaning |
| **I** | causing a change in its voltage<br><br>• ’061 Patent Claim 1 | plain and ordinary meaning |
| | causing the voltage at which said computer processor is operated to change<br><br>• ’061 Patent Claims 15, 23, 30 | plain and ordinary meaning |
| | causing a change in the voltage at which said computer processor is operated<br><br>• ’061 Patent Claims 39 | plain and ordinary meaning |
| | to cause the power supply … to cause voltage furnished to the central processor to change while the central processor is executing instruction<br><br>• ’061 Patent Claim 56 | plain and ordinary meaning |
| | causing adjustment in consumption of power by said apparatus, by … changing said first voltage to a second voltage corresponding to said second frequency<br><br>• ’708 Patent Claim 14 | plain and ordinary meaning |
| **J** | determining a reduced maximum allowable power consumption level from operating conditions of the processor<br><br>• ’061 Patent Claim 1 | plain and ordinary meaning |
| | determining a maximum frequency which provides power not greater than the allowable power consumption level<br><br>• ’061 Patent Claim 1 | plain and ordinary meaning |

| Group | Term[11] | Construction |
|---|---|---|
| | determining a minimum voltage which allows operation at the maximum frequency determined<br><br>• '061 Patent Claim 1 | plain and ordinary meaning |
| | determining a reduced frequency and a voltage at which to operate said computer processor, based on said internal operating conditions<br><br>• '061 Patent Claim 15 | plain and ordinary meaning |
| | determining a reduced frequency and a voltage at which to operate said computer processor, based on said idle time<br><br>• '061 Patent Claim 23 | plain and ordinary meaning |
| | determining a frequency and a voltage at which to operate said computer processor, based on said idle states<br><br>• '061 Patent Claim 30 | plain and ordinary meaning |
| | determining an allowable reduced power consumption level<br><br>• '061 Patent Claim 39 | plain and ordinary meaning |
| | determining a voltage-frequency pair for said allowable power consumption level<br><br>• '061 Patent Claim 39 | plain and ordinary meaning |
| | determining a voltage-frequency pair comprises accessing a table of predetermined voltage-frequency pairs<br><br>• '061 Patent Claim 54 | plain and ordinary meaning |
| | determining a voltage-frequency pair comprises calculating a voltage-frequency pair<br><br>• '061 Patent Claim 55 | plain and ordinary meaning |
| | determines a reduced voltage level and output clock frequency based on the operating conditions<br><br>• '061 Patent Claim 56 | plain and ordinary meaning |

| Group | Term[11] | Construction |
|---|---|---|
| | computer processor determines a core clock frequency and a plurality of different values by which to divide said core clock frequency<br><br>• '061 Patent Claim 60 | plain and ordinary meaning |
| | determining a frequency and voltage in excess of a normal frequency and voltage for said computer processor<br><br>• '061 Patent Claim 67 | plain and ordinary meaning |
| | determining whether said first voltage should be changed based at least in part on said operating characteristic<br><br>• '708 Patent Claim 2 | plain and ordinary meaning |
| | determines whether one or more of said monitored operating characteristics indicate that said voltage should be changed<br><br>• '708 Patent Claim 8 | plain and ordinary meaning |
| | determining whether said monitored operating characteristics indicate that the operating frequency of said processor should be changed<br><br>• '708 Patent Claim 3 | plain and ordinary meaning |
| | determines whether said monitored operating characteristics indicate that said frequency of operation of said processor should be changed<br><br>• '708 Patent Claim 9 | plain and ordinary meaning |
| | determines said second voltage if said frequency of operation of said processor should be changed<br><br>• '708 Patent Claim 9 | plain and ordinary meaning |
| | determines whether said monitored operating characteristics indicate that consumption of power by said processor should be decreased<br><br>• '708 Patent Claim 33 | plain and ordinary meaning |

| Group | Term[11] | Construction |
|---|---|---|
| | determination to decrease the consumption of power<br><br>• '708 Patent Claims 33, 36 | plain and ordinary meaning |
| | determination to adjust said frequency operation<br><br>• '708 Patent Claim 39 | plain and ordinary meaning |
| | determining whether said first frequency should be changed based at least in part on said operating characteristic<br><br>• '708 Patent Claim 52 | plain and ordinary meaning |
| | determining whether said monitored operating characteristics indicate that the operating frequency of said processor should be changed<br><br>• '708 Patent Claim 53 | plain and ordinary meaning |
| | determining said second frequency and said second voltage<br><br>• '708 Patent Claim 3, 53 | plain and ordinary meaning |
| | determines whether said monitored operating characteristics indicate that performance of said processor should be increased<br><br>• '708 Patent Claim 55 | plain and ordinary meaning |
| | determination to increase [the] performance<br><br>• '708 Patent Claims 55, 59 | plain and ordinary meaning |
| | determine an increase in temperature that would result from an increase in said voltage<br><br>• '627 Patent Claims 8, 15 | plain and ordinary meaning |
| | determining an amount of time that operation is permitted with an increase in said voltage without increasing a temperature of said computer system beyond a limit<br><br>• '627 Patent Claim 27 | plain and ordinary meaning |

| Group | Term[11] | Construction |
|---|---|---|
| | determining a level of permitted power consumption by a processing device<br><br>• ’247 Patent Claim 1 | plain and ordinary meaning |
| | determining a highest allowable frequency of operation of the processing device<br><br>• ’247 Patent Claim 1 | plain and ordinary meaning |
| | determining a lowest allowable level of voltage to apply to the processing device<br><br>• ’247 Patent Claim 1 | plain and ordinary meaning |
| | determining a second frequency … for operation of the processing device<br><br>• ’247 Patent Claim 10 | plain and ordinary meaning |
| | determining a second voltage … for operation of the processing device<br><br>• ’247 Patent Claim 10 | plain and ordinary meaning |
| | determine a second frequency of the first clock signal and a second voltage for operation of the processing device<br><br>• ’247 Patent Claim 17 | plain and ordinary meaning |
| | determining the level of permitted power consumption not based upon instructions to be executed by the processing device<br><br>• ’247 Patent Claim 1 | plain and ordinary meaning |
| | determining the second frequency not based upon instructions to be executed by the processing device<br><br>• ’247 Patent Claim 10 | plain and ordinary meaning |
| | determining the second voltage not based upon instructions to be executed by the processing device<br><br>• ’247 Patent Claim 10 | plain and ordinary meaning |

| Group | Term[11] | Construction |
|---|---|---|
| | determine the second frequency and the second voltage not based on instructions to be executed by the processing device<br><br>• '247 Patent Claim 17 | plain and ordinary meaning |
| **K** | safe level<br><br>• '708 Patent Claims 30, 32, 42, 44, 48, 50 | maximum operable temperature |
| **L** | level of permitted power<br><br>• '247 Patent Claim 1 | plain and ordinary meaning |
| **M** | where said [processor/means for executing instructions/processing unit] [is not capable of functioning/can not function] at said [first frequency/first frequency of operation] and said [second voltage/second operating voltage]<br><br>• '708 Patent Claims 1, 7, 14, 20, 23 | plain and ordinary meaning |
| | where said [processor/processing unit] [is not capable of functioning/can not function] at said [second frequency/second frequency of operation] and said [first voltage/first operating voltage]<br><br>• '708 Patent Claims 26, 33, 36, 51, 55, 59 | plain and ordinary meaning |
| | wherein said processor can not function at the frequency of operation greater than said nominal operating frequency and said corresponding operating voltage<br><br>• '708 Patent Claim 45 | plain and ordinary meaning |

**So ORDERED and SIGNED this 13th day of May, 2019.**

RODNEY GILSTRAP
UNITED STATES DISTRICT JUDGE