United States Court of Appeals for the Federal Circuit

2006-1192

(Re-examination Nos. 90/005,384; 90/005,823; 90/005,881;
90/006,051 and 90/006,392)

IN RE TRANSLOGIC TECHNOLOGY, INC.

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Appealed from: United States Patent and Trademark Office
Board of Patent Appeals and Interferences

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DECIDED: October 12, 2007

Before MAYER, RADER, and PROST, Circuit Judges.

RADER, Circuit Judge.

The United States Patent and Trademark Office's Board of Patent Appeals and Interferences ("Board") upheld the examiner's rejection of U.S. Patent No. 5,162,666 ("the '666 patent") in a reexamination proceeding, Appeal No. 2005-1050. Because the '666 patent would have been obvious at the time of invention, this court affirms.

I

The United States Patent and Trademark Office issued the '666 patent, entitled "Transmission Gate Series Multiplexer", on November 10, 1992 from an application filed on March 15, 1991. In addition to this appeal from the Board's decision, the '666 patent is the subject of a patent infringement litigation between Translogic Technology, Inc. ("Translogic") and Hitachi, Ltd. et al. ("Hitachi") in the United States District Court for the District of Oregon. The district court case began on March 24, 1999. Thereafter, on June 4, 1999 and ending on September 27, 2002, Hitachi filed five third-party requests

for reexamination of the '666 patent. The Patent Office merged the various requests into a single proceeding. On March 8, 2004, the merged reexamination resulted in the rejection of claims 16, 17, 39-45, 47 and 48 under 35 U.S.C. § 103(a) because they would have been obvious at the time of invention. The Patent Office found the claims obvious in light of the references Gorai or Tosser in view of Weste. During the reexamination proceedings, Translogic cancelled original claims 1-15 and 18-27, and newly added claims 28-38 and 46. Translogic then appealed to the Board. On July 14, 2005, the Board affirmed the rejection. The Board denied Translogic's request for reconsideration. Translogic then appealed the Board's decision to this court.

During this entire reexamination process, the district court infringement case proceeded in parallel. In October 2003, a jury upheld the patent as valid. In February 2005, the district court granted summary judgment of infringement with respect to some, but not all, of Hitachi's accused products. In May 2005, a jury found Hitachi had induced infringement and held Hitachi liable for $86.5 million in damages. The district court entered a permanent injunction, which, after Hitachi's interlocutory appeal, this court stayed.

After post-trial briefing, the district court entered final judgment against Hitachi in December 2005. Hitachi appealed to this court. This court consolidated the interlocutory appeal with the appeal from the final judgment and added Translogic's reexamination appeal from the Board to the same panel. This opinion only addresses Translogic's reexamination appeal from the Board.

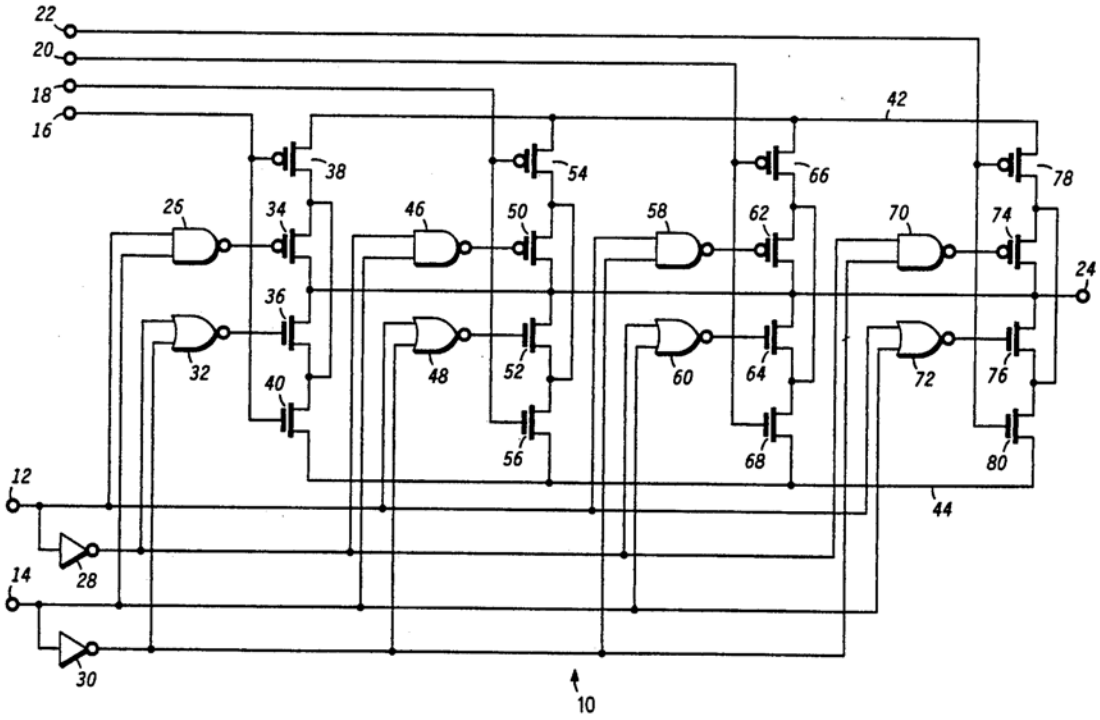
The '666 patent deals with multiplexers. A multiplexer is a type of electrical circuit. A multiplexer has multiple inputs, one or more control lines, and one output.

The signals on the control lines select one of the various inputs to be passed to the output. In a 2:1 multiplexer, a single output value is selected from two inputs. Similarly, in 4:1 and 8:1 multiplexers, a single output is selected from among four or eight inputs, respectively. Thus, the invention selects one of the multiple inputs to pass to the output.

The number of control lines (x) for a conventional multiplexer depends on the number of inputs to the multiplexer. Generally, a given number of control lines (x) can select one output from among a maximum of 2^x inputs. In a 2:1 multiplexer, a single control line (x = 1) can select between 2^1 or 2 inputs, therefore x = 1. In a 4:1 multiplexer, two control lines (x = 2) are used to select among 2^2 or 4 inputs, and in an 8:1 multiplexer, three control lines (x = 3) can select between 2^3 or 8 inputs.

Figure 1 of U.S. Patent No. 5,012,126 (referenced by the '666 patent) shows a 4:1 conventional multiplexer. Lines 16, 18, 20 and 22 are inputs, lines 12 and 14 are control lines and line 24 is the output. The control lines will select which input (i.e., 16, 18, 20 or 22) to pass to the output. This particular circuit passes the inverse of the selected input to the output.[1] For example, if line 12 is a logic 0 and line 14 is a logic 1, then the circuit passes the inverse of the signal on line 18 to output line 24. As another example, if line 12 is a logic 1 and line 14 is a logic 1, then the circuit passes the inverse of the signal on line 16 to output line 24.

[1] The inverse of a signal is often used in circuits and does not change the multiplexer function.



Control Line 12	Control Line 14	Output 24
0	0	Inverse of Line 22
1	0	Inverse of Line 20
0	1	Inverse of Line 18
1	1	Inverse of Line 16

The '666 patent describes a multiplexer that couples together multiple stages of 2:1 multiplexers in series. The '666 patent specifically uses a transmission gate multiplexer ("TGM") as each 2:1 multiplexer. Figure 3 of the '666 patent (see below) illustrates a 4:1 series multiplexer that connects three TGMs (i.e., A, B and C) in series. The inputs are I0, I1, I2 and I3, the output is Z and the control lines are S1, S2 and S3. While a conventional 4:1 multiplexer would have two control lines, the 4:1 series multiplexer, according to the '666 patent configuration, has three control lines.

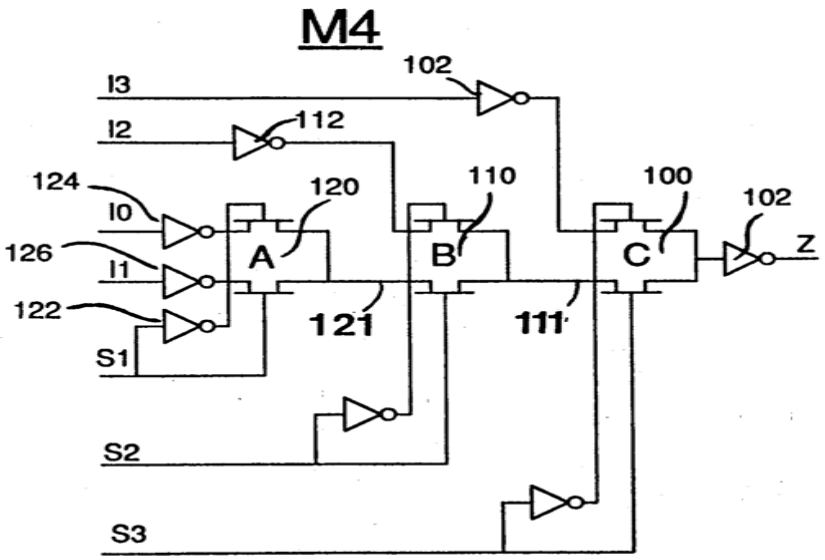


FIG 3

In the figure above, lines S1, S2, and S3 are control lines and lines I0, I1, I2, and I3 are input lines. The series multiplexer operates in cascade by passing the selected input to the output in a series of selections. For example, for the input on I1 to be passed to output Z, S1 must be a logic 1 to pass I1 to the input of TGM B on line 121, S2 must also be a logic 1 to pass I1 to the input of TGM C via line 111, and finally S3 must be a logic 1 to pass the output of TGM B to the output of TGM C. In other words, the line 1 input must prevail in each selection phase. In another example, I3 would be passed to the output Z by setting S3 to logic 0. When the signal on S3 is a logic 0, control lines S1 and S2 do not influence the output because TGM C will pass the value on I3 directly from the input line I3 to the output Z.

The claims on appeal specify multiplexers with multiple 2:1 TGMs connected in series. In the series configuration, the output of one TGM connects to one input of the next TGM. Each TGM is known as a stage. A multiplexer built from a series of TGMs has p control inputs and (p+1) data inputs for a total of (2p+1) overall inputs. For

example, a 4:1 series multiplexer has p=3 control inputs and 4 data inputs thereby resulting in 7 ((2*3) + 1 = 7) overall inputs whereas a conventional 4:1 multiplexer has 4 inputs and 2 control inputs, resulting in 6 overall inputs. During the reexamination, Translogic agreed that all of the claims on appeal stood or fell with claims 47 and 48:

> 47. A multiplexer circuit comprising:
> a first stage TGM circuit having first and second signal input terminals, a control input terminal and an output terminal;
> the first and second signal input terminals coupled to receive first and second input variables, respectively;
> the control input coupled to receive a first control signal;
> a second stage TGM circuit having first and second signal input terminals, a control input terminal and an output terminal;
> one of the second stage input terminals coupled to the first stage output terminal; the other one of the second stage signal input terminals coupled to receive a third input variable;
> the second stage control input terminal coupled to receive a second control signal;
> a third stage TGM circuit having first and second signal input terminals, a control input terminal and an output terminal;
> one of the third stage input terminals coupled to the second stage output terminal;
> the other one of the third stage input terminals coupled to receive a fourth input variable;
> and the third stage control input variable coupled to receive a third control signal whereby the circuit forms a 4:1 multiplexer.
>
> 48. A multiplexer circuit comprising:
> a first stage TGM circuit having first and second signal input terminals, a control input terminal, and an output terminal;
> the first and second signal input terminals coupled to receive first and second input variables, respectively;
> the control input terminal coupled to receive a first control signal;
> a second stage TGM circuit having first and second signal input terminals, a control input terminal and an output terminal;
> one of the second stage signal input terminals coupled to the first stage output terminal;
> the other one of the second stage signal input terminals coupled to receive a third input variable;
> the second stage control input terminal coupled to receive a second control signal;
> a third stage TGM circuit having first and second signal input terminals, a control input terminal and an output terminal;

one of the third stage signal input terminals coupled to the second stage output terminal;
the other one of the third stage signal input terminals coupled to receive a fourth input variable;
the third stage control input terminal coupled to receive a third control signal;
a fourth stage TGM circuit having first and second signal input terminals, a control input terminal and an output terminal;
one of the fourth stage signal input terminals coupled to the third stage output terminal;
the other one of the fourth stage signal input terminals coupled to receive a fifth input variable; and
the fourth stage control input terminal coupled to receive a fourth control signal; whereby the circuit forms a 5:1 multiplexer.

The Board affirmed the rejection of claims 47 and 48 as obvious under § 103(a). In applying the obviousness test, the Board relied on Gorai combined with Weste, as well as Tosser combined with Weste. The Gorai and Tosser references are technical articles; the Weste reference is a textbook:

Gorai, R.K., and Pal, A., Automated synthesis of combinational circuits by cascade networks of multiplexers, IEE Proc., Vol. 137, Pt. E, No. 2, March 1990, pages 164-170.

Weste, Neil H.E., and Eshraghian, Kamran, Principles of CMOS VLSI Design: A Systems Perspective (Addison-Wesley Publ. Co. 1985), pages 14-17 and 172-175.

Tosser, A.J., and Aoulad-Syad, D., Cascade networks of logic functions built in multiplexer units, IEE Proc., Vol. 127, Pt. E, No. 2, March 1980, pages 64-68.

The Board found that Fig. 3 of Gorai (see below) discloses a three-stage multiplexer circuit with four inputs (h_p, g_p, h_{p-1}, h_1) and three control inputs (x_p, x_{p-1} and x_1).

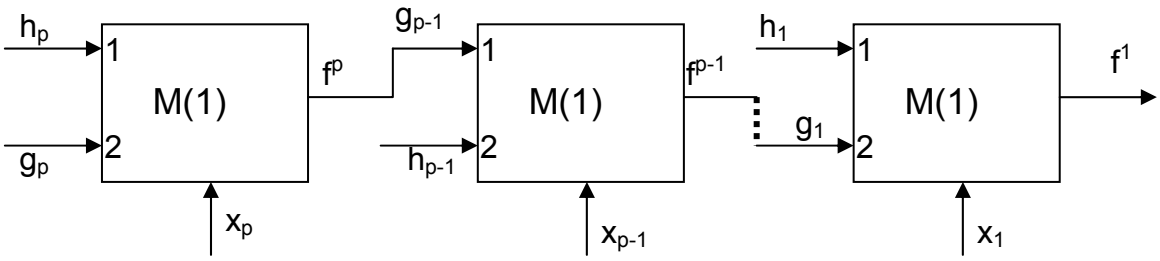


Fig. 3 A cascade network of p-stages of M(1)s

The Board found that Gorai does not disclose use of TGMs for each multiplexer stage (i.e., M(1)) in Fig. 3. The Board, however, found that Weste taught a 2:1 TGM circuit to transfer a logic 0 or a logic 1 between the input and output. The Weste reference discloses and teaches a TGM in its Figs. 1.10 (a) and (b). The figures show the use of complementary switches to pass logic 0s and logic 1s.

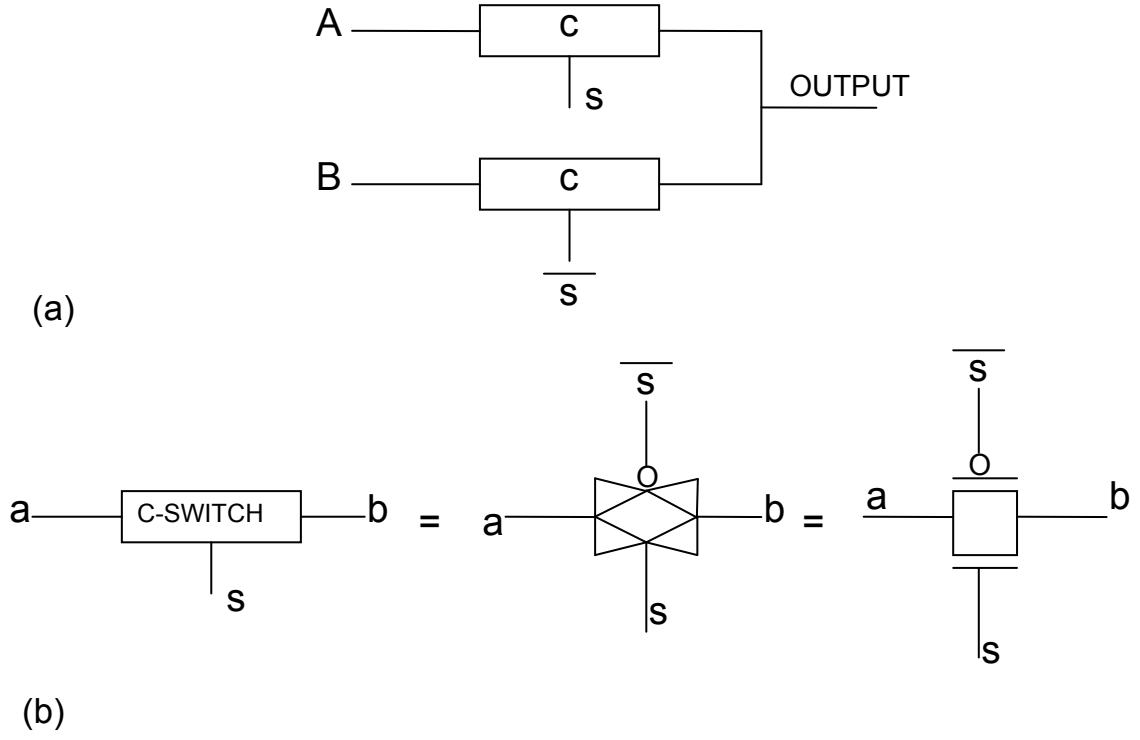


Fig. 1.10. A CMOS 2-input multiplexer

The Board thus found that a person of ordinary skill in the art would have been motivated to use a TGM circuit as taught in Weste for the multiplexer stages in Gorai.

The Board also found that Fig. 9 of Tosser (see below) teaches a 4:1 multiplexer built from three 2:1 multiplexer stages connected in series.

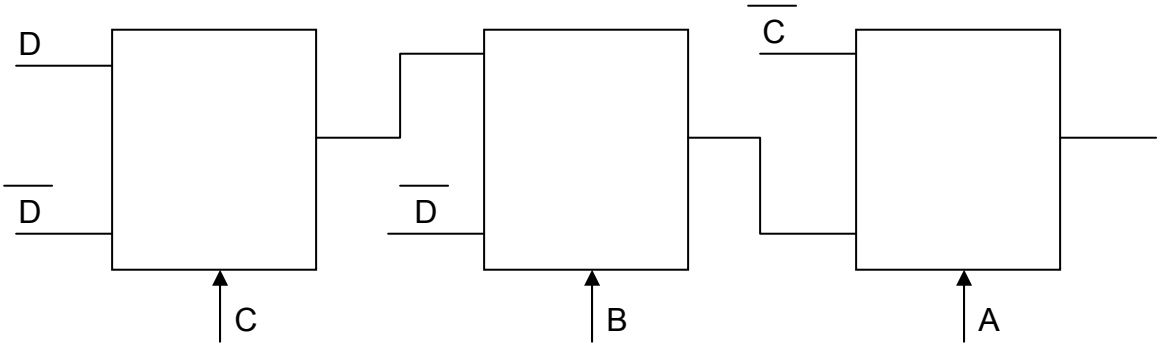


Fig. 9 Cascade 2-input MUX network derived from Fig.

Like the Gorai reference, Tosser does not disclose the use of TGMs for the multiplexer stages. Once again, the Board found that a person of ordinary skill in the art would have been motivated to use a TGM circuit as taught in Weste for the multiplexer stages in Tosser.

While the Board interpreted a number of claim terms during its proceedings, one claim term is important for this appeal. The Board interpreted the term "coupled to receive" in the claim phrase "control input terminal 'coupled to receive' a control signal" as a "[t]erminal capable of receiving a control signal. The control signal itself is not part of the claimed structure." Ex parte Translogic Tech., Inc., Appeal No. 2005-1050, Board of Patent Appeals and Interferences (May 31, 2005).

II

This court reviews claim construction without deference. Cybor Corp. v. FAS Techs., Inc., 138 F.3d 1448, 1456, 46 USPQ2d 1169, 1174 (Fed. Cir. 1998) (en banc); Markman v. Westview Instruments, Inc., 52 F.3d 967, 979 (Fed. Cir. 1995), aff'd, 517 U.S. 370 (1996). "[D]uring examination proceedings, claims are given their broadest reasonable interpretation consistent with the specification." In re Hyatt, 211 F.3d 1367, 1372 (Fed. Cir. 2000).

Section 103 within title 35 of the U.S. Code "forbids issuance of a patent when 'the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.'" KSR Int'l Co. v. Teleflex Inc., 550 U.S. ----; 127 S.Ct. 1727, 1734 (2007); (quoting 35 U.S.C. § 103). "Determination of obviousness under 35 U.S.C. § 103 is a legal conclusion based on underlying facts." In re Kumar, 418 F.3d 1361, 1365 (Fed. Cir. 2005). This court reviews "the Board's ultimate determination of obviousness de novo." In re Kotzab, 217 F.3d 1365, 1369 (Fed. Cir. 2000). However, the Board's underlying findings of fact receive review for substantial evidence. Id. "If the evidence in [the] record will support several reasonable but contradictory conclusions, we will not find the Board's decision unsupported by substantial evidence simply because the Board chose one conclusion over another plausible alternative." In re Jolley, 308 F.3d 1317, 1320 (Fed. Cir. 2002).

III

Translogic puts forth three major arguments that the Board erred in holding the claims of the '666 patent obvious over Gorai in view of Weste. First, Translogic contends that the Board incorrectly construed the claim term "coupled to receive." Second, Translogic contends that the Gorai reference is not relevant prior art with respect to the '666 patent. Third, Translogic contends that the Gorai reference does not disclose the use of TGMs, or in other words, that the record shows no motivation, in Weste or otherwise before the time of invention, to use TGMs for circuits in series. In effect, the Weste reference merely describes TGMs but does not suggest their use in this purported inventive combination.

The Board construed the term "coupled to receive" signals to mean terminals merely "capable of receiving" signals. Translogic argues that the Board should follow the claim construction in the companion infringement case from the United States District Court for the District of Oregon. The Oregon District Court determined that "signal input terminal 'coupled to receive' an input variable" would mean "connected to receive an input variable, directly or through one or more intervening inverters or buffers." Translogic Tech., Inc. v. Hitachi, Ltd., Hitachi America, Ltd., and Renesas Tech. America, Inc., Civ. No. 99-407-PA (D. Or. May 12, 2005) (Claim Construction Chart). Under this construction, representative claims 47 and 48 require each input and control input terminal to be connected to receive a variable signal from a different source. Thus, according to Translogic, the Gorai reference does not disclose that each input and control input terminal must receive a variable signal from a different source.

Instead, according to Translogic, Gorai teaches logic circuits with input terminals coupled to share signals and receive constants.

In Phillips v. AWH Corp., 415 F.3d 1303 (Fed. Cir. 2005) (en banc), this court set forth the best practices for claim construction. According to that decision, the words of a claim "are generally given their ordinary and customary meaning." Id. at 1312. The ordinary and customary meaning "is the meaning that the term would have to a person of ordinary skill in the art in question." Id. at 1313. For this reason, "claims must be read in view of the specification, of which they are a part." Id. at 1315. (internal quotations omitted). The specification "is the single best guide to the meaning of a disputed term." Id.

Representative claim 47, like representative claim 48, clearly claims a multiplexer circuit with a number of 2:1 TGMs connected in series. While claim 47 specifies a 4:1 multiplexer, claim 48 specifies a 5:1 multiplexer. Both claims specify that the multiplexer circuit connects 2:1 TGMs in series. Thus, under the terms of the patent, an N:1 multiplexer connects (N-1) TGMs in series with each TGM controlled by a corresponding (N-1) control input signal. '666 Patent col.3 ll.63-66. Fig. 3 from the '666 patent shows the claimed circuit for the 4:1 multiplexer.

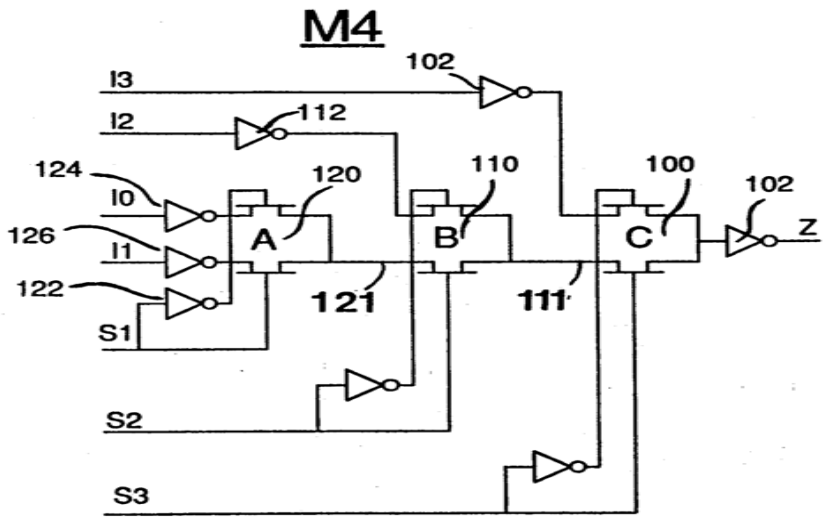


FIG 3

The words of the claim coupled with the specification define the term "input terminals 'coupled to receive' first and second input variables." First, the claim terms do not specify any structural connection for the input terminals. Furthermore, Fig. 3 of the '666 patent and the other figures show no structural connection for the input terminals (i.e., I0, I1, … I(N-1)) or the control input terminals (i.e., S1, S2, S3). In fact, Translogic admits, as is proper for a structural circuit, that the input variables (i.e., signals) are not part of the claimed invention.

A claim language comparison also shows the proper construction for the term at issue for the '666 patent. Claim 47 has two similar, but significantly different phrases, "coupled to receive" and "coupled to." The term "coupled to" in the phrase "second stage input terminal 'coupled to' the first stage output terminal" defines a connection between the TGMs. In other words, "coupled to" in the context of this claim phrase defines the connection between two of the TGMs essential for a series multiplexer.

On the other hand, the term "coupled to receive" in the phrase "input terminals 'coupled to receive' first and second input variables" does not specify a particular

connection. In other words, the claimed circuit does not require any specific input or connection. Instead, like any logic circuit, this part of the circuit only accepts inputs from an external source. As such, "coupled to" and "coupled to receive" are clearly different in the claimed '666 patent multiplexer circuit. As shown in Fig. 3 of the '666 patent, the input terminals (i.e., I0, I1, …, I(N-1)) only need to be "capable of receiving" an input variable for the multiplexer circuit as claimed in the '666 patent. Even if the input terminals are not connected, the circuit claimed in the '666 patent defines a series multiplexer. Therefore, this court agrees with the Board's construction that "coupled to receive" means "capable of receiving." With the disputed term limitation decided, this court now turns to obviousness.

An invention is unpatentable as obvious if the differences between the patented subject matter and the prior art would have been obvious at the time of invention to a person of ordinary skill in the art. In re Gartside, 203 F.3d 1305, 1319 (Fed. Cir. 2000). In a recent case, the Supreme Court reiterated the basic principles for an obviousness inquiry. KSR Int'l Co. v. Teleflex Inc., 550 U.S. ----, 127 S.Ct. 1727 (2007). KSR featured rather simple technology – an adjustable throttle pedal for an automobile, the Engelgau patent (U.S. Pat. No. 6,237,565 ("the '565 patent")). Adjustable pedal technology accommodates an automobile throttle to drivers of different heights. This patented technology combined an adjustable pedal with an electronic sensor to measure the pedal depression. Both of these features were in the prior art. An Asano patent claimed an adjustable pedal like Engelgau; a Rixon patent (as modified by a Smith reference) disclosed electronic calibration features like Engelgau. The PTO had not considered the Asano reference during the prosecution of the Engelgau patent.

When Teleflex sued KSR for infringement, the district court invalidated the '565 patent on summary judgment. This court reversed because the trial court had not made specific findings to show a teaching, suggestion, or motivation to combine ("TSM test"). The Supreme Court, in turn, reversed: "A person having ordinary skill in the art could have combined Asano with a pedal position sensor in a fashion encompassed by claim 4, and would have seen the benefits of doing so." KSR Int'l Co., 550 U.S. at ----, 127 S.Ct. at 1743.

On one level, KSR corrected a rather straightforward error. The error appears right before footnote 3 in this court's opinion:

> In this case, the Asano patent does not address the same problem as the '565 patent. The objective of the '565 patent was to design a smaller, less complex, and less expensive electronic pedal assembly. The Asano patent, on the other hand, was directed at solving the "constant ratio problem."

Teleflex, Inc. v. KSR Int'l, Co., 119 Fed. App'x. 282, 288 (Fed. Cir. 2005). This passage overlooks the fundamental proposition that obvious variants of prior art references are themselves part of the public domain. See KSR Int'l Co., 550 U.S. at ----, 127 S.Ct. at 1743; Dystar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick Co., 464 F.3d 1356, 1361 (Fed. Cir. 2006); In re Dembiczak, 175 F.3d 994, 999 (Fed. Cir. 1999) ("We have noted that evidence of a suggestion, teaching, or motivation to combine may flow from the prior art references themselves, the knowledge of one of ordinary skill in the art, or, in some cases, from the nature of the problem to be solved . . . ."). In the context of KSR, the Asano teachings and its obvious variants were relevant prior art, even if that patent did address a different problem (the constant ratio problem). The Supreme Court highlighted that error in its opinion:

> The primary purpose of Asano was solving the constant ratio problem; so, the court concluded, an inventor considering how to put a sensor on an adjustable pedal would have no reason to consider putting it on the Asano pedal. Common sense teaches, however, that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle. Regardless of Asano's primary purpose, the design provided an obvious example of an adjustable pedal with a fixed pivot point; and the prior art was replete with patents indicating that a fixed pivot point was an ideal mount for a sensor. The idea that a designer hoping to make an adjustable electronic pedal would ignore Asano because Asano was designed to solve the constant ratio problem makes little sense.

KSR Int'l Co., 550 U.S. at ----, 127 S.Ct. at 1742.

The Supreme Court also criticized this court's "rigid and mandatory" application of the motivation to combine test: "The obviousness analysis cannot be confined by a formalistic conception of the words teaching, suggestion, and motivation, or by overemphasis on the importance of published articles and the explicit content of issued patents." Id. at 1741. Instead, the Supreme Court advised that "common sense" would extend the use of customary knowledge in the obviousness equation: "A person of ordinary skill is also a person of ordinary creativity, not an automaton." Id. at 1742. Thus, the Supreme Court set aside any "rigid" application of the TSM test and ensured use of customary knowledge as an ingredient in that equation.

The Supreme Court observed that this court had also "elaborated a broader conception of the TSM test than was applied in [KSR]." Id. at 1743. Specifically the Court referred to Dystar Textilfarben GmbH & Co. v. C.H. Patrick Co., wherein this court noted: "Our suggestion test is in actuality quite flexible and not only permits, but requires, consideration of common knowledge and common sense." 464 F.3d 1356, 1367 (Fed. Cir. 2006) (emphasis original). The Court suggested that this formulation

would be more consistent with the Supreme Court's restatement of the TSM test. KSR Int'l Co., 127 S.Ct. at 1739. In any event, as the Supreme Court suggests, a flexible approach to the TSM test prevents hindsight and focuses on evidence before the time of invention, see, e.g., In re Rouffet, 149 F.3d 1350, 1357 (Fed. Cir. 1998), without unduly constraining the breadth of knowledge available to one of ordinary skill in the art during the obviousness analysis.

This court finds that the claims of the '666 patent were unpatentable under 35 U.S.C. § 103(a). Gorai is within the scope of the relevant prior art because it both pre-dates the '666 patent filing date of March 15, 1991 and discloses series 2-input multiplexer circuits. See Stratoflex, Inc. v. Aeroquip Corp., 713 F.2d 1530, 1535 (Fed. Cir. 1983). Moreover a person of ordinary skill in the art would have a thorough understanding of electrical switching systems and knowledge of actual electrical implementations of multiplexers such as the TGMs in Weste.

Specifically, the Gorai reference uses serial connectivity of 2:1 multiplexers, each described as M(1), to realize logic functions. The subject matter of the Gorai reference explains an approach (i.e., algorithm) to analyze mathematical dependencies among desired inputs and then selects appropriate input connections as well as series connectivity between M(1) multiplexers to realize the specified logic function. For example, the Gorai algorithm could result in the circuit in Fig. 6 defined by logic function: $f_2(x_1, x_2, x_3, x_4) = \Sigma (0, 5, 7, 8, 9, 12, 13)$.

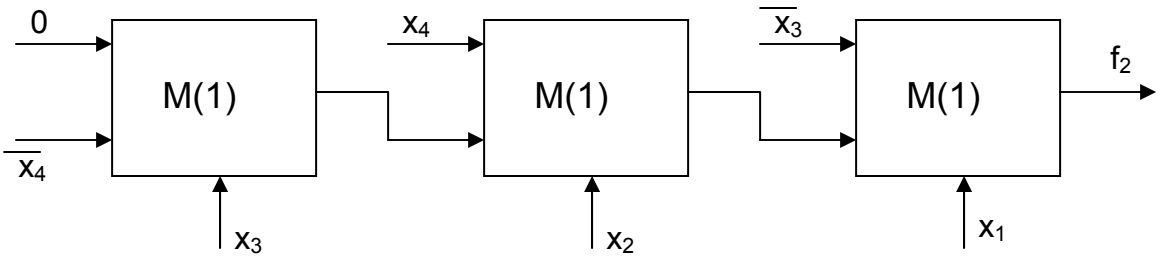


Fig. 6 Cascade network of f_2

In this appeal, Translogic proffers two arguments to attempt to show that the Gorai reference is not prior art with respect to the '666 patent. Initially, Translogic contends that neither the Gorai algorithm nor its circuit realizations provide a multiplexer function. In fact, since the entire point of Gorai's article revolves around logic, not multiplexing, with series connectivity among M(1) circuits, Translogic contends that Gorai teaches away from multiplexers. Next, Translogic contends that the Gorai reference discloses an algorithm capable of providing designs for a large number of circuits, while the inventor of the '666 patent was modifying one circuit, a multiplexer, with utmost regard for its performance. In other words, while Gorai discloses an algorithm to design logic circuits based on functional parameters, the '666 patent improves a known circuit. In sum, Translogic's argument tries to state that the Gorai reference is not relevant prior art because the reference does not specifically disclose a N:1 series multiplexer but only discloses an algorithm to realize logic functions by using 2:1 multiplexers connected in series.

In its prior art argument, Translogic is making the same error corrected by the Supreme Court in KSR. Translogic mistakenly argues that variants of a circuit connecting 2:1 multiplexers in series are not relevant prior art with respect to the '666 patent because these variants do not address the same problem, namely an improved

multiplexer circuit. However, this argument overlooks the fundamental proposition that the series circuits in Gorai are prior art within the public domain and the common knowledge of a person of ordinary skill in the art. Thus, the Gorai reference is a relevant prior art reference with respect to the '666 patent and clearly discloses a series 2:1 multiplexer circuit.

Translogic also puts forth a prior art argument based on the circuit inputs. Translogic contends that Fig. 3 in Gorai (see below) is a half-bare, incomplete circuit because all h and g inputs are undefined (variables or constants) and therefore the Fig. 3 circuit only shows three control inputs (x_1, x_{p-1} and x_p).

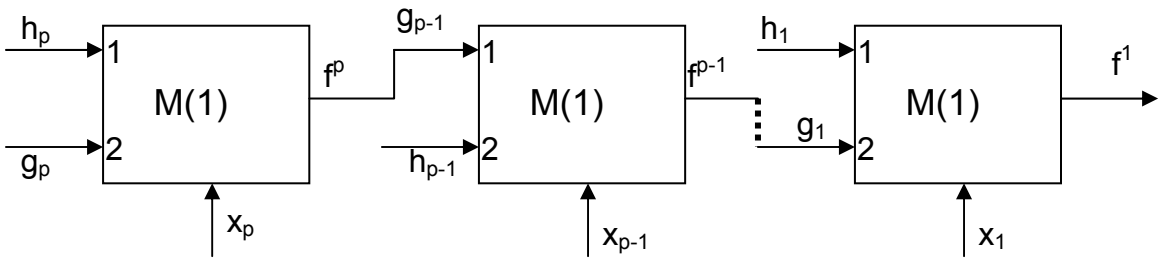


Fig. 3. A cascade network of p-stages of M(1)s

Therefore, Translogic states that the Gorai Fig. 3 circuit cannot be a multiplexer because the inputs are not specifically defined to realize a N:1 series multiplexer circuit (4:1 in this example).

Translogic's input argument is without merit. Claims 47 and 48 of the '666 patent define a series multiplexer circuit. Gorai Fig. 3 discloses the same serial multiplexer circuit. As any person of ordinary skill in the art would understand, the inputs to a circuit do not change the circuit itself. Therefore, this court finds that Gorai discloses a series multiplexer circuit as claimed in the '666 patent. Thus, the Board was correct in concluding that the Gorai reference discloses a series multiplexer circuit.

Lastly, Translogic contends that Gorai does not teach or suggest the use of TGMs for each M(1) stage (i.e., 2:1 multiplexer). Translogic admits that the Weste reference does disclose a TGM circuit; however, Translogic argues that Weste provides no specific teaching, suggestion or motivation to use TGMs in a series circuit such as shown in Gorai Fig. 3. Furthermore, Translogic notes that Weste discloses a TGM used for a single multiplexer but does not include any reference to coupled TGMs in series. Thus, according to Translogic, the Weste reference does not provide the necessary teaching, suggestion or motivation to combine the use of TGMs with the Gorai reference.

As articulated by the Supreme Court in KSR, an obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." 550 U.S. at ----, 127 S.Ct. at 1741. In this case, a person of ordinary skill in the art at the time of the invention would have recognized the value of using a known element, a 2:1 TGM, as taught by Weste, for the 2:1 multiplexers in the series arrangement of multiplexers in Gorai. A person of ordinary skill in the art would have appreciated that any conventional multiplexer circuit could be utilized to implement the 2:1 multiplexer circuits in Gorai. After all, TGMs were well-known multiplexer circuits as evidenced by the Weste 1985 textbook. In other words, in looking for a multiplexer circuit for the individual 2:1 multiplexers disclosed in Gorai, a person of ordinary skill in the art would have solved this design need by "pursu[ing] known options within his or her technical grasp." Id. at 1742. Thus, this court agrees with the Board's determination. The Board based its decision on sound reasoning that a

person of ordinary skill in the art would select a specific circuit based on the need for a 2:1 multiplexer circuit for the individual multiplexers shown in Gorai. Specifically, a person of ordinary skill in the art at the time of the invention would have been able to choose TGMs as an option. While other circuits could have been used to implement the 2:1 multiplexers, TGMs were a well-known circuit as shown by the explanation of TGM circuits in the 1985 textbook by Weste. This court finds that substantial evidence in the record supports the Board's finding that a person of ordinary skill in the art would have used TGMs in the N:1 circuit configuration shown in Gorai. In sum, this court agrees with the Board's conclusion that the '666 patent is unpatentable under 35 U.S.C. § 103(a) over Gorai in view of Weste.

Because this court finds that Gorai in view of Weste renders the '666 patent unpatentable, the court will not address Tosser in view of Weste. However, the analysis of Tosser in view of Weste would undoubtedly reach the same result because Tosser also discloses a series multiplexer circuit.

IV

The decision of the Board, sustaining the final rejection of claims 16, 17, 39-45, 47 and 48 as obvious, is affirmed.

AFFIRMED