United States Court of Appeals for the Federal Circuit

RAMBUS INC.,
Appellant,

v.

TERESA STANEK REA, Acting Director, United States Patent and Trademark Office,
Appellee.

2012-1634

Appeal from the United States Patent and Trademark Office, Board of Patent Appeals and Interferences in Reexamination No. 95/001,134.

Decided: September 24, 2013

JAMES R. BARNEY, Finnegan, Henderson, Farabow, Garrett & Dunner, LLP, of Washington, DC, argued for appellant. With him on the brief were J. MICHAEL JAKES and MOLLY R. SILFEN.

WILLIAM LAMARCA, Associate Solicitor, United States Patent and Trademark Office of Alexandria, Virginia, argued for appellee. With him on the brief were NATHAN K. KELLEY, Deputy Solicitor, and COKE MORGAN STEWART, Associate Solicitor.

Before MOORE, LINN, and O'MALLEY, *Circuit Judges.*

MOORE, *Circuit Judge.*

Rambus Inc. appeals from the decision of the Board of Patent Appeals & Interferences (Board) holding invalid various claims of U.S. Patent No. 6,260,097 ('097 patent) for anticipation and obviousness. Rambus challenges the Board's claim construction and its obviousness decision. Because the Board correctly construed the claims but erred in its obviousness decision, we *affirm-in-part*, *vacate-in-part*, and *remand*.

BACKGROUND

This case relates to memory circuits known as dynamic random-access memory (DRAM). Conventional memory circuits transfer all of the data upon request, asynchronously. Each transfer can tie up the computer system for extended periods of time and create a "bottleneck" that slows down computer operations.

The '097 patent solves this problem using a synchronous memory system to transfer the data. In synchronous systems, a clock signal that alternates between a digital value of 0 and 1 synchronizes the operations within the system. The change in the clock signal from a 0 to a 1 is referred to as the "rising edge" of the clock, and the change in the signal from a 1 to a 0 is referred to as the "falling edge" of the clock. Figure 14 of the '097 patent depicts an exemplary clock signal:

In conventional synchronous memory systems, the data transmitted to the memory ties up the system for a full cycle of the clock signal. In contrast, the '097 patent

claims what Rambus refers to as the "dual-edge / double-data-rate" functionality because the system transfers data at twice the rate by employing both the rising and falling edges of the clock signal. Specifically, the invention separates the data into multiple portions and then transfers a portion during the rising edge of the clock signal and a portion during the falling edge of the clock signal. '097 patent, at [57]. Claim 1 of the '097 patent is representative of the claims at issue:

> A method of controlling a synchronous memory device . . . compris[ing]:
>
> issuing a *write request* to the memory device . . . ;
>
> providing a first portion of data to the memory device synchronously with respect to a rising edge transition of an *external clock signal*; and
>
> providing a second portion of data to the memory device synchronously with respect to a falling edge transition of the *external clock signal*.

'097 patent claim 1 (emphases added). The United States Patent and Trademark Office (PTO) initiated an *inter partes* reexamination of the '097 patent claims and ultimately found that the reexamined claims were not patentable over two references: Unexamined Japanese Patent Application No. 56-88987 (Inagaki) and the Intel iAPX system manual and specification (iAPX).

The following facts regarding Inagaki and iAPX are not in dispute. Inagaki discloses a memory system that transmits one bit during each half-cycle of the external clock. J.A. 2955–58. The half-cycle system disclosed in Inagaki is a modification of a conventional full-cycle system. *Id.* Inagaki achieves the half-cycle functionality by generating two clock signals based on the rising and falling edge of the external clock. *Id.* The two internal clock signals, in turn, synchronize the transfer of data during the two halves of the system clock cycle. *Id.*

The iAPX manual and specification disclose a system that transfers data based on the rising or falling edges of two system clocks. J.A. 3285, 3331. The system, however, utilizes the full clock cycle for each data transfer. *Id.* Thus, because the iAPX system employs a full clock cycle to transfer data to the memory device, the system cannot use both edges of the clock signal to synchronize the transfer of data portions to memory. However, Inagaki discloses a mechanism for converting a conventional full-cycle system into a half-cycle system. J.A. 2955–58.

The examiner rejected claims 1, 2, 7, 8, 10, and 14 as anticipated by Inagaki and rejected claims 1–5, 7, 8, 10–12, 14, 26, 28–32, and 35 as obvious in light of the iAPX system in view of Inagaki. The Board upheld the examiner's rejections. Rambus appeals. We have jurisdiction under 28 U.S.C. § 1295(a)(4)(A).

DISCUSSION

I. Applicable Law

We review the Board's factual findings for substantial evidence and its legal conclusions *de novo*. *In re Kotzab*, 217 F.3d 1365, 1369 (Fed. Cir. 2000). Whether a claim would have been obvious under 35 U.S.C. § 103(a) is a legal conclusion based on underlying factual determinations. *Id.* The factual determinations include (1) the scope and content of the prior art; (2) the differences between the claims and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness. *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17–18 (1966). "[W]hether there is a reason to combine prior art references is a question of fact." *Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1367 (Fed. Cir. 2012).

"[C]laim construction by the PTO is a question of law that we review *de novo* . . . ." *In re Baker Hughes Inc.*, 215 F.3d 1297, 1301 (Fed. Cir. 2000). "While claims are

generally given their broadest possible scope during prosecution, the Board's review of the claims of an expired patent is similar to that of a district court's review." *In re Rambus Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012) (citations omitted).

II. Anticipation

The Board upheld the examiner's finding that Inagaki anticipates a number of the '097 patent claims. As part of that decision, the Board construed the terms "external clock signal" and "write request." Rambus challenges the Board's construction of these claim terms.

A. "External Clock Signal"

The Board held that the "external clock signal" only requires the clock to be periodic during the data input phases, as opposed to being periodic for all system operations. *Rambus, Inc. v. Nvidia Corp.*, No. 2012-000171 (B.P.A.I. June 11, 2012) ("Board Opinion"). It reached this construction based on the established industry meaning of the term "clock" and the failure of the specification to disclose "a computer clock that runs forever or that cannot be turned off." *Id.* at 7-8.

Rambus contends that the intrinsic record requires the "external clock signal" to be continuously periodic. It argues that the claims contain this requirement because they recite a "synchronous memory device," and a clock signal synchronizes all operations in a synchronous device. Rambus contends that, consistent with the claims, the specification only discloses a periodic clock signal. Lastly, Rambus argues that, during prosecution of a related patent, the inventors distinguished the prior art on the basis that it did not teach a periodic clock signal.

The PTO counters that the claim language requires only that the memory device receive data "synchronously with respect to a rising edge transition" and the "falling edge transition" of "an external clock signal." According

to the PTO, this language shows that the "external clock signal" synchronizes data transfer and need not be periodic for all time.

We agree with the PTO. The claimed clock signal synchronizes data transfer to the memory device. The claimed method provides a first portion of data "synchronously with respect to a rising edge transition of an external clock signal" and then provides a second portion of data "synchronously with respect to a falling edge transition of the external clock signal." '097 patent claim 1. Thus, while the "external clock signal" must be periodic during data transfer, nothing in the claim language requires the signal to be periodic for all time. The specification also shows that the external clock signal is periodic during the transfer of data. *Id.* fig. 14. Nothing in the specification limits the external clock signal to a clock that is periodic for all time. Nor does the prosecution history upon which Rambus relies require a narrower construction. There, consistent with the plain language of the claims, the inventors explained that the "external clock signal" is "a periodic signal used to orchestrate timing events." J.A. 2700 n.2 (emphasis omitted). Accordingly, we conclude that the Board properly construed the term "external clock signal."

B. "Write Request"

The Board concluded that the claimed "write request" could include "the state of a signal," which is usually represented by a single bit. Board Opinion at 11–13. The Board held that its construction comported with our holding in a prior case involving the same family of patents as the '097 patent, *Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1093 (Fed. Cir. 2003). In that case, we construed the term "write request" to mean "a series of bits used to request a write of data." *Id.*

Rambus argues that the Board erroneously construed "write request" to cover conventional, transition-based

control signals and disregarded our construction from *Infineon*. It asserts that the specification clearly shows that a "write request" includes multiple bits because each request carries at least two pieces of information.

The PTO responds that the Board properly declined to limit the term "write request" to a sequence of multiple bits. It argues that the plain and ordinary meaning of the term allows for a one-bit signal. The PTO also points to the specification's disclosure of an embodiment in which a single bit determines whether the system requests a read operation or a write operation. Lastly, the PTO argues that the Board's construction is not inconsistent with the construction in *Infineon* because that case did not decide if such a "series of bits" could include one bit or a signal.

We agree with the PTO that the Board correctly construed "write request." As an initial matter, we do not find that the Board disregarded our construction in *Infineon*. In *Infineon*, the dispute centered on the accused infringer's contention that the claimed "request" must include both address and control information. 318 F.3d at 1091. We rejected that argument. *Id.* at 1091–93. At no point did we resolve the claim-scope dispute presented in this appeal: whether the "write request" can be a single bit. Indeed, it appears that the parties in *Infineon* did not dispute the "series of bits" portion of the district court's claim construction, *id.* at 1091–92, and we generally "decline to raise an issue *sua sponte* that the parties have not presented," *WMS Gaming Inc. v. Int'l Game Tech.*, 184 F.3d 1339, 1347 n.2 (Fed. Cir. 1999).

We conclude that "write request" is not limited to a multiple-bit request. The plain language of the claim does not contain that requirement. The claims require a "write request" be issued to the memory device and that, in response to the request, the device sample portions of data. '097 patent claim 1. Moreover, the specification expressly discloses that "write request" can be embodied

in a single bit. '097 patent col. 9 ll. 38–64. The specification discloses a preferred embodiment in which a single bit acts as a "Read/Write switch": if its value is a 1, the system requests a read; if its value is a 0, the system requests a write. *Id.* "A claim construction that excludes the preferred embodiment 'is rarely, if ever, correct and would require highly persuasive evidentiary support.'" *Adams Respiratory Therapeutics, Inc. v. Perrigo Co.*, 616 F.3d 1283, 1290 (Fed. Cir. 2010) (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583–84 (Fed. Cir. 1996)). There is no such evidentiary support here, and Rambus points to nothing in the intrinsic record that limits the claims to multi-bit requests. We conclude that the Board properly construed "write request."

* * * * *

Because the Board correctly construed the "external signal" and "write request" limitations, we affirm the Board's finding that Inagaki anticipates claims 1, 2, 7, 8, 10, and 14 of the '097 patent.

III. Obviousness

The Board held that the reexamined claims would have been obvious in view of iAPX in combination with Inagaki. The Board concluded that one of skill in the art could have modified the existing circuitry in the iAPX system to use both edges of the clock signal to transfer data at twice the rate based on Inagaki. Board Opinion at 21–28. The Board's particular findings, however, differed from those of the examiner. The examiner found that one of skill in the art would have been motivated to modify the iAPX system to transfer data on both the rising and falling edges of the clock signal because the system "does not show that all edges are used." J.A. 1113. All parties appear to agree on appeal that this fact finding was erroneous and that iAPX employs both the rising and falling edges.

The Board found that a skilled artisan "easily could have modified the iAPX system in view of Inagaki's clocking scheme by dropping, instead of replacing, many functions." Board Opinion at 24. It found that a skilled artisan could have achieved data transfer on both clock edges by using a slower clock in Inagaki as a "trigger" for the faster clocks disclosed in iAPX. *Id.* at 24–25. The Board provided a number of reasons why skilled artisans would modify the iAPX system to hold data for less than one full cycle, enabling it to transfer data on both the rising and falling edges of its clocks. *Id.* at 25–27.

The Board then addressed Rambus's objective evidence of nonobviousness, concluding that it lacked a nexus to the '097 patent claims. *Id.* at 28–32. The Board found that Rambus's evidence was not commensurate with the scope of the claims and related to claim limitations that were disclosed in the prior art. *Id.* The Board found that Rambus's licensing evidence lacked a nexus because "it is well established that competitors have many reasons for taking licenses which are not necessarily related to unobviousness (i.e., litigation costs, etc.)." *Id.* at 30.

Rambus argues that the Board erred in its obviousness decision. It contends that the Board erroneously placed the burden on Rambus to demonstrate nonobviousness. It asserts that, rather than rely on the examiner's flawed findings, the Board relied on unsubstantiated conjecture that one could combine iAPX and Inagaki into an operable system. Rambus contends that the reference actually teaches away from using both clock edges to transfer data. It argues that strong objective evidence of nonobviousness, including praise for the dual-edge functionality in industry publications and the licensing of the '097 patent, supports a conclusion that the claims would not have been obvious.

The PTO counters that the Board properly held that the claims would have been obvious. It contends that the only claim limitation that iAPX does not disclose is the synchronous writing of data to memory during the rising and falling edges of a clock signal. It argues that Inagaki expressly discloses that missing feature. The PTO argues that a skilled artisan would have combined iAPX and Inagaki because, even if the combination required further modifications to the combined system, both references seek to increase the speed and efficiency of memory-writing operations. Regarding Rambus's arguments that the Board improperly relied on its own conjecture, the PTO asserts that the Board is entitled to make its own fact findings when interpreting prior art references and is permitted to rely on common sense.

The PTO contends that Rambus's objective evidence of nonobviousness cannot overcome the strong showing of obviousness. It asserts that Rambus's evidence lacks a nexus to the '097 patent claims because the claims do not require a specific clock speed. The PTO further argues that Rambus's patent licenses were not cogent evidence of commercial success because they involved a portfolio of patents, not simply the '097 patent. It argues that Rambus never showed that the value exchanged in the licenses was tied to the value of the invention claimed in the '097 patent, as opposed to the other patents in the portfolio or the licensees' desire to avoid litigation costs.

We agree with Rambus that the Board committed multiple errors in its obviousness decision. Due to these errors, we vacate the Board's decision and remand for further proceedings. We address each of these errors below.

A. Burden of Proof

The Board erroneously placed the burden on Rambus to prove that its claims were not obvious. In reexamination proceedings, "a preponderance of the evidence must

show nonpatentability before the PTO may reject the claims of a patent application." *Ethicon, Inc. v. Quigg*, 849 F.2d 1422, 1427 (Fed. Cir. 1988); *see also In re Jung*, 637 F.3d 1356, 1365–66 (Fed. Cir. 2011) (explaining that while "the applicant must identify to the Board what the examiner did wrong, . . . the examiner retains the burden to show invalidity"). The Board instead concluded that "Rambus ha[d] not demonstrated that skilled artisans . . . would not have been able to arrive at the broadly claimed invention." Board Opinion at 27; *see also id.* at 24 (holding that "Rambus fail[ed] to present evidence that skilled artisans would have been unable to modify" iAPX to achieve the claimed invention). That was legal error.

B. New Fact Findings

The Board also exceeded its limited role to "review of the examiner's decisions during prosecution." *In re Stepan Co.*, 660 F.3d 1341, 1344 (Fed. Cir. 2011). Under the Administrative Procedure Act, the PTO must ensure that the parties before it are "fully and fairly treated at the administrative level." *In re Leithem*, 661 F.3d 1316, 1319 (Fed. Cir. 2011). Namely, the PTO must "provide prior notice to the applicant of all 'matters of fact and law asserted' prior to an appeal hearing before the Board." *Stepan*, 660 F.3d at 1345 (quoting 5 U.S.C. § 554(b)(3)).

This framework limits the Board's ability to rely on different grounds than the examiner. The Board may not "rel[y] on new facts and rationales not previously raised to the applicant by the examiner." *Leithem*, 661 F.3d at 1319. Of course, the Board is not required to "recite and agree with the examiner's rejection *in haec verba*" in order to ensure that the PTO has provided adequate notice. *Id.* And the Board may elaborate on the examiner's findings, so long as the appellant had an adequate opportunity to respond to the Board's findings during the PTO proceeding. *In re Adler*, 723 F.3d 1322, 1328 (Fed. Cir. 2013). The ultimate criterion is whether the appellant has had

before the PTO a "fair opportunity to react to the thrust of the rejection." *Jung*, 637 F.3d at 1365 (quoting *In re Kronig*, 539 F.2d 1300, 1302–03 (CCPA 1976)) (internal quotation marks omitted). If that condition is not met, the Board must designate its decision a new ground of rejection and provide the appellant with an opportunity to respond. *See Stepan*, 660 F.3d at 1346; 37 C.F.R. § 41.77(b). Failure to do so violates the appellant's notice rights and warrants vacatur of the Board's decision. *Stepan*, 660 F.3d at 1346. Whether the Board relied on a new ground of rejection is a legal issue that we review *de novo*. *Id.* at 1343.

The Board erred when it supplied its own reasons to combine iAPX and Inagaki. The examiner issued a specific finding—that one of skill in the art would have been motivated to modify the iAPX system to transfer data on both the rising and falling edges of the clock signal because the system "does not show that all edges are used." J.A. 1113. The PTO does not dispute that this finding was erroneous. iAPX quite clearly employed both the rising and falling edges of the clock signal. Recognizing this problem, the Board instead found that a skilled artisan would have been able to drop functionality that iAPX discloses as occurring during the rising and falling edges of the clock. Board Opinion at 23–24. It also provided additional ways to combine iAPX and Inagaki to create a half-cycle system that could transfer data on both the rising and falling edges of its clocks. *Id.* at 24–27. These findings were completely new; the Board did not elaborate on the examiner's findings with "more detail." *See Adler*, 723 F.3d at 1328. While the Board's findings may ultimately be correct, we will not affirm a Board rejection, like this one, which essentially provides a new motivation to combine the references.

The Board has a procedure for issuing a new ground of rejection in appeals of *inter partes* reexaminations. 37 C.F.R. § 41.77(b). This procedure ensures that appellants

have an appropriate opportunity to respond and, if necessary, supplement the record before the examiner. We cannot let the Board shortcut this procedure and deprive appellants of their due process rights. To be clear, we are not passing judgment on the merits of the Board's findings regarding the motivation to combine.

C. Objective Evidence of Nonobviousness

We also agree with Rambus that the Board erred in its treatment of objective evidence of nonobviousness. Such objective evidence can establish that "an invention appearing to have been obvious in light of the prior art was not." *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 1538 (Fed. Cir. 1984). In some cases, that evidence is "the most probative and cogent evidence in the record." *Id.* It helps "turn back the clock and place the claims in the context that led to their invention." *Mintz v. Dietz & Watson, Inc.*, 679 F.3d 1372, 1378 (Fed. Cir. 2012). "For objective evidence . . . to be accorded substantial weight, its proponent must establish a nexus between the evidence and the merits of the claimed invention." *In re Kao*, 639 F.3d 1057, 1068 (Fed. Cir. 2011) (quoting *Wyers v. Master Lock Co.*, 616 F.3d 1231, 1246 (Fed. Cir. 2010)) (emphasis omitted) (internal quotation marks omitted).

The Board erred when it found that Rambus's objective evidence of nonobviousness lacked a nexus because it related to unclaimed features. Rambus presented uncontested evidence of long-felt need and industry praise due to the claimed dual-edge data transfer functionality claimed in the '097 patent. For example, an article in the Microprocessor Report stated that Rambus "ha[d] unveiled its radical new processor-to-memory interface and DRAM architecture, which promise to create the most significant change in processor/memory system architecture since the introduction of the DRAM two decades ago." J.A. 2633. The article explains that the technology "operat[es] with a 250-MHz clock and transfer[s] a byte of

data on each clock edge," an approach that was "somewhat counter-intuitive." *Id.* A press release issued by Micron Technology, Inc., a Rambus competitor, referred to the dual-edge data transfer functionality as a "revolutionary and pioneering technology" that "vastly improv[ed]" the performance of memory chips. J.A. 1711. The Board did not address any of this evidence.

The Board also erroneously found that Rambus's evidence relating to high-speed memory systems was not commensurate with the scope of the claims because the claims "do not recite a specific clock speed and therefore embrace slow memory devices." Board Opinion at 29–30. Such a strict requirement was improper. Objective evidence of nonobviousness need only be "reasonably commensurate with the scope of the claims," and we do not require a patentee to produce objective evidence of nonobviousness for every potential embodiment of the claim. *Kao*, 639 F.3d at 1068; *In re Glatt Air Techniques, Inc.*, 630 F.3d 1026, 1030 (Fed. Cir. 2011) ("[W]e have consistently held that a patent applicant 'need not sell every conceivable embodiment of the claims in order to rely upon evidence of commercial success.'") (quoting *In re DBC*, 545 F.3d 1373, 1384 (Fed. Cir. 2008)). Moreover, Rambus's evidence shows beyond dispute that the claimed dual-edge data transfer functionality is what enabled the praised high-speed transfer of data. A Byte Magazine article explained that, "by using both edges of a 250-MHz clock," Rambus's memory chips "will deliver a tenfold increase in component throughput." J.A. 2623. The Electronic Engineering Times likewise described the dual-edge functionality as "designed to burst the bottleneck between processors and DRAMs in desktop systems." J.A. 2624–25. The Board did not point to any contrary evidence, and we have not found any in the record.

Nor is there substantial evidence to support the Board's finding that Rambus's licensing evidence lacked a nexus to the reexamined claims. Rambus's undisputed

evidence linked its commercial success to the claimed dual-edge data transfer functionality. For example, an Electronic Engineering Times article relayed that Fujitsu Ltd., NEC Corp., and Toshiba Corp. had paid "substantial license fees to participate in the technology." J.A. 2624. The article noted that a "key part" of Rambus's licensed memory technology is the memory bus that "moves one byte on each clock edge." J.A. 2625. By the mid-1990s, Rambus also obtained licenses from Hitatchi, Ltd., Oki Electric Industry Co., Lucky Goldstar, and Intel Corp. J.A. 2099. The Board held that this evidence lacked a nexus because "competitors have many reasons for taking licenses which are not necessarily related to unobviousness," Board Opinion at 30, but this finding lacks any supporting evidence. Similarly, there is no evidence in the record to support the PTO's assertion that the commercial value of the licenses stemmed from other licensed Rambus patents. Indeed, the only evidence before the Board points to a contrary conclusion.

The Board's finding that all of Rambus's evidence lacked a nexus because dual-edge functionality was already disclosed in Inagaki, and therefore "not novel," is also erroneous. *Id.* at 29–30. While objective evidence of nonobviousness lacks a nexus if it exclusively relates to a feature that was "known in the prior art," *Ormco Corp. v. Align Tech., Inc.*, 463 F.3d 1299, 1312 (Fed. Cir. 2006), the obviousness inquiry centers on whether "the claimed invention as a whole" would have been obvious, 35 U.S.C. § 103. Rambus's objective evidence of nonobviousness was not limited to the dual-edge functionality in Inagaki that transferred a single bit each half-cycle of an external clock. *See* J.A. 2955–58. At least some of Rambus's objective evidence of nonobviousness pertained to Rambus's overall memory device architecture. On remand, the Board should be careful to parse the evidence that relates only to the prior art functionality and the evidence that touted Rambus's patented design as a

whole. We decline to make these fact findings for the first time on appeal. We leave it to the PTO, for the '097 patent claims that remain on remand, to determine if Rambus's objective evidence of nonobviousness pertains to the Rambus device or simply to the dual-edge functionality disclosed in Inagaki.

* * * * *

The Board erred when it failed to provide Rambus an opportunity to respond to its new grounds for rejecting the claims as obvious. The Board also erred in its analysis of Rambus's objective evidence of nonobviousness. Due to these errors, we vacate the Board's decision that claims 3–5, 11, 12, 26, 28–32, and 35 are unpatentable. We express no opinion, however, as to whether those claims should issue.

CONCLUSION

For the foregoing reasons, we *affirm-in-part* and *vacate-in-part* the Board's decision and *remand* for further proceedings.

AFFIRMED-IN-PART, VACATED-IN-PART, AND REMANDED

COSTS

Costs to Appellant.