United States Court of Appeals for the Federal Circuit

POLARIS INNOVATIONS LIMITED,
Appellant

v.

DERRICK BRENT, DEPUTY UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DEPUTY DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE,
Intervenor

2019-1483

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2017-01500.

POLARIS INNOVATIONS LIMITED,
Appellant

v.

DERRICK BRENT, DEPUTY UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DEPUTY DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE,
Intervenor

2019-1484

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2017-00901.

Decided: September 15, 2022

MATTHEW C. PHILLIPS, Laurence & Phillips IP Law LLP, Washington, DC, argued for appellant. Also represented by KEVIN BRENT LAURENCE, DEREK MEEKER; PAUL EHRLICH, MATTHEW D. POWERS, STEFANI SMITH, Tensegrity Law Group LLP, Redwood Shores, CA.

MAUREEN DONOVAN QUELER, Office of the Solicitor, United States Patent and Trademark Office, Alexandria, VA, argued for intervenor in 2019-1483. Also argued by OMAR FAROOQ AMIN in 2019-1484. Also represented by THOMAS W. KRAUSE, ROBERT J. MCMANUS, FARHEENA YASMEEN RASHEED; MICHAEL S. FORMAN in 2019-1483; MELISSA N. PATTERSON, Appellate Staff, Civil Division, United States Department of Justice, Washington, DC.

Before PROST, CHEN, and STOLL, *Circuit Judges*.

STOLL, *Circuit Judge*.

These appeals involve two inter partes review proceedings initiated by NVIDIA Corporation challenging two patents owned by Polaris Innovations Limited—U.S. Patent Nos. 6,532,505 and 7,405,993. The Patent Trial and Appeal Board determined that all challenged claims are unpatentable. Polaris appealed. We remanded the case due

to Appointments Clause issues and it has now returned. We affirm.

BACKGROUND

I

These appeals involve two unrelated patents directed to computer memory. The '993 patent, at issue in the 19-1484 appeal, relates to an improved control component configuration. The '505 patent, at issue in the 19-1483 appeal, involves a shared-resource system in which logical controls are used to manage resource requests.

A

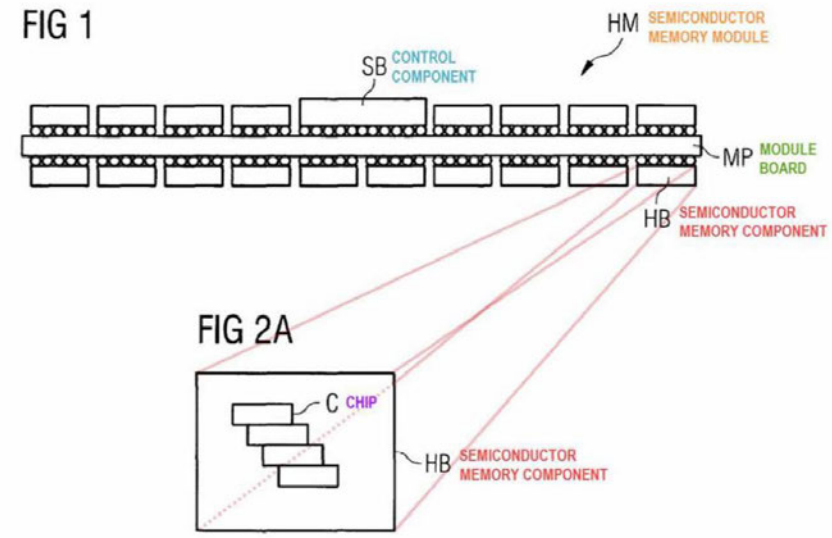
The '993 patent is titled "Control Component for Controlling a Semiconductor Memory Component in a Semiconductor Memory Module." '993 patent, Title. The specification explains that the control component can send both address signals and control signals through the same leads, allowing the control component to perform its functions with fewer leads. *See, e.g.*, *id.* at col. 2 l. 57–col. 3 l. 23.

On appeal, Polaris's argument focuses on dependent claim 2's requirement that the "semiconductor memory component comprises a plurality of memory chips." *Id.* at col. 11 ll. 39–40. Claim 2 (and independent claim 1 from which claim 2 depends) recites:

> 1. A control component for controlling a semiconductor memory component in a semiconductor memory module, comprising:
>
> a control unit for generating control signals for controlling read and write access to the semiconductor memory component and for generating address signals for addressing memory cells in the semiconductor memory component for read and write access;

> a plurality of address terminals for providing the address signals; and
>
> a selection circuit for supplying one of the address terminals with a selected signal selected between one of the address signals and one of the control signals.
>
> 2. The control component as claimed in claim 1,
>
> *wherein the semiconductor memory component comprises a plurality of memory chips*; and
>
> wherein the control unit generates a first of the control signal for selecting one of the memory chips for read and write access.

Id. at col. 11 ll. 25–43 (emphasis added to disputed limitation). Polaris correlates the terms in claim 2 to Figures 1 and 2 of the '993 patent, shown in a combined fashion below:



19-1484 Appellant's Br. 7 (annotating '993 patent, Figs. 1 & 2A). As described in the claims and shown in the figures above, the chips (C) are a part of the semiconductor memory component (HB) which is integrated into the

semiconductor memory module (HM). The semiconductor memory module also includes a control component (SB).

B

The '505 patent describes a "universal resource access controller" (104) for directing requests for a shared resource, such as a shared memory (108):

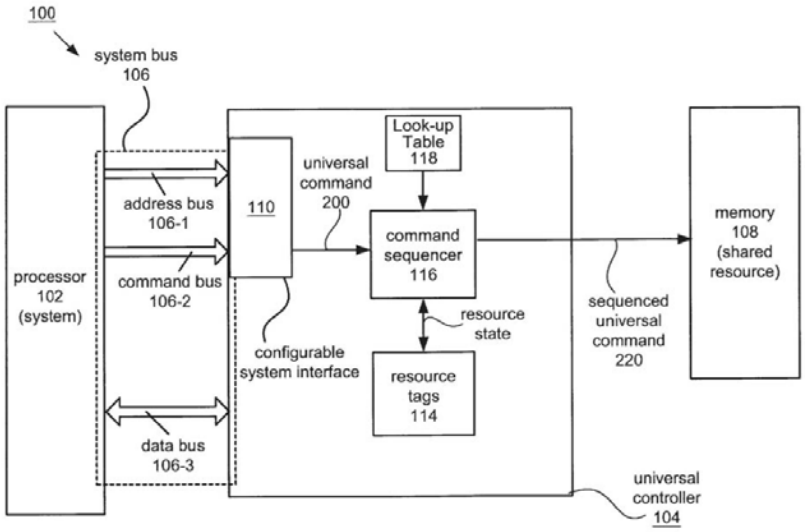


Fig. 1B

'505 patent, Fig. 1B; *see also id.* at Title.

The '505 patent discloses that the controller uses certain information to direct shared-resource requests, including: (1) the "current state" of the shared resource, *id.* at col. 7 ll. 3–29, (2) the "requested state" of a shared resource, *id.* at col. 27 l. 41–col. 30 l. 19, and (3) a "characteristic operating parameter" of the shared resource, *id.* at col. 7 l. 61–col. 8 l. 23, col. 8 l. 56–col. 9 l. 5. The dispute on appeal centers on this shared-resource request information, and in particular where that information is stored. Dependent claim 2 requires these pieces of information to be stored in certain "buffers," as recited below:

1. A universal resource access controller coupled to a requesting system and a resource, wherein when the requesting system desires access to the resource, the requesting system generates a resource access request which is passed to the universal resource controller which, in turn, uses a specific characteristic operating parameter of the requested resource, a current state of the requested resource, and a requested state of the requested resource to generate a corresponding sequenced command suitable for accessing the resource as required by the requesting system.

2. A universal resource access controller as recited in claim 1, wherein the universal resource controller comprises:

a configurable system interface coupled to the requesting system suitably arranged to both receive the resource access request and to generate a corresponding universal command;

a universal command sequencer coupled to the configurable system interface;

a resource tag buffer coupled to the command sequencer arranged to store a resource tag arranged to identify the current state of the requested resource and a resource tag arranged to identify the requested state of the requested resource; and

a characteristic operating parameter buffer coupled to the command sequencer arranged to store the characteristic operating parameter associated with the requested resource,

wherein the universal command sequencer uses the respective resource tags that identify the current state and the requested state of the requested resource and the characteristic operating

> parameter associated with the requested resource to generate the sequenced universal command.

Id. at col. 27 l. 41–col. 28 l. 6 (emphasis added to disputed limitation). As described in claim 2, the "current state" and the "requested state" resource tags are stored in a "resource tag buffer," the disputed term on appeal.

Apart from the claims themselves, the description of the "resource tag buffer" in the specification is light. The specification mentions "resource tag buffer" or "tag buffer" only six times and illustrates that buffer in only two figures (one being Figure 1B, above). *Id.* at col. 7 l. 31, col. 7 ll. 50–51, col. 7 l. 56, col. 7 l. 59, col. 8 l. 67, col. 10 l. 43, Figs. 1B & 1D. These portions of the specification are not illuminating as to the structure of this buffer. Instead, they describe the buffer functionally as storing certain resource tags. And the two figures merely depict the "resource tags 114" as a rectangular box, with no further detail.

II

These appeals involve two IPR proceedings that were remanded by our court in light of our decision in *Arthrex, Inc. v. Smith & Nephew, Inc.*, 941 F.3d 1320 (Fed. Cir. 2019) (*Arthrex I*) due to Appointments Clause issues. While the IPR was on remand, the Supreme Court vacated our decisions vacating the Board's final written decisions based on its decision in *United States v. Arthrex, Inc.*, 141 S. Ct. 1970 (2021) (*Arthrex II*). This vacated vacatur thus reinstated the Board's final written decisions and led to a dispute regarding a joint motion to terminate that was filed during remand, as explained below.

In May 2016, Polaris filed a complaint accusing NVIDIA of infringing certain claims of the '505 and '993 patents, among others. NVIDIA responded by filing IPR petitions challenging certain claims in those patents. NVIDIA filed its petition against the '993 patent on

February 14, 2017, and the Board issued its final written decision on December 19, 2018, holding all challenged claims unpatentable. *NVIDIA Corp. v. Polaris Innovations Ltd.*, No. IPR2017-00901, 2018 WL 6720618 (P.T.A.B. Dec. 19, 2018) (*'993 Decision*). NVIDIA filed its petition against the '505 patent on May 30, 2017, and the Board issued its final written decision on December 4, 2018, holding all challenged claims unpatentable. *NVIDIA Corp. v. Polaris Innovations Ltd.*, No. IPR2017-01500, 2018 WL 6380663 (P.T.A.B. Dec. 4, 2018) (*'505 Decision*).

Polaris appealed both decisions. Polaris and NVIDIA then settled, and thus NVIDIA withdrew from these appeals. The PTO intervened in the appeals to defend the Board's decisions. On March 20, 2020, the cases were calendared for argument on May 8, 2020. Three days later, our court declined to rehear *Arthrex I* en banc.[1] Accordingly, we vacated the Board's decisions and remanded, granting the remedy required by us in *Arthrex I*. 19-1484 ECF No. 65; 19-1483 ECF No. 68.

On remand, the Board administratively suspended the IPRs (along with many others) pending potential Supreme Court action in *Arthrex I*. During that administrative suspension, on June 10, 2020, Polaris and NVIDIA filed a joint motion to terminate the proceedings. 19-1484 SAppx. 7–15 (joint motion to terminate); 19-1483 SAppx. 7–15 (same).[2]

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[1] The panel decision on *Arthrex I* issued on October 31, 2019, well before argument was scheduled, but the court did not decline to rehear the case en banc until March 23, 2020, three days after oral argument was scheduled in this case.

[2] 19-1483 SAppx. citations herein refer to the appendix filed concurrently with Appellant's Motion to Vacate Final Decision. 19-1483 ECF No. 90.

While those motions were pending at the Board, the Supreme Court vacated our decision in *Arthrex I*, substituting an alternative remedy for violation of the Appointments Clause. *Arthrex II*, 141 S. Ct. at 1987–88. In view of its decision in *Arthrex II*, the Supreme Court vacated our vacatur of the Board's final written decisions in these Polaris appeals, thus reinstating the Board's final written decisions. 19-1484 SAppx. 26; 19-1483 SAppx. 25. On remand, we reinstated the appeals and asked Polaris to explain "how it believes its case should proceed in light of *Arthrex* [*II*]." 19-1484 ECF No. 73; 19-1483 ECF No. 72. Polaris argued that we should vacate and remand for the Board to grant termination. The PTO opposed and suggested limited remand for Director review was appropriate. We remanded "for the limited purpose of allowing the parties to seek further action by the Director." 19-1484 ECF No. 84; 19-1483 ECF No. 76.

On remand, Polaris asked the Board for guidance regarding how the remand should proceed. Polaris advocated that the Board should grant Polaris's then-still-pending motion to terminate. 19-1484 SAppx. 25–26; 19-1483 SAppx. 24–25.

Chief Administrative Judge Boalick responded on behalf of the Board on October 29, 2019, in an "Order" specifying the appropriate process on remand. 19-1484 SAppx. 25–27; 19-1483 SAppx. 24–26. The Board determined that termination was not appropriate because, due to the Supreme Court's decision, the "final written decision in each of these cases is not vacated, and it is not necessary for the Board to issue a new final written decision in either of these cases." 19-1484 SAppx. 27; 19-1483 SAppx. 26. Instead of termination, the Board determined "the appropriate course of action on remand . . . [wa]s to authorize [Polaris] to request Director review." 19-1484 SAppx. 27; 19-1483 SAppx. 26. This order effectively denied the joint motions to terminate.

Polaris filed its requests for Director rehearing. Mr. Hirshfeld, performing the functions and duties of the Director, denied rehearing. Polaris then filed notices with our court notifying us of the Director's denial of rehearing.

In the 19-1484 appeal, Polaris filed an amended notice of appeal indicating it was challenging the denial of the motion to terminate. We ordered supplemental briefing on this issue. The parties complied.

In the 19-1483 appeal, on March 23, 2022, Polaris filed a motion for this court to vacate the Board's final written decision and remand for termination. This motion is substantively the same as Polaris's supplemental briefing in the 19-1484 appeal. The PTO responded to the motion in April 2022, and Polaris replied in May 2022.

We have jurisdiction under 28 U.S.C. § 1295(a)(4)(A).

DISCUSSION

Polaris raises three principal arguments on appeal. First, it argues that the Board erred by failing to grant the joint motions to terminate filed in both proceedings before the Board on remand. Second, it argues that the Board misconstrued the term "memory chip" in the IPR involving the '993 patent. Third, it argues the Board misconstrued the term "resource tag buffer" in the IPR involving the '505 patent. We affirm.

The motion-to-terminate issue ultimately turns on interpretation of 35 U.S.C § 317—which governs settlement of IPRs at the Board—and is therefore a question of law that we review de novo. *VirnetX Inc. v. Apple Inc.*, 931 F.3d 1363, 1369 (Fed. Cir. 2019). We also "set aside actions of the Board that are arbitrary, capricious, an abuse of discretion, or otherwise not in accordance with law." *In re Sullivan*, 362 F.3d 1324, 1326, 1328 (Fed. Cir. 2004); 5 U.S.C. § 706(2)(A).

The Board's ultimate claim constructions and any underlying determinations based on intrinsic evidence likewise present a question of law that we review de novo. *Personalized Media Commc'ns, LLC v. Apple Inc.*, 952 F.3d 1336, 1339 (Fed. Cir. 2020). We review for substantial evidence any subsidiary factual findings involving extrinsic evidence. *Id.*

The broadest reasonable interpretation claim construction standard applies in this IPR proceeding.[3] Thus, the Board's interpretation must be reasonable in light of the specification, prosecution history, and the understanding of one skilled in the art. *See Microsoft Corp. v. Proxyconn, Inc.*, 789 F.3d 1292, 1298 (Fed. Cir. 2015), *overruled on other grounds by Aqua Prods., Inc. v. Matal*, 872 F.3d 1290 (Fed. Cir. 2017) (en banc). The broadest reasonable interpretation must also take into account "the context of the entire patent." *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1374 (Fed. Cir. 2019) (quoting *Phillips*, 415 F.3d at 1312–13); *see also In re Translogic Tech., Inc.*, 504 F.3d 1249, 1256–58 (Fed. Cir. 2007) (applying *Phillips* "best practices" to claim construction under broadest reasonable interpretation standard).

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[3] Per regulation, the Board applies the *Phillips* claim construction standard to IPR petitions filed on or after November 13, 2018. See Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340 (Oct. 11, 2018) (codified at 37 C.F.R. § 42.100(b)); *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005). Because NVIDIA filed the petitions before November 13, 2018, the broadest reasonable interpretation standard applies to the IPR decisions on appeal.

I

We first address Polaris's argument that the Board erred in denying its motion to terminate. As explained in detail below, because the Board decided the merits of the IPR before Polaris filed its motion to terminate, Polaris's motion was untimely. Furthermore, the Board properly exercised its discretion to terminate or continue the IPR proceeding. We thus affirm.[4]

Section 317 of Title 35 governs settlement of IPRs at the Board. Section 317(a) is reproduced in full below:

> An inter partes review instituted under this chapter *shall be* terminated *with respect to any petitioner* upon the joint request of the petitioner and the patent owner, *unless the Office has decided the merits* of the proceeding before the request for termination is filed. If the inter partes review is terminated with respect to a petitioner under this section, no estoppel under section 315(e) shall attach to the petitioner, or to the real party in interest or privy of the petitioner, on the basis of that petitioner's institution of that inter partes review. If no petitioner remains in the inter partes review, the Office *may* terminate the review or proceed to a final written decision under section 318(a).

Id. (emphases added). Section 317(a) includes a mandate with a time limit ("shall be terminated") and a separate discretionary authority ("may terminate the review or proceed"). It specifies that the proceeding "shall be terminated with respect to any petitioner" upon joint request of the parties. *Id.* This termination of a petitioner is only

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[4] In the 19-1483 appeal, Polaris filed a motion to vacate the Board's final written decision. 19-1483 ECF No. 89. We deny that motion for the same reasons discussed herein with respect to the 19-1484 appeal.

mandatory so long as the request for termination is filed before "the Office has decided the merits of the proceeding." *Id.* The termination of petitioners notwithstanding, the statute grants discretion to the Board to "proceed to a final written decision under section 318(a)" even if "no petitioner remains" in the proceeding. *Id.*; *see also, e.g.*, *Aqua Prods.*, 872 F.3d at 1311 ("The final sentence of § 317(a) gives the Board the option to proceed to final judgment in any proceeding where the original petitioners choose not to continue their challenge."); *Regents of the Univ. of Minn. v. LSI Corp.*, 926 F.3d 1327, 1336 (Fed. Cir. 2019) ("The statutory provision [§ 317(a)] states that if the petitioner stops participating, the Board may continue on to a final written decision.").

On appeal, Polaris argues that it was entitled to termination of both IPR proceedings because it timely filed its joint motions to terminate. 19-1484 Appellant's Suppl. Br. 11–17. We disagree for two independent reasons. First, the statute provides no mandatory right to termination of the *proceeding*; at best, the statute provides for mandatory termination with respect to a *petitioner*, not termination of the proceeding itself. As regards termination of the proceeding, § 317(a) states that the Board "*may* terminate the review" if, as is the case here, no petitioner remains in the proceeding. Thus, the plain language of the statute gives the Board discretion to carry on to a final written decision—even without any petitioner.

Second, the Board correctly identified Polaris's motion as untimely. The Board issued its final written decisions in these cases in December 2018. Polaris filed its joint motions to terminate more than a year later, in June 2020. Thus, the Board had already "decided the merits" at the time Polaris filed its motion. Chief Administrative Judge Boalick recognized the timing issue in his order on remand,

which effectively denied the motions to terminate.[5] There, he explained that the "Board's final written decision in each of these cases is not vacated, and it is not necessary for the Board to issue a new final written decision in either of these cases." 19-1484 SAppx. 27; 19-1483 SAppx. 26. Accordingly, the Board determined that the proper course was not to terminate the proceedings, as Polaris urged, but instead to allow Polaris to seek Director review. *Id.*

Although the final written decisions had been vacated for a time period after our decision in *Arthrex I*, that vacatur itself was vacated by the Supreme Court. This explains why Chief Administrative Judge Boalick's order noted that the decisions were not vacated at the time the Board was considering the motions to terminate. We thus affirm the Board's decision not to terminate the proceedings under § 317(a) because the motions to terminate were untimely.

Polaris also argues that the Board's decision not to terminate was arbitrary because the Board terminated other proceedings with similar *Arthrex* remands, noting that the motions to terminate in those other proceedings were filed around the same time Polaris filed its motions. 19-1484 Appellant's Suppl. Br. 17–24 (citing *Samsung Elecs. Am., Inc. v. Uniloc 2017, LLC*, No. IPR2017-01797, Paper 39 (P.T.A.B. July 21, 2020); *Fidelity Info. Servs., LLC v. Mirror Imaging, LLC*, No. CBM2017-00061, Paper 70 (P.T.A.B. July 21, 2020); *Samsung Elecs. Co. v. Image Processing Techs. LLC*, No. IPR2017-00353, Paper 45 (P.T.A.B. Sept. 9, 2020)). Polaris argues that the disparate treatment it received was impermissible under the Administrative Procedure Act's requirement for reviewing courts to set aside agency action that is "arbitrary, capricious, an

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[5] At oral argument, Polaris agreed this order was an "effective denial" of its motion to terminate. 19-1484 Oral Arg. at 3:57–4:50, https://oralarguments.cafc.uscourts.gov/default.aspx?fl=19-1484_08012022.mp3.

abuse of discretion, or otherwise not in accordance with law." 19-1484 Appellant's Suppl. Br. 9 (quoting 5 U.S.C. § 706(2)(A)).

The Board's decision denying termination was not arbitrary and instead rested on a significant difference between those cases and Polaris's. In those cases, the Board considered the motion and terminated the proceedings while the final written decisions stood vacated by our court after the mandate issued in *Arthrex I*. Here, our vacatur pursuant to *Arthrex I* had already been vacated by the Supreme Court at the time the Board was evaluating Polaris's motions.

At its core, Polaris's complaint is not that the cases are indistinguishable, but instead that the Board took too long to act in its case. *See, e.g.*, 19-1484 Appellant's Supp. Br. 14–15 (arguing "the Board should have granted the [motion to terminate] promptly after it was filed" and "the fact that the Board sat on the [motion to terminate] for over a year should not be held against Polaris"). Polaris, however, points to no authority mandating that the Board act on its request within any particular time frame.[6] The disparity in timing—the Board taking longer to act on Polaris's motions than Polaris thinks it should have—is not the sort of arbitrariness in decision-making that § 706(2)(A)'s "arbitrary [and] capricious" standard was designed to protect against. Even if the disparate result could be viewed as "arbitrary," in the broader sense of the word, based on

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[6] For the first time at oral argument, Polaris contended that the Board should have acted on its motion earlier pursuant to 5 U.S.C. § 706(1), which permits a reviewing court to "compel agency action unlawfully withheld or unreasonably delayed." *See* 19-1484 Oral Arg. at 7:51–8:34. This argument was not included in its briefs and is therefore waived. *See ABS Glob., Inc. v. Cytonome/ST, LLC*, 984 F.3d 1017, 1027 (Fed. Cir. 2021).

the timing of the Supreme Court's action in this case while Polaris's motion was still pending, the denial was not the product of arbitrary decision-making by the agency. In addition, we simply cannot agree that the Board's decisions to continue these IPRs were arbitrary when the last sentence of § 317(a) gives the Board discretion to either "terminate the review or proceed to a final written decision."

In sum, the Board had already decided the merits of the cases in final written decisions that were not vacated at the time the Board made its decision denying Polaris's motions to terminate. This determination was not arbitrary. We thus affirm the Board's decision that termination was inappropriate.

II

Next, we turn to Polaris's argument that the Board misconstrued the claim terms "memory chips" and "semiconductor memory component" within the claim phrase "wherein the semiconductor memory component comprises a plurality of memory chips" in claim 2 of the '993 patent. We disagree.

Polaris makes these claim construction arguments to avoid the asserted prior art. In its IPR petition, NVIDIA presented prior art that included multiple, separately packaged integrated circuit dies (such as that illustrated below) that NVIDIA argued collectively constituted a "semiconductor memory component" that "comprises a plurality of memory chips" as required by claim 2. '993 patent col. 11 ll. 39–40; *see, e.g.*, 19-1484 J.A. 178–79, 208.

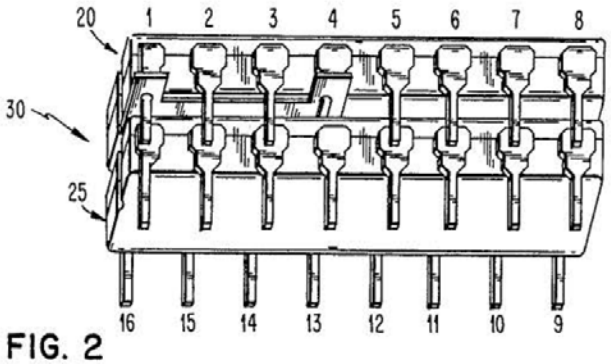


FIG. 2

See, e.g., 19-1484 J.A. 1498. The Board agreed that this disclosure taught the claimed "semiconductor memory component" comprising "a plurality of memory chips." *'993 Decision*, 2018 WL 6720618, at *17.

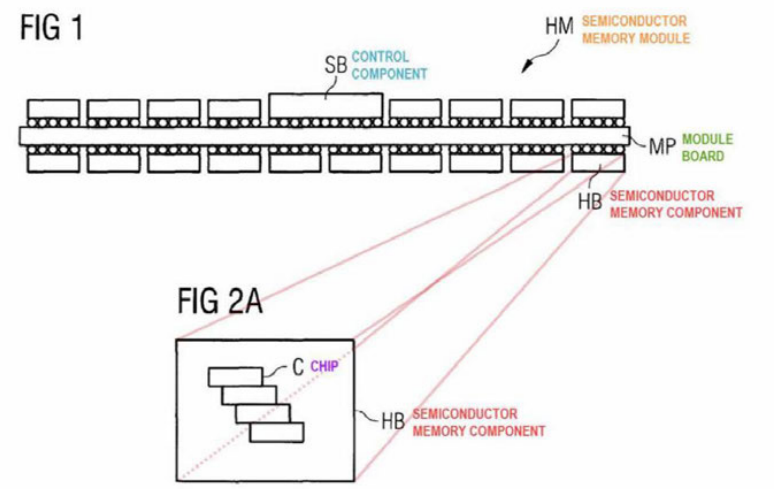
On appeal, Polaris argues (as it did before the Board) that the proper construction of "memory chips" and "semiconductor memory component" excludes the above arrangement (that is, multiple, separately packaged integrated circuit dies) and only contemplates multiple unpackaged dies within a single package. *See, e.g.*, 19-1484 Appellant's Br. 8 (arguing "NVIDIA could only find single-die-in-a-package prior art"); *id.* at 24 (arguing that "the '993 Patent always uses the term 'semiconductor memory component' or just 'memory component' to refer to a packaged device, and always uses the term 'memory chip' to refer to an IC memory die packaged within a component"); *id.* at 56–57. The Board disagreed with Polaris, refusing to limit the broad claim language "memory chips"—which ordinarily encompasses either packaged integrated circuits or unpackaged dies—to a particular embodiment in the specification. *'993 Decision*, 2018 WL 6720618, at *6 (citing *Thorner v. Sony Comput. Ent. Am. LLC*, 669 F.3d 1362, 1366 (Fed. Cir. 2012) ("It is not enough for a patentee to simply disclose a single embodiment or use a word in the same manner in all embodiments[;] the patentee must 'clearly express an intent' to redefine the term.")). Because Polaris points to no persuasive evidence supporting its

proposed claim constructions, we adopt the Board's constructions and affirm its unpatentability determination.

Polaris conceded before the Board (as it should have) that the term "memory chip" would have been understood by a person of ordinary skill as either a packaged integrated circuit or an unpackaged integrated circuit die. 19-1484 J.A. 383 (Patent Owner's Response) (quoting 19-1484 J.A. 1525–26 (Przybylski Decl. ¶ 48)). Thus, as the Board correctly recognized, Polaris must find support in the intrinsic record to limit the broad claim language only to the latter option. *See Thorner*, 669 F.3d at 1365 (explaining that there "are only two exceptions" to the general rule that terms are given their "ordinary and customary meaning as understood by a person of ordinary skill in the art when read in the context of the specification and prosecution history"—lexicography and disavowal). Our examination of the intrinsic record establishes that Polaris has not done so.

First, the plain claim language does not support Polaris's interpretation. Claim 2 simply recites that the "semiconductor memory component comprises a plurality of memory chips." '993 patent col. 11 ll. 39–40. The claim makes no mention of particular packaging required (or forbidden) and does not use the term "die."

The specification likewise does not equate the term "die" with a memory chip or describe the memory chip in terms of its packaging (or lack thereof). Polaris points to very little in the specification to support its narrow construction. It relies exclusively on Figures 1 and 2A, and their corresponding descriptions in the specification, which it describes as "the only relevant disclosure," 19-1484 Appellant's Br. 38:



Id. (annotating '993 patent, Figs. 1 & 2A).

Finally, the prosecution history does not support Polaris's construction. As the Board noted—and Polaris does not contest on appeal—the first office action was a notice of allowability. *'993 Decision*, 2018 WL 6720618, at *5. Thus, there was no amendment nor argument to support Polaris's narrow construction.

On appeal, Polaris makes several arguments. None are persuasive.

First, Polaris argues that "memory chip" means "*either* an [integrated circuit] die or a packaged [integrated circuit] . . . *not both*." 19-1484 Appellant's Br. 27. But the Board did not conclude that "memory chip" must be "both" a packaged and an unpackaged die; it simply concluded, based on Polaris's concession, that the term "memory chip" broadly encompasses either. In Polaris's own words: "In general, the term 'chip' can 'refer to either a packaged integrated circuit or a single die.'" 19-1484 J.A. 383 (Patent Owner's Response) (quoting J.A. 1525 (Przybylski Decl. ¶ 48)); *'993 Decision*, 2018 WL 6720618, at *4–5, *7 (Board repeatedly relying on this admission). Polaris argues that the '993 patent makes "clear" that the term "chip" is limited to single dies. 19-1484 Appellant's Br. 37–39. But Polaris's

argument rests on importing that limitation from an embodiment in the figures, which is improper. *See Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004) ("[I]t is improper to read limitations from a preferred embodiment described in the specification—even if it is the only embodiment—into the claims absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited.").

Second, Polaris argues the Board violated the principle of claim differentiation because the Board's construction eliminates the difference between claim 1, which allows single-chip or multiple-chip semiconductor memory components, and claim 2, which requires a plurality of chips. 19-1484 Appellant's Br. 28–29. But the distinction between the claims regarding number of chips in a semiconductor memory component remains whether or not the chips are individually packaged. Thus, the Board did not violate the principle of claim differentiation.

We have considered Polaris's remaining arguments in support of its construction and find them unpersuasive. Accordingly, we agree with the Board's construction of "memory chips" which encompasses either packaged or unpackaged dies. Because we decide that the term "memory chips" includes packaged dies, we reject Polaris's additional argument that the '933 patent "always uses the term 'semiconductor memory component' . . . to refer to a packaged device" to the extent that it would collaterally limit the term "memory chip" to an unpackaged die. *See, e.g.*, 19-1484 Appellant's Br. 24. We agree with the Board that Polaris has not identified "anything in the specification or prosecution history" limiting "semiconductor memory component" to a packaged device rather than its full scope in claim 2, which "includes one or more memory chips" that each may be unpackaged or packaged die. *See '993 Decision*, 2018 WL 6720618, at *5–7.

Polaris does not dispute that the prior art discloses all claim limitations under the Board's claim constructions. Accordingly, we affirm the Board's unpatentability determination as to the '993 patent.

III

Next, we consider Polaris's argument that the Board misconstrued the claim term "resource tag buffer" in claim 2 of the '505 patent. At its core, Polaris's argument challenges the Board's application of its expert's definition of "single buffer" to the prior art, not the Board's claim construction itself (which adopted the expert's definition). Accordingly, we also discuss the Board's application of the term in evaluating the prior art.

A

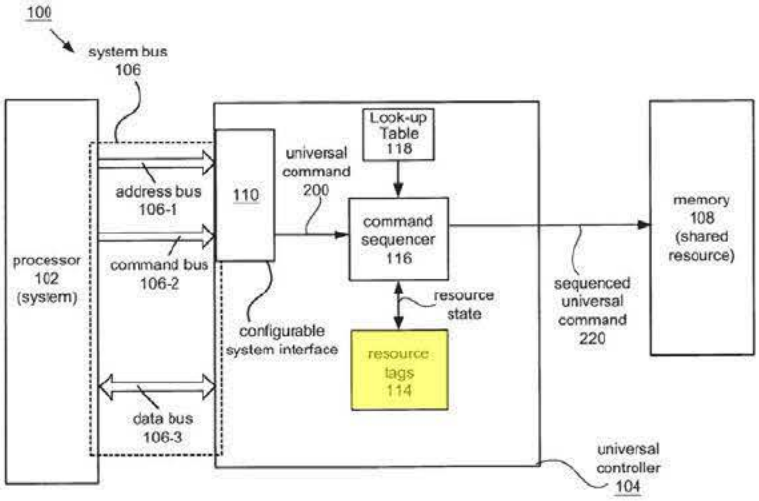
On appeal, Polaris contends that "[t]he Board erroneously interpreted ['resource tag buffer'] to encompass any storage that collectively stores A and B, even if not in the same buffer." 19-1483 Appellant's Br. 39–40; *see also id.* at 36 (arguing the term does not allow "a *set of buffers* that collectively store" the resource tags (emphasis added)), 56 (arguing the "specification does not disclose *two separate buffers* storing [the required] resource tags, like the prior art in this case" (emphasis added)). In other words, Polaris argues the Board erroneously construed the term "resource tag buffer" to include multiple buffers, not just a single buffer.

But this is not what the Board did. The Board found that the prior art disclosed storing the resource tags in a "single buffer" as that term was defined by Polaris's expert. Thus, the bulk of Polaris's argument on appeal—contending that the Board erroneously construed "resource tag buffer" to cover multiple buffers—is founded on a faulty premise. *See, e.g.*, 19-1483 Appellant's Br. 53–56 (emphasizing a supposed "single-buffer structure" illustrated in Figures 1B and 1D).

In analyzing the prior art, the Board applied the "single buffer" definition proffered by Polaris's expert. Polaris's expert, Dr. Steven Przybylski, testified that a single buffer "must be logically or physically a single entity." *'505 Decision*, 2018 WL 6380663, at *6 (quoting 19-1483 J.A. 1222–23 (Przybylski Decl. ¶38)). Dr. Przybylski explained that "[l]ogical unity involves storing one or more values of the same type, typically with a common input and common output." 19-1483 J.A. 1223 (Przybylski Decl. ¶ 38). He noted that values stored in a buffer are "of the same type" if they have "a commonality of purpose or usage." *Id.*

We see no error in the Board's adoption of this construction, which is supported by and consistent with the specification. As the Board noted, the specification mentions the phrases "resource tag buffer 114" or "tag buffer 114" only six times and illustrates it in only two figures. *'505 Decision*, 2018 WL 6380663, at *4 (citing '505 patent col. 7 l. 31, col. 7 ll. 50–51, col. 7 l. 56, col. 7 l. 59, col. 8 l. 67, col. 10 l. 43, Figs. 1B & 1D). The Board correctly observed that none of these passages discloses a particular structure for the buffer. Instead, these passages describe the buffer functionally based on the type of data stored—resource tags. *See, e.g.*, '505 patent col. 7 ll. 30–37 (describing that "command sequencer 116" creates a "sequenced command 220" "[u]sing the resource state information provided by the tags 300 stored in a resource tag buffer 114").

As for the figures, the Board correctly noted they "do not provide any additional insight on the structure of a resource tag buffer." *'505 Decision*, 2018 WL 6380663, at *4. Instead, they merely illustrate a box in a high-level diagram:



'505 patent, Fig. 1B (annotation added).

Before the Board, Polaris argued that the figures showed the tags must be stored in "one place" because the figures depict a single box. 19-1483 J.A. 443 (Patent Owner's Response). But the Board correctly noted that, to the extent this required the "buffer" to be a single, physical unit, this was contradicted by the specification, Polaris's expert's declaration, and Polaris's statements at oral argument. In particular, the Board relied on the following passage in the specification, which discloses that resource tags "may be located in disparate locations":

> [I]n order to track a state of the physical pages in the shared memory 108 having a number of memory banks, for example, a large number of resource tags which would require a large amount of cache memory dedicated to the resource tag buffer 114 are needed. This would slow the performance of the universal controller 104 since it would require substantial amounts of time to retrieve particular resource tags for particular pages of memory each of which may be located in disparate locations.

'505 patent col. 10 ll. 39–47.[7] The Board also relied on Polaris's concession at oral argument that the resource tag buffer "need not be a contiguous unit." *'505 Decision*, 2018 WL 6380663, at *5 (quoting 19-1483 J.A. 603 (Hr'g Tr. 32:4–11)). Rather, as Polaris and its expert explained, the buffer "must, either logically *or physically*[,] be a unit." *Id.* (quoting 19-1483 J.A. 603 (Hr'g Tr. 32:13–17) (emphasis added)).

We conclude that the Board correctly adopted Polaris's expert's definition of "single buffer" as the broadest reasonable interpretation consistent with the specification. We have considered Polaris's other arguments challenging the Board's claim construction and find them unpersuasive. Accordingly, we adopt the Board's construction of "resource tag buffer."

B

Next, we turn to the Board's finding that both Chauvel[8] and Hughes[9] disclose a resource tag buffer as properly construed. *'505 Decision*, 2018 WL 6380663, at *11–13, *24–26. We review the Board's findings regarding the scope and content of the prior art for substantial evidence. *Amazon.com, Inc. v. Barnesandnoble.com, Inc.*, 239 F.3d 1343, 1358 (Fed. Cir. 2001) ("[W]hat a reference teaches is a

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[7] Polaris argues that the Board misconstrued this passage. Polaris contends that the "disparate locations" describes the "pages of memory" rather than the "resource tags" for those pages. 19-1483 Appellant's Reply Br. 12–13. But that interpretation makes no sense in the context of the entire passage, which is focused on the resource tags—that they may "require a large amount of cache memory" and may be slow to retrieve because they "may be located in disparate locations." '505 patent col. 10 ll. 39–47.

[8] U.S. Patent No. 6,253,297.

[9] U.S. Patent No. 5,784,582.

question of fact."); *Fleming v. Cirrus Design Corp.*, 28 F.4th 1214, 1221 (Fed. Cir. 2022) ("We review the Board's . . . factual findings for substantial evidence.").

The Board found that each of Chauvel and Hughes discloses storing the current state of a shared resource and the requested state of a shared resource and comparing those values. *'505 Decision*, 2018 WL 6380663, at *12–13, *24–26. The Board found that the current state and the requested state are values "of the same type" such that, under Dr. Przybylski's definition of a "single buffer," Chauvel and Hughes disclose a logical single buffer even if storage is physically separate. *Id.* at *12 ("Although Chauvel depicts the identified storage areas in different parts of the traffic controller 18, we find that they comprise 'a resource tag buffer' as claimed," and finding that "Chauvel describes such 'logical unity'" under Dr. Przybylski's definition), *12–13 (describing the comparison of the values), *24 ("Although Figure 3 of Hughes depicts the identified storage areas separately in arbiter/controller logic 72, we find that they comprise 'a resource tag buffer' as claimed."), *25 ("Hughes describes such 'logical unity'" under Dr. Przybylski's definition), *25–26 (describing the comparison of the values).

These findings are supported by substantial evidence. The Board reasonably relied on the references' disclosure of comparing the current state and requested state values to determine they are of the same type. In addition, the Board reasonably found that Hughes and Chauvel disclose a "single buffer" based on the "logical unity" definition supplied by Polaris's expert.

On appeal, Polaris distills its argument as follows: "The resolution of this case is a[s] simple as comparing the pertinent block diagrams of the '505 Patent (Figures 1B and 1D), on the one hand, and Chauvel and Hughes, on the other hand. . . . [T]he '505 Patent has one block where Chauvel and Hughes have multiple blocks." 19-1483

Appellant's Reply Br. 8. The problem with this argument is that it is not responsive to the Board's application of Polaris's expert's definition of a "single buffer" based on "logical unity." According to Dr. Przybylski, one must consider whether the locations "stor[e] one or more values of the same type" and have "a commonality of purpose or usage." 19-1483 J.A. 1223 (Przybylski Decl. ¶ 38). That is precisely the inquiry that the Board undertook here. Thus, we reject Polaris's argument on appeal that the blocks illustrated in the figures of the prior art are dispositive.

Polaris also faults the Board for focusing on its expert's definition of logical unity rather than focusing on the rest of his explanation as to why the prior art does not show a single buffer. 19-1483 Appellant's Br. 68–69 (citing 19-1483 J.A. 1239–43 (Przybylski Decl. ¶¶ 67–73)), 72–73 (citing 19-1483 J.A. 1244–45 (Przybylski Decl. ¶ 76)). The portions of Dr. Przybylski's testimony identified by Polaris, however, largely rely on physical distinctness of structures, and thus are irrelevant to the "logical unity" definition applied by the Board. *See, e.g.*, 19-1483 J.A. 1241–42 (Przybylski Decl. ¶ 70) ("Chauvel acknowledges that the memory controller 18a can be on a totally separate integrated circuit"). Furthermore, those portions of the expert's report merely speculate, without support, that the information is stored in a "unique format" or the information is "probably in different formats." 19-1483 J.A. 1239–40 (Przybylski Decl. ¶ 69), 1244–45 (Przybylski Decl. ¶ 76). This unsupported speculation is insufficient to overcome the Board's contrary finding based on the references themselves.

Because substantial evidence supports the Board's finding that the prior art discloses a "resource tag buffer," we affirm.

CONCLUSION

For the reasons above, we affirm the Board's denial of Polaris's motions to terminate and its unpatentability determinations regarding the '505 and '993 patents.[10]

AFFIRMED

[10] Polaris also argues that we should disregard the Office's responses on the merits in these appeals because the Office lacks Article III standing to defend the Board's decisions as an appellee. 19-1483 Reply Br. 1–3; 19-1484 Reply Br. 1–3. Polaris's supplemental briefing regarding its joint motion to terminate, however, admits that our precedent "forecloses this argument." 19-1484 Suppl. Reply Br. 8 (citing *Knowles Elecs. LLC v. Iancu*, 886 F.3d 1369, 1372 n.2 (Fed. Cir. 2018)).