NOTE: This disposition is nonprecedential.

United States Court of Appeals for the Federal Circuit

MICRON TECHNOLOGY, INC.,
Appellant

v.

NORTH STAR INNOVATIONS, INC.,
Cross-Appellant

2020-1303, 2020-1402

Appeals from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2018-00989.

Decided: May 4, 2021

MELANIE L. BOSTWICK, Orrick, Herrington & Sutcliffe LLP, Washington, DC, argued for appellant. Also represented by JARED BOBROW, JEREMY JASON LANG, Menlo Park, CA.

EDWARD C. FLYNN, Eckert Seamans Cherin & Mellott, LLC, Pittsburgh, PA, argued for cross-appellant. Also represented by PHILIP LEVY, NATHANIEL COEN WILKS.

Before NEWMAN, LINN, and CHEN, *Circuit Judges*.

CHEN, *Circuit Judge*.

The Patent Trial and Appeal Board (Board) issued a final written decision in an *inter partes* review (IPR) proceeding regarding the patentability, *vel non*, of claims 1–12, 14–16, and 20–23 of U.S. Patent No. 5,943,274 ('274 patent), owned by North Star Innovations, Inc. (North Star). Micron Technology, Inc. (Micron), the petitioner in the proceeding, appeals the Board's findings that dependent claims 2 and 10 are not unpatentable as anticipated. North Star cross-appeals, contending that the Board erred in finding independent claims 1 and 21 unpatentable as anticipated. For the reasons that follow, we *affirm* the Board's decision as to the challenged grounds in both the appeal and cross-appeal.

BACKGROUND

This case concerns integrated circuit memory chips. Specifically, the memory chips at issue here lie at the section of the memory known as the "output stage," which sits between the data storage cell arrays, that is, the cells that store values in the memory, and the input/output pins that communicate with components outside of the memory. These output stage memory circuits are comprised of a differential amplifier sub-circuit, a level-converter sub-circuit, and a latch sub-circuit, among other circuit components.

A brief background on each of these sub-circuits is warranted. A differential amplifier circuit detects and amplifies a small input voltage difference. '274 patent col. 1 ll. 25–28. Similarly, level converters also perform amplification, converting a small signal input to a higher voltage level output. *Id.* at col. 5 ll. 66–67. Latch circuits are used to store a data signal. *Id.* at col. 1 l. 30. In this type of output stage memory circuit, the latch stores the output signal of the differential amplifier before it is output to the

data input/output pad, such that the output is held at a consistent binary 0 or 1 value instead of fluctuating or toggling between 0 or 1 while the differential amplifier detects the next voltage output value. *Id.* at col. 1. ll. 29–33.

The '274 patent, entitled, "Method and Apparatus for Amplifying a Signal to Produce a Latched Digital Signal," relates "in general to a method and apparatus for amplifying a signal to produce a latched digital signal, and more particularly to an output stage of a memory." *Id.* at col. 1 ll. 6–8. The '274 patent explains that prior art output stage memory circuits utilized two clock signals (circuit timing signals) to operate the circuit: one clock signal for the differential amplifier sub-circuit and one clock signal for the latch sub-circuit. *Id.* at col. 1 ll. 37.

This dual-clock approach, according to the patent, has its drawbacks—"the timing relationship between the two clocks cannot be consistently controlled due to manufacturing process variations, temperature variations, power supply voltage variations, etc." causing the two clocks to provide slightly different timing signals to the sub-circuits. *Id.* at col. 1 ll. 37–40. The '274 patent also explains that precise circuit timing is advantageous. *Id.* at col. 1 ll. 40–45. To solve these problems, the patented output stage memory circuit employs a "clock-free latch circuit," *id.* at col. 2 l. 55, meaning that the latch operates without a clock signal and thus the circuit needs only one clock signal overall, *id.* at col. 5 ll. 25–26.

Claims 1, 2, 10, and 21 of the '274 patent are at issue in this appeal. They recite as follows:

> 1. An apparatus for use as an output stage of a memory device, the apparatus comprising:
>
> a timing circuit;
>
> a differential amplifier responsive to the timing circuit;

> an impedance control circuit;
>
> a level converter responsive to the differential amplifier and the impedance control circuit; and
>
> a clock-free latch responsive to the level converter.
>
> 2. The apparatus of claim 1, wherein the timing circuit is a clock delay circuit.
>
> 10. The apparatus of claim 1, wherein the differential amplifier has an output driven by at least one of an emitter and a source of a transistor.
>
> 21. A memory device comprising:
>
> bit cell array;
>
> an amplifier module responsive to the bit cell array; and
>
> an output stage responsive to the amplifier module, the output stage comprising:
>
> a differential amplifier responsive to a clock signal;
>
> a high impedance control circuit;
>
> a level converter responsive to the differential amplifier and responsive to the high impedance control circuit; and
>
> a clock-free latch responsive to the level converter.

'274 patent at claims 1, 2, 10, and 21.

Micron petitioned for *inter partes* review of the '274 patent on multiple grounds, including that claims 1–3, 8–12, 14–16, 20, and 21 are anticipated by Tachibana[1] under 35

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[1] Japanese Patent Application Publication No. H4-170816 to Tachibana et al., titled "Semiconductor Integrated Circuit," and published June 18, 1992.

U.S.C. § 102(b).[2] The Board agreed with Micron that all the challenged claims were unpatentable, except for dependent claims 2 and 10, which it found were not anticipated by Tachibana. *See Micron Tech., Inc. v. North Star Innovations, Inc.*, No. IPR2018-00989, 2019 WL 5423610, at *41 (P.T.A.B. Oct. 22, 2019) (Final Written Decision). Regarding claim 2, the Board concluded that "Tachibana's timing circuit does not correspond to claim 2's 'clock delay circuit.'" *Id.* at *21. For claim 10, the Board determined that Tachibana did not disclose a differential amplifier with "an output driven by at least one of an emitter and a source of a transistor," and thus, claim 10 was not shown to be anticipated. *Id.* at *23–25.

Micron appeals the Board's findings on claims 2 and 10. North Star cross-appeals the Board's findings on claims 1 and 21. We have jurisdiction pursuant to 28 U.S.C. § 1295(a)(4)(A) and 35 U.S.C. § 141(c).

DISCUSSION

Anticipation is a question of fact that we review for substantial evidence. *In re Rambus, Inc.*, 753 F.3d 1253, 1256 (Fed. Cir. 2014). A prior art document anticipates a claim if it describes every element of the claimed invention, either expressly or inherently. *Husky Injection Molding Sys. Ltd. v. Athena Automation Ltd.*, 838 F.3d 1236, 1248 (Fed. Cir. 2016). "Claim construction is a legal issue reviewed de novo, based on underlying factual findings that are reviewed for substantial evidence." *Personal Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 990 (Fed. Cir. 2017).

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[2] Because the '274 patent's filing date predates the amendment to § 102 made by the Leahy-Smith America Invents Act (AIA), Pub. L. No. 112-29, 125 Stat. 284 (2011), any reference to § 102 refers to the pre-AIA version of the statute.

A

Micron contends that the Board erred in upholding the patentability of claim 2 for two reasons: (1) the Board's construction of "clock delay circuit" was improperly narrow, and (2) Tachibana discloses the "clock delay circuit" even under the Board's construction. We disagree and address both arguments seriatim.

Because the '274 patent is expired, its claim terms are construed according to the principles articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See In re Rambus Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012). The Board construed the "clock delay circuit" of claim 2 to be "a circuit that receives a clock signal as an input and provides different versions of the input clock signal, with one version delayed compared to the other version." *Micron*, 2019 WL 5423610, at *13. Further, because the Board's construction of "clock delay circuit" included the term "clock signal," the Board also construed "clock signal" as "a control signal that enables or disables a circuit element in an output stage, such as a differential amplifier or a level converter." *See id.* at *14. Neither party disputes the Board's "clock signal" construction.

Micron submits that the plain and ordinary meaning of "clock delay circuit" as used in claim 2 is "a circuit that delays a clock signal in some manner." Appellant's Br. at 33. Micron contends that "both parties' experts agreed that the ordinary meaning of the term 'clock delay circuit' is exactly what those words say." *Id.* at 34. The Board's definition is too limiting, suggests Micron, because "a 'clock delay circuit' need not receive a clock signal as an input," *id.* at 37, and "need not create multiple versions of a single signal, with one delayed compared to the other," *id.* at 40. But we see no error in the Board's construction.

We are not persuaded that "clock delay circuit" as used in claim 2 has an ordinary, established meaning in the relevant field. We disagree with Micron that "the parties'

experts agreed that the ordinary meaning of the term 'clock delay circuit'" "requires only 'a circuit that is designed to delay a clock signal in some manner.'" *Id.* at 34; *see also* J.A. 1945 (North Star's expert explaining that clock delay circuit "could have a meaning [] depending on the context in which they're used" and that "that meaning . . . would be different"). Micron points us to its expert's declaration, *see* J.A. 1901, which opines that a clock delay circuit is "a circuit that is designed to delay a clock signal in some manner," *id.* ¶ 22. Expert testimony is generally not "useful to a court" when it contains only "conclusory, unsupported assertions by [the expert] as to the definition of a claim term." *SkinMedica, Inc. v. Histogen Inc.*, 727 F.3d 1187, 1195 (Fed. Cir. 2013) (quoting *Phillips*, 415 F.3d at 1318). Micron does not cite to any other evidence beyond the declaration, and we, like the Board, accord little weight to this testimony.

We agree with the Board that the best understanding of "clock delay circuit" in light of the specification is that it receives a clock signal as an input and outputs two different versions of this input clock signal, delaying one with respect to the other. The Board found that both "the parties and their respective experts agree that a 'clock delay circuit' receives a clock signal as an input," *Micron*, 2019 WL 5423610, at *17, and notwithstanding Micron's current disagreement, the record supports this finding, *see, e.g.*, J.A. 487–88 (Board: "Does a clock delay circuit receive as an input a clock signal" . . . Micron's counsel: "yes."). This admission aside, when the "timing circuit" of claim 2—including the clock delay circuit—is referenced in the written description of the '274 patent, it is always referenced as accepting a clock signal as input. *See* '274 patent col. 5 ll. 19–44.

Citing claim 4, Micron suggests that claim differentiation dictates that construing claim 2 as the Board did renders claim 4 superfluous. Appellant's Br. at 39–40. Claim 4, which, like claim 2, depends from claim 1, recites that

"the timing circuit receives a clock signal." The Board's construction does not violate the principle of claim differentiation because the "clock delay circuit" of claim 2 not only receives a clock signal as input, but also has specific output requirements not found in claim 4; claim 2 and claim 4 thus have different claim scope.

With respect to the "clock delay circuit" output, the written description explicitly details—for the "one embodiment" that uses a timing circuit—that the output of the timing circuit should be "two slightly different versions" of the "only clock" input signal, *id.* at col. 5 ll. 41–44, and that "[the] timing circuit [] is used to provide two versions of [the] clock signal," with one delayed compared to the other version of the clock signal, *id.* at col. 5. ll. 26–29.

Contrary to Micron's contentions, the Board's construction requiring the "clock delay circuit" to provide different versions of the input clock signal is not inappropriately narrow. We note, just as Micron did in its initial petition, that "the only embodiment disclosed in the [']274 Patent for a clock delay circuit" is the timing circuit described in column 5, J.A. 266 (Petition), which describes the timing circuit as outputting "not separate clock signal[s] as used by the prior art, but [instead] merely different versions of the same clock which have a delay between their disabling edges," '274 patent col. 5 ll. 34–37. The specification here, "read as a whole[,] suggests that the very character of the invention requires th[is] [timing circuit limitation of outputting two versions of the input clock signal] be a part of every embodiment [of the clock delay circuit]." *Alloc, Inc. v. Int'l Trade Comm'n*, 342 F.3d 1361, 1370 (Fed. Cir. 2003).

As the Board explained, Micron's proposed construction—that the "clock delay circuit" simply generates a delayed clock signal—fails to accord with the objectives of the '274 patent's invention. *See Micron*, 2019 WL 5423610, at *19 (quoting *OSRAM GmbH v. Int'l Trade Comm'n*, 505

F.3d 1351, 1358 (Fed. Cir. 2007)). The '274 patent explains: "It is advantageous to develop a memory output stage circuit that does not require two or more clocks, and thus does not require that a precise timing relationship be maintained," because "two clocks cannot be consistently controlled due to manufacturing process variations, temperature variations, power supply voltage variations, etc." '271 patent col. 1 ll. 37–44. The specification goes on to explain that, when a timing circuit is included in the output stage memory circuit, the timing circuit is used to create two clock signals that are different versions of the same input clock signal, one delayed with respect to other, which ensures that "these two versions will never vary enough [to impair the system's function] due to manufacturing process variations, temperature variations, power supply voltage variations, etc." *Id.* at col. 5 ll. 38–41. Put another way, the patent contemplates that the benefits sought to be achieved and the problems sought to be avoided are accomplished when the clock delay timing circuit limitation outputs two versions of the same input clock signal, one delayed with respect to the other. In the context of the patent, the Board correctly construed "clock delay circuit" to be "a circuit that receives a clock signal as an input and provides different versions of the input clock signal, with one version delayed compared to the other version."

Micron submits that even under this construction, the Board erred in failing to recognize that Tachibana discloses the "clock delay circuit" of claim 2. Appellant's Br. at 49. We disagree. The Board's finding of no anticipation is supported by substantial evidence.

First, the Board's finding that Tachibana does not disclose a "clock delay circuit" with a clock signal input is well-supported. Micron argues that the input signals of Tachibana's timing circuit are clock signals because "they start the process of signal generation that will *eventually* enable/disable Tachibana's differential amplifier." Appellant's Br. at 49 (emphasis added) (citations and internal

quotation marks omitted). But that is true only after the input signals get manipulated, combined, and modified by Tachibana's timing circuit. In other words, Micron's argument has to rely on the output signals from Tachibana's timing circuit to effectively serve as a stand-in for meeting the clock input signal requirement. We see no error in the Board's rejection of that proposed substitution. Substantial evidence supports the Board's finding that "[n]o input signal to Tachibana's timing circuit corresponds to a 'clock signal,' i.e., 'a control signal that enables or disables a circuit element in an output stage, such as a differential amplifier or a level converter.'"[3] *Micron*, 2019 WL 5423610, at *20.

Second, even if Tachibana disclosed a clock signal as input to its timing circuit, the Board's finding that Tachibana fails to disclose a timing circuit that outputs two versions of the same input clock signal, one delayed with respect to the other, is supported by substantial evidence. We agree with the Board that the signals outputted by Tachibana's timing circuit can hardly be described as two different versions of the same input signal or even two versions of each other. As the Board explained, the "input signals [in Tachibana are manipulated] in various ways to

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[3] Micron contends that the '274 patent's disclosed timing circuit lacks an "input clock signal" under the Board's construction of that term. That argument is beside the point because (1) the relevant question is whether Tachibana discloses a "clock delay circuit," as construed, and (2) neither party disputes the Board's construction of "clock signal." Moreover, we understand the Board's interpretation of clock signal to refer to a signal that itself can enable/disable a circuit element, which is what typical clock signals do, *see* '274 patent at col. 1 ll. 33–45 and col. 5 ll. 20–23, and what the input clock signal 78 of the '274 patent is, *see id.* at col. 5 ll. 41–44.

create new output signals," and each signal "result[s] from different logic circuitry operating on different logic input signals." *Micron*, 2019 WL 5423610, at *21. Accordingly, substantial evidence supports the Board's finding that Tachibana does not anticipate claim 2 because it fails to disclose the "clock delay circuit."

B

We turn next to claim 10, which requires that "the differential amplifier has an output driven by at least one of an emitter and a source of a transistor." The Board found that Micron failed to show that Tachibana anticipated claim 10 because "the differential amplifiers in Figures 15 and 17 [of Tachibana] do not include bipolar transistor 131," and thus, "the differential amplifier does not have an output driven by the emitter of bipolar transistor 131." *Micron*, 2019 WL 5423610, at *25. Micron appeals this finding, averring that the Board erred "by adding to the plain claim language a requirement that the transistor driving the output must be part of the differential amplifier" and that this was arbitrary because "[t]here is no material dispute that Tachibana's transistor 131 performs the function of conveying the differential amplifier output to the [level converter]." Appellant's Br. at 53.

We are unconvinced. The claim language here requires that the differential amplifier output be "driven by" a transistor's emitter or source, and we agree with North Star that describing "a component that 'drives' the output of a circuit element as nothing more than a component that 'conveys' that output, or passes it through, is . . . contrary to the specification [of the '274 patent]." Appellee's Br. at 58. As the Board observed, the specification describes "one circuit element's output driving another circuit element's input," and that in doing so, the circuit element necessarily "includes the component doing the driving." *See Micron*, 2019 WL 5423610, at *24–25. We need not consult a dictionary to understand that a component performing the

function of driving a circuit structure's "output" as used in the '274 patent requires that the driver component be a part of that circuit structure. The specification twice describes the operation of a particular transistor's emitter, and both times it discusses particular transistor emitters *within the differential amplifier* as outputting the differential amplifier's output signal to the level converter. *See* '274 patent at col. 6 ll. 16–19 ("[T]he output of differential amplifier 100 (i.e. the emitters of transistors 123 and 132) provides the amplified differential voltage to the gates of transistors 140 and 142.") and col. 5 ll. 13–17 ("Transistors 123 and 132 then function as emitter followers which provide the larger differential voltage to the input of level converter 102 at the control electrodes of transistor 140 and 142."). In view of the '274 specification, we agree with the Board's understanding of the "driven by" limitation. Accordingly, Tachibana does not disclose a transistor that performs the function of driving the output of the differential amplifier. We thus conclude that the Board's determination that Tachibana does not anticipate claim 10 is supported by substantial evidence.

C

Lastly, we turn to North Star's cross-appeal on claims 1 and 21. North Star asserts the same error with respect to the Board's findings on both claims, i.e., that the Board erred by allowing two claim limitations to be satisfied by the same single circuit element disclosure in Tachibana. *See* Appellee's Br. at 69–70. Specifically, North Star challenges the Board's determination that certain transistors, which are drawn respectively in Tachibana's figures to be located within the differential amplifier and level converter circuits, meet the "impedance control circuit" limitations in claim 1 and claim 21. Because these transistors are part of the differential amplifier and level converter, Micron argues, these transistors cannot also meet the impedance control circuit limitations.

We see no error in the Board's reasoning. Just as with claim 10 (and whether the transistor there was driving the output), the Board focused on whether the relevant transistor circuit elements in Tachibana perform the function of the limitation—here, impedance control. In support of its finding, the Board relied on undisputed expert testimony that transistor 412 of Tachibana performs the impedance control for the differential amplifier and that transistor 340 performs the impedance control for the level converter. *See Micron*, 2019 WL 5423610, at *10.

Contrary to North Star's assertions, the Board explicitly noted that it was mapping separate components to each of the three separate limitations in claims 1 and 21: the differential amplifier, the impedance control circuit, and the level converter. The Tachibana transistors at issue here, 412 and 340, though drawn within the bounds of Tachibana's differential amplifier and level converter respectively, do not carry out any operations for these subcircuits; it is undisputed that they only perform impedance control. The Board explained that, in Tachibana, "separate and distinct components perform differential amplification, separate and distinct components perform level conversion, and separate and distinct components perform impedance control, i.e., PMOS transistor 412 and NMOS transistor 340 for impedance control." *See id.* (citations omitted). Because the evidence demonstrates that neither transistor 412 or 340 "engages in either differential amplification or level conversion," *id.* (citation omitted), substantial evidence supports the Board's conclusion that Tachibana anticipates claims 1 and 21.

CONCLUSION

We have considered the parties' remaining arguments and are unpersuaded. For the reasons stated, the Board's decision is affirmed.

AFFIRMED

COSTS

Each party shall bear its own costs.