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## Exh. C

# Digital Telephony Second Edition 

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A Wiley-Interscience Publication JOHN WILEY \& SONS, INC.
New York • Chichester • Brisbane - Toronto • Singapore

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## Library of Congress Cataloging-in-Publication Data:

## Bellamy, John, 1941-

Digital telephony / John Bellamy. - 2nd ed.
p. cm. - (Wiley series in telecommunications)
"A Wiley-Interscience publication."
Includes bibliographical references and index.

| 1. Digital telephone systems. | I. Title. | II. Series. |
| :--- | ---: | ---: |
| TK5103.7.B44 1990 |  | $90-37906$ |
| 621.385-dc20 |  | CIP |
| ISBN 0-471-62056-4 |  |  |

Printed in the United States of America

Frequency domain voice coders provide improved coding efficiencies by encoding the most important components of the spectrum on a dynamic basis. As the sounds change different portions (formants) of the frequency band are encoded. The period between formant updates is typically 10 to 20 msec . Instead of using periodic spectrum measurements, some higher quality vocoders continuously track gradual changes in the spectral density at a higher rate. Frequency domain vocoders often provide lower bit rates than the time domain coders, but typically produce more unnatural sounding speech.

### 3.4 DIFFERENTIAL PULSE CODE MODULATION

Differential pulse code modulation (DPCM) is designed specifically to take advantage of the sample-to-sample redundancies in a typical speech waveform. Since the range of sample differences is less than the range of individual samples, fewer bits are needed to encode difference samples. The sampling rate is often the same as for a comparable PCM system. Thus the bandlimiting filter in the encoder and the smoothing filter in the decoder are basically identical to those used in conventional PCM systems.
A conceptual means of generating the difference samples for a DPCM coder is to store the previous input sample directly in a sample-and-hold circuit and use an analog subtractor to measure the change. The change in the signal is then quantized and encoded for transmission. The DPCM structure shown in Figure 3.27 is more complicated, however, because the previous input value is reconstructed by a feedback loop that integrates the encoded sample differences. In essence, the feedback signal is an estimate of the input signal as obtained by integrating the encoded sample differences. Thus the feedback signal is obtained in the same manner used to reconstruct the waveform in the decoder.

The advantage of the feedback implementation is that quantization errors do not accumulate indefinitely. If the feedback signal drifts from the input signal, as a result of an accumulation of quantization errors, the next encoding of the difference signal automatically compensates for the drift. In a system without


Figure 3.27. Functional block diagram of differential PCM.
feedback the output produced by a decoder at the other end of the connection might accumulate quantization errors without bound.

As in PCM systems, the analog-to-digital conversion process can be uniform or companded. Some DPCM systems also use adaptive techniques (syllabic companding) to adjust the quantization step size in accordance with the average power level of the signal. (See reference [9] for an overview of various techniques.)

Example 3.4. Speech digitization techniques are sometimes measured for quality by use of an $800-\mathrm{Hz}$ sine wave as a representative test signal. Assuming a uniform PCM system is available to encode the sine wave across a given dynamic range, determine how many bits per sample can be saved by using a uniform DPCM system.

Solution. In essence, the solution is obtained by determining how much smaller the dynamic range of the difference signal is in comparison to the dynamic range of the signal amplitude. Assume the maximum amplitude of the sine wave is $A$, so that

$$
x(t)=A \sin (2 \pi \cdot 800 t)
$$

The maximum amplitude of the difference signal can be obtained by differentiating and multiplying by the time interval between samples:

$$
\begin{gathered}
\frac{d x}{d t}=A \cdot(2 \pi) \cdot(800) \cdot \cos (2 \pi \cdot 800 t) \\
|\Delta x(t)|_{\max }=A \cdot(2 \pi) \cdot(800) \cdot\left(\frac{1}{8000}\right)=0.628 A
\end{gathered}
$$

The savings in bits per sample can be determined as

$$
\log _{2}\left(\frac{1}{0.628}\right)=0.67 \text { bits }
$$

Example 3.4 demonstrates that a DPCM system can use $\frac{2}{3}$ bit per sample less than a PCM system with the same quality. Typically DPCM systems provide a full 1 bit reduction in code word size. The larger savings is achieved because, on average, speech waveforms have a lower slope than an 800 Hz tone (see Figure 3.25).

### 3.4.1 DPCM Implementations

Differential PCM encoders and decoders can be implemented in a variety of ways depending on how the signal processing functions are partitioned between analog and digital circuitry. At one extreme the differencing and integration functions can be implemented with analog circuitry, while at the other extreme

As is demonstrated shortly, the number of crosspoints defined in Equation 5.1 can be significantly lower than the number of crosspoints required for single stage switches. First, however, we must determine how many center stage arrays are needed to provide satisfactory service.

## Nonblocking Switches

One attractive feature of a single stage switch is that it is strictly nonblocking. If the called party is idle, the desired connection can always be established by selecting the particular crosspoint dedicated to the particular input/output pair. When crosspoints are shared, however, the possibility of blocking arises. In 1953 Charles Clos [2] of Bell Laboratories published an analysis of three-stage switching networks showing how many center stage arrays are required to provide a strictly nonblocking operation. His result demonstrated that if each individual array is nonblocking, and if the number of center stages $k$ is equal to $2 n-1$, the switch is strictly nonblocking.

The condition for a nonblocking operation can be derived by first observing that a connection through the three-stage switch requires locating a center stage array with an idle link from the appropriate first stage and an idle link to the appropriate third stage. Since the individual arrays themselves are nonblocking, the desired path can be set up any time a center stage with the appropriate idle links can be located. A key point in the derivation is to observe that since each first-stage array has $n$ inlets, only $n-1$ of these inlets can be busy when the inlet corresponding to the desired connection is idle. If $k$ is greater than $n-1$, it follows that, at most, $n-1$ links to center stage arrays can be busy. Similarly, at most $n-1$ links to the appropriate third-stage array can be busy if the outlet of the desired connection is idle.
The worst case situation for blocking occurs (as shown in Figure 5.7) if all $n-1$ busy links from the first-stage array lead to one set of center stage arrays, and if all $n-1$ busy links to the desired third-stage array come from a separate set of center stage arrays. Thus these two sets of center stage arrays are unavailable for the desired connection. However, if one more center stage array exists, the appropriate input and output links must be idle, and that center stage can be used to set up the connection. Hence if $k=(n-1)+$ ( $n-1$ ) $+1=2 n-1$ the switch is strictly nonblocking. Substituting this value of $k$ into Equation 5.1 reveals that for a strictly nonblocking operation of a three stage switch:

$$
\begin{equation*}
N_{x}=2 N(2 n-1)+(2 n-1)\left(\frac{N}{n}\right)^{2} \tag{5.2}
\end{equation*}
$$

As expressed in Equation 5.2, the number of crosspoints in a nonblocking three-stage switch is dependent on how the inlets and outlets are partitioned into subgroups of size $n$. Differentiating Equation 5.2 with respect to $n$ and setting the resulting expression equal to 0 to determine the minimum reveals


Figure 5.7. Nonblocking three-stage switching matrix.
that (for large $N$ ) the optimum value of $n$ is $(N / 2)^{1 / 2}$. Substituting this value of $n$ into Equation 5.2 then provides an expression for the minimum number of crosspoints of a nonblocking three-stage switch.

$$
\begin{equation*}
N_{x}(\min )=4 N(\sqrt{2 N}-1) \tag{5.3}
\end{equation*}
$$

where $N=$ total number of inlets/outlets.
Table 5.1 provides a tabulation of $N_{x}(\mathrm{~min})$ for various sized nonblocking three-stage switches and compares the values to the number of crosspoints in a single stage square matrix. Both switching structures inherently provide fourwire capabilities, a requirement for digital switches because voice digitization implies four-wire circuits.

TABLE 5.1 Crosspoint Requirements of Nonblocking Switches

| Number <br> of Lines | Number of <br> Corosspoints for <br> Three-Stage Switch | Number of <br> Crosspoints for <br> Single-Stage Switch |
| ---: | :---: | :---: |
| 128 | 7,680 | 16,256 |
| 512 | 63,488 | 261,632 |
| 2,048 | 516,096 | 4.2 million |
| 8,192 | 4.2 million | 67 million |
| 32,768 | 33 million | 1 billion |
| 131,072 | 268 million | 17 billion |

