UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

VOLTERRA SEMICONDUCTOR CORPORATION,

Plaintiff,

v.

PRIMARION, INC., ET AL.,

Defendants.
_____/

Case No. C-08-05129 JCS

CLAIM CONSTRUCTION ORDER

## I. INTRODUCTION

On November 12, 2008, Plaintiff Volterra Semiconductor Corporation ("Volterra") filed a complaint alleging infringement and contributory infringement by Defendants of the following patents: 1) U.S. Patent No. 6,278,264 (the "'264 patent"); 2) U.S. Patent No. 6,462,522 (the "'522 patent"); 3) U.S. Patent No. 6,713,823 (the "'823 patent"); 4) U.S. Patent No. 6,020,729 (the "'729 patent"); and 5) U.S. Patent No. 6,225,795 (the "'795 patent"). Currently before the Court is the task of construing certain terms used in the '264, '522 and '823 patents. Some of the terms were tentatively construed in the Court's ruling on Plaintiff's motion for a preliminary injunction. The Court's final constructions are set forth below.[1]

## II. OVERVIEW OF THE TECHNOLOGY

In its Order denying Plaintiff's motion for a preliminary injunction, the Court provided a detailed background regarding the technology at issue in the '522 and '264 patents ("the Burstein patents"). Therefore, the Court provides here only a brief summary of the technology associated with the patent that was not addressed in the Court's previous order, the '823 patent.

[1]The parties have consented to the jurisdiction of a United States Magistrate Judge pursuant to 28 U.S.C. § 636(c).

The '823 patent, issued March 30, 2004, is entitled "Conductive Routings in Integrated Circuits" and lists Charles Nickel as inventor. The '823 patent relates to a metal routing structure that can be used in integrated circuits, including those that use flip-chip packaging technology. '823 patent, 1: 6-7, 7: 51-54. The routing structure provides "substantially continuous conductive planes for the flow of electrical currents" in which current is routed from the doped regions to pads located above the doped regions, in contrast to typical implementations, where the pads are arranged along the perimeter of the chip. '823 patent, 1: 6-38. As a result of this arrangement, the length of conductive routings from doped regions in a substrate to conducting pads can be shortened, resulting in reduction of interconnection resistance and power loss. *Id*. The shorter conductive routings also increase the area available for functional devices in a chip. *Id*.

## III. LEGAL STANDARDS

### A. Infringement Standards

A determination of infringement is a two-step process. *Wright Med. Tech., Inc. v. Osteonics Corp.*, 122 F.3d 1440, 1443 (Fed. Cir. 1997). The first step is claim construction, which is a question of law to be determined by the court. *Id*. The second step is an analysis of infringement, in which it must be determined whether a particular device infringes a properly construed claim. *Id*. This analysis is a question of fact. *Id*. A device literally infringes if each of the elements of the asserted claims is found in the accused device. *Id*. In the alternative, a device may infringe under the doctrine of equivalents "if every limitation of the asserted claim, or its 'equivalent,' is found in the accused subject matter, where an 'equivalent' differs from the claimed limitation only insubstantially." *Ethicon Endo-Surgery, Inc. v. United States Surgical Corp.*, 149 F.3d 1309, 1315 (Fed. Cir. 1998).

### B. Claim Construction Standards

"It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (quoting *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). Generally, claim terms are given the ordinary and customary meaning that would be ascribed to them by a person of ordinary skill in the field of the invention. *Id*. at 1313;

*see also Rexnord Corp. v. Laitram Corp.*, 274 F.3d 1336, 1342 (Fed. Cir. 2001)("[U]nless compelled to do otherwise, a court will give a claim term the full range of its ordinary meaning as understood by an artisan of ordinary skill").

The most "significant source of the legally operative meaning of disputed claim language" is the intrinsic evidence of record, that is, the claims, the specification and the prosecution history. *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). This is because "the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Phillips*, 415 F.3d at 1312. In some cases, the specification may reveal a "special definition" given by the inventor that differs from the meaning the term might otherwise possess. *Id*. at 1316; *see also Irdeto Access, Inc. v. Echostar Satellite Corp.*, 383 F.3d 1295, 1300 (Fed. Cir. 2004) (holding that where a disputed claim term has "no previous meaning to those of ordinary skill in the art, its meaning, then, must be found elsewhere in the patent"). In such instances, "the inventor's lexicography governs." *Phillips*, 415 F.3d at 1312. Similarly, a specification may reveal "an intentional disclaimer, or disavowal, of claim scope by the inventor." *Id*.

"[T]he Federal Circuit has held that if commonly understood words are used, then the 'ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words.'" *Board of Trustees of Leland Stanford University v. Roche Molecular Systems, Inc.*, 528 F. Supp. 2d 967, 976 (N.D. Cal. 2007) (quoting *Phillips*, 415 F.3d at 1314); *see also United States Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997) (holding that "[c]laim construction is a matter of resolution of disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims, for use in the determination of infringement. It is not an obligatory exercise in redundancy"). Thus, in *Board of Trustees of Leland Stanford University v. Roche Molecular Systems, Inc.*, the court held that a claim term did not need construction where it was "neither unfamiliar to the jury, confusing to the jury, nor affected by the specification or prosecution history." 528 F. Supp. 2d at 976. Other courts have held, held, however, that even if the meaning of a

disputed term is "readily apparent," the Court should, nonetheless, construe the term. *See, e.g.*, *Maytag Corp. v. Electrolux Home Products, Inc.*, 411 F.Supp.2d 1008, 1037 (N.D. Iowa 2006) ("It has been this court's experience that parties in patent cases rarely agree on the ordinary meaning of patent terms as understood by a person of skill in the art, so that asserting that such a meaning should apply, without further construction, merely begs the question of what that meaning is").

A person of ordinary skill in the art also looks to the prosecution history of a patent to understand how the patent applicant and the Patent Office understood the claim terms. *Phillips*, 415 F.3d at 1313. In particular, arguments and amendments made during patent prosecution limit the interpretation of claim terms to exclude interpretations that were disclaimed to obtain allowance of a claim. *Southwall Technologies, Inc. v. Cardinal IG Co.*, 54 F.3d 1570, 1576 (Fed. Cir. 1995).

While claims are to be construed in light of the specification, courts must be careful not to read limitations from the specification into the claim. *Phillips*, 415 F.3d at 1323. If a patent specification describes only a single embodiment, that does not mean the claims of the patent necessarily must be construed as limited to that embodiment. *Id*. Rather, it is to be understood that the purpose of the specification "is to teach and enable those of skill in the art to make and use the invention" and that sometimes, the best way to do that is to provide an example. *Id*. Similarly, the Federal Circuit has cautioned that "patent coverage is not necessarily limited to inventions that look like the ones in the figures," noting that taking such an approach to claim construction would amount to "import[ing] limitations onto the claim from the specification, which is fraught with danger." *MBO Laboratories, Inc. v. Becton, Dickinson & Co.*, 474 F.3d 1323, 1333 (Fed. Cir. 2007).

Courts may also use extrinsic evidence in construing claim terms if it is necessary, so long as such evidence is not used to "vary or contradict the terms of the claims." *Markman*, 52 F.3d at 980; *see also Verve, LLC v. Crane Cams, Inc.*, 311 F.3d 1116, 1119 (Fed. Cir. 2002) ("Patent documents are written for persons familiar with the relevant field; the patentee is not required to include in the specification information readily understood by practitioners, lest every patent be required to be written as a comprehensive tutorial and treatise for the generalist, instead of a concise statement for persons in the field. Thus resolution of any ambiguity arising from the claims and specification may

be aided by extrinsic evidence of usage and meaning of a term in the context of the invention"). As the court explained in *Markman*, "[extrinsic] evidence may be helpful to explain scientific principles, the meaning of technical terms, and terms of art that appear in the patent and prosecution history." 52 F.3d at 980. The Federal Circuit has warned, however, that such evidence is generally "less reliable than the patent and its prosecution history." *Phillips*, 415 F.3d at 1318. Thus, courts are free to consult dictionaries and technical treatises so long as they are careful not to elevate them "to such prominence that it focuses the inquiry on the abstract meaning of the words rather than on the meaning of the claim terms within the context of the patent." *Phillips*, 415 F.3d at 1321-22.

In recent years, the Federal Circuit has offered considerable guidance on the role extrinsic evidence should play in claim construction. In *Phillips*, the Federal Circuit rejected a methodology that it had previously set forth in *Texas Digital Systems, Inc. v. Telegenix, Inc.*, 308 F.3d 1193 (Fed. Cir. 2002) for the use of extrinsic evidence, warning that it placed too great an emphasis on dictionary definitions and other treatises. 415 F.3d at 1321. The Federal Circuit explained its conclusion as follows:

> Although the concern expressed by the court in *Texas Digital* was valid, the methodology it adopted placed too much reliance on extrinsic sources such as dictionaries, treatises, and encyclopedias and too little on intrinsic sources, in particular the specification and prosecution history. While the court noted that the specification must be consulted in every case, it suggested a methodology for claim interpretation in which the specification should be consulted only after a determination is made, whether based on a dictionary, treatise, or other source, as to the ordinary meaning or meanings of the claim term in dispute. Even then, recourse to the specification is limited to determining whether the specification excludes one of the meanings derived from the dictionary, whether the presumption in favor of the dictionary definition of the claim term has been overcome by "an explicit definition of the term different from its ordinary meaning," or whether the inventor "has disavowed or disclaimed scope of coverage, by using words or expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope." 308 F.3d at 1204. In effect, the *Texas Digital* approach limits the role of the specification in claim construction to serving as a check on the dictionary meaning of a claim term if the specification requires the court to conclude that fewer than all the dictionary definitions apply, or if the specification contains a sufficiently specific alternative definition or disavowal. . . . That approach, in our view, improperly restricts the role of the specification in claim construction.

*Id*.

These principals were illustrated in *Nystrom v. TREX Co., Inc.*,424 F.3d 1136, 1145 (Fed. Cir. 2005). In that case, the Federal Circuit held that the word "board" encompassed only "wood decking materials cut from a log," even though a few dictionary definitions swept more broadly to

include similarly-shaped items made of materials other than wood. In reaching this conclusion, the Federal Circuit rejected the plaintiff's argument that the broader definition should be adopted because there had been no disclaimer of claim scope during the prosecution of the patent. *Id*. The Court noted that the parties agreed that the ordinary and customary meaning of "board" was an item made of wood. *Id*. Further, it was undisputed that the written description and prosecution history consistently used "board" to refer to an item made of wood. *Id*. The court reasoned:

> What *Phillips* now counsels is that in the absence of something in the written description and/or prosecution history to provide explicit or implicit notice to the public – i.e., those of ordinary skill in the art – that the inventor intended a disputed term to cover more than the ordinary and customary meaning revealed by the context of the intrinsic record, it is improper to read the term to encompass a broader definition simply because it may be found in a dictionary, treatise, or other extrinsic source.

*Id*.

Similarly, in *AquaTex Indus., Inc. v. Techniche Solutions*, the Federal Circuit held that the term "fiberfill" referred only to synthetic materials and did not encompass natural materials because the patentee consistently used the term in this way in the specification. 419 F.3d 1374, 1380 (Fed. Cir.2005). The court reached this conclusion even though the specification stated that the composition of the fiberfill was not known to be critical, noting that although there was no disavowal of fiberfill that used natural material, the description consistently used the term with reference to synthetic material, and extrinsic dictionary definitions also supported this construction. *Id*.

On the other hand, in *Phillips*, the Federal Circuit held that the term "baffle" "did not require any specific angle – even in view of the written description's limited disclosure of baffles oriented at right angles to the walls – because the ordinary meaning of the term 'baffle,' as reflected in a dictionary definition to which the parties stipulated and as supported by the overall context of the written description, was simply 'objects that check, impede, or obstruct the flow of something.'" *Nystrom*, 424 F.3d at 1145 (quoting *Phillips*, 415 F.3d at 1324).

"A word or phrase used consistently throughout a claim should be interpreted consistently." *Phonometrics, Inc. v. Northern Telecom Inc.*, 133 F.3d 1459, 1465 (Fed.Cir.1998). On the other hand, where a claim term is used "in two contexts with a subtle but significant difference" the term

"should not necessarily be interpreted to have the same meaning in both phrases." *Epcon Gas Systems, Inc. v. Bauer Compressors, Inc.*, 279 F.3d 1022, 1031 (Fed. Cir. 2002). Further, the modifiers "first" and "second" before a claim term is a "common patent-law convention to distinguish between repeated instances of an element or limitation." *3M Innovative Properties Co. v. Avery Dennison Corp.*, 350 F.3d 1365, 1371 (Fed. Cir. 2003) (holding that "first pattern" and "second pattern" is equivalent to "Pattern A" and "Pattern B"); *see also Swapalease, Inc. v. Sublease Exchange.com, Inc.*, 2009 WL 204408, *11 (S.D.Ohio, Jan. 27, 2009)(holding that "first webpage" and "second webpage" are specific webpages and that "first webpage" is different from "second webpage").

**C. Indefiniteness Standards**

The requirement that claims be sufficiently "definite" is set forth in 35 U.S.C. § 112, ¶ 2, which provides that, "[t]he specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention." "The definiteness inquiry focuses on whether those skilled in the art would understand the scope of the claim when the claim is read in light of the rest of the specification." *Union Pacific Resources Co. v. Chesapeake Energy Corp.*, 236 F.3d 684, 692 (Fed. Cir. 2001). In order to "accord respect to the statutory presumption of patent validity," a claim should be found indefinite "only if reasonable efforts at claim construction prove futile." *Exxon Research and Engineering Co. v. United States*, 265 F.3d 1371, 1375 (Fed. Cir. 2001). Thus, a claim is not indefinite simply because its meaning is not ascertainable from the face of the claims. *Amgen, Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1311, 1342 (Fed. Cir. 2003). Further, a claim is not indefinite simply because it covers "some embodiments that may be inoperable." *Exxon Research and Engineering Co.*, 265 F.3d at 1382. A claim is indefinite, however, if it is "insolubly ambiguous, and no narrowing construction can properly be adopted." *Amgen*, 314 F.3d at 1342 (citations omitted).

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## IV. DISPUTED CLAIM TERMS

The parties submitted ten claim terms for construction, consistent with Patent Local Rule 4-3 and the Court's Amended Case Management and Pretrial Order [Docket No. 91]. In addition, Defendants seek a determination that another claim term is indefinite because it is insolubly ambiguous.[2] The Court addresses these claim terms below.

### A. The '264 and '522 Patents

#### 1. "integrated circuit"

| Claim Term | Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|---|
| integrated circuit | An interconnected arrangement of passive and active elements forming at least part of a voltage regulator circuit including a power switch, which is implemented on a single semiconductor substrate | A miniaturized electronic circuit (a.k.a. an IC, microcircuit, silicon chip, chip, or die) consisting of interconnected circuit elements that have been manufactured in, on, and above the surface of a substrate of semiconducting material. |

Claim 26 of the '264 patent and claims 9, 18 and 22 of the '522 patent claim an "integrated circuit." Defendants challenge two aspects of Volterra's proposed construction of this claim term. First, they dispute that the term requires passive elements. Although Defendants initially agreed with Plaintiff that an integrated circuit requires passive elements, in their final Patent L.R. 4-3 constructions, they removed this requirement from their proposed construction. Second, Defendants assert that Volterra improperly limits the scope of the term by including in its proposed construction the words "forming at least part of a voltage regulator circuit including a power switch."

Defendants offer an alternative construction that does not include either of the limitations

[2]Defendants assert that the claim term "power switch" cannot be construed, and therefore, that this term does not exceed the five terms that Defendants may offer for construction under Patent Local Rule 4-3 and the Court's case management order. Defendants have not offered any authority in support of their interpretation of the local rule, which the Court finds unpersuasive. Indeed, Defendants acknowledge in their responsive claim construction brief that the indefiniteness inquiry is an exercise in claim construction, citing *Datamize, L.L.C. v. Plumtree Software, Inc.*, 417 F.3d 1342, 1347 (Fed. Cir. 2001) for the proposition that the question of whether a claim term is insolubly ambiguous is a question of law decided during claim construction. Nonetheless, as the parties and their experts have addressed the issue, the Court will do so as well.

discussed above, taken from the IEEE Standard Dictionary of Electrical and Electronics Terms (with some modifications). Plaintiff challenges Defendants' proposed construction on two grounds. First, it asserts that Defendants are bound by the statements of their former expert regarding the passive component requirement. Second, Plaintiff argues that Defendants' proposed construction should not be adopted because it relies too heavily on extrinsic evidence and does not take into account the fact that the term was consistently used in the Burstein patents in the context of a voltage regulator circuit. Volterra argues that because such a circuit contemplates the inclusion of control circuitry, which typically includes passive components such as resistors or capacitors, the term "integrated circuit" must be construed to require passive components.

**a. Passive Elements Requirement**

**i. Whether Dr. Baker's Statements are Binding**

As a preliminary matter, the Court addresses Plaintiff's argument that the statements of Defendants' previous expert, Dr. Baker, are binding with respect to the question of whether the term "integrated circuit" requires passive components. The Court concludes that they are not.

When the Court addressed Plaintiff's preliminary injunction motion, Plaintiff's expert, Dr. Szepesi, and Defendants' former expert, Dr. Baker, agreed that the term "integrated circuit" should be construed to require passive components. Now, Defendants have changed their position, relying on the opinion of their new expert, Dr. Fair, in support of a proposed construction that does not require passive components. Plaintiff asserts that Dr. Baker's position is binding on Defendants. Given that Dr. Baker's statements were made at an early stage of this litigation, the Court rejects Plaintiff's assertion that they are binding. Nor does the case cited by Plaintiff, *Fin Control Systems v. OAM, Inc.*, 265 F.3d 1311 (Fed. Cir. 1311), stand for that proposition because it did not involve statements made by an expert in the context of a preliminary claim construction. Therefore, the Court turns to the evidence cited by the parties to determine whether the term "integrated circuit," as used in the asserted claims of the '522 and '264 patents, requires passive components.

**ii. Arguments**

In support of its position that the term "integrated circuit," requires passive components, Volterra cites to the specification of the Burstein patents, which describes integrated circuits in preferred embodiments of the invention as having control circuits or sensors. *See* '264 patent, 2: 24 - 29 ("A portion of the control circuit, such as an interpreter to interpret commands from the portion of the control circuit fabricated on the second chip, or a sensor that directs measurements to the portion of the control circuit fabricated on the second chip, may be fabricated on the first chip"); 6: 50-55 ("Additional unillustrated circuitry on the IC chip may measure a characteristic of a switching circuit, e.g., the current flowing through the PMOS transistor array 30 and NMOS transistor array 32, and pass the measurement back to the rest of the control circuitry via the control pads."). According to Plaintiff's expert, these control circuits and sensors "typically" include passive components. *See* Declaration of Jeffrey M. Fisher in Support of Volterra's Opening Claim Construction Brief ("Fisher Claim Construction Decl."), Ex. 9 (Szepesi Depo.) at 318 ("this integrated circuit chip . . . may include a sensor. And sensors are analog circuits and typically have – they need bias circuits to bias them up. And all those bias circuits that I know – most of them have resistors and capacitors, which are passive elements"), 319 ("So this section ['264 patent, 6:50-55] relates also to analog circuitry. . . . And . . .these are typically including passive components, resistors and capacitors").

In addition, Plaintiff points to a dictionary definition of the term "integrated circuit" found in the McGraw-Hill Dictionary of Electrical and Electronic Engineering, which defines "integrated circuit" as an "interconnected array of active and passive elements integrated with a single semiconductor substrate or deposited on the substrate by a continuous series of compatible processes, and capable of performing at least one complete electronic circuit function." Fisher Claim Construction Decl., Ex. 13 at VLTSA00040890. Therefore, Plaintiff argues, both the intrinsic and extrinsic evidence supports its position that the term "integrated circuit" requires passive components.

Defendants disagree, asserting that in 1998,[3] one of ordinary skill in the art understood that while integrated circuits often included passive components, there were also integrated circuits that did not include any passive components. *See* Declaration of Vera M. Elson in Support of Primarion, Inc., Infineon Technologies North America Corp., and Infineon Technologies AG's Responsive Claim Construction Brief ("Elson Claim Construction Decl."), Ex. 1 (Declaration of Dr. Richard Fair in Support of Defendants' Responsive Claim Construction Brief ("Fair Claim Construction Decl.")), ¶ 61. In particular, according to Defendants' expert, Dr. Fair, it would have been understood by a person of ordinary skill in the art that an integrated circuit "could have included only two or more transistors and some routing – with no passive components – and still have been considered an integrated circuit by a person of ordinary skill in the art." *Id.*, ¶ 29. Indeed, Defendants cite to deposition testimony by Plaintiff's expert that in 1998, he was aware that there were integrated circuits without passive elements. *See* Declaration of Vera M. Elson in Support of Primarion, Inc., Infineon Technologies North America Corp., and Infineon Technologies AG's Supplemental Claim Construction Brief ("Elson Supp. Claim Construction Decl."), Ex. 43 (Szepesi Depo.) at 557-559.[4]

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[3]The parties agree that for the purposes of claim construction, it makes no difference whether the Court looks to April 3, 1998 – the date that Volterra contends was the date of invention – or the later date when the '264 application was filed, February 4, 2000, to determine how a person of ordinary skill in the art would have understood the disputed claim terms.

[4]At his deposition, Dr. Szepesi testified as follows:

Q: And were you ever aware prior to 1998 of any integrated circuit that did not include passive elements?

A: Not in the context of the Burstein patent.

Q. Set aside the context of the Burstein patent. I'm asking you whether, prior to 1998, were you ever aware of any integrated circuit that did not include passive elements?

. . .

A: I'm not aware of any integrated circuit for switching regulator or for voltage regulator which – in the prior art which wouldn't include passive elements.

Q: I'm not limiting my question to voltage regulators, sir. I'm asking you whether, prior to 1998, you were ever aware of any integrated circuit that did not include passive elements.

Defendants also point to the IEEE Standard Dictionary of Electronical and Electronics Terms (Sixth Ed.), which includes the following definition of "integrated circuit" among several definitions: "a combination of connected circuit elements (such as transistors, diodes, resistors and capacitors) inseparably associated on or within a continuous substrate." Elson Claim Construction Decl., Ex. 1 (Fair Claim Construction Decl.), ¶ 59; Ex. 20 (IEEE definition).

Further, to the extent the specification offers any guidance, Defendants assert, it suggests that the inventors did not limit the term "integrated circuit" to exclude chips that have no passive components. Defendants note that the language in the specification upon which Volterra relies to support the inclusion of passive components in its construction is permissive, stating only that the chip "may" have control circuits or sensors. Similarly, Dr. Szepesi testified in his deposition only that the circuits described in the specification "typically" include passive components. Defendants also point to a passage in the specification in which the inventors referred to "a load 14, such as an integrated circuit." *See* Elson Claim Construction Decl., Ex. 1 (Fair Claim Construction Decl.), ¶ 60 (citing '264 patent, 4: 48-59). In particular, the specification states as follows: "the switching regulator 10 is also coupled to a load 14, such as an integrated circuit, by an output terminal 23." '264 patent, 4: 58-60. Defendants assert that in this context, the inventors were using the "term integrated circuit" to refer to an integrated circuit that is not part of a voltage regulator, and therefore, would not necessarily include passive components. At oral argument, Plaintiff conceded that the "load" referred to in this passage is not part of a voltage regulator. *See* 1/22/10 Transcript at 80.[5]

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. . .

A: So outside the context of the patent, if the integrated circuit, what you are asking, is not part of the switching regulator or the voltage regulator, it is possible to create a logic circuit like – there was an integrated circuits [sic] called 7404 or 7606, which is a hex inverter. And I assume it didn't have passive element, but it is not an integrated circuit for switching regulator or voltage regulator. It's a logic circuit.

[5]At oral argument, Defendants asserted, in response to a question by the Court, that an integrated circuit for a voltage regulator does not require passive components, pointing to Figure 1 of the '264 patent. According to counsel, Figure 1 shows that an "integrated circuit" may be just two transistors. 1/22/10 Transcript at 85. Because Defendants do not cite to any expert testimony in support of this argument, which was raised for the first time at oral argument, the Court does not consider it.

Plaintiff counters that Defendants' proposed construction of "integrated circuit" is improper because it relies on extrinsic evidence that does not take into account the context of the Burstein patents. Plaintiff notes that Dr. Fair, when asked at his deposition whether the term "integrated circuit" should be construed in light of the specification and file history of the Burstein patents, answered, "Not necessarily. I think it's a term, that's why I didn't cite any intrinsic evidence, that's why I've used dictionary definitions." *See* Declaration of June Tai in Support of Volterra Semiconductor Corporation's Supplemental Reply Claim Construction Brief (Tai Supp. Claim Construction Decl."), Ex. A (Fair Depo., 11/20/2009) at 129. Plaintiffs also point out that while one of the definitions of "integrated circuit" in the IEEE dictionary does not require passive components, another definition found in the same entry does. In particular, one of the definitions is "[a] solid-state circuit consisting of interconnected active and passive semiconductor devices diffused into a single silicon chip." *See* Elson Decl., Ex. 20 (IEEE definition).

**iii. Analysis**

As discussed above, while claims are to be construed in light of the specification, courts must be careful not to read limitations from the specification into the claims. *Phillips*, 415 F.3d at 1323. Thus, if a patent specification describes only a single embodiment, that does not mean the claims of the patent necessarily must be construed as limited to that embodiment. *Id*. Rather, it is understood that the purpose of the specification "is to teach and enable those of skill in the art to make and use the invention" and that sometimes, the best way to do that is to provide an example. *Id*. On the other hand, courts must not elevate the extrinsic evidence "to such prominence that it focuses the inquiry on the abstract meaning of the words rather than on the meaning of the claim terms within the context of the patent." *Phillips*, 415 F.3d at 1321-22. In *Phillips*, the Federal Circuit acknowledged, "the distinction between using the specification to interpret the meaning of a claim and importing limitations from the specification can be a difficult one to apply in practice." *Id*. That point is illustrated here.

Defendants have pointed out that the specification of the Burstein patents does not address the question of whether an integrated circuit requires passive elements. Further, although all of the embodiments described in the specification include sensors and control circuits – implying that

"integrated circuits," as that term is used in the Burstein patents, include passive components – these sections are phrased permissively, that is, stating that these *may* be features of the invention, not that they are required features. Similarly, Dr. Szepesi's testimony is that passive components are "typical" of integrated circuits with control circuits or sensors. In addition, Plaintiff has conceded that the term "integrated circuit" is used at least once in the specification to refer to an integrated circuit that is not a voltage regulator. *See* '264 patent, 4: 58-60. This reference indicates that the inventors did not ascribe the narrower meaning of "integrated circuit" advanced by Plaintiff, requiring passive components.

The extrinsic evidence in the record supports this conclusion. In particular, the extrinsic evidence indicates that in 1998, the definition of "integrated circuit" in the IEEE Dictionary was broad enough to encompass devices that did not include passive components. In addition, both experts appear to agree that a person of ordinary skill in the art in 1998 would have known that integrated circuits without passive components existed at that time.

The Court concludes that the term "integrated circuit," as used in the Burstein patent, does not require passive components.

**b. Whether the phrase "forming at least part of a voltage regulator circuit including a power switch" should be included in construction of "integrated circuit"**

The issues raised with respect to this proposed claim limitation are similar to those discussed above. In particular, Plaintiff cites to numerous statements in the specification indicating that in the Burstein patents, the integrated circuit was to be used in a voltage regulator application with a power switch. *See* '264 patent, 1: 4-7, 1: 65 - 2:5, 2: 24-29, 2: 33-36, 2: 50-55, 3: 62 - 4:1, 6: 50-55. Defendants, on the other hand, point to evidence that in 1998, a person of ordinary skill in the art would have known that there were integrated circuits with no relation to voltage regulators (as discussed above). Defendants' expert also points to the passage in the specification that he asserts refers to an integrated circuit that is *not* part of a voltage regulator circuit, that is column 4, lines 48-59. *See* Elson Claim Construction Decl., Ex. 1 (Fair Claim Construction Decl.), ¶ 60 (citing '264 patent, 4: 48-59). In particular, the specification states as follows: "the switching regulator 10 is also coupled to a load 14, such as an integrated circuit, by an output terminal 23." *Id*. According to

Dr. Fair, one of ordinary skill in the art would understand that this "load" could be another type of integrated circuit and typically, it would not be a voltage regulator. *Id*. Finally, Defendants argue that if this limitation were included in the construction, it would render superfluous language in claim 26 to the extent it claims "an integrated circuit *with a power switch for a voltage regulator fabricated thereon*."

The Court concludes that Defendants are correct on this question. Although it is undisputed that the integrated circuit disclosed in the Burstein patents is for use in a voltage regulator, this use is evident from separate claim limitations and therefore need not be included in the Court's construction of the term "integrated circuit." Further, as noted by Defendants, the patentees used the term "integrated circuit" at least once in the specification to refer to an integrated circuit that is *not* part of a voltage regulator. *See* '264 patent, 4: 48-59. Therefore, the Court declines to include this proposed limitation in its construction of the claim term "integrated circuit."

The Court construes "integrated circuit" as "[a] miniaturized electronic circuit consisting of interconnected circuit elements, which is implemented on a semiconductor substrate."

**2. "metalized pads"**

| **Claim Term** | **Plaintiff's Proposed Construction** | **Defendants' Proposed Construction** |
|---|---|---|
| metalized pads | Pads that include an under-bump metalization layer (UBM) that forms an interface between the top metal layer of the integrated circuit and the solder balls (bumps) that are often used in flip-chip type integrated circuits. Pads in an integrated circuit are openings in the top passivation layer that allow connection to the top metal layer, to enable formation of connections between the integrated circuit and external circuit element | An array of "metalized pads" wherein each pad in the array consists of: (i) an individual and distinct raised island of metal separated a fixed distance from the other metalized pads; (ii) a passivation layer that lies partially over the island of metal; and (iii) an under-bump metal (UBM) that partially overlaps both the island of metal and the passivation layer |

Claim 26 of the '264 patent and claim 22 of the '522 Patent claim the use of "metalized pads." The parties agree that while the term "pads" was well-known in the art, the term "metalized

pads" was not a term of art at the time of the invention. *See* Rebuttal Declaration of Dr. Thomas Szepesi in Support of Volterra's Reply Claim Construction Brief ("Szepesi Claim Construction Reply Decl."), ¶ 30 ("The Burstein Patents used/coined a term 'metalized pad' which was not used in prior art, describing the two well-known structures, the standard 'pads' with [under-bump metalization]"); Elson Claim Construction Decl., Ex. 1 (Fair Claim Construction Decl.), ¶ 64 ("The term 'metalized pads' is not a common term in the integrated circuit art"). Therefore, the Court must look to the specification to construe the term.[6] The primary issue in dispute with regard to construction of "metalized pads" is whether the final metal layer of the metalized pad is limited to "individual and distinct raised island of metal separated a fixed distance from the other metalized pads," as Defendants contend, or rather, whether the metal layer can extend to multiple pads, as Plaintiff asserts.[7]

**a. Arguments**

Defendants argue that the specification teaches that a "metalized pad" requires, *inter alia*, an "individual and distinct raised island of metal separated a fixed distance from the other metalized pads." Defendants point to Figure 4A and the accompanying description, which explains that in that figure, "each pad includes a final metal layer 80, such as aluminum, a nitride passivation layer 82, and an under-bump metalization (UBM) layer 84." *See* '264 patent, 7: 4-7. Defendants note the use of the word "each" in the previous sentence, arguing that it shows the inventors intended that there must be an individual and distinct metal component for *each* pad. Similarly, Defendants cite the language in the specification stating that "the center-to-center distance between *each* pad in a row may be about 300 microns," '264 patent, 7: 1-3 (emphasis added), and that "the final metal layer 80 can have an edge-to-edge distance of about 115 microns." *Id.*, 7: 12-13. They also assert that in Figure 4A, final metal layer 80 is depicted as a distinct raised island of metal. Further, Defendants

[6]The parties have not cited to any evidence from the prosecution history in support of their proposed constructions of the term "metalized pad."

[7]In Their Objections and Motion to Strike [Docket No. 592] ("Motion to Strike"), Defendants assert that Dr. Szepesi has offered a new proposed construction in his reply declaration in which he defines a "metalized pad" as a combination of a pad and UBM. Defendants ask that the Court strike these opinions. As stated in a separate order, and for the reasons stated on the record at the Claim Construction hearing, the Motion to Strike is DENIED.

argue that the schematic plan view of the pad shown in Figure 4B depicts "final metal layer 80" of the pad as "distinct from any other 'final metal layer 80' that might form another pad." Defendants argue that their construction is also supported by the fact that while the specification states that "the pads can be shapes other than rectangular and octagonal," '264 patent, 9: 9-10, the only other shape disclosed is the circular pads in Figure 3B. Because the metal layer of the pad is a distinct and individual structure in all of the embodiments described in the specification, Defendants assert, it would be improper to construe the term to allow for a metal layer that extended beyond a single pad.

Plaintiff argues, on the other hand, that while the metal layer is a distinct and individual structure in the preferred embodiments, nothing in the specification limits the term "metalized pads" to structures in which the metal layer is a distinct and individual island of metal. Rather, Plaintiff asserts, the specification refers to metalization layers that carry current from the doped regions to the pads on the surface of the chip. '264 patent, 6: 9-13 ("The IC chip can include two or more metalization layers, e.g., three layers, formed over the semiconductor substrate to carry current from the doped regions to the electrode pads on the surface of the chip"); 6: 22-25 ("A grid-like gate 64 separates each pair of source and drain regions. Unillustrated metalization layers formed over the semiconductor substrate can carry current from the doped regions to the electrode pads on the surface of the chip"); 6: 29-33 ("in one implementation, the PMOS switch includes a regular array of source pads 70 and drain pads 72, with alternating rows of the pads connected by the unillustrated metalization layers to the source regions and the drain regions, respectively, of the distributed transistor), 6: 33-38 ("Similarly, the NMOS switch includes a regular array of source pads 74 and drain pads 76, with alternating rows of pads connected by unillustrated metalization layers to the source regions 60 and drain regions 62, respectively"). One of these metalization layers, Plaintiff asserts, which extend under multiple pads, can be the "final metal layer 80" described in the specification.

Further, Plaintiff argues, the figures do not support Defendants' proposed limitation, contrary to Defendants' assertion. In particular, the figures that show schematic side views of the metalized pad – Figures 2 and 4A – do not limit how far the metal layer under the pad opening might extend beyond the pad opening. Similarly, Figures 3A and 3B show a top-down view of the pads but don't

preclude the final metal layer extending beyond the pad opening. Finally, Plaintiff argues, Figure 4B does not provide any details showing how the pad is connected to the underlying doped regions or to the other pads of the device. In any event, Plaintiff asserts, even if it shows the metal layer of the pad as an individual and distinct structure, Figure 4B is only one embodiment and does not limit the scope of the claim.

Defendants respond that Plaintiff is incorrect in asserting that the metalization layers discussed in the patent can be the final metal layer 80 that is part of the pad. Defendants argue that the part of the specification on which Plaintiff relies, '264 patent column 6, lines 9 - 13, makes clear that the function of the metalization layers is to carry current from the doped regions *to* the electrode pad on the surface of the chip, indicating that the metalization layer cannot itself be part of the metalized pad. *See* Elson Claim Construction Decl., Ex. 1 (Fair Claim Construction Decl.), ¶ 73. Defendants argue that other parts of the specification also distinguish between the pads and the metalization layer. *See* '264 patent, 6: 22-24 ("unillustrated metalization layers . . .carry current from the doped regions to the electrode pads on the surface of the chip"); 6: 29-37 ("row of pads connected by unillustrated metalization layers"). Defendants also argue that while the metalization layers are described in the specification as "unillustrated," the final metal layer shown in Figures 4A and 4B is illustrated. Therefore, Defendants assert, a person of ordinary skill in the art would have understood that the metalization layers cannot themselves be part of the metalized pads. In addition, Defendants argue that Plaintiff's position is inconsistent with the language of claim 26, which refers to an "array of metalized pads," implying an arrangement of distinct objects. *See* Supplemental Declaration of Dr. Richard Fair in Support of Defendants' Supplemental Claim Construction Brief ("Fair Supp. Claim Construction Decl."), ¶ 74.

Plaintiff responds, however, that Defendants are incorrect in asserting that the metalization layer described in the Burstein patents cannot be part of the metalized pad. Plaintiff asserts that Defendants' former expert, Dr. Baker, contradicted this argument when he wrote in his own textbook that if a process has five layers of metal, "then the top layer (just like the top floor in a five-story building) is metal5. Therefore, metal5 is the layer the bonding wire is connected to." *See* Reply Declaration of Jeffrey M. Fisher in Support of Volterra's Reply Claim Construction Brief

("Fisher Reply Decl."), Ex. 23 (excerpt of R. Jacob Baker, *CMOS: Circuit Design, Layout and Simulation* (Second Edition 2005)) at VLTS52279.

Dr. Szepesi also relies on a 1985 text by Sidney Soclof entitled *Analog Integrated Circuits* (Prentice-Hall 1985), citing the following passage:

> The final step in the wafer processing sequence is that of metalization. The purpose of this process is to produce a thin-film metal layer that will serve as the required conductor pattern for the interconnection of various devices and circuit elements on the chip. The metalization pattern is also used to produce metalized areas called bonding pads around the periphery of the chip to provide areas for the bonding of wire leads from the package to the chip.

*See* Fisher Reply Decl., Ex. 38.

Dr. Szepesi argues further that Dr. Fair interprets the specification incorrectly in making the argument that the metalization layers described in the specification are unillustrated whereas metal layer 80 that is part of the metalized pad is illustrated in Figs. 4A & B. He explains that the '264 specification at column 6, lines 8-38, does not show that all of the metalization layers are unillustrated. Instead, Dr. Szepesi reads this description as follows:

> Assuming a 3 metal layer structure, where the third layer, M3, is the top or final metal layer, unillustrated metal layers that carry current from the doped regions to the pads means the first two metal layers, M1 and M2, which indeed are "unillustrated" in the Patents. There is nothing in the text to say that all the metal layers that participate in carrying the current are "unillustrated." The text talks about "unillustrated metal layers" which can mean two or more unillustrated metal layers. The third, top/final metal layer is partially shown in Figure 4A and 4B: the M3 top/final (octagon shaped) metal area under the pad opening is shown, but other metal patterns that may connect to the pad on M3 are unillustrated.

Szepesi Claim Construction Reply Decl., ¶ 32.

In addition, Dr. Szepesi contends that prior art identified by Defendants in their invalidity contentions shows that a person of ordinary skill in the art at the time of the invention would have been aware that the top metal layer that underlies the pad openings may include a large number of metal patterns that provide connections between components of the integrated circuit chip, some of which are connected to the pads. *Id*. (citing Fisher Claim Construction Reply Decl., Ex. 25 (Defendants' Invalidity Contentions) & Ex. 43 at PRIM01925691-716 (showing integrated circuits EL7560 and HIP5020). According to Dr. Szepesi, the metal areas under the pad openings in this prior art was not raised; nor are they "islands." *Id*.

**b. Analysis**

Although neither the claims nor the specification expressly require that each pad include an "individual and distinct raised island of metal," Defendants assert that this limitation must be read into the claim term "metalized pad" based on the claims and specification of the Burstein patents. The Court disagrees.

First, the Court finds Defendants' reliance on claim 26 of the '264 patent, claiming an "array" of metalized pads to be unpersuasive. While the use of the word "array" suggest that each pad is a discrete structure, it is not helpful for determining whether the metal layer that is a component of each metalized pad must be a discrete structure as well. Rather, it is possible that the metalized pads described in the Burstein patents are discrete structures by virtue of the individual opening in the passivation layer that are part of each pad. For the same reason, the Court finds unpersuasive Defendants" reliance on the references in the specification to "each" pad, listed above.

The Court also rejects Defendants' argument that the metalization layers described in the specification do not include final metal layer 80. Rather, the Court finds persuasive Dr. Szepesi's reading of the specification, namely, that it describes both illustrated and unillustrated metalization layers, and while the latter carry current from the doped regions *to* the metalized pads, the former may be the illustrated "final metal layer 80" that is *part of* the metalized pad. *See* Szepesi Claim Construction Reply Decl., ¶ 32 (addressing significance of '264 patent, 6: 8-38). The Court therefore rejects the opinion of Dr. Fair on this issue.

Finally, the Court notes that the extrinsic evidence cited by Dr. Szepesi in his Reply Declaration (cited above) lends further support to the conclusion that a person of ordinary skill in the art would have understood that the final metal layer in the metalized pads claimed in the Burstein patents was not limited to embodiments in which the final metal layer was an individual and distinct raised island of metal for each pad. Rather, a person of ordinary skill in the art knew that a standard pad sometimes extended underneath multiple passivation openings and on that basis would understand that metal layer 80 in the Burstein patents could extend under more than one passivation opening. The Court rejects Defendants' assertion, at oral argument, that this extrinsic evidence should be disregarded because it referred to the standard pads used in wire-bond chips, which the

Burstein patents teach away from. Plaintiff's expert expressly rejected this reading of the Burstein patents, testifying that "there was a pad before [it was] wire bonded, so the pad doesn't include the wire bonding." 1/122/10 Transcript at 119. In other words, the Burstein patents did not reject the plain and ordinary meaning of the term "pad" when they coined the term "metalized pad." Defendants did not point to any evidence to the contrary.

Accordingly, the Court adopts Plaintiff's proposed construction of the term "metalized pad."

**3. "flip-chip type integrated circuit chip"**

| **Claim Term** | **Plaintiff's Proposed Construction** | **Defendants' Proposed Construction** |
|---|---|---|
| flip-chip type integrated circuit chip | An integrated circuit chip that is mounted onto a printed circuit board (PCB) face down, i.e., flipped over, using solder ball or solder bump connections which are only attached to one surface of the die, where the solder balls are under the integrated circuit chip | An integrated circuit chip (a.k.a. a die) oriented such that its external connection points are facing the structure upon which it is being mounted (a.k.a. a flip-chip configuration). |

Claims 9 and 18 of the '522 patent claim a "flip-chip type integrated circuit chip." There are two main differences between the parties' proposed constructions. First, Plaintiff's proposed construction describes the orientation of the flip-chip integrated circuit chip with reference to the printed circuit board, whereas Defendants describe its orientation with reference to the "structure upon which [the chip] is being mounted." Second, Plaintiff includes the limitation "using solder ball or solder bump connections which are only attached to one surface of the die, where the solder balls are under the integrated circuit chip" while Defendants' version does not contain this limitation.

**a. Arguments**

Plaintiff cites to two passages in the '522 specification in support of its proposed construction, arguing that they show that the integrated circuit chip is mounted to the PCB face down, using solder balls or bumps. *See* '522 patent, 2: 16-19 ("[t]he first integrated circuit chip may be mounted on the substrate with an array of solder bumps, and the substrate may be mounted on the printed circuit board with solder balls"); 3: 67-4:1 ("having a first flip-chip type integrated circuit chip mounted

directly on the printed circuit board"). Plaintiff further cites to Figures 2, 3A, 6, 7 and 8A-8G, which it asserts depict the flip-chip in the same manner.

In addition, Plaintiff cites extrinsic evidence in support of its proposed construction. First, it cites to the following definition of "flip-chip" in the McGraw-Hill Dictionary of Electrical and Electronic Engineering:

> A tiny semiconductor die having terminations all on one side in the form of solder pads or bump contacts; after the surface of the chip has been passivated or otherwise treated, it is flipped over for attaching to a matching substrate.

Fisher Claim Construction Decl., Ex. 13 (dictionary excerpt). Second, it cites to an excerpt of a text entitled Device Electronics for Integrated Circuits, produced to Plaintiff by Defendants, which states as follows:

> In some cases the *IC* chips are bonded face down on the substrates so that the metal pads on the *IC* chip are directly above corresponding pads on the ceramic. All leads are then simultaneously bonded by melting pre-formed *solder bumps* on the *IC* pads in what is called *flip-chip* bonding.

*Id*., Ex. 15 (emphasis in original). Finally, Plaintiff cites the deposition testimony of Primarion's corporate witness, Laura Carpenter, who described a flip-chip as follows: "it has some kind of bump ball, stud, usually in some type of an array pattern, but it doesn't have to be, and that when the chip is mounted, it is, quote, flipped with the backside of the silicon facing up and the front side of the silicon facing down towards the board." Fisher Claim Construction Decl., Ex. 14 at 71; *see also* Szepesi Claim Construction Decl., Ex. 1 (Expert Report), ¶ 63 (quoting Carpenter deposition).

Plaintiff rejects Defendants' proposed construction to the extent that it describes a flip-chip integrated circuit chip as "facing the structure upon which it is mounted" rather than facing the printed circuit board. At oral argument, Plaintiff asserted that this construction could encompass tape automated bonding ("TAB") packaging because in that type of packaging the chip is oriented such that its external connection points are facing the lead frame on which it is mounted. *See* Tai Supp. Claim Construction Decl., Ex. A (Fair Depo., 11/20/2009) at 68 (testifying about Figure 6.1 of Lau, which depicts TAB bonding). Such a result runs counter to the specification and the extrinsic evidence, according to Plaintiffs, to the extant that in TAB packaging, the active side of the die faces *away* from the printed circuit board.

Defendants argue that at the time of the invention, "flip-chip" was a common technique for mounting an integrated circuit chip on a structure, in which the external connections of the integrated circuit were oriented such that they faced the structure on which it was being mounted. Defendants cite to United States Patent No. 5,777,383 (the "Stager patent"), which was cited by the Examiner during the prosecution of the '264 patent. Elson Claim Construction Decl., Ex. 11 (Stager patent); *see also* Fisher Claim Construction Decl., Ex. 16 at VLTR00000128 (Prosecution history, citing Stager patent). The Stager patent issued in July 1998 and states, in part, as follows:

> Another well known technique is known as "flip chip", "C4" or "ball grid array" technology which is used as a means of building low cost, high performance, high input/output density assemblies. In these types of assemblies, metal bumps, studs, or balls of metals (collectively referred to herein as "bump-type" interconnections) are usually applied in a two-dimensional array pattern, either directly to the active surface of the semiconductor chip, or alternatively, to an intermediate substrate carrier of the semiconductor. The assembly is made by flipping the active, bumped surface over and then aligning the bumps of the chip with the corresponding pads on a substrate to which the electrical connection is to be made. . . The metal bumps are commonly fabricated of a solder composition that can be mass reflowed in an oven . . . In another variant of the flip-chip method, metal studs or "stud-bumps" are attached to the chip by a wire-bond method . . . . There is also a flip chip assembly method that uses thermo-compression as a method of joining mating gold or aluminum bumps.

Elson Claim Construction Decl., Ex. 11 (Stager patent), 1: 38-67. Defendants also cite to Figure 2 of the Burstein patents, which shows an integrated circuit chip mounted face down on substrate 40.

Defendants challenge Plaintiff's inclusion of the words "mounted on a printed circuit board" in it's proposed construction, arguing that this language excludes Figure 2, in which, according to Defendants, the chip is mounted to the substrate rather than the printed circuit board.[8] Defendants also argue that inclusion of the words "mounted on" in the construction is improper because it repeats the language of some of the claims. For example, claim 9 of the '522 patent claims "a first flip-chip type integrated circuit chip mounted on the printed circuit board." Further, Defendants argue, the construction of this claim term should not depend on what the chip is mounted on.

Defendants also reject Plaintiff's inclusion of the words "using solder ball or solder bump connections . . . where the solder balls are under the integrated circuit chip." Defendants argue that this aspect of Plaintiff's construction should be rejected because it repeats the language of the claims.

[8]This argument turns, in part, on Defendants' contention that the term "mounted on" requires that the chip be *directly* mounted, as discussed below.

For example, dependent claim 3 of the '264 patent claims "[t]he voltage regulator of claim 1, wherein the integrated circuit chip is mounted on the substrate with an array of solder bumps or solder balls." According to Defendants, Plaintiff's proposed construction would render claim 3 superfluous. Defendants also cite to claim 34 of the '264 patent, which claims "[t]he chip of claim 26, wherein the first plurality of pads are connected to a first plurality of solder balls and the second plurality of pads are connected to a second plurality of solder balls interleaved with the first plurality of solder balls across a surface of the chip."

In addition, Defendants assert that a reference to solder balls or bumps in the Court's construction is inappropriate because the term "flip-chip" should not include components that are external to the chip that are used to attach the chip. Dr. Fair notes that the passage in the specification cited by Plaintiff actually supports Defendants' position because the section uses permissive language, stating that "[t]he first integrated circuit chip *may* be mounted on the substrate with an array of solder bumps, and the substrate *may* be mounted on the printed circuit board with solder balls." *See* Elson Claim Construction Decl., Ex. 1 (Fair Claim Construction Decl.), ¶ 81 (citing '522 patent, 2: 16-19). Dr. Fair also rejects the "solder ball" limitation proposed by Volterra on the basis that it was well-known at the time of the invention that some flip-chip integrated circuits were not mounted using solder at all but rather, used gold balls that were bonded to a structure using thermocompression. Fair Supp. Claim Construction Decl., ¶ 88; *see also* Elson Claim Construction Decl., Ex. 11 (Stager patent), 1: 38-67.

Plaintiff responds that claim 3 is not rendered redundant by the inclusion of the "solder bump" language in its proposed construction because that claim refers to an "array" of solder bumps. Thus, Plaintiff argues, the claim describes the arrangement of the solder bumps, which is not addressed in Plaintiff's proposed construction. Plaintiff further asserts that the Stager reference upon which Defendants rely supports Plaintiff's proposed construction in that it makes clear that a flip-chip integrated circuit chip is flipped over so that its active side faces the PCB.

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**b. Analysis**

The Court must resolve two issues. First, it must determine how to characterize the orientation of "flip-chip integrated circuit." Second, it must decide whether the construction should include a limitation requiring that the chip be attached with solder balls or bumps.

On the question of the orientation of the chip, the parties appear to agree that the active side of a "flip-chip integrated circuit chip," as that term is used in the Burstein patents, must face the printed circuit board. Indeed, both the intrinsic and the extrinsic evidence cited by the parties (including the Stager patent cited by Defendants) supports the conclusion that the active face of a flip-chip integrated circuit chip must face the PCB. Nor is it necessary to use the words "mounted on," to which Defendants object, in the construction of the term. Rather, the Court concludes that the orientation can be described as follows: "an integrated circuit chip oriented such that its active side faces the printed circuit board."

Next, the Court addresses whether the construction should include the limitation proposed by Plaintiff, relating to the use of solder balls or bumps to attach the chip. The Court concludes that it should not. First, claims 3 and 34 of the '264 patent indicate that the solder balls are a separate structure that should not be considered part of the flip-chip integrated circuit chip. Although Plaintiff argues that claims 3 and 34 add separate limitations and therefore would not be rendered superfluous by its proposed construction, the Court finds that at least claim 3 does not contain any limitation other than the solder ball attachment and that the word "array" is not sufficient to give rise to a separate limitation.

Looking from the claims to the specification, the Court also finds persuasive Defendants' argument that the use of solder balls or bumps, when discussed in the specification, is described using permissive language. *See, e.g.*, '522 patent, 2: 16-19; 3: 67-4:1.

The extrinsic evidence also indicates that a person of ordinary skill in the art at the time of the invention would have been aware of other methods of attachment, such as the use of

thermocompression to join mating gold or aluminum bumps, as described in the Stager patent.[9] Further, the Stager patent supports Defendants' assertion that even where solder balls are used, they are not *part* of the flip-chip but rather, a separate structure. In particular, in Stager, the patentee describes the use of solder balls that are applied directly to the active surface of the die *or* to an intermediate substrate. *See* Plaintiff's Supplemental Brief at 8 (citing Stager, 1: 42-47).

Finally, the Court does not place great weight on the deposition testimony of Defendant's 30(b)(6) witness, Laura Carpenter, as to the construction of "flip-chip." *See* Szepesi Claim Construction Decl., Ex. 1 (Expert Report), ¶ 63 (quoting Carpenter deposition). There is no indication that Carpenter's testimony reflects the view of a person of ordinary skill in the art at the time of the invention. In any event, Carpenter's description of "flip chip" is not limited to *solder* balls or bumps and therefore does not support Plaintiff's proposed construction.

Therefore, the Court construes the term "flip-chip type integrated circuit chip" as "an integrated circuit chip oriented such that its active side faces the printed circuit board."

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[9]At oral argument, Volterra conceded that the gold balls described in Stager are not solder balls or bumps.

**4. a "first plurality of doped regions" and a "second plurality of doped regions" arranged in an "alternating pattern"**

| Claim Term | Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|---|
| a " first plurality of doped regions" and a "second plurality of doped regions" arranged in an "alternating pattern" | plain and ordinary meaning<br><br>OR<br><br>"doped region": a region where an impurity has been introduced into a substrate which changes the semiconductor's electrical properties.[10] | "doped region": Either p+ regions fabricated in an n-type region where the p+ regions form the source regions (or drain regions) of the transistor, or n+ regions fabricated in a p-type region where the n+ regions form the source regions (or drain regions) of the transistor<br><br>"first plurality of doped regions": A set of two or more sources (or alternatively drains)<br><br>"second plurality of doped regions": A set of two or more drains (or alternatively sources)<br><br>"alternating pattern": Either (i) an "a" "b" "a" "b" pattern of parallel stripes; or (ii) a checkerboard pattern of rectangles.<br><br>Note, this construction is in the context of "a first plurality of doped regions" and "a second plurality of doped regions" arranged in an alternating pattern. E.g., claim 26 states in relevant part "a substrate having a first plurality of doped regions and a second plurality of doped regions, the first and second pluralities of doped regions arranged in a |

[10]In their Motion to Strike, Defendants argue that this is a new construction that should be stricken because it was offered for the first time in Plaintiff's reply brief. As stated above, the Motion to Strike is denied. The Court notes that Defendants have suffered no prejudice as a result of the new proposed construction, especially in light of the lengthy supplemental brief they were permitted to file prior to the hearing.

Claim 26 of the '264 patent and claims 9 and 22 of the '522 patent claim "a substrate having a first plurality of doped regions and a second plurality of doped regions, the first and second pluralities of doped regions arranged in a first alternating pattern." The Court is asked to construe the terms "doped regions," "first plurality of doped regions," "second plurality of doped regions," and "alternating pattern." The primary issue in dispute is whether the "doped regions" should be construed in accordance with the generally accepted definition of doping, that is, as a region of a semiconductor substrate that contains either a p-type or n-type impurity that changes the electrical characteristics of the substrate, or rather, the inventors used the term more narrowly to refer to particular types of doped regions. The parties also dispute whether the term "alternating pattern" is limited to an "a" "b" "a" "b" or checkerboard pattern, as Defendants contend, or rather, whether the term could encompass other configurations.

**a. Doped Regions**

**i. Arguments**

Defendants assert that the term "doped regions" must be construed in light of the specification, which makes clear that this term was intended to mean a certain *type* of doped regions, namely p+ regions in an n-type region and n+ regions in a p-type region. *See* '264 patent, 2: 14-18 ( "[t]he flip-chip type integrated circuit chip may include a p-type region and an n-type region, and the power switch may include a plurality of p+regions fabricated in the n-type region, and a plurality of n+ regions fabricated in the p-type region"); 3: 3-4 ("[t]he first and second pluralities of doped regions may be p+ regions formed in an n-type well or substrate"); 3: 6-8 ("[t]he first and second pluralities of doped regions may be n+regions formed in a p-type well"); 5: 65-6:8 ("[a]s shown in FIG. 3A and 3B, each switch in the switching circuit 16 on IC chip 42 is fabricated as a distributed array of parallel transistors. Each switch includes multiple doped regions arranged to form parallel stripes, and alternating stripes are connected to form source and drain regions of the distributed transistor. Specifically, the NMOS transistor 32 includes alternating stripes of n-doped source regions 60 and drain regions 62 in a p-type well or substrate. The PMOS transistor array 30 will be constructed similarly, with alternating stripes of p-doped source regions and drain regions in an n-type well or substrate"); 6: 14-21 ("[i]n another implementation, as shown in FIG. 3C, the distributed

transistor can be fabricated in a regular array. Specifically, the NMOS transistor 32 includes rectangular n-doped source regions 60 and drain regions 62 laid out in a checkerboard pattern in a p-type well or substrate. The PMOS transistor array 30 will be constructed similarly, with alternating rectangular p-doped source regions and drain regions in an n-type well or substrate").

According to Defendants, these passages indicate that in the context of the Burstein patents, the term "doped regions" refers to the n+/p limitation that structurally describes the doped regions. Thus, Defendants assert, the specification repeatedly equates the n+ regions (or p+ regions) with sources or drains. *See* '264 patent, 5:65 - 6:9 (quoted above), 6: 14-25 (quoted above), FIG.s 3B & C. Dr. Fair offers the following explanation in support of Defendants' construction:

> In my opinion, in the context of the Burstein patents, a person of ordinary skill in the art would have understood the term "doped regions" in the asserted claims to be describing the characteristic alternating pattern of sources and drains of either a PMOS or NMOS transistor, which the patent repeatedly describes as: either p+ regions fabricated in an n-type region where the p+ regions form the source regions (or drain regions) of the transistor, or n+ regions fabricated in a p-type region where the n+ regions form the source regions (or drain regions) of the transistor.

Fair Supp. Claim Construction Decl., ¶ 99.

Defendants also rely on the prosecution history of the Burstein patents in support of their proposed construction.[11] Defendants argue that even though claim 26 (then claim 27) was not amended in response to the Examiner's rejection of all of the original claims, the applicants' amendment to claim 1, limiting the doped regions to a specific kind of transistor structure, also applies to claim 26. In particular, Defendants assert that the applicants made a "global argument" when they asserted that the claims should be allowed based on the "various limitations relating to the layout of the doped regions." *See* Declaration of Vanessa Lefort in Support of Defendants' Opposition to Plaintiffs' Motion for Partial Summary Judgment on Infringement, Ex. 4 ('264 file history) at PRIM 4214.[12] Defendants cite to *ACCO Brands, Inc. v. Micro Security Devices, Inc.*, 346

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[11]In its order denying Plaintiff's request for a preliminary injunction, the Court provided an overview of the prosecution history. Therefore, the Court does not repeat those details here.

[12]The inventors argued that with the amendment to Claim 1, the remaining claims (except original claims 5 and 45, which were canceled) should be allowed because the prior art did not "teach or suggest the various limitations relating to the layout of the doped regions and pads and their connections to the terminals." *Id*. at 4214. The applicants continued, "For example, Hallberg, Stager

F.3d 1075 (Fed. Cir. 2003) in support of their position that the scope of a claim that was not amended may be limited by an amendment to another claim that is worded differently where it is clear that the Examiner and the applicants understood that the limitation would extend to all the claims.

Plaintiff argues that the term "doped regions" should be given its "plain and ordinary meaning," which Plaintiff asserts is "a region where an impurity has been introduced into a substrate which changes the semiconductor's electrical properties." *See* Szepesi Claim Construction Reply Decl., ¶ 45. Plaintiff cites to the testimony of both experts in support of this proposed construction. In particular, Dr. Szepesi states that "[t]he plain and ordinary meaning of 'doped region,' as it is generally understood by [a person of ordinary skill in the art ], is a region where an impurity has been introduced into a semiconductor substrate which changes the semiconductor's electrical properties." *Id*. Similarly, Dr. Fair states in the background section of his expert report that "[d]oping is the process of intentionally introducing impurities into a semiconductor substrate to change the semiconductor's electrical properties." Elson Claim Construction Decl., Ex. 1 (Fair Claim Construction Decl.), ¶ 32. Plaintiff asserts that Defendants' proposed construction, limiting the doped regions to either p+ regions fabricated in an n-type region or n+ regions fabricated in a p-type region, is an improper attempt to import features of the preferred embodiments described in the specification into the claims.

Plaintiff points to the claims themselves in support of its proposed construction. In particular, Plaintiff notes that nothing in issued claim 26 of the '264 patent requires that doped regions are limited to p+ regions fabricated in an n-type region or n+ regions fabricated in a p-type region. Further, to the extent these requirements are added in dependent claims 30 and 32, Plaintiff asserts, Defendants' proposed construction would render these claims superfluous.[13] Plaintiff also rejects Defendants' characterization of the prosecution history of the '264 patent and particularly,

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and Honn do not teach doped regions in an array with alternating regions of the array connected to different terminals, an array of pads with two pluralities of pads arranged in an alternating pattern and electrically connected to two doped regions, or two electrodes having interdigited fingers." *Id*.

[13]Claim 30 recites: "The chip of claim 26, wherein the first and second pluralities of doped regions are p+ regions formed in an n-type well or substrate. Claim 32 recites: "The chip of claim 26, wherein the first and second pluralities of doped regions are n+ regions formed in a p-type well or substrate."

Defendants' assertion that the amendment to claim 1 in response to the Examiner's rejection also limits the scope of the term "doped region" in issued claim 26. Plaintiff points out that after the Examiner rejected the original claims of the '264 patent, the applicants specifically recounted the elements of both claim 1 and issued claim 26 in their response to the office action, stating as follows:

> Claim 1 calls for a flip-chip type integrated circuit chip that includes a power switch to alternately couple and decouple the input terminal to the output terminal. The chip includes a p-type region and an n-type region, and the first power switch includes a plurality of p+ regions fabricated in the n-type region in a first array, and a plurality of n+ regions fabricated in the p-type region in a second array, and wherein alternating p+ regions are conected to the input terminal and to an intermediate terminal, and alternating n+ regions [of the] chip are connected to the intermediate terminal and to ground.
>
> Claim 27 [issued claim 26] calls for a substrate having a first plurality of doped regions and a second plurality of doped regions and an array of metalized pads fabricated on a surface of the substrate. The first and second pluralities of doped regions are arranged in a first alternating pattern. The array of pads includes a first plurality of pads and a second plurality of pads arranged in a second alternating pattern. The first plurality of pads are electrically connected to the first plurality of doped regions, the second plurality of pads are electrically connected to the second plurality of doped regions, the first plurality of pads are connected to a first terminal of the voltage regulator, and the second plurality of pads are connected to a second terminal in the voltage regulator.

Fisher Decl., Ex. 16 at VLTR 00000134. Further, after the Examiner responded with a Notice of Allowability, the Applicants filed "Comments on Statement for Reasons for Allowance," stating as follows:

> Independent claims 27, 36, 44 do not require all of the elements recited by the Examiner in the Statements of Reasons for Allowance.

*Id*. at VLTR 143.

**ii. Analysis**

The Court finds that Defendants' proposed construction of "doped regions" impermissibly imports limitations from the specification based on the preferred embodiments. Instead, the Court construes the term "doped region" as "a region where an impurity has been introduced into a substrate which changes the semiconductor's electrical properties."

First, nothing in the language of the claims points toward the conclusion that the term "doped regions" should be limited to either p+ regions fabricated in an n-type region or n+ regions fabricated in a p-type region. To the contrary, claims 30 and 32, which depend from claim 26 of the '264

patent, add this limitation. These claims would be rendered superfluous if the Court were to adopt Defendants' proposed construction.

Second, although all of the preferred embodiments described in the specification are consistent with Defendants' proposed construction, the language cited by Defendants is permissive. *See, e.g.,* '264 patent, 2: 14-18 ( "[t]he flip-chip type integrated circuit chip *may* include a p-type region and an n-type region, and the power switch may include a plurality of p+regions fabricated in the n-type region, and a plurality of n+ regions fabricated in the p-type region"); 3: 3-4 ("[t]he first and second pluralities of doped regions *may* be p+ regions formed in an n-type well or substrate"); 3: 6-8 ("[t]he first and second pluralities of doped regions *may* be n+regions formed in a p-type well"); 6: 14-21 ("[i]n another implementation, as shown in FIG. 3C, the distributed transistor *can* be fabricated in a regular array").

Third, Defendants mischaracterize the prosecution history. The communications between the applicants and the Examiner quoted above make clear that the applicants did not disavow a construction of "doped regions" that covers embodiments in which p+ and n+ regions are not bounded by the opposite type of doping. To the contrary, the applicants distinguished between original claim 1 and original claim 27 when they amended claim 1 in response to the Examiner's rejection. Nor does *ACCO Brands*, cited by Defendants, stand for a contrary result. In that case, the Federal Circuit held that a limitation added to one of the original claims following rejection by the Examiner also applied to another claim that had been rejected, even though the latter claim was not amended, because it was "clear that the examiner and the applicant understood" that the limitation applied to both. 346 F.3d at 1079. In light of the prosecution history cited above, the Court concludes that in this case there was no such understanding on the part of the applicants in this case.

Therefore, the Court adopts Plaintiff's proposed construction of "doped regions."

**b. Alternating Pattern**

**i. Arguments**

Plaintiff asserts that there is no basis to limit the term "alternating pattern" to the two embodiments described in the specification, that is, either a checkerboard pattern of rectangles or an "a" "b" "a" "b" pattern of alternating stripes. Further, at oral argument, Plaintiff argued that the

words "of parallel stripes" and "of rectangles" in Defendants' proposed construction added limitations that are not supported by the specification. Plaintiff does not, however, offer an alternative construction, asserting instead that the term is not technical and would be understood by a jury without the assistance of the court.

Defendants assert that the term alternating pattern requires construction, pointing to Dr. Szepesi's recent deposition testimony that an "a" "b" pattern, by itself, might be an alternating pattern. *See* Elson Supp. Claim Construction Decl., Ex. 43 (Szepesi Depo., 11/24/09) at 595.[14] According to Defendants, Plaintiff has refused to pin itself down as to this term, adopting new meanings as the case evolves. Defendants argue that to the extent Plaintiff's expert previously stipulated that he was prepared to accept that the term "alternating pattern" was limited to the two variants described above, Plaintiff's should not now be permitted to argue that the term might encompass other arrangements. *See* Motion to Strike at 11.

**ii. Analysis**

The Court concludes that this claim term requires construction. Although the words themselves are not highly technical, the scope of the term, as used in the Burstein patents, is not obvious. This is evident from Dr. Szepesi's own uncertainty in his recent deposition as to the scope of the term. Although Defendants' proposed construction limits the term to the preferred embodiments, the Court adopts that construction, for the most part, because Plaintiff has not offered its own construction as an alternative. However, the Court omits the words "of parallel stripes" and "of rectangles" on the basis that Defendants have not cited to intrinsic or extrinsic evidence indicating that the patentees intended the term "alternating pattern" to include these particular limitations. Therefore, the Court construes "alternating pattern" as follows: "Either (i) an 'a' 'b' 'a' 'b' pattern; or (ii) a checkerboard pattern."

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[14]At oral argument, Plaintiff stipulated that an "a" "b" pattern does not satisfy the "alternating pattern" limitation.

**5. "substrate"**

| Claim Term | Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|---|
| substrate | plain and ordinary meaning<br><br>OR<br><br>semiconductor substrate | Definition 1:<br><br>The base layer of an integrated circuit chip that contains the doped regions, and above which are deposited additional layers, such as metal and insulators, to form the whole integrated circuit chip.<br><br>Definition 2:<br><br>A planar structure disposed between the integrated circuit chip and the printed circuit board that includes a first signal layer on the top surface facing the integrated circuit chip, and a second signal layer on the bottom surface facing the printed circuit board. |

Claim 26 of the '264 patent and claims 9 and 22 of the '522 patent claim an integrated circuit chip that includes a "substrate." While Defendants offer alternate definitions of the word "substrate" as used in the specification, depending on whether the term is used in connection with integrated circuits or packaging, only the former relates to the term as it is used in the asserted claims. Plaintiff initially asserted that the term "substrate" should be given its "plain and ordinary meaning." In the reply declaration of its expert, however, Dr. Szepesi stated that the term "substrate," as used in the asserted claims, means "semiconductor substrate." *See* Szepesi Claim Construction Reply Decl., ¶ 12; *see also* Declaration of David Dolkas in Support of Defendants' Objections and Motion to Strike New Claim Constructions and Evidence in Plaintiff's Reply Claim Construction Papers ("Dolkas Motion to Strike Decl."), Ex. E (Szepesi Depo., 11/24/09) at 685-686. The dispute as to this term revolves around Defendants' assertion that the term is limited to the "base layer" of the chip where the dopant is deposited, as distinct from the additional layers, such as metal and insulators, that are deposited over this base layer to form the chip.

**a. Arguments**

Defendants argues that the claims, specification and extrinsic evidence all support their proposed construction. *See* Elson Claim Construction Decl., Ex. 1 (Fair Claim Construction Decl.), ¶¶ 131-145. First, Dr. Fair points to claim 26 of the '264 patent, which claims "a substrate having a first plurality of doped regions and a second plurality of doped regions." According to Dr. Fair, this language supports Defendants' proposed construction because the doped regions are diffused only into the bottom layer of the chip. Dr. Fair also cites to claim 34 of the '264 patent, which claims "solder balls across a surface of a chip," in support of Defendants' position that the inventors knew how to distinguish between "a surface of the chip" and "a surface of a substrate." *Id.*, ¶ 119.

Second, Dr. Fair points to language in the specification indicating that the substrate is the layer that contains the doped regions. *See, e.g.,* '264 patent, 3: 3-8 ("the first and second pluralities of doped regions may be p+ regions formed in an n-type well or substrate . . . The first and second pluralities of doped regions may be n+ regions formed in a p-type well or substrate"); 6: 3-8 ("Specifically, the NMOS transistor 32 includes alternating stripes of n-doped source regions 60 and drain regions 62 in a p-type well or substrate"). In addition, Dr. Fair asserts, the inventors used different language in the specification when referring to the base layer of the chip containing the diffused source and drain regions, as opposed to "structures on the overall chip including the multiple layers above the substrate." Elson Claim Construction Decl., Ex. 1 (Fair Claim Construction Decl.), ¶ 135. In particular, as to the former, Dr. Fair asserts, the inventors referred to the "semiconductor substrate" whereas the inventors referred to the latter as "the surface of the chip." *See, e.g.,* '264 patent, 6: 9-13 ("The IC chip can include two or more metalization layers, e.g., three layers, formed over the semiconductor substrate to carry current from the doped regions to the electrode pads on the surface of the chip"); 6: 22-23 ("Unillustrated metalization layers formed over the semiconductor substrate can carry current from the doped regions to the electrode pads on the surface of the chip"); 6: 26-28 ("As shown in FIG. 3A, on the surface of the chip, overlying the buried array of distributed transistors, is an array of drain pads and source pads").

Defendants also note in their responsive claim construction brief that the Summary of the Burstein patents states that "[t]he chip includes a substrate having a first plurality of doped regions

and a second plurality of doped regions and an array of metalized pads on a surface of the substrate." Defendants' Responsive Brief at 16 (citing '264 patent, 2: 54-55). Defendants do not explain why they are taking the position, contrary to the opinion expressed by their former expert, that this statement *supports* Defendants' proposed construction. *See* Baker Expert Report, ¶ 65 (stating that this language was inconsistent with Defendants' proposed construction).

Third, Dr. Fair asserts that the extrinsic evidence supports his construction. Specifically, he cites a textbook which includes a figure depicting an integrated circuit in cross-section, with the bottom layer labeled "p-substrate." Elson Claim Construction Decl., Ex. 1 (Fair Claim Construction Decl.), ¶ 138 (citing Elson Claim Construction Decl., Ex. 15 at PRIM00000178 (R. Jacob Baker et al.,CMOS Circuit Design, Layout, and Simulation (1998)). He also cites one of several definitions of "substrate" in the IEEE Standard Dictionary of Electrical and Electronic Terms (6th Ed. 1996), which states as follows:

> **substrate (1) (integrated circuit)** The supporting material upon or within which an integrated circuit is fabricated or to which an integrated circuit is attached.

Elson Claim Construction Decl., Ex. 20 at PRIMC00000197.

Plaintiff challenges Defendants' proposed construction on the grounds that it contains unnecessary and confusing limitations. In particular, Volterra argues that the reference to additional layers that do *not* constitute part of the substrate would confuse a jury. Plaintiff also argues that the reference from the Summary cited above, describing "metalized pads fabricated on a surface of the substrate," is inconsistent with Defendants' proposed construction. If the Court were to adopt Defendants' proposed construction, Plaintiff asserts, it would read out *all* of the embodiments of the patents because no embodiments are disclosed in which metalized pads are directly on the base layer of the substrate. Plaintiff cites to the deposition testimony of Dr. Fair in support of its position, noting that Dr. Fair testified that a person of ordinary skill in the art would have understood that the metalization of the metalized pads would be accomplished through an "intermediate metal layer." *See* Tai Supp. Claim Construction Decl.," Ex. A (Fair Depo., 11/20/2009) at 156. According to Plaintiff, this testimony amounts to an admission that the metalized pads cannot be "fabricated on a surface of the substrate," as described in the Summary, if Defendants' proposed construction is

adopted.

Defendants respond that this passage actually supports their proposed construction because the phrase "surface of the substrate" refers to the outermost boundary of the substrate. *See* Defendants' Supp. Claim Construction Brief at 41-42. Defendants further assert that their proposed construction does not read out all of the embodiments of the patent. Rather, Defendants assert, the description in the Summary reveals an embodiment in which the metalized pads are fabricated directly on the base layer of the chip. Even if this results in a non-functioning device, Defendants assert, the Court has no choice but to accept Defendants' construction because it must construe the claims as written.

**b. Analysis**

In its preliminary injunction order, the Court tentatively concluded that Defendants' proposed construction improperly limited the term "substrate," relying, in part, on the language in the Summary, discussed above. In particular, the Court found that if it were to adopt Defendants' position, it would exclude all of the embodiments in the patents because it is undisputed that a person of ordinary skill in the art would understand that the metalized pads could not be directly on the base layer of the integrated circuit if the device was to function. The Court now confirms that Defendants' proposed construction is incorrect.

Defendants' assertion that the Court must adopt its proposed construction because it is required to construe the claims "as written" turns claim construction on its head. The role of the Court is to determine what the claim term means in light of the language of the claims, the specification, and, when appropriate, the extrinsic evidence. Here, the Court concludes that the claims and specification do not support Defendants' construction and therefore, the Court does not look to the extrinsic evidence.

First, the Court notes that Defendants propose a construction of "substrate" that includes other limitations of claim 26. Specifically, Defendants argue that the term "substrate" must refer to the layer of the chip that includes the doped regions. Yet claim 26 of the '264 patent, and claims 9 and 22 of the '522 patents all include separate claim terms limiting the substrates to ones that include doped regions. Thus, the claims themselves indicate that the term "substrate," on its own, should not

be limited to those with doped regions.

Second, while the specification often describes substrates that contain doped regions, it also uses the term more broadly, for example, in the Summary of invention discussed above. Contrary to Defendants' argument that this description discloses a separate embodiment of the invention – albeit non-functioning – the Court finds that this description shows that Defendants' proposed construction of the term "substrate" is improperly narrow.

Having reached this conclusion, the Court turns to Plaintiff's assertion that this claim term need not be construed but instead, should be given its plain and ordinary meaning, that is, "semiconductor substrate." This construction appears to be correct, as far as it goes. In particular, the Court notes that Defendants' expert himself pointed out that the inventors, when referring to the type of substrate that is at issue here, used the term "semiconductor substrate" consistently throughout the specification. *See* Elson Claim Construction Decl., Ex. 1 (Fair Claim Construction Decl.), ¶135 (citing '264 patent, 6: 9-13, 6: 22-25, 6: 26-28). The Court is concerned, however, that this construction does not offer sufficient guidance to a jury to the extent that it assumes an understanding of technical terms that are themselves subject to dispute. Indeed, Defendants' expert argues that the term "semiconductor substrate" refers only to the base layer of the chip while Plaintiff's expert appears to take the position that this term to sweep more broadly.

The Court construes the term "substrate" as follows: "The supporting material upon or within which an integrated circuit is fabricated or to which an integrated circuit is attached."[15]

[15]As the Court noted at oral argument, construction of the term "substrate" does not necessarily resolve what appears to be the real dispute between the parties, namely, what does the term "on the surface of" the substrate mean. Because this claim term was not included in the terms identified by the parties to be construed, and because it was not fully addressed by the experts or the parties, the Court declines to construe that term here.

**6. "mounted on"**

| Claim Term | Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|---|
| mounted on | plain and ordinary meaning<br><br>OR<br><br>One item is securely fixed to the other item and is provided support by the upper surface of the other item[16] | directly placed and soldered onto. |

Claim 9 of the '522 patent claims a voltage regulator that includes a flip-chip integrated circuit chip "mounted on" the printed circuit board. The parties' dispute turns on the word "directly" in Defendants' proposed construction.

**i. Arguments**

In support of their construction of the claim term "mounted on," Defendants point to the claims of the '264 patent, arguing that they describe two mounting options – a preferred embodiment in which the chip is mounted onto a substrate, which is then mounted onto the printed circuit board (depicted in Figure 2) (hereinafter, "Option 1"), and an alternative embodiment in which the chip is mounted directly on a printed circuit board (depicted in Figure 9) (hereinafter, "Option 2"). Elson Claim Construction Decl., Ex. 1 (Fair Claim Construction Decl.), ¶ 151. According to Dr. Fair, the two mounting options can be seen in claims 18, 19, 21 and 22 of the '264 patent. *Id*., ¶ 148. Those claims provide as follows:

> Claim 18: The voltage regulator of claim 17, wherein the inductor is mounted on the substrate.
>
> Claim 19: The voltage regulator of claim 17, wherein the inductor is mounted on the printed circuit board.
>
> Claim 21: The voltage regulator or claim 20, wherein the capacitor is mounted on the substrate.

[16]In their Motion to Strike, Defendants object to this new proposed construction, which they have asked the Court to strike on the basis that it was offered untimely. As stated above, that motion is denied.

> Claim 22: The voltage regulator or claim 20, wherein the capacitor is mounted on the printed circuit board.

Dr. Fair reasons that claims 18 and 21 correspond to Option 1, while claims 19 and 22 correspond to Option 2. *Id*., ¶ 148. He asserts that if the term "mounted on" encompassed both direct and indirect mounting, claims 19 and 22 would be superfluous. *Id*., ¶ 149.

Dr. Fair also cites to the specification of the patents in support of his construction, noting that the Abstract, as well as the majority of the specification, describes the preferred embodiment depicted in Figure 2, in which the chip is mounted on a substrate and the substrate is then mounted on the printed circuit board. *Id*., ¶ 150. According to Dr. Fair, when the applicants meant to refer to the combination of the integrated circuit chip and the substrate, they referred to it as a "package." *Id*., ¶ 152 (quoting '264 patent, 5: 47-50, stating in reference to Figure 2 that "the switching circuit 16 can be fabricated in a flip-chip package 40 that includes an integrated circuit chip 42 and a substrate 44. The flip-chip package 40 is attached to a printed circuit board (PCB) 46 . . . "). Dr. Fair further notes that when the applicants described mounting Option 2, used in the alternative embodiment, they explained that the chip was to be mounted "directly on" the printed circuit board. *Id*., ¶ 153. In particular, he points out that Option 2 is depicted in Figures 8A-G, which are described as follows:

> In another implementation, the integrated circuit chip 42" may be *mounted directly on* a printed circuit board. As shown in FIGs. 8A-8G, the printed circuit board may have an input voltage electrode '90, a ground electrode 92', and an intermediate voltage electrode 94'.

*Id*. (quoting '264 patent, 8:15-19) (emphasis added in Fair Decl.). Elsewhere in the specification, Figures 8A-8G are described as follows:

> FIGS. 8A-8G are schematic plan views of several configurations for the drain and source pads and the overlying electrodes *to enable direct mounting of a flip chip to a printed circuit board*.

*Id*. (quoting '264 patent, 4: 43-46). Thus, based on the claims and specification of the two patents, Dr. Fair concludes that one of ordinary skill in the art would have understood that "claim 9 of the '522 patent claims this alternate embodiment described and illustrated in the specification whereby the flip-chip type integrated circuit is directly placed and soldered onto the printed circuit board, ie., without any intervening packaging, such as a substrate." *Id*., ¶ 158.

Dr. Fair also cites to dictionary definitions of "mounted" and "on" in support of Defendants' proposed construction. In particular, he cites the American Heritage Dictionary (1982), which includes as a definition of "mount" "to fix securely to a support." Elson Claim Construction Decl., Ex. 39 at PRIMC00001351. Dr. Fair also cites Websters' Third New International Dictionary (1993), which includes among its definitions of "mount" "to attach to a support or assemble for use." *Id*., Ex. 27 at PRIM01946873. Finally, Dr. Fair points to the definition of "on" found in Websters' Third New International Dictionary, that is, "in or into the position of being in contact with the upper surface of something or of being supported from beneath by the upper surface." *Id*. at PRIMC00001353.

Volterra argues that Defendants are attempting to read into claim 9 a limitation that does not exist in arguing that the term "mounted on" requires a *direct* connection to the PCB. Szepesi Claim Construction Decl., Ex. 5 (SJ Rebuttal Expert Report) at ¶¶ 81-86; Szepesi Claim Construction Reply Decl., ¶¶ 36-38. Rather, Plaintiff asserts, the patents clearly envision two embodiments, one in which the chip is mounted to a substrate and one in which it is mounted to the printed circuit board, and the words "mounted on" can cover either. Volterra argues that when the patentees described in the specification embodiments that required that the chip be mounted *directly* on the PCB, they were limiting what they were describing to the latter type of embodiment. *Id*. Volterra also points out that one of the original claims in the application, original claim 45, claimed a "first flip-chip type integrated circuit chip mounted *directly* on the printed circuit board," indicating that the patentees used this phrase when they wanted to limit the term "mounted on" to an embodiment in which the chip is mounted directly on the PCB. In addition, Volterra argues that Defendants' proposed construction should be rejected because it excludes the preferred embodiment, which is rarely correct.

Plaintiff rejects the argument of Defendants' expert that claims 19 and 22 would be superfluous unless Defendants' construction is adopted. Rather, Volterra asserts, claims 18 and 21 require that the chips be mounted to a substrate in order to mount them to printed circuit boards whereas claims 19 and 22 do not *require* that a substrate be used. In other words, Volterra asserts, the claims simply differ in scope. In addition, Volterra argues that Defendants' proposed construction should be rejected because it excludes the preferred embodiment described in the

specification, which is rarely correct. Volterra also asserts that the dictionary definitions proffered by Defendants, quoted above, actually support Plaintiff's position. In particular, Plaintiff points out that the dictionary definition of "on" is broad enough to encompass use of an intervening structure, such as a lead frame, to the extent that it includes "being supported from beneath by the upper surface" without requiring direct contact. Dr. Szepesi relies on this dictionary definition in support of his own proposed construction, set forth in his Reply declaration. *See* Szepesi Claim Construction Reply Decl., ¶ 38.

Defendants respond that Plaintiff's reliance on original claim 45 is misplaced because there is nothing in the prosecution history that indicates why the inventors cancelled the claim.

**ii. Analysis**

In its preliminary injunction order, the Court tentatively concluded that Defendants' proposed construction improperly limited the term "mounted on." Having considered the parties' claim construction submissions addressing this question, the Court is persuaded that its conclusion was correct. The Court finds that neither the claims nor the specification require that the term "mounted on" be construed to impose a requirement that the chip be "directly placed and soldered onto" the PCB. In particular, the Court rejects Defendants' assertion that claims 19 and 22 are superfluous without such a limitation. Rather, these claims simply have a broader scope than the claims that immediately precede them. Further, the Court declines to adopt this limitation because it would exclude the preferred embodiment. In addition, the Court finds that the dictionary definitions cited by Defendants do not support their position. Instead, they support Plaintiff's assertion that the term "mounted on" does not require direct contact.

The Court construes "mounted on" as follows: "supported by and securely fixed, either directly or indirectly, to the other surface."

### 7. "maintain the DC voltage substantially constant"

| Claim Term | Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|---|
| maintain the DC voltage substantially constant | plain and ordinary meaning<br>OR<br>maintain the output voltage within well-defined tolerance limits in the face of changing input voltage and load for a substantial period of time, where a substantial period of time is a period of time which is substantial relative to the switching period of the switching regulator[17] | to maintain a fixed and stable output voltage. |

Claim 9 of the '522 patent claims a voltage regulator that includes "a filter disposed to provide a substantially DC voltage at the output terminal" and "a control circuit connected to the gate region to control the power switch to maintain the DC voltage substantially constant." The primary dispute between the parties turns on Defendants' inclusion of the word "fixed" in their proposed construction, which is based on their contention that the voltage regulators disclosed in the Burstein patents were "static" rather than "dynamic" voltage regulators.

#### i. Arguments

In support of their proposed construction, Defendants' expert states that a person of ordinary skill in the art would have understood that this claim language referred to a traditional "static" voltage regulator, designed to maintain an output DC voltage that is fixed and stable. Elson Claim Construction Decl., Ex. 1 (Fair Claim Construction Decl.), ¶ 160. Dr. Fair asserts that the specification supports his construction. *See id*. (citing '264 patent, 1: 9-10 ("voltage regulators . . .are used to provide *stable* voltage sources for electronic systems"), 2: 5-8 ("a filter is disposed to provide

[17]This proposed construction comes from Dr. Szepeszi's Reply Claim Construction Decl., ¶ 27 and Dr. Szepesi's testimony at his recent deposition. *See* Elson Supp. Claim Construction Decl., Ex. 43 (Szepesi Depo.) at 679. In their Motion to Strike, Defendants object to Plaintiff's new proposed construction as untimely. As stated above and in a separate order, the Court denies the motion.

*a substantially DC voltage* at the output terminal, and a control circuit controls the power switch to maintain the DC voltage substantially constant"); 5: 20-33 ("the output filter 26 converts the rectangular waveform of the intermediate voltage at the intermediate terminal into a *substantially DC output voltage*"); 5: 38-46 ("[t]he output voltage is regulated, or *maintained at a substantially constant level*, by a feedback loop in the controller assembly . . . . The measured voltage and current are used to control the pulse modulator 18 so that the output voltage at the output terminal *remains* substantially constant") (emphasis added in Fair Decl.)).

Dr. Fair further opines that the Burstein patents include no written description to support or enable the concept of a voltage regulator that is designed to change its output voltage upon command. *Id*., ¶ 166. Defendants point to Dr. Szepesi's deposition testimony on this issue. *Id*. In particular, when asked whether there was "any disclosure in the Burstein patents that would teach one of ordinary skill in the art how to either adjust the output voltage or dynamically change the output voltage," Dr. Szepesi responded, "[n]ot in any particular way, no." Fisher Claim Construction Decl., Ex. 9 (Szepesi Depo., 9/17/09) at 314.

Dr. Fair also cites to extrinsic evidence in support of Defendants' proposed construction. First, Dr. Fair notes that the distinction between "static" and "dynamic" voltage regulators was highlighted in the dissertation of Volterra's founder, Dr. Anthony Stratakos, in which Dr. Stratakos states as follows:

> To dynamically trade performance for decreased energy consumption at system run-time, a new type of DC-DC converter, called a *dynamic DC-DC converter* or *tracking converter*, is required. A dynamic DC-DC converter is quite different from a conventional static DC-DC converter. Whereas a static DC-DC converter must maintain a substantially DC output, a dynamic DC-DC converter must be capable of rapidly slewing its output.

Elson Claim Construction Decl., Ex. 1 (Fair Claim Construction Decl.), ¶ 164 (quoting Elson Claim Construction Decl., Ex. 22 (*High-Efficiency Low-Voltage DC-DC Conversion for Portable Applications*, Anthony Stratakos, University of California, Berkeley, Fall 1998) ("Stratakos Dissertation") at PRIM 1387).

Second, Dr. Fair points to Dr. Szepesi's deposition testimony that a person of ordinary skill in the art would understand that a substantially constant output voltage for a switching voltage regulator

would stay within 5% of the (nominal) target output voltage. *Id*., ¶ 161 (citing Elson Claim Construction Decl., Ex. 22 (Szepesi Depo., 7/30/09) at 234:10-20).

Third, Dr. Fair cites the McGraw-Hill Electronic Dictionary, Fifth Edition (1994), which defines a voltage regulator as follows:

> A circuit that includes a sensor capable of monitoring the load and restoring the output voltage to close tolerance limits despite changes in both the load and input voltage. This circuitry is now available in low-cost integrated circuits capable of holding DC output voltage levels of 3 to 30 V constant within +2%.

*Id*., ¶ 163 (quoting Elson Claim Construction Decl., Ex. 21 at PRIMC202).

Finally, Dr. Fair explains that his position applies not only to the claim term that is before the Court for construction but also the terms "voltage regulator" and "substantially DC voltage at the output terminal." *Id*., ¶ 172. Thus, according to Dr. Fair, a "voltage regulator," as used in the Burstein patents, is a "device that maintains a fixed and stable output." *Id*. Similarly, the claim term "substantially DC voltage at the output terminal" means, according to Dr. Fair, "a fixed and stable output voltage." *Id*.

Volterra's expert rejects Dr. Fair's construction of these phrases, asserting that there is no basis for the requirement that the DC current be "fixed," either in the patent or in the extrinsic evidence. Szepesi Claim Construction Decl., Ex. 5 (SJ Rebuttal Expert Report), ¶¶ 4-35; Szepesi Claim Construction Reply Decl., ¶¶ 19- 28. According to Dr. Szepsi, it was well-known in the prior art that voltage regulators included both fixed and adjustable types. Szepesi Claim Construction Decl., Ex. 5 (SJ Rebuttal Expert Report), ¶ 7. He defines "fixed voltage regulator" as "one that can only operate with a single fixed regulated substantially constant output voltage." *Id.* An "adjustable voltage regulator," on the other hand, "is capable of operating with a wide range of regulated substantially constant output voltages." *Id*. (citing Horowitz-Hill: The Art of Electronics (Second Edition), Cambridge University Press, 1989). It was well-known in the art, according to Dr. Szepesi, that in the latter type of voltage regulator, the value of the output voltage could be changed by the user to a target nominal value in a variety of ways. *Id*., ¶¶ 7-8. Once the target value was achieved, however, the adjustable voltage regulators, like the fixed voltage regulators, held the output voltage "substantially constant, with[in] a certain tolerance . . . for long periods of time" *Id*., ¶¶ 7, 11.

Dr. Szepesi points to the MAX749 switching voltage regulator as an example of an adjustable switching voltage regulator in the prior art. *Id*., ¶ 11. This device, manufactured by Maxim Integrated Products, Inc., with a datasheet date of 1995, allowed the output voltage of the regulator to be digitally adjusted in a wide range, providing a regulated substantially constant output voltage, before and after the output voltage was changed by digital command. *Id*. Dr. Szepesi opines, "there would be no reason for someone with ordinary skill in the art to exclude these types of prior art voltage regulators from the scope of the Burstein patents nor do I see any evidence that this was intended by the Burstein patents." *Id*.

Dr. Szepesi rejects Defendants' reliance on the Stratakos Dissertation in support of their proposed construction. Szepesi Claim Construction Reply Decl., ¶ 22. First, Dr. Szepesi states that he is unaware of any prior art in which the terms "static" and "dynamic" were used to describe voltage regulators.[18] *Id*. More importantly, even assuming the distinction was accepted, Dr. Szepesi takes the position that the Stratakos Dissertation makes clear that the function of both static and dynamic voltage regulators is to "maintain a substantially constant output voltage," as claimed in the Burstein patents. *Id*. Dr. Szepesi explains his conclusion as follows:

> . . .Dr. Fair's reliance on the Stratakos PhD Thesis to support [Defendants'] flawed definition of the terms is . . .incorrect and lacks basis. This is readily obvious looking at the often quoted paragraph that they use for support:
>
> > To dynamically trade performance for decreased energy consumption at system run-time, a new type of DC-DC converter, called a *dynamic DCDC converter* or *tracking converter*, is required. A dynamic DC-DC converter is quite different from a conventional static DC-DC converter. Whereas a static DC-DC converter must maintain a substantially DC output, **a dynamic DC-DC converter must be capable of rapidly slewing its output.** (emphasis add) [BR2 at #146, pp. 66-67; FD1 at #164, p. 173]
>
> The "dynamic" DC-DC converter of the Stratakos Thesis "must be capable of rapidly slewing its output," when their target output voltage is changed (typically by a digital code). However, they are still DC-DC converters, meaning that the input voltage and output voltage are DC. After the "slewing" is completed these "dynamic" voltage regulators maintain a DC regulated i.e. substantially constant output voltage, which is why they are called DC-DC converters. . . Hence, a DC-DC converter circuit [] that corresponds to the circuit described in the Stratakos PhD Thesis above (whether it is "dynamic" or "static," as long as it is a DC-DC converter), converts a DC input voltage to a DC output voltage at a different level. DC output

[18]Volterra takes the position that the Stratakos Dissertation is not prior art. The Court has not decided this issue and need not do so here because even if it were prior art, the Court's conclusions would be the same.

> voltage means an output voltage that essentially does not change its value (or if it does the change is so small that it may be neglected), i.e., substantially constant. In fact, I note that Dr. Stratakos' PhD Thesis also states that dynamic voltage converters "must maintain substantially DC output voltage" and that "[b]etween voltage adaptations, the converter maintains a precisely regulated DC output voltage." Fisher [Claim Construction] Decl., Ex. 21 at 126 & 127 (emphasis added).

*Id*.

Dr. Szepesi opines that the dictionary definitions previously cited by both Plaintiff and Defendants, as well as a third dictionary definition, also support his position. As noted above, Defendants' expert cited the 1994 McGraw-Hill Electronic Dictionary, which defines a voltage regulator as "a circuit that includes a sensor capable of monitoring the load and restoring the output voltage to close tolerance limits despite changes in both the load and input voltages." *Id*., ¶ 24 (quoting Elson Claim Construction Decl., Ex. 21 at PRIMC00000202). Dr. Szepesi cited a 1984 edition of the McGraw-Hill dictionary, which defined a voltage regulator as "a device that maintains terminal voltage of a generator or other voltage source within required limits despite variations in input voltage or load." *Id*. Dr. Szepesi also quotes the IEEE Standard Dictionary of Electrical and Electronic Terms, Fourth Edition (1988), which defines "voltage regulator" as "[a] direct current power supply whose output voltage is automatically controlled to remain within specified limits for specified variations in supply voltage and load currents." *Id* (quoting Fisher Claim Construction Reply Decl., Ex. 27). According to Dr. Szepesi, all three of these definitions agree that the output voltage of a voltage regulator should be "maintained within required/specific/close tolerance limits" and none contains any limitation regarding changing the output voltage due to changing reference voltage. *Id*. As a result, all of the definitions "accommodate and include programmable voltage regulators that can change their output voltage due to changing target/reference voltage." *Id*.

Dr. Szepesi points out that Dr. Fair has conceded that even dynamic voltage regulators must maintain a "steady voltage for some unspecified period of time." *Id*., ¶ 27 (quoting Elson Claim Construction Decl., Ex. 1 (Fair Claim Construction Decl.), ¶ 165). Thus, he asserts, the question of whether the Burstein patent encompasses dynamic voltage regulators depends on how long a voltage regulator must maintain a substantially constant output voltage. As none of the definitions specify a particular length of time, Dr. Szepesi asserts, a person of ordinary skill in the art "would understand

that if a circuit is capable of [maintaining its output voltage within specified limits to meet the requirements] for an unspecified period of time (in my opinion for a period of time which is substantial relative to the switching period of the switching regulator) then it meets the definition and is a 'voltage regulator.'" *Id.*

Dr. Fair responds that Dr. Szepesi's position as to how long the output voltage must be maintained substantially constant is "arbitrary and indefinite." Fair Supp. Claim Construction Brief, ¶ 131. Dr. Fair notes that the dictionary definitions cited by Dr. Szepesi do not specify any particular time period. *Id.* He states further that one of ordinary skill in the art would understand the Burstein patents "to be describing circuits that regulate output voltage within a tolerance of a target value whenever the circuit is operating, and not just for some arbitrary, indefinite transient time." *Id.*, ¶ 133.

Dr. Fair also rejects Dr. Szepesi's assertion that the Burstein patents cover both the static and dynamic voltage regulators described in the Stratakos Dissertation, arguing that the Burstein patents include no disclosure that would allow a person of ordinary skill in the art to design a switching voltage regulator in which the output voltage can be digitally programmed to "change its output voltage on the fly." *Id.*, ¶¶ 135-139. In support of this conclusion, Dr. Fair points to Figure 1 of the Burstein patents, which depicts a switching voltage regulator that he asserts corresponds to the static switching voltage regulator depicted in Figure 5.1 of the Stratakos Dissertation. *Id.* According to Dr. Fair, Figure 1 does not show any communication path between load 14 and the switching regulator 10 and therefore, the '264 specification only supports a static switching voltage regulator. *Id.*, ¶ 138. Dr. Fair continues, "[t]o provide an enabling disclosure of a dynamic switching regulator, the specification of the '264 patent would have to . . .specify how such a regulator would be designed to meet AC characteristics, including being able to respond to changing commands within a specified time, and to do so without jeopardizing the stability of the circuit control loop, while avoiding undesired (and potentially damaging) transient output spikes/excursions." *Id.*, ¶ 139.

**iii. Analysis**

This claim term requires the Court to resolve two questions. First, what do the words "substantially constant" mean? Second, what does the word "maintain" mean. The first question is

straightforward, and although the parties offer different formulations, they appear to agree that the words "substantially constant" mean that the output voltage of the device must be held within a certain, fairly narrow range. Defendants use the word "stable" to capture this meaning, while Plaintiff suggests this meaning should be conveyed with the words "within well-defined tolerance limits." The Court concludes that Plaintiff's formulation is preferable because it is somewhat more precise than Defendants'.

The more difficult issue facing the Court is the meaning of the word "maintain" in this claim term. Although neither side has framed its arguments with reference to this specific word – in fact, both have included it in their proposed constructions – it is clear that the parties offer very different conceptions of what it means to "maintain" an output voltage. For Defendants, this word means, in the context of the Burstein patents, that there may be only *one* output voltage during the entire time the device is in operation. Defendants convey this meaning through the use of the word "fixed" in their proposed construction. Hence, their expert also concludes that a "voltage regulator" (again, as used in the Burstein patents) includes only what Defendants characterize as a "static voltage regulator."

For Plaintiff, on the other hand, the word "maintain" does not preclude changing the output voltage on command, such that a "voltage regulator," in the Burstein patents, includes what Volterra's expert calls "adjustable voltage regulators." In an effort to get at this feature, Plaintiff's expert proposes language in Volterra's construction that addresses the question of *how long* the output voltage must be held within a certain range to satisfy the requirements of this claim term. In particular, Plaintiff's expert proposes that the duration for which the output voltage must be held substantially constant is a "substantial period of time, where a substantial period of time is a period of time which is substantial relative to the switching period of the switching regulator."

Having reviewed the claims and the specification, the Court finds that the patentees did not directly address this issue, whether it is framed as a question of whether the output voltage can be changed on command, or alternatively, in terms of the amount of time the output voltage must be held substantially constant. In particular, nowhere in the specification do the patentees state that there can be only a single output voltage while the device is in operation, or that the output voltage cannot be

changed on command. Conversely, while the specification is not necessarily inconsistent with Dr. Szepesi's "substantial period of time" formulation, it also does not expressly articulate such a concept anywhere. Under these circumstances, the Court looks to the extrinsic evidence to understand what a person of ordinary skill in the art at the time of the invention would have understood a "voltage regulator," as disclosed in the Burstein patents, to be. From this understanding, the Court may find guidance as to the meaning of the word "maintain" in the claim term that is before it.

The extrinsic evidence suggests that the ordinary and customary meaning of "voltage regulator" (a term the Court did not agree to construe but which is, nonetheless, closely related to the issue at hand) at the time of the invention included both fixed (or static) voltage regulators and those for which the target output voltage could be changed. Both types of voltage regulators were known at the time of the invention and the dictionary definitions encompassed both. The question, then, is whether the claim term "maintain the DC voltage substantially constant" should be construed in a manner that limits the claims to static voltage regulators. The Court concludes that it should not.

In contrast to *Nystrom* and *AquaTex*, in this case Defendants' proposed construction is not consistent with the ordinary and customary meaning of the term "voltage regulator" at the time of the invention. Rather, it is *narrower* than the ordinary and customary meaning of that term. The Court finds persuasive Dr. Szepesi's reasoning that the term "maintain the DC voltage substantially constant" would have been understood by a person of ordinary skill in the art to apply to *any* voltage regulator, including the dynamic voltage regulators described in the Stratakos Dissertation. While Figure 1 of the '264 patent apparently depicts a static voltage regulator, the Court concludes that it would be improper to import this limitation from a preferred embodiment in construing the term "maintain the DC voltage substantially constant."

Having reached this conclusion, the Court must construe the word "maintain" to capture the idea that the output voltage of the invention may be fixed or may be changed on command while the voltage regulator is in operation Rather than attempting to describe the amount of time the output voltage must remain substantially constant, the Court concludes that this concept is better conveyed with reference to whether the word "maintain" precludes changing the output voltage on command. As the Court concludes that it does not, it adopts the following construction of the claim term

"maintain the DC voltage substantially constant": "maintain the output voltage within well-defined tolerance limits in the face of changing input voltage and load, where the output voltage may be fixed, or may be adjusted on command such that over time, there may be more than one output voltage."

**8. "power switch"**

**i. Arguments**

Defendants argue that all of the asserted claims are invalid because the term "power switch" is indefinite. In particular, according to Defendants' expert, the term is used in two inconsistent ways in the patents. Elson Claim Construction Decl., Ex. 1 (Fair Claim Construction Decl.), ¶ 42. According to Defendants, in some places in the patents, the term "power switch" refers to a combination of both the high-side switch and the low-side switch, whereas in other places the term refers to only a single switch, either the high-side switch or the low-side switch. *Id*., ¶ ¶ 42, 43, 48. As a result, Defendants assert, one of ordinary skill in the art could not conclusively determine the meaning and scope of the asserted claims. *Id*.

In support of his assertion that the term "power switch" is used inconsistently in the patents, Dr. Fair points to what he asserts are inconsistent uses of the term in the claims. First, he argues that "power switch" as used in Claim 1 of the '264 Patent is internally inconsistent with dependent claims 12 and 14. *Id*., ¶ 49. Claim 1 includes the following limitation:

> wherein the flip-chip type integrated circuit chip includes a p-type region and an n-type region, and **the first power switch includes a plurality of p+ regions fabricated in the n-type region in a first array, and a plurality of n+ regions fabricated in the p-type region in a second array**, and wherein alternating p+ regions are connected to the input terminal and to an intermediate terminal, and alternating n+ regions chip are connected to the intermediate terminal and to ground.

*Id*. (quoting '264 patent, claim 1 (excerpt) (emphasis added by Court)). Dr. Fair takes the position that one of ordinary skill in the art would understand that the "first power switch" includes *both* the "plurality of p+ regions fabricated in the n-type region in a first array" and the "plurality of n+

regions fabricated in the p-type region in a second array" and therefore, that the term "power switch" means the combination of the high-side switch and the low side switch. *Id.* [19]

However dependent claim 12 is inconsistent with this understanding, according to Dr. Fair, because it refers to a "second power switch." *Id.*, ¶ 49. Dr. Fair reasons, "[s]ince there is no support in the specification for the use of four switches, claim 12 would suggest that the first power switch must be a single high-side switch and the 'second power switch' is a single low-side switch." *Id.* Similarly, Dr. Fair asserts, claim 14 (which also depends from claim 1) refers to a "first power switch" that "includes a distributed array of PMOS transistors" and a "second power switch" that "includes a distributed array of NMOS transistors," thus "compounding the confusion." *Id.*, ¶51.

Second, Dr. Fair argues that the use of the term "power switch" in claim 26 of the '264 patent is ambiguous. *Id.*, ¶ 52. As noted above, the preamble of claim 26 calls for "[a]n integrated circuit chip with a power switch for a voltage regulator fabricated thereon." According to Dr. Fair, it is

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[19]Dr. Fair also points to Claims 35 and 43 of the '264 patent as examples of claims in which the term "power switch" means the combination of the high-side switch and the low-side switch. *Id.* ¶ 43. Claim 35 states, in part, as follows:

> A power switch for a voltage regulator having an input terminal and an output terminal, comprising:
>
> a PMOS switch fabricated on a chip with a first alternating pattern of source pads and drain pads;
>
> an NMOS switch fabricated on the chip with a second alternating pattern of source pads and drain pads;
>
> . . .

'264 patent, claim 35 (excerpt). Claim 43 provides as follows:

> A power switch for a voltage regulator, comprising:
>
> a chip having an array of pads formed thereon, each pad connected to a plurality of doped regions to create a distributed array of transistors; and
>
> a substrate having a signal layer formed thereon, the signal layer having a first electrode and a second electrode, the first electrode having a body and a plurality of fingers that extend from the body toward the second electrode, the second electrode having a body and plurality of fingers that extend toward the first electrode, wherein the fingers in the first electrode and are interdigited with the fingers of the second electrode and each finger overlies and is electrically coupled to a row of pads on the chip.

'264 patent, Claim 43.

unclear whether "power switch" in claim 26 (which he finds to be a claim limitation, even though it is in the preamble of the claim) refers to a single switch or a combination of the high-side and low-side switches. *Id*. In further support of his argument that this term is ambiguous in claim 26, he points to dependent claims 30 and 31, which appear to describe a device in which the power switch is a high-side switch, and dependent claims 32 and 33, which describe a device using a low-side switch. *Id*.

Finally, at oral argument, Defendants relied heavily on claim 9 of the '522 patent in support of their assertion that the term "power switch" is used inconsistently in the claims of the Burstein patents. Claim 9 states, in part, as follows:

> 9. A voltage regulator having an input terminal and an output terminal, comprising:
>
> . . .
>
> a first flip-chip type integrated circuit chip mounted on the printed circuit board, the first integrated circuit chip including *a first power* switch fabricated therein to alternately couple and decouple the input terminal to the output terminal, wherein *the power switch* includes . . .

'522 patent, claim 9 (emphasis added). According to Defendants, the terms "first power switch" and "power switch" are used interchangeably, indicating that Plaintiff cannot resolve the ambiguity among the claims by distinguishing between a "power switch" and a "first power switch" or "second power switch."

Dr. Fair also relies on the specification of the Burstein patents in support of his argument. He opines that "the bulk of the disclosures in the specification . . support the interpretation that the 'power switch' is the combination of both [the high side and the low-side] switches." *Id*.,¶ 44 (citing '264 patent, 3: 17-21 ("The power switch has a PMOS switch fabricated on a chip with a first alternating pattern of source pads and drain pads, an NMOS switch fabricated on the chip with a second alternating pattern of source pads and drain pads, and a substrate . . ."); 2: 16-20 ("the power switch may include a plurality of p+ regions fabricated in the n-type region, and a plurality of n+ regions fabricated in the p-type region"). In addition, according to Dr. Fair, the figures of the Burstein patents also show the "power switch" as a combination of a low-side and a high-side switch. *Id*., ¶ 45. In particular, Figure 1 shows "switching circuit 16 which serves as a power switch." *Id*. (quoting '264 patent, 4: 62-65). Switching circuit 16, in turn, consists of two transistors, first

transistor 30 and second transistor 32, as can be seen in the figure. Similarly, Figure 3A, which is described as a "schematic plan view of a power switch fabricated on a flip-chip according to the invention ," *id*. (quoting '264 patent, 4: 26-27), "shows two transistors as comprising the power switch; one represented by the array of pads on the left and one represented by the array of pads on the right." *Id*.

Volterra rejects the assertion that the term "power switch" is indefinite, asserting that the term is used consistently in the claims and that the specification makes it clear what the term means in the claims. In particular, Dr. Szepesi asserts that the term "power switch" or "switch" is used in the patents, as it is in the art of power electronics and switching regulators generally, to refer to "one or more switches" and thus, encompasses both a pair of switching transistors and a single switching transistor. Szepesi Claim Construction Decl., Ex. 5(Szepesi Rebuttal Expert Report (Infringement)), ¶¶ 37-38; *see also* Szepesi Claim Construction Reply Decl., ¶ 6 ("this term would have been clear, based on the context, even though it refers to two different things: a single switching element (i.e. a single switching transistor) or two switching elements (i.e. two switching transistors)"). Further, when the terms "first power switch" and "second power switch" are used in the patents, they consistently refer to the high-side switch and the low-side switch, respectively. *Id*., ¶ 39.

Dr. Szepesi rejects Dr. Fair's assertion that claim 1 of the '264 patent uses the term "power switch" in a manner that is inconsistent with dependent claims 12 and 14. Specifically, he disagrees with Dr. Fair's reading of claim 1 with respect to the term "first power switch," which Dr. Fair finds includes both the low-side and the high-side switches . *Id*., ¶ 41. Rather, Dr. Szepesi finds that the phrase "and a plurality of n+ regions fabricated in the p-type region in a second array" does not relate to the "first power switch" but instead, describes the "second power switch" that is part of the flip chip type integrated circuit. *Id*. Dr. Szepesi acknowledges that this is not "spelled out expressly" in claim 1, but asserts that when claim 1 is read in tandem with dependent claims 12 and 14, it is clear that the "first power switch" is the high-side switch and the "second power switch" is the low-side switch. *Id*.

Dr. Szepesi also rejects the assertion of Defendants' expert that the use of the term "power switch" in claim 26 is ambiguous. He agrees with Dr. Fair that the term, as used in the preamble of

the claim, is a limitation, but asserts that it can be read on either the low-side or the high-side n-channel MOSFET of the accused devices. *Id*., ¶ 47. Thus, he notes, in Plaintiff's infringement contentions, the claim chart shows that claim 26 can be read on the accused devices either based on their inclusion of the high-side switch (which is also consistent with claims 30 and 31) or, in the alternative, the low-side switch (which is covered by claims 32 and 33).

Volterra also argues that even if some unasserted claim were found indefinite, this would not render all of the other claims indefinite as well because each claim of the patent is presumed valid independent of the validity of the other claims. Therefore, Dr. Szepesi asserts, a person of ordinary skill in the art would understand the references to a "first power switch" and a "second power switch" in the context of the asserted claims of the patent. *Id*., ¶ 50.

Dr. Szepesi finds further support for his position in the prior art. In particular, he cites to U.S. Patent Nos. 5,481,178 and 6,580,258 (the "'178 and '258 patents"). *Id*. ¶ 37. According to Dr. Szepesi, in these patents, which were "widely litigated," the term "power switch" was used to refer to either a pair of switching transistors or a single switching transistor and none of its claims were found to be ambiguous. *Id*. In the specification of the '178 patent, the patentees stated as follows:

> It will also be apparent that although the present invention has been discussed above with reference to FIGS. 1-10, wherein the power switches were either a pair of complementary MOSFETS (i.e. one p-channel and one n-channel) or a single p-channel MOSFET (FIG. 3), the present invention is applicable to other types of switches as well. For example, the power switch could include a pair of N-channel MOSFETS, a pair of P-channel MOSFETS, or bipolar junction transistors.

*Id*. (quoting '178 patent, 6: 17-24).

In addition, Dr. Szepesi cites other prior art that he concludes supports his position. In particular, he conducted a search of the term "power switch" in the IEEE Xplore database, turning up 28 publications that he found relevant and that were published in or before 2000. Szepesi Claim Construction Reply Decl., ¶ 9; *see also* Fisher Claim Construction Reply Decl., Ex. 22 (copies of the 28 publications). Of these, he found 21 that used the term power switch to designate a single switching element, four that used the term to designate two switching elements and one that used the term either to designate a single switching element or to designate a combination of two switching elements and their driver circuitry. *Id*., ¶ 10. Dr. Szepesi concludes, on the basis of this extrinsic

evidence, that the term "power switch" was widely used in the prior art and that, consistent with its use in the Burstein patents, it was used to refer to switch arrangements consisting of "either a single switching element (e.g. a single switching transistor), or two switching elements (e.g. two switching transistors), or both." *Id*.

Defendants reject Volterra's reading of claim 1, arguing that it is grammatically unsupportable because the parallel construction of the two phrases beginning with "a plurality of" associates them together. Defendants also point to the Summary of the specification, which they assert mirrors claim 1 and clearly describes the power switch as having two switches. The Summary states:

> The flip-chip type integrated circuit chip may include a p-type region and an n-type region, and the power switch may include a plurality of p+ regions fabricated in the n-type region, and a plurality of n+ regions fabricated in the p-type region.

'264 patent, Summary.

Dr. Fair also rejects Dr. Szepesi's reliance on the '178 patent as evidence that the term "power switch" can cover a device with two switching elements or just one. Dr. Fair notes that the term "power switch," while used in the specification of the '178 patent, was *not* used in the claims. Rather, the '178 patent claimed "a pair of synchronously switched switching transistors" in the relevant claims. Elson Claim Construction Decl., Ex. 1 (Fair Claim Construction Decl.), ¶ 53. According to Dr. Fair, the fact that the patentees did not use the term "power switch" in the claims of the '178 patent actually supports Defendants' position, showing that they believed the term "power switch" to be too ambiguous to use in their claims. *Id*. With respect to the 28 prior art publications found by Dr. Szepesi that used the term "power switch," Dr. Fair concludes that this prior art simply reinforces the conclusion that "there was no one common meaning or understanding of 'power switch' in the prior art." Fair Supp. Claim Construction Decl., ¶ 7. As further support for that point, Dr. Fair points out that the term "power switch" cannot be found in the IEEE technical dictionaries cited by the parties. *Id*., ¶ 31.

Dr. Fair rejects Plaintiff's position that the term "power switch" can have different meanings depending on the context, or that "first power switch" and "second power switch" are different terms. *Id*., ¶¶ 25, 34. Further, he asserts in his Supplemental Claim Construction Declaration that even if

this were permissible, it is not appropriate here because the specification does not include any disclosure of a power switch that contains only one switching element.[20] *Id.*, ¶ 25. Dr. Fair rejects Dr. Szepesi's deposition testimony in which he cited to the '264 patent, column 4, lines 65-67, to show that the specification of the Burstein patents discloses a power switch with only one switching element. *Id.*, ¶ ¶ 28-29. That citation states that "[t]he switching circuit 16 includes a rectifier, such as a switch or diode, coupling the intermediate terminal 22 to ground." At his deposition, Dr. Szepsi testified that a diode is not a switching element and therefore, the power switch depicted in Figure 1 would have only a high-side transistor." Elson Supp. Claim Construction Decl., Ex. 43 (Szepesi Depo., 11/24/09) at 489. Dr. Fair, however, stated that a person of ordinary skill in the art would know that diodes were switching elements. Fair Supp. Claim Construction Decl., ¶¶ 28-29. Dr. Fair cites to several prior art publications in which diodes are described as switching elements, including a publication cited by Dr. Szepesi himself, a publication by Dennis Jarc and Donald Novotny. *Id.* (citing Fisher Claim Construction Reply Decl., Ex. 22-02).

Dr. Szepesi dismisses Defendants' reliance on the absence of the term "power switch" in the IEEE dictionaries to support their position, asserting that composite terms often are not found in those dictionaries but are well understood in the art. Szepesi Claim Construction Reply Decl., ¶ 8. Dr. Szepesi further notes that the term "switching device" is defined in the 1988 edition of the IEEE dictionary and that that definition supports his position. *Id.*, ¶ 11 (citing IEEE Standard Dictionary of Electrical and Electronic Terms, 1988 Edition at 972)(defining "switching device (switch) (power switchgear)" as "[a] device designed to close or open, or both, one or more electric circuits").

Finally, at oral argument, Plaintiff rejected Defendants reliance on claim 9 of the '522 patent to show that "first power switch" and "power switch" must have the same meaning. Plaintiff points out that the words "power switch" in the passage quoted above is modified by the word "the" rather than "a" and therefore clearly refers to the "first power switch" mentioned earlier in the claim.

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[20]The Court notes that the assertion that in the Burstein patents there is no disclosure of a power switch with a single switching element appears to be inconsistent with Dr. Fair's earlier Claim Construction Declaration. There, he stated that a person skilled in the art would have understood that "other portions of the patent support an inconsistent understanding of power switch, namely: a single high-side device or a single low-side device, but not both." *See* Elson Decl., Ex. 1 (Fair Claim Construction Decl.), ¶ 48 (citing '264 patent, 2: 37-40).

**ii. Analysis**

Defendants argue that the term "power switch" is indefinite because it is used in two different ways in the patent and in some cases, the usages even appear to be internally inconsistent. The Court disagrees.

As noted above, it is well-established that "[a] word or phrase used consistently throughout a claim should be interpreted consistently." *Phonometrics, Inc. v. Northern Telecom Inc.*, 133 F.3d 1459, 1465 (Fed.Cir.1998). On the other hand, where a claim term is used "in two contexts with a subtle but significant difference" the term "should not necessarily be interpreted to have the same meaning in both phrases." *Epcon Gas Systems, Inc. v. Bauer Compressors, Inc.*, 279 F.3d 1022, 1031 (Fed. Cir. 2002). Further, the use of a modifier, such as "first" or "second" before a term is a convention that is used to distinguish between slightly different structures. For example, in *3M Innovative Properties Co. v. Avery Dennison Corp.*, the Federal Circuit held that the terms "first pattern" and "second pattern" were equivalent to "Pattern A" and "Pattern B." *See also Swapalease, Inc. v. Sublease Exchange.com, Inc.*, 2009 WL 204408, *11 (S.D.Ohio, Jan. 27, 2009)(holding that "first webpage" and "second webpage" are specific webpages and that "first webpage" is different from "second webpage").

In the claims of the Burstein patents, the term "power switch" is used in somewhat different ways, at times referring generally to "a power switch" and at other times referring more specifically to a "first power switch," a "second power switch" or "the power switch." Having carefully considered the claims of both patents, the Court concludes that the term "power switch" is not insolubly ambiguous and that when read in light of the specification, the meaning of the term would have been clear to a person of ordinary skill in the art. In particular, it would have been understood that the term "power switch" is a general term that encompasses switches with only a high-side device, switches with only a low-side device and switches with both a high-side and a low-side device. As discussed further below, however, the person of ordinary skill would also have understood that the term was used in some claims to refer to only one of these variants.

First, the Court looks to claim 1 of the '264 patent, the meaning of which has been the source of much discussion among the parties and the Court. Defendants' expert concludes that a person of

ordinary skill in the art would understand that the "first power switch" in claim 1 refers to a combination of a high-side device and a low-side device. According to Defendants, though, an inconsistency would arise beginning at dependent claim 12, which refers to a "second power switch." Because there is no support in the specification for a device with 4 switching elements, this claim would lead a person of ordinary skill in the art to conclude that the "first power switch" in claim one must be only a high side switch. Yet the two meanings could not both be true. Plaintiff, on the other hand, asserts that a person of ordinary skill in the art would understand that the "first power switch" in claim 1 is just a high-side device, as this is apparent from reading claim 1 together with the dependent claims that follow it. Plaintiff asserts that the grammatical structure of claim 1 permits such a reading and therefore, that this construction should be adopted to preserve the validity of the claims.

In its preliminary injunction order, the Court tentatively concluded that claim 1 could be read in the manner proposed by Plaintiff, even though such a reading was awkward. The Court now reconsiders that conclusion. The Court agrees that the parallel construction of the two phrases in claim 1 beginning with "a plurality of" is the most natural reading of this claim language. Plaintiff's argument that the second phrase, referring to a "plurality of n+ regions fabricated in the p-type region in the second array," refers to a "second power switch" that is "not spelled out expressly" until dependent claim 12 is unpersuasive, both because it renders the quoted language in claim 1 superfluous and because the description in the Summary, which mirrors the language of claim 1, strongly suggests that the patentees were using the term "first power switch" to refer to the combination of both the high side and the low side devices. *See* '264 patent, 2: 14-18.

Having reached this conclusion, however, the Court rejects Defendants' argument that the term "power switch" is indefinite because the term "first power switch" in claim 1 appears to be inconsistent with dependent claims 12 and 14. Defendants have stated repeatedly that claim 1, when read by itself, would have been clear to person of skill in the art and reflects the embodiment shown in Figure 1. In particular, the "first power switch" of claim 1 refers to a combination of a high-side switch and a low-side switch. The fact that this construction may render the devices claimed in dependent claims 12 and 14 inoperable to the extent that they would include 3 or 4 switching

elements does not mean that the term is indefinite in claim 1. It may, however, give rise to a question of enablement as to the dependent claims.

The Federal Circuit's decision in *Exxon Research and Engineering Co. v. United States* is directly on point. 265 F.3d 1371, 1383 (Fed. Cir. 2001). There, a claim term did not set any upper limit on the size of a particle that was claimed as part of the invention, even though the specification stated that particles that were larger than a certain size would render the invention inoperable. *Id*. The defendants argued that the claim was indefinite because it expressly covered particles that were larger than those described in the specification, but the Federal Circuit rejected the argument. *Id*. It reasoned:

> A patent claim to a fishing pole would not be invalid on indefiniteness grounds if it contained a limitation requiring that the pole be "at least three feet long," even though a 50 foot long fishing pole would not be very practical. By the same token, there is nothing indefinite about the claim language at issue in this case simply because it covers some embodiments that may be inoperable.

*Id*. The issue, the Federal Circuit explained, was not one of indefiniteness but rather, enablement. *Id*.; *see also Miles Laboratories, Inc. v. Shandon Inc.*, 997 F.2d 870 (Fed. Cir.1993)("The invention's operability may say nothing about a skilled artisan's understanding of the bounds of the claim"). Thus, the Court concludes that notwithstanding any confusion created by claims 12 and 14,[21] the term "power switch" is not indefinite because of those claims.

Next, the Court rejects Defendants' reliance on claim 26 of the '264 patent in support of its indefiniteness argument. Using Plaintiff's proposed construction of "power switch," claim 26 covers devices with one switching element –either high-side or low-side – or two switching elements, while the dependent claims that follow claim 26, namely, claims 30 and 33, describe devices with either a high-side switch (claims 30 and 31) or a low-side switch (claims 32 and 33).

Finally, the Court finds Defendants' reliance on claim 9 of the '522 patent unpersuasive. In particular, Defendants make much of the fact that claim uses the term "the power switch" interchangeably with the term "first power switch," arguing that Plaintiff cannot get around the ambiguity of the term "power switch" by distinguishing between "power switch" and "first power

[21]The Court does not reach the question of whether claims 12 and 14 fail for lack of enablement, which has not been briefed by the parties.

switch." The Court finds that the use of the word "the" to modify "power switch" makes it clear, in claim 9, that the patentees are referring to the "first power switch" referenced earlier in the claim. As a result, claim 9 does not support Defendants' position.

The Court also reject Defendants' assertion that the term "power switch" should not be construed to encompass a structure with only one switching element because the specification only discloses one "context," that is, a power switch made up of both a high-side and a low-side device, as shown in Figure 1. Defendants' own expert took the position that the specification reveals *both* meanings and the Court agrees. *See* Elson Claim Construction Decl., Ex. 1 (Fair Claim Construction Decl.), ¶ 48 ("One of ordinary skill in the art would understand that other portions of the patent support an inconsistent understanding of "power switch," namely: a single high-side device or a single low-side device, but not both"). In particular, Dr. Fair cited as an example of such a use of the term the statement found at column 2, lines 37-40 of the '264 patent, which states, "[t]he first power switch may include a distributed array of PMOS transistors and the second power switch may include a distributed array of NMOS transistors." Thus, the patentees used the term "power switch" in two, slightly different ways, sometimes referring to a single switching device and sometimes referring to a combination of a high-side and low-side switching device.

The patentees use of the term "power switch" as a broad term covering both types of devices is consistent with the prior art. In particular, regardless of whether the IEEE dictionary contains the term "power switch," Defendants acknowledge that the term "power switch" was used in at least 28 publications that qualify as prior art, and that in these publications, the term was sometimes used to cover a switch with only one switching device while in others, it covered switches with two switching devices. In the '178 patent, it was used in the specification to refer to both. That the prior art did not contain a *single* definition does not render the claim term indefinite in the Burstein patents to the extent that a person skilled in the art would be aware that the term could be used either way *and* to the extent that it is clear from the context which meaning of the term the patentees were using in the specification and claims when they used the term "power switch."

The Court concludes that the term power switch is not indefinite.

**B. The '823 Patent**

**1. "substantially continuous plane/isolated structure"**

| Claim Term | Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|---|
| substantially continuous plane/isolated structure | A substantially continuous plane of conductive material is a plane of conductive material, e.g., metal, which has one or more discontinuities that include isolated structures to provide a vertical conductive coupling between conductive elements located below and above the substantially continuous plane of conductive material. The one or more discontinuities have a total area that is a relatively small portion of the area of the substantially continuous plane of conductive material. The one or more isolated structures that are included in the one or more discontinuities are electrically isolated from the substantially continuous plane of conductive materials that includes them. The '823 Patent describes and claims two separate, electrically isolated substantially continuous planes of conductive materials next to each other. The isolated structures inside one substantially continuous plane of conductive material are electrically connected to the other substantially continuous plane of conductive material. | A large uninterrupted surface, relative to the extended regions at the edge of the surface, such that a straight line that joins any two of its points lies wholly in that surface, except for: (1) isolated structures within the boundaries of the surface; and (2) small extended regions, relative to the uninterrupted surface, at the edge of the surface.<br><br>A relatively small conductive insert (i.e., island of metal) bounded on all sides by a window-like cutout in the relatively large conductive area, wherein the conductive insert is electrically isolated from the conductive area by an insulator. |

Claim 23 of the '823 patent, from which all of the asserted claims depend, claims a "first conductive area" that is a "substantially continuous plane of a conductive material . . . having at least one isolated structure within the first conductive area . . . ." Plaintiff construes "substantially continuous plane" with reference to "isolated structure," taking the position that the terms should be

construed together because "the 'substantially continuous planes' are 'substantially' – not wholly – continuous planes of conductive material because they have these discontinuities." Szepesi Claim Construction Decl., ¶ 19. Defendants do not dispute that the terms "substantially continuous plane" and "isolated structures" are closely related, but argue that each term should be separately construed. While the parties challenge many aspects of the others' proposed constructions, the primary dispute is whether the isolated structures must be bounded on all sides by the conductive area, as Defendants contend.

**i. Arguments**

**a. Defendants' Proposed Construction**

Plaintiff argues that Defendants' proposed construction of "substantially continuous plane" is confusing and wrong, and further, that their proposed construction of "isolated structure" improperly imports limitations from the preferred embodiments.

With respect to the term "substantially continuous plane," Plaintiff argues that Defendants' proposed construction is wrong because, to the extent it calls for an "uninterrupted surface," it reads out the preferred embodiments. In particular, Dr. Szepesi points out that in Figure 1 of the specification, it is clearly shown that the substantially continuous plane is interrupted by the windows 46a and 46b, including conductive inserts 48a and 48b, which correspond to the "isolated structures." Szepesi Claim Construction Decl., ¶ 21 (citing'823 patent, 5: 20-24 & Fig. 1). Dr. Szepesi further notes that the term "uninterrupted" does not appear anywhere in the '823 patent.

Next, Plaintiff asserts that the phrase "such that a straight line that joins any two of its points lies wholly in that surface" is "confusing and ambiguous," and in any event, is rendered meaningless by the exception for the "isolated structures" and "small extended regions." Plaintiff states, "if a straight line intersected an isolated structure in the substantially continuous plane (as is clearly possible based on the preferred embodiment depicted in Figure 1), it would not 'lie[] wholly within' the surface of the substantially continuous plane." Plaintiff's Claim Construction Brief at 24. Plaintiff's expert notes that to the extent Defendants sought to define a "plane" in their proposed construction, they could have used the *first* definition of a plane in Webster's Dictionary (the

Defendants cited the *second* definition), that is, "a smooth and level surface." Szepezi Claim Construction Decl., ¶¶ 67-68 (citing Fisher Reply Decl., Ex. 26).

Plaintiff further objects to the inclusion of the phrases "within the boundaries of the surface" in Defendants' proposed construction of "substantially continuous plane" and "bounded on all sides," in their construction of "isolated structures." According to Plaintiff, these proposed limitations improperly import features of the preferred embodiments that are not found in the claims. *See* Szepezi Claim Construction Decl., ¶ 73. According to Dr. Szepesi, the only limitation relating to this question is the requirement that the isolated structures must be "within" the substantially continuous plane. *Id*. Dr. Szepesi cites to the New Webster Dictionary of the English Language, College Edition, 1975, in support of his conclusion that the word "within" does not require the limitations proposed by Defendants. *Id*., ¶ 74. In particular, that dictionary provides numerous definitions of "within," all of which, according to Dr. Szepesi, convey the meaning of "not beyond" and "not exceeding not overstepping" and do not require that a structure that is "within" be "bounded by [it] on all sides." *Id*. Therefore, Plaintiff asserts, the isolated structures need not be bounded on all sides by the substantially continuous plane. Volterra Reply Claim Construction Brief at 13. For example, the claim language also covers embodiments in which the isolated structure extends to the edge of the substantially continuous plane. *Id*.

To illustrate the difference between Plaintiff's position and Defendants' position on this issue, Dr. Szepesi offers several figures depicting embodiments that he asserts would fall within Plaintiff's proposed construction. *See* Szepesi Reply Claim Construction, ¶¶ 76-79. One of these shows the "discontinuities" and the "isolated structures" within them as stripes that extend the entire width of the plane, thus dividing the "substantially continuous plane" into discrete sections. *Id*., ¶ 79 (Figure 5). Because of Defendants' proposed limitation that the isolated structures must be "within the boundaries of the surface"and "bounded on all sides" by the substantially continuous plane, this embodiment would fall outside the scope of claim 23 and its dependent claims if Defendants' proposed constructions were adopted.

Plaintiff also objects to Defendants' proposed construction of "isolated structure" to the extent it calls for "islands of metal." According to Plaintiff's expert, there is no reference in the '823

patents to "islands" in connection with the isolated structures. Szepesi Claim Construction Decl., ¶ 25.

Finally, Plaintiff argues that Defendants' proposed construction of "isolated structure" is inadequate because it does not specify the size of the "window-like cut-outs" relative to the substantially continuous plane, even though it does specify that the conductive inserts are "relatively small." Szepesi Claim Construction Reply Decl., ¶ 85.

Defendants respond that their proposed construction does not exclude the preferred embodiments because the "uninterrupted limitation" is qualified by the exception for the isolated areas in their proposed construction.[22] Further, Dr. Fair asserts that the phrase "such that a straight line that joins any two of its points" is appropriate because it is "the mathematically and readily demonstrable definition of a plane." Elson Decl., Ex. 1 (Fair Claim Construction Decl.), ¶ 189. Dr. Fair points to the definition of "plane" in Webster's Third New International Dictionary (1993): "a surface such that a straight line that joins any two of its points lies wholly in that surface." *Id*., ¶ 191; *see also* Elson Claim Construction Decl., Ex. 27 at PRIM01946881-82 (Webster's Third International Dictionary (1993)).

With respect to the phrases "within the boundaries of the surface" and "bounded on all sides," Defendants assert that this limitation is consistent with the claim language and the description of the invention in the specification. Dr. Fair points to the claim language requiring that the isolated structure must be "within" the substantially continuous plane. He asserts that the plain English meaning of "within," as set forth in Webster's Dictionary is: "on the inside or on the inner side"; "inside the bounds of a place or a region"; "lying or to be found inside: ENCLOSED." Elson Decl., Ex. 1 (Fair Claim Construction Decl.), ¶ 201 (citing Elson Claim Construction Decl., Ex. 27 at PRIMC00001355 (Webster's Third International Dictionary (1993)).

Turning to the specification, Dr. Fair points to Figures 1 and 3, which show the "isolated structures" as being bounded on all sides by the first conductive area. *Id*., ¶ 197. He also points out

[22]Defendants note that Plaintiff does not challenge their proposed construction of "substantially continuous plane" in so far as it relates to "extended regions." *See* Fair Supp. Claim Construction Decl., ¶ 160 (citing Szepesi Claim Construction Reply Decl., ¶ 76).

that in the specification, the term "windows" is used to describe the openings in which the isolated structure are found. *Id*., ¶ 198 (quoting '823 patent, 5: 20-36). According to Defendants, the dictionary definition of "window" supports their proposed construction. In particular, they cite to the Webster's definition of "window" as "any of various openings resembling or suggestive of a window." *See* Defendants' Responsive Claim Construction Brief at 24 (citing Elson Claim Construction Decl., Ex. 27 (Webster's Third New International Dictionary (1993) at PRIMC000013454)).

Dr. Fair rejects Dr. Szepesi's assertion that the "substantially continuous plane" claimed in claim 23 can cover multiple separate sheets of metal "simply by designating a boundary around the separate pieces." Fair Supp. Claim Construction Decl., ¶ 151. He notes that the specification does not offer guidance as to how to determine where the boundary would be drawn and that this would be necessary to determine whether an isolated structure was "within" the substantially continuous plane. *Id*., ¶¶ 152-154. Dr. Fair also opines that two or more separate planes of metal would not be a plane at all, much less a "substantially continuous plane." *Id*., ¶ 150. Rather, it would be "completely discontinuous." *Id*. Defendants point out that in his deposition, Dr. Szepesi conceded that the patent only describes a "substantially continuous plane" as a "single contiguous piece of metal." Elson Supp. Claim Construction Decl., Ex. 43 (Szepesi Depo.) at 712.

With respect to the size of the "window-like cut-out," Dr. Fair asserts that a person of ordinary skill in the art would understand that it, like the conductive inserts, would be relatively small. *See* Fair Supp. Claim Construction Decl., ¶ 169.

**b. Plaintiff's Proposed Construction**

Defendants argue that Plaintiff's proposed construction is wrong because: 1) Plaintiff conflates the terms "substantially continuous plane" and "isolated structure," even though they are separately recited in the claim and have different functions, and does not offer any construction for "isolated structure" or "plane"; 2) Plaintiff uses "discontinuity" even though it is not used in the patent and is itself a technical mathematical term that would not be understood by the jury; 3) the last two sentences are not a claim construction but rather, a general description of the '823 patent; and 4) Plaintiff's expert offers no opinion as to what one of ordinary skill in the art would have understood

these terms to mean.

With respect to the term "discontinuity" in Plaintiff's proposed construction, Defendants' expert argues that Dr. Szepesi has taken inconsistent positions as to whether the term is being used in its technical sense or rather, whether a lay definition of the term is being used. *See* Fair Supp. Claim Construction Brief, ¶¶ 141-142.

**ii. Analysis**

As a preliminary matter, the Court agrees with the parties that the term "substantially continuous plane" is closely related to the term "isolated structures." Therefore, the Court construes both claim terms. In construing these terms, there appear to be three primary issues. First, how should the plane be described? Second, how should the openings in the plane that contain the isolated structures be described? And third, how should the isolated structures themselves be described? In answering these questions, the Court's goal is to craft a construction that is both accurate, in the context of the Burstein patents, and understandable to a jury that will not necessarily be familiar with the mathematical terminology and concepts that both experts have, at times, used in their proposed constructions.

First, with respect to the word "plane," Defendants have offered a mathematical definition, characterizing a plane as a region in which a straight line connects any two points. They have then tailored the definition to fit the claims of the Burstein patents by including exceptions for the openings and the extended regions. The Court agrees with Plaintiff that this definition may be confusing to the jury. Instead, the Court finds that the more common definition of plane, as "a smooth and level surface" will be better understood by jurors.

Second, the Court must decide how to describe the openings in the plane. It is undisputed that the openings must be small, relative to the plane. The dispute, rather, is what shape the openings should take. In particular, the parties dispute whether the openings may encompass gaps that break the plane into discrete, entirely separate rectangles (as Plaintiff asserts) or rather, whether the openings must be bounded on all sides by the plane, as Defendants assert. The Court finds that Defendants are correct that the openings must be bounded on all sides by the plane. Not only do all of the preferred embodiments show the openings as being bounded on all sides. This is also

consistent with the claim language, which describes each conductive area as being "a substantially continuous plane" and the openings as being "within" that plane. As the claim describes a single plane, embodiments that use separate rectangles of metal to create the conductive area could only be considered a "substantially continuous plane" if the boundaries of the "plane" included stretches where whatever material that made up the plane was absent. In other words, Plaintiff's position is based on boundaries that are drawn around the rectangles to make the embodiments *appear* as if there is one plane. As the specification offers no guidance as to how such boundaries would be drawn, however, the Court finds Plaintiff's approach to be arbitrary and without support in the patents. Therefore, the Court rejects Plaintiff's position and finds instead that the openings must be bounded on all sides.

Having reached the conclusion that the openings must be "bounded on all sides," the Court declines to adopt Defendants' characterization of the openings as "window-like cut-outs." The Court agrees with Plaintiff that this phrase, though used in the specification to describe a preferred embodiment, might be interpreted by jurors to refer to a traditional rectangular window, which would be overly narrow in light of the '823 specification. On the other hand, the Court agrees with Defendants that Plaintiff's use of the word "discontinuities" may be confusing to the jury to the extent it has a mathematical meaning with which jurors may not be familiar. Instead, the Court will use the word "opening," which Defendants' expert sometimes uses in his report and which Plaintiff's expert implicitly approves. *See* Szepesi Claim Construction Decl., ¶ 75 ("I notice that Dr. Fair's formulation in some sections of his Declaration use terms like "openings" . . . describing the discontinuities of the substantially continuous plane. An 'opening' certainly includes but is not limited to a 'window-like cut out,' and does not seem to require or imply the same narrow construction that Defendants advocate.")

Finally, the Court turns to the isolated structures that are within the openings in the '823 patent. The parties are in agreement that the "isolated structure" is the conductive insert described in the specification and that it is "isolated" from the plane by an insulator. They also agree that the isolated structure must be small relative to the plane. Further, as discussed above, the Court finds that the opening – and thus, the isolated structure as well – must be bounded on all sides. The only

remaining dispute relates to the question of whether the isolated structures should be described as "islands of metal." The Court does not find support for this limitation in the claims or specification and therefore omits this limitation from its construction.

Therefore, the Court construes "substantially continuous plane" as follows: "a smooth and level surface containing openings, within the boundaries of the surface, that are small relative to the surface, where the openings contain isolated structures that are also small relative to the surface." The Court construes "isolated structure" as "a conductive insert that is electrically isolated from the substantially continuous plane, that is, the smooth and level surface, by an insulator."

**2. "lateral protrusion"**

| **Claim Term** | **Plaintiff's Proposed Construction** | **Defendants' Proposed Construction** |
|---|---|---|
| lateral protrusion | plain and ordinary meaning | a region of a conductive area that juts out of the side of that conductive area |

Claims 29 and 34 of the '823 patent claim extended regions with a "lateral protrusion." Defendants rely on the dictionary definitions of "lateral" and "protrusion" in support of their proposed construction. *See* Elson Claim Construction Decl., Ex. 1 (Fair Claim Construction Decl.), ¶ 217 (citing Webster's Third International Dictionary (1993) at PRIM01946894 & PRIM01946908). In its reply brief, Volterra argues that construction of "lateral protrusion" is not necessary and further, that the word "jut" in Defendants' proposed construction is confusing and is "simply another synonym for 'protrusion.'" Reply at 13. The Court finds that to the extent this term requires construction, the word "protrude" will be understood by the jury as well a "jut" and will stay closer to the language of the claims. Therefore, the Court construes "lateral protrusion" as "a region of conductive area that protrudes out of the side of that conductive area."

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## VI. CONCLUSION

For the reasons stated above, the Court adopts the following claim constructions:

| Claim Term | Court's Construction |
|---|---|
| "integrated circuit" | a miniaturized electronic circuit consisting of interconnected circuit elements, which is implemented on a semiconductor substrate. |
| "metalized pads" | Pads that include an under-bump metalization layer (UBM) that forms an interface between the top metal layer of the integrated circuit and the solder balls (bumps) that are often used in flip-chip type integrated circuits. Pads in an integrated circuit are openings in the top passivation layer that allow connection to the top metal layer, to enable formation of connections between the integrated circuit and external circuit element |
| "flip-chip type integrated circuit chip" | An integrated circuit chip oriented such that its active side faces the printed circuit board |
| a "first plurality of doped regions" and a "second plurality of doped regions" arranged in an "alternating pattern" | "doped region": a region where an impurity has been introduced into a substrate which changes the semiconductor's electrical properties<br><br>"alternating pattern": Either (i) an "a" "b" "a" "b" pattern; or (ii) a checkerboard pattern |
| "substrate" | The supporting material upon or within which an integrated circuit is fabricated or to which an integrated circuit is attached. |
| "mounted on" | supported by and securely fixed, either directly or indirectly, to the other surface |
| "maintain the DC voltage substantially constant" | maintain the output voltage within well-defined tolerance limits in the face of changing input voltage and load, where the output voltage may be fixed, or may be adjusted on command such that over time, there may be more than one output voltage |
| "power switch" | one switching element or two switching elements |

| | |
|---|---|
| "substantially continuous plane/isolated structure" | "substantially continuous plane": a smooth and level surface containing openings, within the boundaries of the surface, that are small relative to the surface, where the openings contain isolated structures that are also small relative to the surface."<br><br>"isolated structure": a conductive insert that is electrically isolated from the substantially continuous plane, that is, the smooth and level surface, by an insulator. |
| "lateral protrusion" | a region of a conductive area that protrudes out of the side of that conductive area |

IT IS SO ORDERED.

Dated: February 22, 2010

JOSEPH C. SPERO
United States Magistrate Judge