IN THE UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

KILOPASS TECHNOLOGY INC.,

Plaintiff,

v.

SIDENSE CORP.,

Defendant.
_____/

No. C 10-02066 SI

ORDER RE: CLAIM CONSTRUCTION

On August 1 and 2, 2011, the Court held a tutorial and a claim construction hearing. After consideration of the parties' papers and presentations, the Court construes the claims at issue as follows.

BACKGROUND

Plaintiff Kilopass Technology, Inc., is a company that markets "a novel way of storing data permanently inside integrated circuits . . . by creating a breakdown in the transistor, safely and reliably." Second Am. Compl. 8. Plaintiff alleges that defendant Sidense Corporation "has knowingly copied Kilopass' patented technology and has been selling and offering for sale Kilopass' patented technology without authorization from Kilopass." *Id.* at 18. In particular, plaintiff alleges that defendant infringed U.S. Patent Nos. 6,940,751 ("'751 Patent"), 6,777,757 ("'757 Patent"), and 6,856,540 ("'540 Patent"). *Id.* at 10, 17. Plaintiff also alleges that defendant has been "sowing deceit in the marketplace" by "falsely alleg[ing] in the marketplace statements to the effect that Kilopass has no intellectual property issues with Sidense." *Id.* at 24.

Plaintiff originally filed suit in this Court on May 14, 2010. Plaintiff filed its second amended complaint on October 14,. 2010. On December 13, 2010, the Court granted in part and denied in part

a motion to dismiss, leaving six causes of action in the case: three patent infringement claims, one false advertisement and disparagement claim, one intentional interference with prospective economic relations claim, and one unfair competition claim.

LEGAL STANDARD

Claim construction is a matter of law. *Markman v. Westview Instr., Inc.*, 517 U.S. 370, 372 (1996). Terms contained in claims are "generally given their ordinary and customary meaning." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005). "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Id.* at 1312. In determining the proper construction of a claim, a court begins with the intrinsic evidence of record, consisting of the claim language, the patent specification, and, if in evidence, the prosecution history. *Id.* at 1313; *see also Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). "The appropriate starting point . . . is always with the language of the asserted claim itself." *Comark Communications, Inc. v. Harris Corp.*, 156 F.3d 1182, 1186 (Fed. Cir. 1998); *see also Abtox, Inc. v. Exitron Corp.*, 122 F.3d 1019, 1023 (Fed. Cir. 1997).

Accordingly, although claims speak to those skilled in the art, in construing a claim, claim terms are given their ordinary and accustomed meaning unless examination of the specification, prosecution history, and other claims indicates that the inventor intended otherwise. *See Electro Medical Systems, S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 1053 (Fed. Cir. 1994). The written description can provide guidance as to the meaning of the claims, thereby dictating the manner in which the claims are to be construed, even if the guidance is not provided in explicit definitional format. *SciMed Life Systems, Inc. v. Advanced Cardiovascular Systems, Inc.*, 242 F.3d 1337, 1344 (Fed. Cir. 2001). In other words, the specification may define claim terms "by implication" such that the meaning may be "found in or ascertained by a reading of the patent documents." *Vitronics*, 90 F.3d at 1584 n.6.

The claims must be read in view of the specification. *Markman*, 52 F.3d at 978. Although claims are interpreted in light of the specification, this "does not mean that everything expressed in the specification must be read into all the claims." *Raytheon Co. v. Roper Corp.*, 724 F.2d 951, 957 (Fed.

Cir. 1983). For instance, limitations from a preferred embodiment described in the specification generally should not be read into the claim language. *See Comark*, 156 F.3d at 1187. However, it is a fundamental rule that "claims must be construed so as to be consistent with the specification." *Phillips*, 415 F.3d at 1316. Therefore, if the specification reveals an intentional disclaimer or disavowal of claim scope, the claims must be read consistent with that limitation. *Id.*

Finally, the Court may consider the prosecution history of the patent, if in evidence. The prosecution history limits the interpretation of claim terms so as to exclude any interpretation that was disclaimed during prosecution. *See Southwall Technologies, Inc. v. Cardinal IG Co.*, 54 F.3d 1570, 1576 (Fed. Cir. 1995). In most situations, analysis of this intrinsic evidence alone will resolve claim construction disputes. *See Vitronics*, 90 F.3d at 1583. Courts should not rely on extrinsic evidence in claim construction to contradict the meaning of claims discernable from examination of the claims, the written description, and the prosecution history. *See Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1308 (Fed. Cir. 1999) (citing *Vitronics*, 90 F.3d at 1583). However, it is entirely appropriate "for a court to consult trustworthy extrinsic evidence to ensure that the claim construction it is tending to from the patent file is not inconsistent with clearly expressed, plainly apposite, and widely held understandings in the pertinent technical field." *Id.* Extrinsic evidence "consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises." *Phillips*, 415 F.3d at 1317. All extrinsic evidence should be evaluated in light of the intrinsic evidence. *Id.* at 1319.

DISCUSSION

I. Agreements

The parties agree that each term that they have identified, though appearing in multiple independent claims in as many as three different patents, always means the same thing whenever it is used in the patents.

The parties agree on the following definitions for terms:

- **Memory array**: "a grid of memory cells that are organized in rows and columns"

- **Floating**: "not electrically connected to a voltage source"
- **Programmable memory array**: "a memory array comprised of programmable memory cells"
- **Memory cell which has been programmed**: "a programmable memory cell which, during programming, has been physically changed"
- **Breakdown**: "physically changing the electrical insulating characteristics of a gate dielectric under voltage induced stress"

See Pl. Br. at 21.

At the claim construction hearing, it became clear that the parties also agree on the following definitions:

- **Spaced apart relationship**: "not in physical contact"[1]
- **Gate dielectric**: "a gate insulating film"
- **Programmed**: [having had] "a physical conducting link between the gate and the channel formed by breaking down the gate dielectric"
- **Laterally separated by a distance D**: "no overlap in the vertical direction between the gate and the second doped region"

The parties agreed that a slightly edited combination of their two definitions of **semiconductor**[2] was accurate, and the Court adopts that definition: "a material, like silicon, whose conductivity is in the range between that of metals and insulators, and whose conductivity can be altered by the introduction of an impurity."[3]

Finally, the parties agree that a person of ordinary skill in the art is "a person with at least a bachelor's degree in electrical engineering, chemical engineering, mechanical engineering, materials sciences, computer sciences, or equivalent, with at least two years of graduate or related work experience in the semiconductor field." Expert Decl. of Dean Niekirk (Doc. 114), ¶ 5 (Kilopass); Expert Decl. of Milton Gosney (Doc. 127), ¶ 5 (Sidense).

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[1] Plaintiff agreed to this definition, which had been proposed by defendant, upon defendant's assurances that "not in physical contact" does not mean not in electrical contact.

[2] The term **semiconductor** never appears in the patent claims outside of the phrase **doped semiconductor region**.

[3] The parties also agreed that their proposed definitions for **programmable memory cell** were nearly indistinguishable, though each insisted that its definition was preferable.

II. Disagreements

The remaining constructions about which the parties disagree are of the terms: **bitline/column bitline**; **wordline/row wordline**; **transistor**; **memory cell**; **programmed doped region**; **doped semiconductor region**; **gate**; **channel region**; **substrate**; **lightly doped region**; **conductive material**; and **row wordline segment**. The parties included in their list of the ten claim terms whose constructions they believed to be most significant to the resolution of this case, and to be case- or claim-dispositive, the terms **bitline/column bitline**; **wordline/row wordline**; **transistor**; **memory cell**; **programmed doped region**; **doped semiconductor region**; **gate**; and **channel region**. These terms are used throughout the three patents, and, as explained above, the parties agree that each term need only be defined once.

A. Infringement contentions

In its infringement contentions, plaintiff alleges that defendant is infringing, contributing to the infringement of, and inducing the infringement of: (1) claims 1, 2, 7, 8, 12, and 14 of the '757 Patent; (2) claims 1, 3, 5, and 6 of the '540 Patent; and (3) claims 1, 2, 3, 5, 6, 9, 10, 12, and 14 of the '751 Patent. *See* Infringement Contentions (Doc. 97). Those claims are listed below. Nearly every word or phrase was identified in the parties' joint claim construction statement as disputed. The eight remaining disputed, significant, and potentially dispositive terms are highlighted in bold.

1. The '757 patent: claims 1, 2, 7, 8, 12, and 14

> 1. A programmable **memory cell** useful in memory array having **column bitlines** and **row wordlines**, the **memory cell** comprising:
>
> a **transistor** having a **gate**, a gate dielectric between the **gate** and over a substrate, and first and second **doped semiconductor regions** formed in said substrate adjacent said **gate** and in a spaced apart relationship to define a **channel region** therebetween and under said **gate**, the **gate** being formed from one of said **column bitlines**;
>
> a row wordline segment coupled to the second **doped semiconductor region** of the **transistor**, said row wordline segment connected to one of said **row wordlines**; and
>
> a **programmed doped region** formed in said substrate in said **channel region** when said **memory cell** has been programmed.

2. The **memory cell** of claim 1 wherein said **column bitlines** are connected to said **gate** by a column bitline segment.

[. . .]

7. The **memory cell** of claim 1 wherein said first **doped semiconductor region** is floating.

8. A programmable memory array comprising a plurality of **row wordlines**, a plurality of **column bitlines**, and a plurality of **memory cells** at respective crosspoints of the **row wordlines** and **column bitlines**, each of the **memory cells** comprising:

> a **transistor** having a **gate**, a gate dielectric between the **gate** and over a substrate, and first and second **doped semiconductor region**s formed in said substrate adjacent said **gate** and in a spaced apart relationship to define a **channel region** therebetween and under said **gate**, the **gate** being formed from one of said **column bitline**s;
>
> a row wordline segment coupled to the second **doped semiconductor region** of the **transistor**, said row wordline segment connected to one of said **row wordline**s; and
>
> wherein said **memory cell**s further including a **programmed doped region** formed in said substrate in said **channel region** when said **memory cell** has been programmed.

[...]

12. The memory array of claim 8 wherein said **transistor**s have their **gate** and said second **doped semiconductor region** is laterally separated by a distance D.

[...]

14. The memory array of claim 8 wherein the **transistor**s have their first **doped semiconductor regions** floating.

'757 Patent, Col. 10 ln. 36–Col. 12 ln. 21.

2. The '540 Patent: claims 1, 3, 5, and 6

1. A programmable **memory cell** useful in a memory array having **column bitlines** and **row wordlines**, the **memory cell** comprising:

> a **transistor** having a **gate**, a gate dielectric between the **gate** and over a substrate such that there is a stack comprising said **gate**, gate dielectric, and substrate, without any intervening conductive material, and first and second **doped semiconductor regions** formed in said substrate adjacent said **gate** and in a spaced apart relationship to define a **channel region** therebetween and under said **gate**, the **gate** being formed from one of said **column bitlines**;
>
> a row wordline segment coupled to the second **doped semiconductor region** of the **transistor**, said row wordline segment connected to one of said **row wordlines**; and

a **programmed doped region** formed in said substrate in said **channel region** when said **memory cell** has been programmed.

[...]

3. The **memory cell** of claim 1 wherein the **gate** and said second **doped semiconductor region** is laterally separated by a distance D.

[...]

5. The **memory cell** of claim 1 wherein said first **doped semiconductor region** is floating.

6. The **memory cell** of claim 1 further including a lightly doped region formed in said substrate in said **channel region**.

'540 Patent, Col. 10 ln. 61–Col. 12 ln. 31.

3. The '751 Patent: claims 1, 2, 3, 5, 6, 9, 10, 12, and 14

1. A programmable **memory cell** useful in a memory array having **column bitlines** and **row wordlines**, the **memory cell** comprising:

a **transistor** have a **gate**, a gate dielectric between the **gate** and over a substrate, and first and second **doped semiconductor regions** formed in said substrate adjacent said **gate** and in a spaced apart relationship to define a **channel region** therebetween and under said **gate**; and

wherein the second **doped semiconductor region** of the **transistor** is connected to one of said **row wordlines**, and where in said gate dielectric is formed such that the gate dielectric is more susceptible to breakdown near the first **doped semiconductor region** than said second **doped semiconductor region**.

2. The **memory cell** of claim 1 wherein said **row wordlines** are formed from a buried N+ layer.

3. The **memory cell** of claim 1 wherein the gate dielectric of the **transistor** is thicker proximal to the second **doped semiconductor region** than to the first **doped semiconductor region**.

[...]

5. The **memory cell** of claim 1 wherein said **gate** is formed from one of said **column bitlines**.

6. The **memory cell** of claim 1 wherein said **memory cells** further including a **programmed doped region** formed in said substrate in said **channel region** when said **memory cell** has been programmed.

[...]

9. A programmable memory array comprising a plurality of **row wordlines**, a plurality of **column bitlines**, and a plurality of **memory cells** at respective crosspoints of

the **row wordlines** and **column bitlines**, each of the **memory cells** comprising:

a **transistor** having a **gate**, a gate dielectric between the **gate** and over a substrate, and first and second **doped semiconductor regions** formed in said substrate adjacent said **gate** and in a spaced apart relationship to define a **channel region** therebetween and under said **gate**, the **gate** being formed from one of said **column bitlines**; and

wherein the second **doped semiconductor region** of the **transistor** is connected to one of said **row wordlines**, said gate dielectric is formed such that the **gate** dielectric is more susceptible to breakdown near the first **doped semiconductor region** than said second **doped semiconductor region**.

10. The memory array of claim 9 wherein said **row wordlines** are formed from a buried N+ layer.

[...]

12. The memory array of claim 9 wherein the gate dielectric of the **transistor** is thicker proximal to the second **doped semiconductor region** than to the first **doped semiconductor region**.

[...]

14. The memory array of claim 9 wherein said **memory cells** further including a **programmed doped region** formed in said substrate in said **channel region** when said **memory cell** has been programmed.

'751 Patent, Col. 14 ln. 29–Col. 16 ln. 27.

B. Disputed terms

1. Bitline/column bitline and wordline/row wordline

The parties agree that **bitline** and **column bitline** are interchangeable terms, and that **wordline** and **row wordline** are interchangeable as well.[4] Plaintiff argues that all four terms mean the same thing: "a line that connects to one terminal of each memory cell in a memory array." Defendant argues that **bitline** and **column bitline** should be defined as "the line that connects the memory cell to the sensing circuit during the read operation"; and that **wordline** and **column wordline** should be defined differently, as "the line connected to the memory cell, which is selected by the row addresses."

Plaintiff argues that "[a]s long as the wordlines and bitlines are arranged so that all memory cells connected to such wordlines and bitlines can be addressed, the wordlines and bitlines are

[4] The term **bitline** never appears in the patent claims outside of the phrase **column bitline** and the term **wordline** never appears in the patent claims outside of the phrase **row wordline**.

interchangeable." Joint Appendix (Doc. 103-1), at 9. However, in briefing and at the claim construction hearing, plaintiff repeatedly acknowledges that wordlines and bitlines are distinguishable within a memory array because they are orthogonal. The Court will not define two different terms to mean precisely the same thing when they are not identical.

Defendant argues that plaintiff's patent claims are limited to memory cells where the bitline is connected to the gate and the wordline is connected to the source. However, defendant's proposed definitions do not merely relate to where the wordlines and bitlines are connected to each memory cell, but more specifically places them within an external structure and operating procedure. Defendant is contended to have infringed claims regarding the internal workings of memory cells and the memory arrays containing such cells, not external structures and operating procedures.[5]

The meaning of the terms contained in the patents in suit are as follows:

- **Bitline** and **column bitline** are defined identically as: "a line orthogonal to the row wordline that connects to a terminal of each memory cell in a memory array."
- **Wordline** and **row wordline** are defined identically as: "a line orthogonal to the column bitline that connects to a terminal of each memory cell in a memory array."

2. Transistor

Plaintiff argues that the term **transistor** should be given its ordinary and customary meaning, and provides a definition from an internet source: "a solid-state semiconductor device that can regulate electric current flowing through it." *See* Joint Appendix at 15 (citing http://www.businessdictionary.com/definition/transistor.html). Defendant argues that **transistor** should be defined as "a MOS transistor structure."[6] Defendant argues that each time the term is used in the patent claims, it is described as having a particular structure, and that only MOS transistors have that

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[5] The patentee for the '540 Patent and the '751 Patent makes certain claims for "method[s] of operating a programmable memory array," but plaintiff does not make infringement allegations with regard to those claims. It will be of little assistance to the adjudication of this case to adopt definitions containing highly technical terms such as "sensing circuit" that themselves are nowhere defined and are, at most, tangentially related to the claims at issue in this suit.

[6] Previously, defendant proposed the definition "a MOS transistor." Joint Appendix at 15.

structure. Defendant argues there is no indication that the patentee contemplated any alternative to the MOS transistor structure. Plaintiff argues that defendant's definition is tautological and artificially limited, and that it would limit the invention to a single embodiment.

The parties do not merely disagree over whether transistor, as used in the patent claims, refers only to a MOS transistor. They have an identical disagreement with regard to the **memory cell**, **doped semiconductor region**, **gate**, **channel region**, and **substrate**, as defendant wishes the Court to construe each as limited to how the element appears in or in relation to a MOS transistor or MOS transistor structure. Of particular import appears to be the question of whether the claims are limited to memory cells containing transistors that have both source and drain regions.

The parties agree that the transistors in the memory cells claimed in plaintiff's patents are not traditional MOS transistors. For example, certain claims are for memory cells in which one doped semiconductor region is left "floating," *e.g.* '757 Patent, claims 7 & 13 (which the parties agree means "not electrically connected to a voltage source"), which is different from a traditional MOS transistor. Plaintiff argues that it is incorrect, therefore, to limit its claims to memory cells with MOS transistor structures. Defendant argues that the differences between the transistors in the claimed memory cells and traditional MOS transistors all relate to the way the transistors are connected and operate, not to how they are structured, and therefore the claims are limited to memory cells containing MOS transistor structures.

Defendant's distinction between the structure of a transistor on the one hand, and the operation and connectivity of a transistor on the other, is artificial and confusing. The patentee discusses "floating" drains as both a structural requirement of certain claimed memory cells, *see* '757 Patent, claim 7 (memory cell); '540 Patent, claim 5 (memory cell); '757 Patent, claim 14 (memory cells in a memory array), and as an attribute of a claimed method of operation, *see* '540 Patent, claim 8.[7] To the extent that defendant is concerned about restricting the claims to transistors with certain components, claim 1 in each patent lists specific transistor components, as do claim 8 of the '757 Patent and claim 9 of the '751

[7] In the '757 Patent, claims 1-7 are for particular "programmable memory cell[s] useful in memory array," and claims 8-14 are for particular "programmable memory array[s]." In the '540 Patent, claims 1-6 are for memory cells, and claims 7-11 are for "method[s] of operating a programmable memory array."

Patent, and each infringement contention alleges infringement of either one of those claims, or of another claim that incorporates by reference those claimed memory cells or memory arrays. *See Hynix Semiconductor Inc. v. Toshiba Corp.*, No. C–04–04708 VRW, 2006 WL 2547463, * 10 (N.D. Cal. Sept. 1, 2006) (declining to construe a term "as necessarily including . . . limitations" that are themselves specified in the claim containing the term, because "it makes little sense" and is "redundant").

For these reasons, the term **transistor** does not mean "a MOS transistor structure." And for these same reasons, the terms **memory cell**, **doped semiconductor region**, **gate**, **channel region**, and **substrate**, do not mean those components or units only as they are contained in or otherwise a part of a MOS transistor or MOS transistor structure, or comprised of a MOS transistor, as urged by defendant and discussed in more detail below. Rather, **transistor** should be given its ordinary and customary meaning: "An active component of an electronic circuit consisting of a small block of semiconducting material to which electrical contacts are made, and which may be used as an amplifier, detector, or switch to control the flow of current." *See* Transistor, McGraw-Hill Dictionary of Scientific and Technical Terms 2176 (6th ed. 2003); Transistor, The Authoritative Dictionary of IEEE Standards Terms (7th ed. 2000).

3. Memory cell

Plaintiff argues that **memory cell** should be defined as "a basic unit of memory." At one point, defendant argued that **memory cell** should be defined as "a semiconductor memory device comprised of a single MOS transistor that stores data." Defendant now argues that the terms means "a single MOS transistor that stores data."

It appears that defendant is now arguing that the memory cell *is* the transistor that it comprises. Defendant does not explain then why two different terms are used, and defendant's expert does not make any assertions in support of this definition or any other definition of memory cell. Additionally, defendant proposes that the transistors in the memory cells are MOS transistors, and the Court has already rejected defendant's more limited contention that the transistors in the patent claims are structured—but not connected or operated—as MOS transistors.

Each patent claims a particular memory cell in claim 1, and variations of that memory cell in

subsequent claims. To define memory cell with reference only to a number of transistors is incorrect as a matter of law. To define memory cell differently for each claim is cumbersome; the parties agree that it is unnecessary; and to do so accurately essentially would involve transcribing the patent.

The Court determines that the term **memory cell** does not require construction. *See Phillips*, 415 F.3d at 1314 ("In some cases, the ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words.").

4. Programmed doped region

Plaintiff argues that **programmed doped region** should be defined as "a doped region in a channel region of a substrate under the gate caused by breaking down the gate dielectric." Defendant argues that **programmed doped region** should be defined as "a highly doped n+ (or p+) region formed in the channel region of the oppositely doped substrate of a [programmed] memory cell as a result of programming." Previously, defendant argues that **programmed doped region** should be defined as "a highly doped (n+ or p+) region formed in the substrate of a programmed memory cell as a result of programming."[8]

The main disagreements between the parties are whether the term **programmed doped region** is limited to "highly doped n+ (or p+) region," and whether it is limited to being formed in the channel region of the "oppositely doped substrate." In support of its argument, defendant derives limitations from the specifications, but the specifications do not disclaim or disavow the ordinary and customary meaning of the term. *See Phillips*, 415 F.3d at 1316; *Raytheon*, 724 F.2d at 957.

The parties have already agreed to the definition of the term programmed. Both parties use the phrase "doped region" to define the term programmed doped region. And, below, the Court defines **doped semiconductor region** by reference to the parties' agreed upon definition for **semiconductor**, and according to the ordinary and customary definition of **programmed . . . region**.

[8] Defendant noted in the joint claim construction filings that part of its argument was based on similarities of crosshatching in figures included in the '757 Patent. Defendant appears to have abandoned this argument before briefing.

Accordingly, the Court defines **programmed doped region** as "a doped region formed in the channel region of the substrate of a memory cell as a result of programming."

5. Doped semiconductor region

Plaintiff argues that **doped semiconductor region** means "a semiconductor region that contains a level of impurity." Defendant argues that it means "the source or drain structure of a MOS transistor structure." Defendant previously argued that it means "a region of semiconductor material, to which impurities are added to create one side of a p-n junction." Plaintiff does not object to defendant's prior definition, except to the extent that it believes that inclusion of the phrase "p-n junction" is confusing, and that the claims also leave room for the impurities to create p-p junctions and n-n junctions. The Court agrees.

The Court has already rejected defendant's argument that parts of the claimed transistors should be limited to being parts of MOS transistors or MOS transistor structures. The Court defines **doped semiconductor region** as "a region of semiconductor material to which impurities are added to modify the electron or hole concentration in that semiconductor."

6. Gate and channel region

Plaintiff argues that a **gate** is "an electrode region that is above the channel region," and that a **channel region** is "a region under the gate in the substrate where the channel is located." Defendant argues that the **gate** is "the MOS transistor electrode which controls conductivity of the channel region," and that the **channel region** is "in a MOS transistor, a region of the substrate beneath the gate defined by the space between first and second doped semiconductor regions, whose electrical conductivity is controlled by the gate." Previously, defendant defined channel region without the phrase "in a MOS transistor."

The Court has already rejected defendant's argument that parts of the claimed transistors should be limited to being parts of MOS transistors or MOS transistor structures. The Court has also rejected defendant's argument that terms should be defined in relation to methods of operation. The Court defines **gate** as "an electrode region that is above the channel region," and **channel region** as "a region

of the substrate beneath the gate defined by the space between the first and second doped semiconductor regions."

CONCLUSION

The Court hereby adopts the following constructions, with respect to every claim in each patent in which the word or phrase appears. Based on the agreement of the parties:

- **Memory array**: "a grid of memory cells that are organized in rows and columns"
- **Floating**: "not electrically connected to a voltage source"
- **Programmable memory array**: "a memory array comprised of programmable memory cells"
- **Memory cell which has been programmed**: "a programmable memory cell which, during programming, has been physically changed"
- **Breakdown**: "physically changing the electrical insulating characteristics of a gate dielectric under voltage induced stress"
- **Spaced apart relationship**: "not in physical contact"[9]
- **Gate dielectric**: "a gate insulating film"
- **Programmed**: [having had] "a physical conducting link between the gate and the channel formed by breaking down the gate dielectric"
- **Laterally separated by a distance D**: "no overlap in the vertical direction between the gate and the second doped region"
- **Semiconductor**: "a material, like silicon, whose conductivity is in the range between that of metals and insulators, and whose conductivity can be altered by the introduction of an impurity."

For the reasons stated above:

- **Bitline** and **column bitline**: "a line orthogonal to the row wordline that connects to a terminal of each memory cell in a memory array."
- **Wordline** and **row wordline**: "a line orthogonal to the column bitline that connects to a

[9] Plaintiff agreed to this definition, which had been proposed by defendant, upon defendant's assurances that "not in physical contact" does not mean not in electrical contact.

terminal of each memory cell in a memory array."

- **Transistor**: "An active component of an electronic circuit consisting of a small block of semiconducting material to which electrical contacts are made, and which may be used as an amplifier, detector, or switch to control the flow of current."
- **Doped semiconductor region**: "a region of semiconductor material to which impurities are added to modify the electron or hole concentration in that semiconductor."
- **Gate**: "an electrode region that is above the channel region"
- **Channel region**: "a region of the substrate beneath the gate defined by the space between the first and second doped semiconductor regions."

Also, for the reasons stated above, the Court declines to construe the terms **memory cell** and **programmed doped region**. And the Court declines to construe the terms the usage of which the parties continue to dispute that are not listed by the parties as most significant to the resolution of this case.

IT IS SO ORDERED.

Dated: August 31, 2011

SUSAN ILLSTON
United States District Judge