IN THE UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

SHARED MEMORY GRAPHICS LLC,

Plaintiff,

v.

APPLE INC., ET AL.,

Defendants.
_____/

No. C -10-02475 MMC (JSC)

ORDER GRANTING IN PART DEFENDANTS' MOTIONS TO STRIKE (Dkt. Nos. 419, 421)

In this patent infringement dispute, Plaintiff Shared Memory Graphics LLC ("SMG") contends that the Sony and Nintendo defendants ("Defendants") infringe claim 3 of U.S. Patent No. 5,712,664 ("the '664 patent") and claims 2, 6, and 8 of U.S. Patent No. 6,081,279 ("the'279 patent"). Sony moves to strike SMG's amended patent infringement contentions ("PICs") and to dismiss SMG's claims against Sony. (Dkt. No. 421.) Nintendo likewise moves to strike SMG's amended PICs and preclude SMG from further amending its PICs. (Dkt. 419.) After carefully considering the papers submitted by the parties, and having had the benefit of oral argument on August 25, 2011, the Court GRANTS Defendants' motions to strike in part without leave to amend.

BACKGROUND

1. The'664 and '279 Patents

The '664 patent, entitled Shared Memory Graphics Accelerator System and originally filed in 1993, was issued to Alliance Semiconductor Corporation ("Alliance") in 1998. The'279 patent, originally filed in 1997, and also entitled Shared Memory Graphics Accelerator System and a closely related companion to the '664 patent, was also issued to Alliance in 2000. (Dkt. No. 1 at ¶¶ 35, 38.)

These patents claim to rectify a bandwidth shortcoming in art graphics systems used to process images for display in video games. Prior to the technological improvements reportedly addressed by the patents-in-suit, image data was stored in a single-memory element before it was displayed on a viewing device like a television screen. A graphics processor transferred pixel data that comprised an image to a frame buffer memory, which was on a separate chip connected to a graphics accelerator by a "data bus" connection. A frame buffer memory provides temporary storage to link between the image memory location and a colored pixel that will appear on a viewing device. The'664 patent claims to make this transfer process faster by dividing the frame-buffer memory such that one part is on the same chip as the graphics accelerator ("on-chip") while the other portion of the frame-buffer memory is stored on a separate chip ("off-chip"). These two portions of frame buffer memory communicate with the graphics accelerator via a "data distribution bus." This split allows the selective distribution of fast-moving and slow-moving data between on-chip and off-chip frame buffer memory elements, thus increasing speed and efficiency for picture quality. The'279 patent claims to further increase efficiency by enabling the on-chip frame buffer to have a higher refresh frequency than the off-chip frame buffer, which reduces on-chip power loss over time.

Among other elements, the parties agree that each claim at issue requires a display data distribution bus connecting the on-chip and off-chip frame buffer memory elements to a graphics accelerator. (Dkt. No. 444 at 7:6-13.) For example, Claim 3 of the '664 patent requires

> an on-chip frame buffer element connected to receive graphics display data from the graphics accelerator via a *display data distribution bus*; and off-chip frame buffer memory element connected to receive graphics display data from the graphics accelerator via *the data distribution bus.*

'664 patent at 6:34-40 (emphasis added); see also '279 patent at 6:1-7; 7:2-7; 7:27-33.

Three of the four claims at issue also require the graphics accelerator to "selectively distribute" display data to the on-chip frame buffer memory and the off-chip frame buffer memory. '664 patent at 6:41-4; '279 patent at 6:8-12; 7:34-38. In addition, the three '279 patent claims at issue require the on-chip frame buffer memory to have a higher refresh frequency than the off-chip frame buffer memory in order to reduce on-chip power dissipation. '279 patent at 6:21-23; 7:8-12;

8:1-4.

Alliance sold the‘664 and ‘279 patents to Acacia Patent Acquisition Corporation (“Acacia”) in 2007. (Dkt. No. 1 at ¶ 45.) Acacia is a publicly traded patent-holding company that acquires patents and then creates subsidiaries that bring suits on behalf of these patents for patent infringement and which claims “$90 million in cash and additional funds” and advertises itself as “able to bring and sustain legal actions against infringers.” (Dkt. No. 435 at 13.) On May 13, 2009, Acacia transferred all rights to the ‘664 and ‘279 patents to newly-created subsidiary SMG. (Dkt. No. 1 at ¶ 47.)

2. Procedural History

According to Sony, in the fall of 2001 Alliance approached Sony about alleged infringement of the ‘279 patent by Sony’s PlayStation 2 product. Sony informed Alliance that the PlayStation 2 “did not have, among other things, an ‘off-chip frame buffer memory element’ as required by each of the claims in the ’279 patent.” (Dkt. No. 301 at 4.) Communications between the two companies regarding the patent ceased in 2003. In 2005 and 2006, Alliance again contacted Sony, at one point claiming to be in the process of “extensive analysis” of PlayStation products, but Sony did not hear anything further until this lawsuit. (Dkt. No. 301 at 5.) SMG subsequently filed this action in the Western District of Arkansas in July 2008. SMG alleges infringement of claim 3 of the ‘664 patent and claims 2, 6 and 8 of the ‘279 patent, and it seeks both damages and injunctive relief. The initial complaint named Apple, Sony, and Nintendo as defendants. A subsequent amendment added Samsung as a defendant.

On May 27, 2010, and pursuant to a motion by Defendants, the Arkansas district court transferred this lawsuit to the Northern District of California. Approximately 10 months later, defendants Apple and Samsung reached an agreement under which SMG’s claims against Apple and Samsung were dismissed with prejudice as were these defendants’ counterclaims against SMG.

SMG challenges two of Nintendo's products, both of which are video-game operating systems: the GameCube and the Wii. SMG now challenges only one Sony product, the pre-MCL iteration of the PlayStation, which is also a video-game operating system.[1]

Upon the lawsuit's transfer to the Northern District of California, the local patent rules became applicable, including Local Rule 3-1 ("L.R. 3-1"). Rule 3-1 required SMG to provide PICs to Defendants within 14 days of the September 2, 2010 case management conference. SMG provided Sony with initial infringement contentions on September 16, 2010, and, after Sony complained about perceived shortcomings, SMG provided a first amended version on October 8, 2010. (Dkt. No. 301.) SMG provided Nintendo with PICs on September 19, 2010 and an amended version on October 1, 2010. (Dkt. No. 296.)

In November 2010, Sony and Nintendo moved to compel SMG to provide amended PICs on the ground that SMG's PICs did not satisfy L.R. 3-1. Defendants argued that SMG failed to identify where in the accused products certain key limitations are found; in particular, they asserted that SMG had not identified the required "display distribution bus" limitations as well as the "selectively distributes" and "fast and slow moving images" limitations of the claims at issue. (Dkt. Nos. 295, 301, 316.)

SMG responded that under the circumstances it had sufficiently complied with L.R. 3-1. First, it complained that Defendants had stonewalled SMG's discovery requests. (Dkt. Nos. 11 at 3 & 312 at 2.) Relying on Renesas Technology Corp. v. Nanya Technology Corp., 2004 WL 2600466 (N.D. Cal. Nov. 10, 2004), SMG also argued that it is not required to reverse engineer every accused product and can instead rely on other materials in formulating PICs. (Dkt. Nos. 311 at 5 & 312 at 6.) SMG specifically argued that due to the miniscule size of modern-day electronics, it would be prohibitively expensive for SMG to perform reverse engineering or other work necessary to identify the specific components that satisfy the limitations at issue in the motions to compel. (Dkt. No. 312 at 6, 8.) SMG asserted further that it had sufficiently complied with LR 3-1 and that as a matter of law a patent infringement plaintiff may "assume" the presence of a limitation, such as the display

[1]Sony and SMG entered into a stipulation on July 28, 2011 under which all claims and counterclaims against one another were dismissed with respect to Sony Play Station 2 and 3 products. (Dkt. No. 438.)

data distribution bus, in an accused product. (Dkt. Nos. 311 at 7 & 312 at 8.) Finally, SMG argued that the "selectively distributes" and "refresh frequency" claim language does not create required elements because the language follows a "wherein" clause and, in any event, SMG had sufficiently identified where in the accused products the limitations are found. (Dkt. Nos. 311 at 8-9 & 312 at 8.)

Following oral argument on Defendants' motions to compel, former Magistrate Judge Edward Chen, to whom the case was then assigned for discovery purposes, granted Defendants' motions in a written order. (Dkt. No. 346.) Judge Chen specifically held that SMG had failed to identify the required data distribution bus:

> [S]everal of Plaintiff's ICs are too vague to provide fair notice as to what components and circuitry of the accused products infringe their patents. For instance, the claim charts fail to specifically identify the display data distribution bus limitation in Defendants' products. . . Rather than provide a meaningful description of its theories, SMG's vague contentions and conclusory statements invite Defendants and the Court merely to *assume* the presence of a data distribution bus. . . . The Court therefore finds that SMG's disclosure falls short of the level of specificity required by Local Rule 3-1.

(Dkt. No. 346 at 6.) The court also specifically rejected SMG's argument that the elements following a "wherein" clause are not mandatory. (Id.) Accordingly, the court ordered SMG to file an Amended Disclosure of Claims and Infringement Contentions consistent with the court's order. (Id.)

The district court disqualified SMG's counsel in December 2010 due to the firm's previous dealings with Nintendo. SMG eventually retained new counsel and filed further amended infringement contentions on June 13, 2011. (Dkt Nos. 415 & 416.) Defendants now move to strike these amended PICs with respect to the "data distribution bus" and "selectively distributes" and "refresh frequency" limitations on the ground that SMG's contentions are not materially different from those presented to Judge Chen and thus still fail to comply with Local Rule 3-1.

DISCUSSION

Local Rule 3-1 requires, in pertinent part:

> . . . a party claiming patent infringement shall serve on all parties a 'Disclosure of Asserted Claims and Infringement Contentions' . . . [which] shall contain the following information:

> (a) Each claim of each patent in suit that is allegedly infringed by each opposing party, including for each claim the applicable statutory subsections of 35 U.S.C. §271 asserted;
>
> (b) Separately for each asserted claim, each accused apparatus, product, device, process, method, act, or other instrumentality ("Accused Instrumentality") of each opposing party of which the party is aware. This identification shall be as specific as possible. Each product, device, and apparatus shall be identified by name or model number, if known. Each method or process shall be identified by name, if known, or by any product, device, or apparatus which, when used, allegedly results in the practice of the claimed method or process;
>
> (c) A chart identifying specifically where each limitation of each asserted claim is found within each Accused Instrumentality, including for each limitation that such party contends is governed by 35 U.S.C. § 112(6), the identity of the structure(s), act(s), or material(s) in the Accused Instrumentality that performs the claimed function.

As Judge Chen concluded, and SMG agrees, "all courts agree that the specificity under Local Rule 3-1 must be sufficient to provide reasonable notice to the defendant why the plaintiff believes it has a 'reasonable chance of proving infringement.'" (Dkt. No. 346 at 4 (quoting View Engineering, Inc. v. Robotic Vision Systems, Inc., 208 F.3d 981, 986 (Fed. Cir. 2000).) The infringement contentions "must be sufficient to raise a 'reasonable inference that all accused products infringe.'" (Dkt. No. 346 at 4 (quoting Antonious v. Spalding & Evenflo Cos., Inc., 275 F.3d 1066, 1075 (Fed. Cir. 2002).)

The dispute here is whether SMG has sufficiently complied with Rule 3-1(c), that is, whether it has identified specifically "where each limitation of each asserted claim is found within each Accused Instrumentality." In particular, whether SMG has complied with Judge Chen's order that SMG identify which circuitry in the GameCube and Wii (for Nintendo) and the Playstation (for Sony) constitute the data distribution bus that connects the on-chip and off-chip frame buffer memory to the graphics accelerator. The Court finds that it has not.

A. The data distribution bus and the on-chip and off-chip frame buffer memory

As explained above, all claims at issue require that the on-chip frame buffer memory and the

off-chip frame buffer memory be connected to a graphics accelerator via a data distribution bus.[2] See supra at 2. As SMG admitted at oral argument, the amended PICs presently before this Court are essentially identical to those before Judge Chen with respect to these particular data distribution bus limitations. (Dkt. No. 444 at 20:12-25, 22:2-5, & 30:23-31:2.) The PICs before Judge Chen did not identify any circuitry that allegedly satisfy these data distribution bus limitations and the further amended PICs before this Court still do not identify any specific circuitry as constituting the above required data distribution bus; instead, SMG's amended PICs simply state that "these connections are too small to be seen" in the accused devices. (See, e.g., Dkt. No. 416-1 at 10.)

SMG's insistence that it need not identify the specific circuitry that purportedly satisfy these limitations because to do so would take months and cost hundreds of thousands, or even millions, of dollars is not well taken.

First, as explained above, supra at 4, SMG made this same "it is too expensive" argument to Judge Chen, who nonetheless ordered SMG to identify the specific circuitry that supposedly constitute the data distribution bus connecting the graphics accelerator to the on-chip and off-chip frame buffers. (Dkt. No. 346 at 4 (stating that "Rule 3-1 does not necessarily require the patent holder to produce evidence of infringement, but it must map specific elements of Defendants' alleged infringing products onto the Plaintiff's claim construction").)

Second, SMG's argument contradicts the plain language of Local Rule 3-1(c). The Rule requires the party claiming infringement to produce a chart "identifying specifically where each limitation of each asserted claim is found within each Accused Instrumentality." There is no exception in the Rule for parties who do not want to spend the time and resources necessary to identify specifically where each limitation is found. In Bender v. Maxim Integrated Products, Inc., 2010 WL 2991257 (N.D. Cal. July 29, 2010), for example, the district court specifically rejected this very argument:

> Plaintiff's difficulties in attempting to amend his infringement contentions arise from his unwillingness or inability to reverse engineer the accused products in order to

[2]The parties dispute whether the same data distribution bus must connect the on-chip and off-chip frame buffers to the graphics accelerator. This claim construction dispute is immaterial to the present motions because for the most part SMG has not identified any data distribution bus.

> determine how he believes they infringe . . . Plaintiff is correct that there is no absolute requirement that a plaintiff engage in reverse engineering of an accused product prior to filing an infringement claim . . . Cases in which reverse engineering was not required, however, have tended to involve situations in which analyzing the accused product was either impracticable or unnecessary to create a basis for adequate ICs.

Id. at *5. The plaintiff in Bender, as SMG here, complained that reverse engineering was too expensive, but the district court was not persuaded: "While the Court recognizes that reverse engineering may well pose a financial hardship to plaintiff, it appears that he cannot maintain this lawsuit without undertaking reverse engineering or some equivalent that will enable him to better articulate his claims." Id; see also Network Caching Technology, LLC, 2002 WL 32126128 at *5 (N.D. Cal. Aug. 13, 2002) (holding that reverse engineering or its equivalent is required); Intertrust Technologies Corp. v. Microsoft Corp., 2003 WL 23120174 at *2 (N.D. Cal. Dec. 1, 2003) (stating that "[a]t the Patent Local Rule 3-1 Disclosure stage, a plaintiff must put forth information so specific that either reverse engineering or its equivalent is required"). As Judge Chen previously ruled, SMG was similarly required to perform reverse engineering or its equivalent if it wants to pursue its patent infringement claims.

SMG next argues that it is reasonable to *assume* that there is at least one data distribution bus that connects the on-chip frame buffer memory and the off-chip frame buffer memory to the graphics accelerator even if SMG cannot at this stage in the litigation identify any particular circuitry as the required data distribution bus. Judge Chen, however, specifically rejected this argument too:

> Rather than provide a meaningful description of its theories, SMG's vague contentions and conclusory statements invited Defendants and the Court merely to *assume* the presence of a data distribution bus. . . . The Court therefore finds that SMG's disclosure falls short of the level of specificity required by Local Rule 3-1.

(Dkt. No. 346 at 6:2-7.) Moreover, SMG's argument is, again, inconsistent with the case law. In Bender, for example, the court held that a "plaintiff cannot simply rely on [defendant's] publicly-available datasheets to diagram his claims, and then attempt to escape his obligation to locate each element of each claim within the accused device by stating that he assumes an element of the claim must be present, although not depicted." Bender, 2010 WL 2991257 at *2. It is thus unsurprising that at oral argument SMG was unable to identify any case to suggest that under Local

Rule 3-1(c) a patent infringement plaintiff may simply assume that a limitation is present in an accused device without specifically identifying what in the device satisfies the limitation. (Dkt. No. 444 at 26:8-9.)

SMG's reliance on Renesas Technology Corp. v. Nanya Technology Corp., 2004 WL 2600466 (N.D. Cal. Nov. 10, 2004) highlights the continued inadequacy of SMG's PICs. In Renesas the patent infringement plaintiff expended the resources necessary to reverse engineer three of several accused products and thus was able to specifically identify where in each of those accused products each limitation was allegedly met. Id. at *3. The court held that the plaintiff was not required to reverse engineer "every one of defendant's products" because the plaintiff had provided declarations that established that "it is the practice in this industry not to change product circuitry when going from one version of a product to the next." Id. at *4. Here, in contrast, SMG has been unable to identify *any* circuitry as the data distribution bus that connects the on-chip frame buffer to the graphics accelerator in any product of any defendant, let alone offer expert testimony that a data distribution bus found in one device is likely to be present in another. And while it has identified circuitry that it contends constitute the data distribution bus connecting the GDDR off-chip frame buffer to the graphics accelerator in the GameCube, it offers no competent evidence that the same circuitry would be present in Nintendo's Wii or Sony's PlayStation. Instead, SMG simply recites the claim language and baldly asserts that the data distribution bus limitations are satisfied. This it cannot do. See Network Caching, 2002 WL 32126128 at *6 (stating that "it is inappropriate to 'simply mimic[ ] the language of the claim,' providing 'no further information to defendants than the claim language itself.'").

Finally, SMG contends that the Court should require defendants to produce discovery that would reveal whether the data distribution bus limitations are found in each accused device. SMG's theory is that since Defendants know what is in their devices, the Court should just make them show their hand. This argument, however, as does SMG's others, violates Local Rule 3-1(c). The Rule requires the patent infringement plaintiff to specify where each limitation of each asserted claim is found in each accused device within 14 days of the case management conference, that is, generally before discovery has commenced. Moreover, courts in this District routinely stay discovery *until* the

plaintiff has met its Rule 3-1(c) obligations. See, e.g., Network Caching Technology, LLC, 2002 WL 32126128 at * 7. Indeed, discovery in this case has been stayed pending SMG's efforts to submit adequate PICS. (Dkt. No. 346 at 7 & Dkt. 408.) There is simply no support, in the case law or otherwise, for SMG's request that it be excused from complying with Local Rule 3-1(c) for certain limitations, and that instead Defendants bear the burden of establishing through discovery whether their devices practice the limitations at issue. To the contrary, SMG's theory directly contradicts the well-established law that for certain technologies, such as those at issue here, patent infringement plaintiffs must perform reverse engineering or its equivalent to satisfy its PICs burden. See supra at 7-8.

In sum, as it is undisputed that SMG's claim chart neither identifies the circuitry in the accused devices which supposedly satisfy the limitation that the on-chip frame buffer memory be connected to the graphics accelerator via a data bus distribution, nor the circuitry in the accused devices which supposedly satisfy the limitation that the off-chip frame buffer memory be connected to the graphics accelerator via a data bus distribution (except for Nintendo's GameCube), Defendants' motions to strike SMG's PICs with respect to the on- and off-chip data distribution bus limitations are granted.

B. The "selectively distributes" and "sequence frequency" limitations

Defendants contend that SMG has not modified its claim charts with respect to the "selectively distribute display data" and "refresh frequency" limitations and therefore has not complied with Judge Chen's Order that SMG address these limitations. (Dkt. No. 346 at 6:9-17.) SMG admits that it is relying on essentially the same allegations that were before Judge Chen (Dkt. No. 444 at 60-61), but asserts that it has in fact identified "where these limitations are found" in the accused devices by identifying the graphics accelerator and the on- and off-chip frame buffers that allegedly perform these limitations.

It is unclear from Judge Chen's written order whether he specifically found that SMG's PICs with respect to these limitations were inadequate, or whether he merely addressed SMG's novel argument that because the elements are preceded by a "wherein" clause they are not required. (Dkt. No. 346 at 6.) Further, the Court is unclear how a patent infringement plaintiff would identify where such limitations are found in an accused device other than to do what SMG did here, that is, identify

where the graphics accelerator and on- and off-chip frame buffers are found. At oral argument Nintendo argued that SMG could submit evidence that it had tested Defendants' devices and found that the refresh frequency for the off-chip frame buffer memory is less than for the on-chip, and by how much. Such evidence, Nintendo argued, would at least support a reasonable inference that the accused products infringe. (Dkt. No. 444 at 50.) Nintendo, however, seems to be arguing that SMG must do more than show where in the accused device the limitation is found as required by Local Rule 3-1(c). Defendants may be correct that SMG should have engaged in such inquiry before filing suit. They may also be correct that what SMG has submitted thus far is insufficient to support a reasonable inference of infringement. But the Court is not fully persuaded that SMG was required to submit such evidence to comply with Local Rule 3-1(c). See Network Caching Tech Corp., 2003 WL 21699799 at * 4 (holding that to comply with Local Rule 3-1 the plaintiff is not required to produce evidence of infringement or to support its contentions); Samsung SDI Co., LTD., 2006 WL 5097360 at * 4 (C.D. Cal. June 5, 2006) (same).

This discussion, however, appears academic because the Court has found that SMG did not comply with Local Rule 3-1(c) with a very basic limitation, that is, showing where in the accused devices the data distribution bus connecting the on- and off-chip frame buffers to the graphics accelerator can be found. If they are not so connected then presumably the devices also do not satisfy these additional limitations, at least in any meaningful way.

C. Leave to Amend

Now that the Court has found that SMG's second amended PICs still fail to comply with Local Rule 3-1(c) with respect to the data distribution bus limitations, and therefore that the PICs with respect to those limitations should be stricken, the question is whether SMG should be granted leave to file third amended PICs. The Court concludes that it should not. First, SMG has not even asked for leave to amend. (Dkt. Nos. 431 & 432.) To the contrary, it has steadfastly maintained that it should not be required to incur the time and expense required to engage in the reverse engineering or its equivalent necessary to specifically identify the circuitry in the accused products which purportedly satisfy the data distribution bus limitations or that it is appropriate to assume that the circuitry can be found in the accused products. Moreover, it has already amended its PICs twice,

and the patents-in-suit and the accused products have existed for many years.

Sony also asks for an order dismissing SMG's claims. Nintendo has not asked for a similar order; instead, at oral argument Nintendo explained that it will take this final version of SMG's PICs and move for summary judgment. The Court agrees that this is the better procedure. Accordingly,

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the Court recommends that Sony's request for dismissal be denied without prejudice.[3]

CONCLUSION

For the foregoing reasons, Defendants' Motions to Strike are GRANTED in part without leave to amend. SMG's infringement contentions relating to the following limitations are stricken:

1. "Data distribution bus" connecting the graphics accelerator to the on-chip frame buffer memory for all remaining accused devices; and
2. "Data distribution bus" connecting the graphics accelerator to the off-chip frame buffer memory for all remaining accused devices other than the Nintendo GameCube.

The stay of discovery shall remain in effect until further court order. This Order disposes of Docket Nos. 419 and 421.

IT IS SO ORDERED.

Dated: September 2, 2011

Jacqueline S. Corley

JACQUELINE SCOTT CORLEY
UNITED STATES MAGISTRATE JUDGE

[3] As the request for dismissal involves a dispositive ruling, this magistrate judge may only "report and recommend" a ruling on this issue. (Dkt. No.423 n.1.)