

United States District Court  
For the Northern District of California

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IN THE UNITED STATES DISTRICT COURT  
FOR THE NORTHERN DISTRICT OF CALIFORNIA  
SAN FRANCISCO DIVISION

RAMBUS, INC.,

No. C 10-05446 RS  
No. C 10-05449 RS

Plaintiff,

v.

**CLAIM CONSTRUCTION ORDER**

LSI CORPORATION,

Defendant.

RAMBUS, INC.,

Plaintiff,

v.

STMICROELECTRONICS N.V., and  
STMICROELECTRONICS, INC.,

Defendants.

I. INTRODUCTION

This claim construction is only the latest salvo in a long-standing patent war over Dynamic Random Access Memory (“DRAM”), initiated by patentee Rambus against the many suppliers of constituent technologies. Defendants LSI Corporation and STMicroelectronics furnish chip makers with “memory controllers,” which generally facilitate communications between the processor and the DRAM, and which allegedly infringe ten Rambus patents from the heavily-litigated Farmwald-

1 Horowitz family of patents, including U.S. Patent No. 6,426,916 (“the ’916 patent”).<sup>1</sup> Pursuant to  
2 *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc), *aff’d*, 517 U.S.  
3 370 (1996), and Patent Local Rule 4-3, the parties have presented ten terms found in the claims of  
4 the patents for construction by the Court. After defendants filed their responsive brief to Rambus’s  
5 opening claim construction brief, the Court of Appeals for the Federal Circuit handed down an  
6 opinion reviewing *ex parte* reexamination of U.S. Patent No. 6,034,918 (“the ’918 patent”), also of  
7 the Farmwald-Horowitz family, addressing some of the issues disputed here. *See In re Rambus Inc.*,  
8 --- F.3d ----, 2012 WL 3329675 (Fed. Cir. 2012). Accordingly, defendants move, unopposed, for  
9 leave to file a joint sur-reply addressing that ruling, and Rambus also moves, unopposed to file a  
10 response. Those motions are hereby granted, and in consideration of the briefing, the arguments  
11 presented at the *Markman* hearing, and for all the reasons set forth below, the disputed terms are  
12 construed as follows.

## 13 II. BACKGROUND

14 The Farmwald-Horowitz patents are directed to Synchronous Dynamic Random Access  
15 Memory (“SDRAM”) chips and related interface and memory control technology. DRAM serves as  
16 the primary memory resource for temporary storage and data in use by the Central Processing Unit  
17 (“CPU” or “processor”). It is a relatively inexpensive and fast form of temporary memory used in a  
18 wide variety of common computer devices. For example, DRAM is used to store display data, and  
19 to make information retrieved from the slower hard drive readily accessible to software applications.  
20 DRAM cells are composed of one transistor and one capacitor in large, two-dimensional arrays,  
21 organized into columns and rows. Each cell stores a bit of data as a small charge, traditionally  
22 denoted as “0” for a low-voltage charge, or a “1” for a higher voltage charge. Over time, the  
23 capacitors lose their charge, and must be “dynamically” refreshed to preserve the integrity of the  
24 stored information. As a consequence of this charge “leaking,” DRAM loses information rapidly  
25 once the device is turned off, unlike non-volatile memory resources, such as flash memory.

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27 <sup>1</sup> The Farmwald-Horowitz patents all descended from U.S. Patent App. Ser. No. 07/510,898, and  
28 share similar written descriptions and diagrams. For simplicity’s sake, the Court adopts the parties’  
convention of referring exclusively to the ’916 patent.

1 Defendants' memory controllers are the accused device in this litigation, and although  
2 "controller/controller device" is a disputed claim term, generally speaking, the controller's function  
3 is to intermediate between the DRAM assembly and the processor. How precisely it achieves that  
4 goes to the heart of the dispute between Rambus and defendants. The memory controller may be  
5 integrated into the processor or exist as a separate, standalone chip. In either case, it communicates  
6 with the DRAM assembly via a series of traces or wires, commonly referred to as the "memory  
7 bus." The bus typically includes a separate "control bus," "address bus," and "data bus." The  
8 control bus also specifically includes a "Row Address Strobe" ("RAS") and "Column Address  
9 Strobe" ("CAS"), which direct the selection of particular memory cells for "reading" and "writing"  
10 operations.

11 Interposed between the bus and the memory array is a component of the DRAM assembly  
12 called the "sense amplifiers." The amplifiers access individual memory cells through "bit line"  
13 circuitry to facilitate read/write operations, by amplifying and "loading" the charge information in  
14 selected rows of DRAM cells (also called a "page" or "word lines"). To achieve this, the sense  
15 amplifiers are "precharged," or primed with an intermediate charge that enables the circuitry to  
16 perceive the stored charge (high or low) correctly. Once the row and column are selected, through  
17 operation of the control bus, address bus, and sense amplifiers, data is transmitted over the data bus.

18 Existing "asynchronous" DRAM systems generally perform read operations according to the  
19 following chronology: first, the RAS bus transitions from low to high voltage to prompt the sense  
20 amplifiers to precharge. It then transitions back to low voltage and holds there, activating and  
21 loading a particular row of memory cells into the sense amplifiers. The CAS bus then transitions  
22 from high voltage to low, identifying a particular column, which effectively selects a single memory  
23 cell. The data stored in that cell is then transmitted over the data bus. Write operations are executed  
24 in a similar fashion.

25 The claims of the Farmwald-Horowitz patents asserted in this litigation are directed to the  
26 controller and circuitry that communicates with the DRAM assembly, as well as methods for  
27 operating them. Unlike conventional asynchronous systems, the claimed inventions synchronize the  
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1 transmission of signals from the controller to the DRAM assembly with a “clock signal” for the  
2 purpose of improving the speed and efficiency of operations.

3 III. LEGAL STANDARD

4 Claim construction is a question of law to be determined by the Court. *Markman*, 52 F.3d at  
5 979. “Ultimately, the interpretation to be given a term can only be determined and confirmed with a  
6 full understanding of what the inventors actually invented and intended to envelop with the claim.”  
7 *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005) (quoting *Renishaw PLC v. Marposs*  
8 *Societa’ per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998)). Accordingly, a claim should be  
9 construed in a manner that “most naturally aligns with the patent’s description of the invention.” *Id.*

10 The first step in claim construction is to look to the language of the claims themselves. “It is  
11 a ‘bedrock principle’ of patent law that ‘the claims of a patent define the invention to which the  
12 patentee is entitled the right to exclude.’” *Phillips*, 415 F.3d at 1312 (quoting *Innova/Pure Water,*  
13 *Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). A disputed claim  
14 term should be construed in a manner consistent with its “ordinary and customary meaning,” which  
15 is “the meaning that the term would have to a person of ordinary skill in the art in question at the  
16 time of the invention, i.e., as of the effective filing date of the patent application.” *Phillips*, 415  
17 F.3d at 1312-13. The ordinary and customary meaning of a claim term may be determined solely by  
18 viewing the term within the context of the claim’s overall language. *See id.* at 1314 (“[T]he use of a  
19 term within the claim provides a firm basis for construing the term.”). Additionally, the use of the  
20 term in other claims may provide guidance regarding its proper construction. *Id.* (“Other claims of  
21 the patent in question, both asserted and unasserted, can also be valuable sources of enlightenment  
22 as to the meaning of a claim term.”).

23 A claim should also be construed in a manner that is consistent with the patent’s  
24 specification. *See Markman*, 52 F.3d at 979 (“Claims must be read in view of the specification, of  
25 which they are a part.”). Typically the specification is the best guide for construing the claims. *See*  
26 *Phillips*, 415 F.3d at 1315 (“The specification is . . . the primary basis for construing the claims.”).  
27 *See also Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996) (“[T]he

1 specification is always highly relevant to the claim construction analysis. Usually, it is dispositive;  
2 it is the single best guide to the meaning of a disputed term.”). In limited circumstances, the  
3 specification may be used to narrow the meaning of a claim term that otherwise would appear to be  
4 susceptible to a broader reading. *See SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*,  
5 242 F.3d 1337, 1341 (Fed. Cir. 2001); *Phillips*, 415 F.3d at 1316. Precedent forbids, however, a  
6 construction of claim terms that imposes limitations not found in the claims or supported by an  
7 unambiguous restriction in the specification or prosecution history. *Laitram Corp. v. NEC Corp.*,  
8 163 F.3d 1342, 1347 (Fed. Cir. 1998) (“[A] court may not import limitations from the written  
9 description into the claims.”); *Comark Commc’ns., Inc. v. Harris Corp.*, 156 F.3d 1182, 1186 (Fed.  
10 Cir. 1998) (“[W]hile . . . claims are to be interpreted in light of the specification, it does not follow  
11 that limitations from the specification may be read into the claims.”); *SRI Int’l v. Matsushita Elec.*  
12 *Corp. of Am.*, 775 F.2d 1107, 1121 (Fed. Cir. 1985) (en banc) (“It is the *claims* that measure the  
13 invention.”) (emphasis in original). A final source of intrinsic evidence is the prosecution record  
14 and any statements made by the patentee to the United States Patent and Trademark Office (PTO)  
15 regarding the scope of the invention. *See Markman*, 52 F.3d at 980.

16 The court also may consider extrinsic evidence, such as dictionaries or technical treatises,  
17 especially if such sources are “helpful in determining ‘the true meaning of language used in the  
18 patent claims.’” *Phillips*, 415 F.3d at 1318 (quoting *Markman*, 52 F.3d at 980). Ultimately, while  
19 extrinsic evidence may aid the claim construction analysis, it cannot be used to contradict the plain  
20 and ordinary meaning of a claim term as defined within the intrinsic record. *Phillips*, 415 F.3d at  
21 1322-23. Once the proper meaning of a term used in a claim has been determined, that term must  
22 have the same meaning for all claims in which it appears. *Inverness Med. Switzerland GmbH v.*  
23 *Princeton Biomeditech Corp.*, 309 F.3d 1365, 1371 (Fed. Cir. 2002). Several terms disputed in  
24 these related actions have already been construed in prior litigation involving other alleged  
25 infringers. While the parties agree that those constructions are not binding, and were adopted in  
26 consideration of different, allegedly infringing devices, and in some cases without the benefit of the  
27 arguments raised here, “uniformity in the treatment of a given patent” is also generally desirable.

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1 *Markman*, 517 U.S. at 390. Those previous constructions may be viewed as “persuasive and highly  
 2 relevant.” *Verizon Cal. Inc. v. Ronald Katz Tech. Licensing, P.A.*, 326 F. Supp. 2d 1060, 1069 (C.D.  
 3 Cal. 2003); *Comcast Cable Commc’ns Corp. v. Finisar Corp.*, No. C 06-04206, 2007 WL 1052821  
 4 at \*2 (N.D. Cal. Apr. 6, 2007) (“Prior constructions may be persuasive, but this Court may reach  
 5 different conclusions.”).

6 IV. DISCUSSION

No.	Claim term	Rambus’s construction	Defendants’ construction
1.	controller/controller device	an integrated circuit device that includes circuitry to direct the actions of one or more memory devices	a device that controls one or more devices

10 The parties debate the appropriate scope of the limitation “controller,” or equivalently,  
 11 “controller device.” The dispute focuses on Rambus’s suggestions that the claim term refers to (1)  
 12 “an integrated circuit device,” i.e., a single chip device, and (2) that it must control “memory  
 13 devices,” specifically. As defendants note, the term actually only appears in the claims of the ’916  
 14 patent, not its specification. The specification refers, instead, to “master or bus controller devices,  
 15 such as CPUs ... [which] send[] control signals” and “slave devices, such as DRAM, SRAM or  
 16 ROM memory devices ... [which] respond[] to control signals.” The claims, on the other hand,  
 17 recite a “method of controlling a synchronous memory device by a controller.” ’916 patent, col.  
 18 25:66-67.

19 Turning to the first point, the parties here have stipulated, consistent with the Federal  
 20 Circuit’s opinion in *Rambus v. Infineon Techs. Ag*, 318 F.3d 1081, 1091 (Fed. Cir. 2003), that  
 21 “integrated circuit device” means “a circuit constructed on a single monolithic substrate, commonly  
 22 called a ‘chip.’” (See Joint Claim Construction and Prehearing Statement (Dkt. No. 95) at 1).  
 23 Rambus argues that the term “controller” implies that it is an “integrated circuit device” because the  
 24 specification describes the “Field of the Invention” as follows: “An *integrated circuit* bus interface  
 25 for computer and video systems is described which allows high speed transfer of blocks of data,  
 26 particularly to and from memory devices, with reduced power consumption and increased system  
 27 reliability.” ’916 patent, col. 1:22-27 (emphasis added). Rambus also points out that the  
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1 specification elaborates: “The bus architecture of this invention connects master or bus controller  
2 devices, such as CPUs, Direct Memory Access devices (DMAs) or Floating Point Units (FPUs), and  
3 slave devices such as DRAM, SRAM or ROM memory devices.” *Id.*, col. 6:16-21. Finally,  
4 Rambus emphasizes that in the *Hynix* litigation, the parties stipulated that “memory controller”  
5 means “[a]n integrated circuit device that includes circuitry to direct the actions of one or more  
6 memory devices.” (See Exh. B to Detre Decl. in Supp. of Opening Br., at 2 (*Hynix I* Joint Claim  
7 Construction and Prehearing Statement)). Of course, that is of relatively limited significance.

8 Defendants in this action argue that nothing in the specification requires the controller,  
9 specifically, to be a single chip device. They argue that Rambus could have drafted claims stating  
10 that the controller must be formed on a single semiconductor substrate, but did not. Defendants also  
11 emphasize that prior art, in the form of U.S. Patent No. 4,315,308 (“the ’308 patent” or “the Jackson  
12 patent”), discloses a device that controls communications with a memory device, described in the  
13 Rambus patents as containing “a single CPU,” *see* ’916 patent, col. 2:22-31, but actually comprised  
14 of “two separate chips.” ’308 patent, col. 4:22-23, 4:44-47. They therefore argue that the state of  
15 the art contradicts Rambus’s suggestion that a controller is known within the field as a single chip  
16 device. To that point, Rambus replies that the Jackson patent was filed in 1978, and therefore  
17 should not be given much weight in assessing the terminology of the art at the time of the invention,  
18 many years later. On balance, the controversy over the Jackson prior art is not dispositive.

19 More instructive is the Federal Circuit’s recent opinion in *In re Rambus*, 2012 WL 3329675  
20 at \*4, which addresses arguments similar to those advanced here in the course of reviewing on  
21 appeal the reexamination of another Farmwald-Horowitz patent (also asserted in this litigation),  
22 U.S. Patent No. 6,034,918 (“the ’918 patent”). In that matter, the Board of Patent Appeals and  
23 Interferences (BPAI), construing “memory device,” rejected Rambus’s argument that the term  
24 necessarily consisted of an integrated circuit device. Upon review the Court agreed, holding that  
25 while the claim could be satisfied by a single chip device, it was not so limited: “The specification  
26 language Rambus cites shows only that the invention can be carried out with a single chip memory  
27 device, it does not require the invention to be so performed. ... To the extent Rambus wanted to

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1 limit the memory device to a single chip component, it could have expressly done so. It did not, and  
2 this court will not do so here.” *Id.*

3           Recognizing that *In re Rambus* concerned a different claim term, the same logic applies to  
4 the debate here over the meaning of “controller.” While the ’916 patent’s specification supports  
5 Rambus’s view that its claims could be embodied by a single chip device, it does not go so far as to  
6 require as much. To hold otherwise would contravene the principle that limitations not found in the  
7 claims or supported by an unambiguous restriction in the specification or prosecution history are not  
8 to be read into the claims. *Laitram Corp.*, 163 F.3d at 1347. Rambus protests that defendants’  
9 alternative suggestion is wholly divorced from the field of the invention, and thus too general.  
10 While Rambus is correct that the claims must be construed in light of the specification, and the file  
11 history, its suggestion that defendants’ proposed construction would potentially cover “the anti-lock  
12 brake controller on an automobile, the controller of a back yard irrigation system, and a host of other  
13 technologies with no connection whatsoever to the patented inventions at issue here” is greatly  
14 overstated. Even with defendants’ broader proposed construction of controller, given the context  
15 provided by the intrinsic record, a person skilled in the art would plainly understand that the  
16 controller is embodied by circuitry, and not some other random form of technology. That  
17 understanding may be preserved without importing the further requirement that the controller must  
18 be an integrated circuit.

19           As for the second issue – that is, whether the device directs or controls<sup>2</sup> “memory devices”  
20 in particular, as Rambus suggests, or “devices” more generally, as defendants submit – the claims  
21 recite a “method of controlling a synchronous memory device by a controller.” ’916 patent, col.  
22 25:66-67. In fact, all of the asserted claims refer to control of memory devices. Defendants argue  
23 the specification teaches that “master or bus controller devices, such as CPUs” are operable with the  
24 alleged invention. *Id.*, col. 6:16-17. *See also id.*, col. 6:27-30 (“semiconductor devices, including  
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27 <sup>2</sup> Rambus favors the verb “direct” over “control” and argues that the latter, defendants’ suggestion,  
28 is circular and unhelpful. While “direct” is generally synonymous with “control,” because there is  
no discernible difference, “control” is more faithful to the claims language, and since the word has  
no demonstrated meaning peculiar to the art, it needs no further construction.



1 devices, disk controllers, or other special purpose devices such as *high speed switches* can be  
 2 modified for use with the bus of this invention” (emphasis added)). Rambus replies that its  
 3 proposed construction does not suggest the controller is limited to controlling *only* memory devices,  
 4 and agrees that a controller may, as the specification suggests, control other devices. If that is so,  
 5 Rambus cannot credibly object to the inclusion of a reference to control other devices. Accordingly,  
 6 the first term is construed to mean, “a device that controls one or more memory devices or other  
 7 devices.”

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No.	Claim term	Rambus’s construction	Defendants’ construction
2.	clock signal	a signal that is continuously present and continuously repeats at regular intervals, to provide timing information	a periodic signal that is continuously present and repeats at regular intervals to provide timing information
3.	external clock signal	a signal that is continuously present and continuously repeats at regular intervals, from a source external to the device to provide timing information	a periodic signal that is continuously present and repeats at regular intervals to provide timing information from a source external to the device

16 The dispute over the second and third terms is relatively limited. The ’916 patent describes a  
 17 two clock system which, together, “provide a synchronized, high speed clock for all the devices on  
 18 the bus.” ’916 patent, col. 8:35-36. As their respective constructions suggest, the parties agree that  
 19 the claimed “clock signal” must be “periodic,” “continuously present,” “repeat[ed] at regular  
 20 intervals,” and “provide timing information.”<sup>3</sup> They further agree that an “external clock signal” is  
 21 one “from a source external to the device.” The parties disagree, however, as to whether a  
 22 “periodic” signal, by its nature, must be “continuously present” and “continuously repeat[ing] at  
 23 regular intervals,” with Rambus arguing in the affirmative, and defendants countering that a signal

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 26 <sup>3</sup> Rambus initially proposed, “a periodic signal, i.e. one that is continuously present and repeats at  
 27 regular intervals to provide timing information.” At the hearing, however, it suggested eliminating  
 28 the term “periodic” and instead adopting the phrase “that is continuously present and continuously  
 repeats,” as the table above reflects. Defendants would not agree to that proposal because it implies  
 that the signal must always be repeating.

1 may be intermittently periodic, and yet still “continuously present.” In other words, the parties  
2 agree that, at least during operations, the clock signal must look like this:



7 Disagreement arises, however, as to whether the signal must always repeat the pattern represented  
8 above, as Rambus urges, or may go “flat” at times, as defendants insist.

9 Neither side relies on the intrinsic record in support of their respective positions.<sup>4</sup> Instead,  
10 both look to extrinsic sources of evidence for support. Rambus argues that the lay dictionary  
11 definition of “periodic” is “occurring, appearing, or recurring at regular intervals.” *Webster’s New*  
12 *World Dictionary of American English* 1004 (3d College Ed. 1988). It therefore maintains that a  
13 periodic signal is necessarily “repeat[ed] at regular intervals.” Rambus also reasons that if the signal  
14 is not continuously present, then it cannot possibly repeat at regular intervals, because the pattern  
15 would be disrupted by the absence of the signal.

16 Rambus notes that in another coordinated action in this District, the Court construed  
17 “external clock signal” to mean a “periodic signal from a source external to the device to provide  
18 timing information” without further glossing the word “periodic.”<sup>5</sup> That decision, however,  
19 followed a stipulated construction in an earlier *Hynix* case. *Hynix Semiconductor Inc. v. Rambus*  
20 *Inc.* (“*Hynix I*”), No. C 00-20905, 2004 WL 2610012 at \*20 (N.D. Cal. Nov. 15, 2004) (“The parties  
21 agree that ‘external clock signal’ should be construed as ‘a periodic signal from a source external to  
22 the device to provide timing information.’”). In the later, coordinated actions, the Court declined to  
23 adopt the alleged infringers’ position that the claimed external clock signal must be “continuous.” It  
24 did so recognizing that “[n]either side has developed this argument to the extent the court feels

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26 <sup>4</sup> Although defendants invoke the ’916 patent’s specification to provide some general context and  
27 suggest that the clock signal must be continuously present, that does not appear to be in dispute.

28 <sup>5</sup> Those cases are *Rambus Inc. v. Hynix Semiconductor Inc., et al.*, No. C 05-0034 RMW (N.D. Cal.), *Rambus Inc. v. Samsung Electronics Co. Ltd., et al.*, No. C 05-02298 RMW (N.D. Cal.), and *Rambus Inc. v. Micron Technology, Inc., et al.*, No. C 06-00244 RMW (N.D. Cal.).

1 comfortable determining whether an ‘external clock signal’ must be continuous.” *Rambus Inc v.*  
 2 *Hynix Semiconductor Inc.*, 569 F. Supp. 2d 946, 985 (N.D. Cal. 2008). Consequently, that decision  
 3 is of little assistance.

4 Defendants here stress that the PTO rejected the position Rambus now urges in its  
 5 reexamination of the Farmwald-Horowitz patents. *Rambus Inc. v. NVIDIA Corp.*, Appeal No. 2012-  
 6 000171, BPAI decision on Appeal at 7-8 (June 11, 2012). It held that the claimed clock signal must  
 7 be continually present “during data inputs to synchronize data transfers,” not at all times. *Id.* at 8.  
 8 Defendants also suggest that Rambus took an inconsistent position before the PTO in reexamination  
 9 proceedings, stating that the clock signal “is a *continuously present* periodic signal,” suggesting that  
 10 a periodic signal is not, by its very nature, “continuously present.” (Exh. D to Cadkin Decl. in  
 11 Supp. of Defs.’ Br. (Reex. App. No. 95/001,169, Decl. of Robert J. Murphy Under 37 C.F.R. §  
 12 1.132 at 24 (Sep. 4, 2009))). Rambus responds that defendants have misread the submission to the  
 13 PTO, and points to other deposition testimony from the same quoted expert suggesting that a  
 14 periodic signal must be continuous whenever the device is turned on. (*See* Exh. B to Detre Decl.  
 15 (Dep. of Robert J. Murphy, Apr. 25, 2005) at 127:9-24).

16 Neither side has identified any persuasive evidence to suggest how a person skilled in the art  
 17 would understand the term “periodic,” or, more generally, “clock signal.” In the absence of some  
 18 greater demonstration by plaintiff, it is not at all self-evident why a periodic signal must, by its  
 19 nature, be continuously repeating and continuously present. Although Rambus suggests defendants  
 20 have failed to respond to its argument that a discontinuous signal cannot repeat regularly, that is not  
 21 entirely accurate. Defendants’ position is apparently that of the PTO. They reason a periodic signal  
 22 may be intermittent, e.g., present during read or write operations, without being always present.  
 23 Because neither the intrinsic nor extrinsic evidence indicates otherwise, defendants’ proposed  
 24 constructions of “clock signal” and “external clock signal” are hereby adopted.

No.	Claim term	Rambus’s construction	Defendants’ construction
4.	operation code	one or more bits to specify a type of action	one or more control bits to specify a type of action

1           The parties largely agree on the appropriate construction of the fourth claim term, as well.  
 2 Disagreement focuses solely on defendants’ inclusion of the phrase “*control* bits” (emphasis added).  
 3 Rambus maintains “control bits” is not a term of art, and argues the concept of “control” is captured  
 4 by the phrase, “to specify a type of action.” It notes its proposed construction is consistent with that  
 5 adopted by the Court in the *Hynix I* litigation. *See Hynix I*, 2004 WL 2610012 at \*13 (“Therefore,  
 6 the court finds ‘operation code’ is properly construed as ‘one or more bits to specify a type of  
 7 action.’”). Defendants respond that the modification of “bits” with “control” was not considered in  
 8 the earlier case. They maintain there is agreement “operation code” refers to “control information,”  
 9 not “address information” or “data.” *See, e.g.*, ’916 patent. Col. 4:11-13 (a memory “device[]  
 10 receive[s] *address* and *control* information over the bus and transmits[s] or receive[s] requested *data*  
 11 over the same bus” (emphasis added)); U.S. App. No. 09/796,206, Resp. to Office Action at 3 (Nov.  
 12 26, 2001) (stating that “operation code” does not include “address information” and refers only to  
 13 “control information”). At argument, Rambus acknowledged operation code refers to “control  
 14 information,” but nonetheless insists its proposed construction adequately conveys that meaning by  
 15 stating the bits “specify a type of action.” Absent a debate as to whether one skilled in the art would  
 16 understand “operation code” denotes “control information,” then the construction should clearly  
 17 reflect that, for the benefit of the jury. Because Rambus appears to be correct that “control bits” is  
 18 not a term of art, the “bits of control information” is a superior formulation. Defendants do not  
 19 oppose that edit. Accordingly, the term shall be construed to mean “one or more bits of control  
 20 information to specify a type of action.”<sup>6</sup>

No.	Claim term	Rambus’s construction	Defendants’ construction
5.	precharge information	one or more bits indicating whether the sense amplifiers and/or bit lines (or portion of the sense amplifiers and/or bit lines) should be precharged	ordinary, plain meaning; no construction necessary  alternatively, information denoting whether the sense amplifiers and/or bit lines (or

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 27 <sup>6</sup> At argument, the Court suggested a clarification that “bits” refers to “bits of information,” and the  
 28 parties did not object. Nonetheless, upon further reflection, it does not appear such elaboration is  
 necessary.

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			portion of the sense amplifiers and/or bit lines) should be precharged
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The parties’ disagreement as to “precharge information” turns, in the first instance, on whether or not the term requires any construction. If Rambus prevails on that preliminary question, the parties agree the function of precharge information is to determine “whether the sense amplifiers and/or bit lines (or a portion of the sense amplifiers and/or bitlines) should be precharged,” and disagree whether “information” should be construed to mean “one or more bits indicating...,” as Rambus suggests, or “information denoting...,” as defendants submit.

On the initial question, defendants argue that because there is basic agreement as to the function of the precharge information, there is no need to construe the term further. They suggest the parties agree precharge information is simply “information” related to the step of “precharging.” That argument misses the point: it is not at all self-evident from a lay perspective what the meaning of “precharge information” is, and furthermore, there is some disagreement between the parties as to its precise meaning, as reflected in defendants’ position, extensively briefed, that “precharge information” is not limited to “one or more bits” as Rambus insists. Rambus points out, however, “[a] determination that a claim term ‘needs no construction’ or has the ‘plain and ordinary meaning’ may be inadequate when a term has more than one ‘ordinary’ meaning or when reliance on a term’s ‘ordinary’ meaning does not resolve the parties’ dispute.” *O2 Micro Int’l Ltd. v. Beyond Innovation Tech. Co., Ltd.*, 521 F.3d 1351, 1361 (Fed. Cir. 2008). Accordingly, the term cannot simply be left for the jury, as is; it must be construed.

Turning to the parties’ proposed constructions, Rambus concedes defendants’ proposal is “not necessarily incorrect,” but argues that to the extent their construction defines “information” using the word “information,” it is circular and unhelpful. (Pl.’s Br. at 15:14-15). Rambus goes on to point out that the specification uniformly refers to the precharge information as consisting of some number of bits. For example the ’916 patent specifies that control information is sent to the memory devices in “two 4 bit fields.” ’916 patent, col. 9:46-47. Rambus notes the parties agree the 4 bit fields of control information include an “AccessType” field that determines the “access mode,”

1 or in other words, “whether the DRAM should precharge the sense amplifiers or save the contents of  
2 the sense amps for a subsequent page access mode.” ’916 patent, col. 10:47-55. One particular bit  
3 of the “AccessType” fields is specified to be the “precharge/save-data switch.” *Id.*, col. 11:44.

4 In response, defendants concede, “certain claims [in the Farmwald-Horowitz family] require  
5 ‘precharge information’ to be represented as ‘one or more bits,’” (Defs.’ Br. at 13:15-16 (citing U.S.  
6 Patent No. 6,564,281 (“the ’281 patent”), col. 25:25-27)), but proceed to insist that other claims use  
7 the “broader” term “precharge information,” which may include “a binary bit.” (*Id.* at 13:20-25  
8 (citing U.S. Patent No. 6,751,696 (“the ’696 patent”), col. 26:16-24)). The claims defendants rely  
9 upon require the precharge information consist of a single bit or “includes a binary bit.”<sup>7</sup> ’281  
10 patent, col. 25:25-27 (“wherein the precharge information is encoded in the first bit of the operation  
11 code”); ’696 patent, col. 26:16-24 (“wherein the precharge information includes a binary bit”). It  
12 does not follow, as defendants suggest, that the identified claims undermine Rambus’s position or  
13 somehow imply the claim term must be interpreted more broadly than “one or more bits.” As  
14 Rambus also points out, the parties similarly agree that precharge information is included in the  
15 operation code, which is itself defined as “one or more bits of information,” consistent with the  
16 Federal Circuit’s opinion in *Infinion*. 318 F.3d at 1093 (construing “read” and “write request[s]” as  
17 “a series of bits...”).

18 Finally, Rambus emphasizes that the Court in *Hynix I* adopted the construction it urges.  
19 While defendants note that, during earlier stages of the *Hynix I* litigation and the later, coordinated  
20 actions, Rambus agreed with the Court that precharge information should be construed as  
21 “information denoting whether the sense amplifiers and/or bit lines (or a portion of the sense  
22 amplifiers and/or bit lines) should be precharged,” *see, e.g., Hynix I*, 2004 WL 2610012 at \*14-15,  
23 the Court in the coordinated actions subsequently revised the construction of “precharge  
24 information” to conform exactly to the proposal Rambus advances now. *See* 569 F. Supp. 2d 946  
25 (Appendix A). In view of the foregoing, Rambus has the stronger position on this question:

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27 <sup>7</sup> At the hearing, defendants noted they had identified a single, unasserted claim that did not describe  
28 the precharge information in terms of bits. That evidence was not presented in the papers, and is of  
marginal significance anyway, given that the claim is not at issue.

1 “precharge information” is construed as “one or more bits indicating whether the sense amplifiers  
2 and/or bit lines (or portion of the sense amplifiers and/or bit lines) should be precharged.”

No.	Claim term	Rambus’s construction	Defendants’ construction
6.	register	a storage element or group of storage elements not part of a memory array that can store one or more bits of information	a storage element that can store information

7 The parties agree that the claim term “register” refers to a “storage element” and the dispute  
8 focuses on (1) whether it is separate from the memory array, and (2) whether it stores only bits or,  
9 more broadly, information.<sup>8</sup> With respect to the first issue, both parties claim the support of the  
10 intrinsic evidence. Rambus primarily objects to defendants’ proposal on the grounds that it is so  
11 broad as to permit the conflation of the claimed register with the memory array’s cells. It notes the  
12 title of the ’916 patent describes a “[m]emory device having a variable data output length and a  
13 programmable register,” with the specification further elaborating: “[r]egisters are provided which  
14 may store control information, device identification, device-type and other information appropriate  
15 for the chip such as the address range for each independent portion of the device.” ’916 patent, col.  
16 4:23-27. *See also id.* at col. 23:52-54 (“The DRAM memory array is divided into a number of  
17 subarrays ... Each subarray is divided into arrays [] of memory cells.”). If a register were no  
18 different than a memory cell in the DRAM array, Rambus reasons, every “memory device” would  
19 necessarily entail a multitude of programmable registers. That result is not supported by the  
20 specification, which differentiates between the two elements, or by the state of the art. *See, e.g.,*  
21 *IEEE Standard Dictionary of Electrical and Electronics Terms* 797 (5th ed. 1993) (defining  
22 “memory cell” as “[t]he smallest subdivision of a memory into which a unit of data has been or can  
23 be entered....”).

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26 <sup>8</sup> Defendants do not address Rambus’s inclusion of the phrase “... or group of storage elements...,”  
27 and therefore may be deemed not to oppose that language. Because Rambus’s opening brief  
adequately supports its contention that the register need not consist of a single storage element, this  
28 aspect of its construction may be adopted.

1 Defendants argue the specification of the '916 patent is silent as to whether the register may  
2 be included in the memory array, and emphasize that Figure 15 does not illustrate any registers at  
3 all. They note the Farmwald-Horowitz patents claim “a ‘memory device’ which includes ‘an array  
4 of memory cells,’ as well as separate ‘interface circuitry *including* an access-time register...”  
5 (Defs.’ Br. at 15:8-10 (citing U.S. Patent No. 5,841,580, col. 25:22-31)), and suggest those two  
6 components are “separate and distinct parts of the memory device.” (*Id.* at 15:12-13 (citing U.S.  
7 App. No. 10/973,268 at Claim 163)). That evidence appears to support Rambus’s position that the  
8 registry should not be conflated with memory cells. Defendants also point out that a leading  
9 technical dictionary defines a “register” as “[a] device capable of retaining information, often that  
10 contained in a small subset (for example, one word), of the aggregate information in digital  
11 computer,” and while there are some similarities between the foregoing definition and the dictionary  
12 definition of “memory cell” identified by Rambus, significantly, they are not the same. *See IEEE*  
13 *Dictionary of Electrical and Electronic Terms* 808 (4th ed. 1988). Because neither the intrinsic nor  
14 extrinsic evidence support the high level of generality urged by defendants, Rambus’ position must  
15 prevail.<sup>9</sup>

16 Turning to the second issue, whether the register should be construed to “store one or more  
17 bits of information,” or more generally, “store information,” Rambus argues the specification  
18 supports its position that the information stored in the register may be included in “bytes” (e.g.,  
19 eight bits) transmitted by the controller to a memory device. '916 patent, col. 10:13-15; *IEEE*  
20 *Dictionary* 118 (1988) (defining “byte” as a “binary string operated on as a unit and usually eight  
21 bits long”). Defendants, on the other hand, insist certain claims in the Farmwald-Horowitz require  
22 the register to store other types of “information.” *See, e.g.*, U.S. Patent No. 5,983,320 (“the '320  
23 patent”), col. 26:15-27; '916 patent, col. 6:34-37 (“device identification (device ID) register [], a  
24 device-type descriptor register [] control registers [] and other registers containing other information  
25 relevant to that type of device”). While defendants’ position is not necessarily incorrect,  
26 significantly, they do not suggest such “information” takes the form of something other than bits.

27 \_\_\_\_\_  
28 <sup>9</sup> That result comports, again, with the stipulation of the parties in the coordinated *Hynix II* actions.



1 The weight of the record demonstrates that, in this context, “information” denotes, more  
 2 specifically, “one or more bits.” That appears to be how one skilled in the art would understand  
 3 references to “information.” Accordingly, Rambus’s construction of “register” is hereby adopted.

No.	Claim term	Rambus’s construction	Defendants’ construction
7.	representative of	indicates	ordinary, plain meaning; no construction required

7 The seventh claim term, “representative of,” appears in a variety of contexts. *See, e.g.*, ’916  
 8 patent, col. 26:3-5 (“...wherein the value is *representative of* a number of cycles of an external clock  
 9 signal...” (emphasis added)). Rambus favors construing the term as meaning “indicates” because it  
 10 fears defendants may argue, at a later stage of litigation, that any relationship between two values  
 11 means one is “representative of” the other, in service of the position that Rambus’s patents are  
 12 anticipated by prior art, an argument asserted in other litigation on the Farmwald-Horowitz patents.  
 13 It maintains a possible, future dispute over anticipation confirms there is a live disagreement  
 14 between the parties as to the meaning of “representative of,” and again invokes *O2 Micro* to demand  
 15 a construction of the term. *See* 521 F.3d at 1361.

16 Of course, potential legal defenses do not have any bearing on the proper construction of the  
 17 asserted claims, and as defendants rightly point out, Rambus has failed to adduce any evidence to  
 18 suggest that “representative of” has a peculiar meaning, either within the context of the Farmwald-  
 19 Horowitz patents or to persons skilled in the art. To the extent the *Hynix I* Court substituted  
 20 “indicates” for “representative of” in the course of construing various other claim terms, that does  
 21 not imply, as Rambus suggests, any need to construe the prepositional phrase here.<sup>10</sup> Thus, while  
 22 there may be a dispute to the extent Rambus requests a specific lay meaning of the term, and  
 23 defendants insist no specificity is required, there is no cognizable legal basis or compelling evidence  
 24 in the record to support Rambus’s position. Again, a possible anticipation defense in later

25 <sup>10</sup> Of course, Rambus is free to advance arguments directed to the merits at the appropriate stage of  
 26 proceedings. It may not, however, rely on language extracted from other cases in support of its  
 27 proposed construction, without acknowledging the highly context-specific nature of such holdings.  
 28 *See, e.g., Tehrani v. Hamilton Med., Inc.*, 331 F.3d 1355, 1361 (Fed. Cir. 2003) (“the statement that  
 one item ‘represents’ another cannot be interpreted so broadly as to include any case in which the  
 two items are related in some way”).

1 proceedings does not mandate a particular construction of a term, absent evidence of what the term  
 2 ought to mean in light of the claims. Those circumstances distinguish the present case from *O2*  
 3 *Micro*, 521 F.3d at 1361, which concerned a substantive dispute about the meaning of “only if”  
 4 within the specific context of the claims. Here, no such dispute is apparent, and “representative of”  
 5 may be equated with the plain, ordinary meaning of the term as it reads in the claims, with no need  
 6 for further construction.

No.	Claim term	Rambus’s construction	Defendants’ construction
8.	sample/sampled/ sampling	obtain(s) at one or more discrete points in time/obtained at one or more discrete points in time/obtaining at one or more discrete points in time	capture(s)/captured/capturing

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 8 Again, both parties insist their proposed constructions for “sample” and variants thereof find  
 9 support in the intrinsic record. Rambus maintains its proposed construction is consistent with the  
 10 specification, the Court’s construction in the coordinated *Hynix II* actions, and the ordinary meaning  
 11 of the term. The specification employs the concept of sampling, often in verb form, to describe, for  
 12 example, “clocked receivers” that “sample” input signals.” ’916 patent, cols. 21:61-62, 23:12-14  
 13 (“input receivers [] sample the bus clocks just as they transition”), and 22:45 (reference to “sample  
 14 period”). In *Hynix II*, the Court construed “‘sample’ to mean ‘to obtain at a discrete point in time,’  
 15 ‘samples’ as ‘obtains at discrete points in time,’ and ‘sampling’ as ‘obtaining at discrete points in  
 16 time.’” *Hynix II*, 569 F. Supp. 2d at 988. Rambus offers only a slight variation on that framework,  
 17 to clarify that sampling may occur at “one or more” times,<sup>11</sup> but not continuously, as it believes  
 18 defendants’ preferred construction implies. The construction adopted in *Hynix II* also derived some  
 19 support from the *IEEE Dictionary*’s definition of the term “sampling data,” that is, “[d]ata in which  
 20 the information content can be, or is, *ascertained only at discrete intervals of time.*” *IEEE*  
 21 *Dictionary* 855 (1988) (emphasis added). Defendants argue Rambus’s opponents in *Hynix II* failed

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 27 <sup>11</sup> Defendants, for their part, do not directly address this addition to the construction adopted in  
 28 *Hynix II*. Rambus is generally correct, however, that the *Hynix II* Court’s construction of the term  
 contemplates – or at least, does not foreclose – sampling at “one or more” points.

1 to present intrinsic evidence to suggest that the term “sampling” has a meaning distinct from its  
2 ordinary and plain sense, and contend they have done so here.

3 Defendants also make much of the fact that Rambus concedes “‘sampling’ does involve  
4 capturing values of a signal,” and, apparently in other proceedings, has interpreted the term  
5 “sampling” as referring to “captu[ring] data on the bus.” (Def. Br. at 17:25-27); (Exh. U to Cadkin  
6 Decl. at 33). Defendants also note that an Administrative Law Judge of the International Trade  
7 Commission (ITC), in the context of construing asserted claims from another group of Rambus  
8 patents (the Barth family), characterized “sampling” of data in a write operation as meaning  
9 “capture[] data off the data bus.” *In the Matter of Certain Semiconductor Chips and Prods.*  
10 *Containing the Same*, Initial Determination on Violation of Section 337, Inv. No. 337-TA-753, at  
11 234 (Mar. 2, 2012) (“the strobe signal ‘initiates sampling’ of data by the memory device such that  
12 the memory device captures valid data received from the memory controller via the data bus”).  
13 Such collateral matters, while arguably of some relevance and persuasive weight, are hardly  
14 dispositive here. More fundamentally, the difference between “capture” and “obtain” is not so  
15 great, and of somewhat marginal significance from Rambus’s point of view.

16 Ultimately, the more significant disagreement between the parties is limited to the frequency  
17 and duration of the claimed sampling. On that question, Rambus urges sampling “is well  
18 understood in the art to refer to capturing those values only at points in time, rather than, for  
19 example, continuously.” (Pl.’s Br. at 19:26-28). Unlike *Hynix II*, defendants in this case have  
20 identified some intrinsic evidence to suggest the duration and frequency of the sampling procedure  
21 may vary, but that is consistent with the ordinary sense of the word, which implies nothing about the  
22 required frequency or length of time data must be obtained. Moreover, defendants have not  
23 identified any intrinsic evidence to suggest the claimed sampling may occur continuously – a notion  
24 that does not comport with the technical or ordinary definition of the word.

25 Rambus maintains the specification’s reference to “sample period” and “sampl[ing] the bus  
26 clocks just *as they transition*” (emphasis added), necessarily implies “discrete points of time” rather  
27 than continuous “capturing.” ’916 patent, cols. 22:45, 23:12-14. As noted above, that concept is  
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1 also supported by the 1988 *IEEE Dictionary* definition of “sampling data.” In reply, defendants  
 2 insist Rambus’s construction is ambiguous. For example, they ask: is a “discrete” point in time  
 3 instantaneous? Addressing this apparent ambiguity in the record, Rambus answers a “point in time”  
 4 is basically instantaneous, but insists the patents’ references to “sample period[s]” indicate that there  
 5 is a period of time during which sampling may occur (for example, half of a clock signal), not a  
 6 duration during which continuous sampling occurs. *See id.*, col. 22:45. Along somewhat similar  
 7 lines, defendants also correctly note the Farmwald-Horowitz patents describe sampling as occurring  
 8 at various frequencies. *See, e.g.*, U.S. Patent No. 6,304,937, col. 24:65-67 (“sampling the first  
 9 portion of data synchronously with respect to a rising edge transition of an external clock signal”).  
 10 It is not apparent, however, why the term “sample” and variants thereof must necessarily be limited  
 11 to a particular frequency or duration, as defendants seem to imply. That understanding is not what  
 12 Rambus urges, and does not appear to be the common understanding of those skilled in the art. As  
 13 best as can be discerned, defendants so argue merely to cast doubt on the definiteness of Rambus’s  
 14 proposed construction. In any case, the ambiguity identified by defendants may be eliminated by  
 15 simply replacing “discrete” with “known,” which accords the limitation the flexibility it requires.  
 16 Accordingly, consistent with *Hynix II*, and for all the reasons set forth above, Rambus’s proposed  
 17 construction shall be adopted. “Sample” means “obtain(s) at one or more known points in time.”

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No.	Claim term	Rambus’s construction	Defendants’ construction
9.	synchronous dynamic random access memory device	an integrated circuit device in which information can be stored and retrieved electronically, not including a memory controller, that receives an external clock signal which governs the timing of the response to a read request, write request, or operation code and includes one or more arrays of DRAM cells	a memory device in which an external clock signal is used to regulate the timing of device operations

The principal disputes between the parties regarding “synchronous dynamic random access memory device” (“synchronous DRAM device”) are: (1) whether a synchronous DRAM device

1 must be an integrated circuit device, i.e., a single chip device, (2) whether a synchronous DRAM  
2 device may include a memory controller, (3) what the requirement a device be “synchronous”  
3 entails, and (4) whether it is necessary to specify a synchronous DRAM device includes “one or  
4 more arrays of DRAM cells.” As an initial matter, it is important to note that synchronous DRAM  
5 device does not actually appear in the specification of the asserted patents and only some of the  
6 asserted claims.

7 On the first question, as noted above, and as Rambus’s reply brief candidly acknowledges in  
8 a footnote, the Federal Circuit’s recent reexamination opinion, *In re Rambus*, 2012 WL3329675 at  
9 \*4-6, squarely rejected Rambus’s argument that term “synchronous memory device” is limited by  
10 the Farmwald-Horowitz patents, and in particular by the ’918 patent, to single chip devices.  
11 Nonetheless, Rambus advances virtually the same argument here in connection with the term  
12 synchronous DRAM device. As the Court of Appeals explained in *In re Rambus*:

13 This court agrees with the Board that the specification does not restrict the invention  
14 to single chip memory devices. There are no words of manifest exclusion or clear  
15 disavowals of multichip devices—there are only preferred embodiments and goals of  
16 the invention that Rambus argues are better met by single chip devices. The  
specification language Rambus cites shows only that the invention can be carried out  
with a single chip memory device, it does not require the invention to be so  
performed.

17 *Id.* at \*4. Rambus seeks to limit the impact of *In re Rambus* on these actions by emphasizing that  
18 the former claim construction opinion pertains to the term “memory device,” rather than  
19 synchronous DRAM device. While that is true, the Federal Circuit’s logic is highly relevant and,  
20 ultimately, also applicable here, for the reasons set forth below.

21 In its opening claim construction brief, Rambus argues – much as it did before the Federal  
22 Circuit in *In re Rambus* – that the language and figures in the ’916 patent refer to “DRAM chips”  
23 and illustrate “DRAM devices” as single chips.<sup>12</sup> See, e.g., ’916 patent, col. 3:43-45, and Figs. 1, 2,

24  
25 <sup>12</sup> To the extent Rambus seeks to distinguish *In re Rambus* on the grounds that it construed  
26 “memory device” rather than the narrower term, “synchronous DRAM device,” the effort fails,  
27 given that before the Federal Circuit’s order was issued, it took the position *In re Rambus* would  
28 “determine whether a memory device, and therefore a synchronous dynamic random access memory  
device, may or may not include a memory controller, and will be binding here.” See Pl.’s Br. at  
22:18-21. Rambus’s simultaneous reliance on intrinsic evidence concerning the term “DRAM  
device,” another partial variant of the term to be construed here, also appears conveniently selective

1 3, 9, 15. The fact that the Farmwald-Horowitz specifications describe single chip devices as DRAM  
2 devices does not, however, compel the converse conclusion that the term “synchronous DRAM  
3 device” must be construed as encompassing only single chip devices. Without “manifest exclusion  
4 or clear disavowals,” such a limitation may not be imported from the specification into the claims.  
5 *In re Rambus*, 2012 WL3329675 at \*4. While Rambus seeks to characterize the BPAI’s decision  
6 below in *In re Rambus* as helpful, that opinion is of very limited assistance to it. *See* BPAI Decision  
7 on Appeal, Appeal 2010-011178, at 29 (“As the Examiner further noted, Appellant directed at least  
8 one claim more narrowly to a ‘memory (DRAM) device in claim 3 of U.S. 5,841,715, thereby  
9 implying a memory device is broader than a chip.”).

10 Notably, the Federal Circuit’s opinion in *In re Rambus* comports with the District Court’s  
11 holding in *Hynix II*. In *Hynix I*, construing the term “synchronous memory device,” the District  
12 Court accepted the parties’ stipulated construction of “memory device” as “an integrated circuit  
13 device in which information can be stored and retrieved electronically,” and focused instead on the  
14 disputed meaning of the modifier “synchronous.” 2004 WL 2610012 at \*6-8. In *Hynix II*, the Court  
15 had occasion to revisit the meaning of “memory device” to resolve “whether a ‘memory device’  
16 incorporates the definition of an “integrated circuit device,” and with it, the single chip limitation  
17 from *Infineon*.” Like the Federal Circuit in *In re Rambus*, the District Court ultimately concluded:  
18 “[b]ecause the specification does not clearly limit the scope of the invention to a single chip, the  
19 court declines to read the phrase ‘memory device’ so narrowly. ... A ‘memory device’ is ‘a device  
20 in which information can be stored and retrieved electronically.’ It need not be on a single chip.”  
21 569 F. Supp. 2d at 973. Rambus seeks to limit all these unfavorable rulings as construing different  
22 claim terms, *but see supra* note 12, and instead emphasizes the passing observation of the District  
23 Court in *Hynix II*, that claims directed to “a method of operation of a synchronous dynamic random  
24 access memory device” apparently reflect “limits on the scope of ‘memory device’ ...  
25 demonstrating that Rambus knew how to limit its claims to a single chip when it wished to do so.”  
26 *Id.* at 974. That passage is of limited import: “synchronous DRAM device” was not construed in  
27 and fundamentally inconsistent with its position that “synchronous DRAM device” must be  
28 understood entirely distinctly.

1 *Hynix II*, and other than the quoted passage, the opinion does not explain how the foregoing  
2 conclusion was drawn.

3 Defendants on the other hand, stress Rambus has taken supposedly inconsistent positions in  
4 the course of litigating its many cases, variously construing “synchronous DRAM device” as “a  
5 synchronous semiconductor device which includes one or more arrays of DRAM cells,” or “a  
6 dynamic random access memory device that receives an external clock signal which governs the  
7 timing of a response to the transaction request.” (Defs.’ Br. at 20 n.16). Defendants also advance  
8 an argument they raised in connection with the term “controller/controller device,” above: that is,  
9 had Rambus acted as its own lexicographer to limit expressly the claim term “synchronous DRAM  
10 device” to one which is “formed on a single semiconductor substrate” or consists of an “integrated  
11 circuit device,” its proposed construction might be supportable. It has not done so, of course. *See*  
12 *also In re Rambus*, 2012 WL 3329675 at \*5 (“memory devices ‘formed on a single semiconductor  
13 substrate’ are properly limited to single chip devices”).

14 Ultimately, then, on this first question, defendants must prevail. The intrinsic record does  
15 not support limitation of “synchronous DRAM device” to an integrated circuit device. First, the  
16 claims do not suggest any such thing. As the Federal Circuit and *Hynix II* observed, Rambus  
17 certainly knew how to claim a single-chip device and did not employ language in drafting its claims  
18 indicating such intention. Second, the specification does not contain a clear disavowal of multi-chip  
19 devices sufficient to support such a narrowing of Rambus’s claims. *See In re Rambus*, 2012  
20 WL3329675 at \*4 (“There are no words of manifest exclusion or clear disavowals of multichip  
21 devices—there are only preferred embodiments and goals of the invention that Rambus argues are  
22 better met by single chip devices.”). Consistent with the logic employed by other Courts, here,  
23 Rambus’s suggestion that “synchronous DRAM device” must be “an integrated circuit device” must  
24 be rejected.

25 The next point of disagreement concerns whether or not a synchronous DRAM device may  
26 include a memory controller. *In re Rambus* sheds some light on that question, as well, if only,  
27 again, indirectly. Before the BPAI and the Federal Circuit, Rambus categorically argued the term  
28

1 “memory device cannot include a memory controller,” *id.* at \*7, a position both the agency and the  
2 Court rejected:

3 Rambus’s construction broadly excluding any memory controller that provides more  
4 functionality than simple control logic fails. ... In fact, the claims [of the ’918 patent]  
5 expressly calls for the memory device to provide the control functionality of receiving  
6 block size requests and outputting specific amounts of data. Nothing in the claim  
prevents the memory device from consisting of a storage chip and a device that  
facilitates the receiving and outputting from that storage chip.

7 *Id.* The Court then went on to hold that a “memory device,” as the term is used in the Farmwald-  
8 Horowitz patents, “may have a controller that, at least, provides the logic necessary to receive and  
9 output specific data, but does not perform the control function of a CPU or bus controller.” *Id.*

10 Rambus’s opening claim construction brief conceded the Federal Circuit’s opinion would  
11 control this issue. (*See* Pl.’s Br. at 22:18-21). In light of the result reached by the Court of Appeals,  
12 Rambus now insists CPUs and bus controllers may not be included in a synchronous DRAM device.  
13 Defendants also rely on *In re Rambus*, but contend a “memory controller” indeed “provides the  
14 logic necessary to receive and output specific data,” and therefore may be included in the  
15 synchronous DRAM device. Consistent with both parties’ views, the term may be construed in  
16 accordance with the Federal Circuit’s opinion to specify a “synchronous DRAM device” “may have  
17 a controller that provides the logic necessary to receive and output specific data, but does not  
18 perform the control function of a CPU or bus controller.”

19 Turning to the third point of contention, the parties agree a synchronous DRAM device must  
20 use an external clock for timing purposes, but disagree as to how that component of the device  
21 should be described. Rambus proposes “device ... that receives an external clock signal which  
22 governs the timing of the response to a read request, write request, or operation code,” whereas  
23 defendants submit, more simply, “device in which an external clock signal is used to regulate the  
24 timing of device operations.” Rambus attacks defendants’ suggestion as vague as to whether, for  
25 example, all operations are regulated by the clock, or if not, which ones. Rambus rightly points out  
26 defendants’ construction leaves it unclear how the device uses the clock signal to regulate the timing  
27 of operations if it is not “received.” Finally, Rambus also claims the support of the *Hynix I* claim



1 construction, which construed “synchronous memory device” as “a memory device that receives an  
2 external clock signal which governs the timing of the response to a transaction request.” 2004 WL  
3 2610012 at \*6-8. In its proposed construction, Rambus has substituted “a read request, write  
4 request, or operation code” in place of “transaction request,” because the latter term is not included  
5 in any of the asserted claims in this case.

6 Defendants respond that a construction requiring the synchronous DRAM device to *receive* a  
7 clock signal will render some claim language superfluous. *See, e.g.*, U.S. Patent No. 6,324,120, col.  
8 26:30-34 (claiming a “method of operation of a synchronous dynamic random access memory  
9 device[,] ... the memory device comprising: clock circuitry to receive an external clock signal”),  
10 *and* ’696 patent, col. 24:58-61 (reciting a “synchronous memory device ... [which] comprises: clock  
11 circuitry to receive an external clock signal”). There does not appear to be much dispute, then, as a  
12 substantive matter, that the claims invoke reception of the clock signal. The transitional phrase  
13 “comprising,” however, suggests the synchronous DRAM device includes “circuitry to receive an  
14 external clock signal,” precisely as Rambus suggests.<sup>13</sup> Although defendants also insist Rambus  
15 has, in other proceedings, generally supported their suggestion the clock signal is used to regulate  
16 the timing of device operations, that advocacy, is not strictly inconsistent with the position it urges  
17 here.

18 Finally, defendants argue Rambus’s construction of a synchronous DRAM device as  
19 “includ[ing] one or more arrays of DRAM cells” is redundant and unhelpful, given that there is no  
20 disagreement a synchronous DRAM device is a variant of a DRAM device and must include one or  
21 more DRAM memory arrays. Rambus does not directly dispute that fair point. Accordingly, the  
22 term “synchronous DRAM device” is construed as “a memory device in which information can be  
23 stored and retrieved electronically, and which uses an external clock signal to regulate the timing of  
24 device operations. It may have a controller that provides the logic necessary to receive and output  
25 specific data, but does not perform the control function of a CPU or bus controller.”

26  
27 <sup>13</sup> As Rambus also points out, the “clock circuitry” limitation is an antecedent to other claims, and  
28 therefore actually not redundant.

No.	Claim term	Rambus’s construction	Defendants’ construction
10.	synchronously with respect to	having a known timing relationship with respect to	operating in step (or in phase) with respect to

The parties’ disagreement as to the appropriate construction of the final term is limited to the meaning of “synchronously,” with Rambus insisting it means “having a known timing relationship...,” and defendants submitting, alternatively, “operating in step (or in phase)....” As an initial matter, the parties debate the implications of defendants’ proposed construction. Rambus maintains the phrase “or in phase” suggests the timing of operations must be in phase with the clock, as “in phase” is offered as synonymous with “in step.” Defendants responded that is not so, given the conjunction “or,” and at the hearing, offered to eliminate the parentheses in their proposed construction to memorialize such understanding. In any case, the larger question is whether or not such a specific construction of the root “synchronous” is appropriate, given Rambus’s much more general construction, “having a known timing relationship....”

The parties dispute the significance of the intrinsic record. Rambus argues Figure 13 of the ’916 patent makes clear the delay line output signals designated 107 and 108, which are “synchronized with the two bus clocks,” are not “in phase” with them, but are instead “phase-shifted” so that the outputs are timed to correspond to the rising and falling edges of the second bus clock. ’916 patent, col. 23:14-22. Defendants reply Rambus has misrepresented the function of the output signals, because Figure 13 represents the timing diagram for “how the internal device clock is generated from two bus clock signals using a set of adjustable delay lines.” ’916 patent, col. 5:19-21. Defendants insist it is the internal device clock which must ultimately be synchronized with the bus clocks to facilitate read and write operations. *Id.*, col. 23:13-24. While that may be the broader point of the alleged invention, the term “synchronized” is used in both contexts, in broader fashion, and in contravention of defendants’ understanding of the term.

Defendants also maintain the file history supports their view of the term. Specifically, they argue Rambus responded to the PTO’s rejection of claims that required “providing a first portion of the first amount of data to the memory device synchronously with respect to a first transition of an external clock signal,” by arguing the claimed operation was “synchronous,” in the sense that data

1 was provided “synchronously with respect to falling edges of the true and complement internal  
2 device clocks....” U.S. App. Ser. No. 09/510,213, Response to Office Action at 3 (Aug. 31, 2000).  
3 Defendants insist this reflects an understanding of “synchronously” as something more than “a  
4 known timing relationship,” but rather something closer to “in step.” Defendants’ position is  
5 unpersuasive. Rambus’s argument to the PTO does not circumscribe the meaning of “synchronize;”  
6 it merely limits the timing relationship with respect to that particular limitation.

7           Ultimately, it is clear the term is used to describe a variety of timing relationships in the  
8 Farmwald-Horowitz patents. It would therefore be inappropriate to limit the term as defendants  
9 suggest, without unambiguous support from the specification. Both parties invoke various  
10 definitions found in technical dictionaries, but those do not suggest persons skilled in the art have a  
11 consistent understanding of the term distinct from the plain and ordinary meaning. *See, e.g., IEEE*  
12 *Dictionary* 978 (1988) (defining “synchronization” as requiring “fixed phase relationship”);  
13 *Illustrated Dictionary of Electronics* 537 (4th ed. 1998) (defining “synchronous” as “condition of  
14 operating in step (phase) with some reference”). Nonetheless, given the parties’ apparent  
15 disagreement as to the meaning of the term, some construction is required. *O2 Micro*, 521 F.3d at  
16 1361.

17           While the parties raise additional arguments, they shed no further light on the issue.<sup>14</sup>  
18 Accordingly, Rambus’s construction shall be adopted: “synchronously with respect to” means  
19 “having a known timing relationship with respect to.”

## 20 V. CONCLUSION

21           The disputed claim terms of the patents-in-suit are hereby construed as set forth above.  
22 Where the order has identified terms that may require further construction, such matters shall be  
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24 \_\_\_\_\_  
25 <sup>14</sup> Yet another quarrel arises as to whether defendants’ construction permits any margin of error,  
26 with Rambus arguing that it does not, contrary to the reasonable expectations of one skilled in the  
27 art, and defendants insisting that their construction simply minimizes the imprecision or “skew,”  
28 consistent with the specification. ’916 patent, cols. 19:4-9, 23:37-39. There being no real and  
discernible disagreement on this point, it need not be resolved.

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presented, if it becomes necessary, in the context of any dispositive motions or at the time of  
formulating jury instructions.

IT IS SO ORDERED.

Dated: 9/26/12



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RICHARD SEEBORG  
UNITED STATES DISTRICT JUDGE