IN THE UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

SYNOPSYS, INC.,

Plaintiff,

v.

MENTOR GRAPHICS CORPORATION,

Defendant.
_____/

No. C 12-6467 MMC

ORDER CONSTRUING CLAIMS

Before the Court is the parties' dispute regarding the proper construction of eleven terms in U.S. Patents 5,530,841 ("'841 patent"), 5,680,318 ("'318 patent"), 5,748,488 ("'488 patent"), and 6,836,420 ("'420 patent"). Plaintiff Synopsys, Inc. ("Synopsys") and defendant Mentor Graphics Corporation ("Mentor") have submitted briefing and evidence in support of their respective positions. The matter came on regularly for hearing on October 28, 2013. M. Patricia Thayer, Philip Woo, Aseem S. Gupta, Sue Wang, and Cynthia Chen of Sidley Austin LLP and Vickie Feeman of Orrick, Herrington & Sutcliffe LLP appeared on behalf of Synopsys. Jeffrey S. Love, John D. Vandenberg, and Andrew M. Mason of Klarquist Sparkman, LLP and Mark E. Miller of O'Melveny & Myers LLP appeared on behalf of Mentor.

Having considered the parties' respective written submissions and the arguments of counsel, the Court rules as follows.

LEGAL STANDARD

In construing disputed claims, a district court's primary source is the intrinsic evidence of the patent. See Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582-83 (Fed. Cir. 1996). Intrinsic evidence includes "the claims, the specification and, if in evidence, the prosecution history," see id., 90 F.3d at 1982, as well as the abstract, see Hill-Rom Co. v. Kinetic Concepts, Inc., 209 F.3d 1337, 1341 (Fed. Cir. 2000). Language used in the patent is given its ordinary meaning, unless it is clear that the inventor intended the terms to have a different meaning. See Vitronics, 90 F.3d at 1582. The patent specification "may act as a sort of dictionary, which explains the invention and may define terms used in the claims." See Markman v. Westview Instruments, Inc., 52 F.3d 967, 979 (Fed. Cir. 1995), aff'd, 517 U.S. 370 (1996). Although a district court considers the specification in determining the meaning of a disputed claim, it generally is improper to limit the scope of the claim to the examples set forth in the specification "absent a clear indication in the instrinsic record that the patentee intended the claims to be so limited." See Dealertrack, Inc. v. Huber, 674 F.3d 1315, 1327 (Fed. Cir. 2012). The claims of the patent, not the specification, "measure the invention." See SRI Int'l v. Matsushita Elec. Corp. of America, 775 F.2d 1107, 1121 (Fed. Cir. 1985). As noted, the district court also reviews the prosecution history, which "can often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be." See Phillips v. AWH Corp., 415 F.3d 1303, 1317 (Fed. Cir. 2005) (en banc).

Further, in addition to intrinsic evidence, the court may consider extrinsic evidence, which "consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises." See id. Extrinsic evidence "can help educate the court regarding the field of the invention and can help the court determine what a person of ordinary skill in the art would understand claim terms to

mean." See id. at 1319. Nevertheless, "while extrinsic evidence can shed useful light on the relevant art, . . . it is less significant than the intrinsic record in determining the legally operative meaning of claim language." See id. at 1317 (internal quotations and citation omitted).

DISCUSSION

The four patents at issue relate generally to the field of electronic circuit design. See '420 patent, col. 1:7; see also '841 patent, col. 1:37-40. Specifically, the '841 patent, the '488 patent, and the '318 patent (collectively, the "Gregory patents") describe "[a] method and system . . . for generating a logic network using a hardware independent description means." See '841 patent, Abstract. The '420 patent (the "Seshadri patent") describes "a method and apparatus for a resetable memory and a design approach for the same." See '420 patent, col. 1:8-10. The parties dispute the proper construction of a number of terms contained in the claims of the subject patents. Representative claims in which the disputed terms appear are as follows:

> 1. A method for converting a **hardware independent user description of a logic circuit**, that includes flow control statements including an IF statement and a **GOTO statement**, and directive statements that define levels of logic signals, into logic circuit hardware components comprising:
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> converting the flow control statements and directive statements in the user description for a logic signal Q into an **assignment condition** AL(Q) for an **asynchronous load function** AL( ) and an **assignment condition** AD(Q) for an **asynchronous data function** AD ( ); and
>
> generating a **level sensitive latch** when both said **assignment condition** AL(Q) and said **assignment condition** AD(Q) are non-constant;
>
> wherein said **assignment condition** AD(Q) is a signal on a data input line of said flow through latch;
>
> said **assignment condition** AL(Q) is a signal on a latch gate line of said flow through latch; and
>
> an output signal of said flow through latch is said logic signal Q.

See '841 patent, col. 62:61-63:12 (emphasis added to designate disputed terms).

> 2. A method for converting a hardware independent user description of a logic circuit, that includes flow control statements, and directive statements that define

levels of logic signals, into logic circuit hardware components as in claim 1 [of the '488 patent] wherein said plurality of functions further comprises a **synchronous load function** SL( ), and a **synchronous data function** SD( ).

See '488 patent, col. 62:53-59 (emphasis added to designate disputed terms).

25. A method for generating a logic network comprising the steps of:
generating a structure having a plurality of nodes interconnected by edges using only **operational characteristics of said logic network** as input signals;
wherein each of selected edges include an edge condition; and variables are assigned values in said nodes; and
generating a logic network using said structure and edge conditions.

See '318 patent, col. 65:52-61 (emphasis added to designate disputed terms).

40. The method of claim 39 [of the '318 patent] wherein said logic circuit creating step further comprises:
generating a level sensitive latch in response to **predetermined assignment conditions**.

See '318 patent, col. 66:64-65.

1. A method, comprising:
a) **inferring** the existence of a **resetable memory** from a behavioral or RTL level description of a semiconductor circuit; and
b) incorporating a resetable memory design into a design for said semiconductor circuit.

See '420 patent, col. 9:48-53 (emphasis added to designate disputed terms).

Pursuant to Markman v. Westview Instruments, Inc., 517 U.S. 370, 384-91 (1996), the Court next construes the disputed claims.[1]

1. "Assignment Condition" ('841 Patent, Claim 1; '488 Patent, Claims 1 and 8; '318 Patent, Claims 30-32, 35, 36, 39, 40, and 42-45)

The parties dispute the proper construction of "assignment condition" as found, for example, in Claim 1 of the '841 patent. See '841 patent, col. 63:1-2, 4-5, 7, and 9. Synopsys proposes the term be construed as "the condition under which the hardware description function (e.g., 'AL' or 'AD') is true for a particular variable (e.g., 'Q') in the user description." Mentor proposes the term be construed as "a condition used to create or select a hardware element, by determining the logic OR of all the conditions under which a

[1] Where the Court has adopted a party's proposed construction as to a term, the adopted construction is set forth below without further discussion.

hardware description function is true for a particular variable."[2]

The Court, for the reasons stated by Synopsys, hereby construes "assignment condition" as "the condition under which the hardware description function is true for a particular variable in the user description."[3]

2. "Predetermined Assignment Conditions" ('318 Patent, Claims 40 and 42-45)

The parties dispute the proper construction of "predetermined assignment conditions" as found, for example, in Claim 40 of the '318 patent. See '318 patent, col. 66:64-65. Synopsys proposes the term be construed by using Synopsys's above-referenced construction for "assignment condition," along with the plain and ordinary meaning of "predetermined," which, according to Synopsys, is "determined beforehand." Mentor proposes the term be construed as "an assignment condition that is set in the user description." At the hearing, the Court suggested the term be construed as "an assignment condition that is determined before the logic element is generated," which construction was accepted by Synopsys.[4]

Accordingly, the Court, for the reasons stated by Synopsys, hereby construes "predetermined assignment condition" as "an assignment condition that is determined before the logic element is generated."

3. "Asynchronous/Synchronous Data Function" ('841 Patent, Claim 1; '318 Patent, Claims 32 and 36; '488 Patent, Claims 1, 2, 8, and 9)

The parties dispute the proper construction of "asynchronous/synchronous data

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[2] The parties' respective constructions as set forth herein are taken from their "Revised Exhibit A to the Parties' Joint Claim Construction Statement," filed September 24, 2013, with the exception of Mentor's proposed constructions for "assignment condition," "hardware independent user description," "GOTO statement," and "operational characteristics of said logic network," which are set forth as amended by Mentor in its Responsive Claim Construction Brief, filed October 3, 2013.

[3] The Court's construction omits the parenthetical examples, which are not contained in the definition on which Synopsys relies, specifically the definition provided by the applicant in the specification. See, e.g., '841 patent, col. 16:7-9.

[4] It is not clear whether Mentor likewise accepted the Court's suggested construction or only indicated it preferred such construction to "determined beforehand."

function" as found, for example, in Claim 1 of the '841 patent ("asynchronous") and Claim 2 of the '488 patent ("synchronous"). See '841 patent, col. 63:3; '488 patent, col. 62:58-59. Synopsys proposes the term be construed as "a hardware description function for data specifying the condition or conditions under which the variable is [asynchronously/ synchronously] assigned a value." Mentor proposes the term be construed as "a hardware description function specifying the condition or conditions under which the variable is [asynchronously/synchronously] assigned a logic one value."

The Court, for the reasons stated by Synopsys, hereby construes "asynchronous/ synchronous data function" as "a hardware description function for data specifying the condition or conditions under which the variable is [asynchronously/synchronously] assigned a value."

4. "Asynchronous/Synchronous Load Function" ('841 Patent, Claim 1; '318 Patent, Claims 32 and 36; '488 Patent, Claims 1, 2, 8, and 9)

The parties dispute the proper construction of "asynchronous/synchronous load function" as found, for example, in Claim 1 of the '841 patent ("asynchronous") and Claim 2 of the '488 patent ("synchronous"). See '841 patent, col. 63:1-2; '488 patent, col. 62:58. Synopsys proposes the term be construed as "a hardware description function for load specifying the condition or conditions under which the variable is [asynchronously/ synchronously] assigned a value." Mentor proposes the term be construed as "a hardware description function specifying the condition or conditions under which the variable is [asynchronously/synchronously] assigned a value."

The Court, for the reasons stated by Synopsys, hereby construes "asynchronous/ synchronous load function" as "a hardware description function for load specifying the condition or conditions under which the variable is [asynchronously/synchronously] assigned a value."

5. "Synchronous"; "Asynchronous" ('841 Patent, Claim 1; '318 Patent, Claims 32 and 36; '488 Patent, Claims 1, 2, 8, and 9)

The parties dispute the proper construction of "synchronous" and "asynchronous" as found, for example, in Claim 2 of the '488 patent ("synchronous") and Claim 1 of the '841 patent ("asynchronous"). See '488 patent, col. 62:58; '841 patent, col. 63:1, 3. Synopsys contends the terms should be given their plain and ordinary meanings, and that the plain and ordinary meaning of "synchronous" is "triggered by a timing signal" and the plain and ordinary meaning of "asynchronous" is "not synchronous." Mentor proposes "synchronous" be construed as "occurring on a clock edge" and "asynchronous" be construed as "not controlled by a clock edge."

The Court, for the reasons stated by Mentor, hereby construes "synchronous" as "triggered by a clock signal" and "asynchronous" as "not triggered by a clock signal."[5]

6. "Hardware Independent User Description of a Logic Circuit" ('841 Patent, Claim 1; '488 Patent, Claims 1, 2, 8, and 9)

At the outset, the parties dispute whether the term "hardware independent user description of a logic circuit" is limiting, in that it is found only in the preambles of the subject claims. See Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc., 289 F.3d 801, 808 (Fed. Cir. 2002) ("In general, a preamble limits the invention if it recites essential structure or steps, or if it is necessary to give life, meaning, and vitality to the claim[;] [c]onversely, a preamble is not limiting where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention.") (internal quotations and citation omitted). Synopsys contends the term is not limiting. Mentor contends the term is limiting. If the term is limiting, the parties dispute its proper construction as found, for example, in Claim 1 of the '841 patent. See '841 patent, col. 62:61-62.

[5] At the hearing, Mentor stated it would accept "triggered by," which prompted the Court's additional change from "clock edge" to "clock signal."

For the reasons stated by Synopsys, the Court finds "hardware independent user description" is not a limitation, and, accordingly, said term is not construed herein.

7. "GOTO Statement" ('841 Patent, Claim 1)

Similarly, the parties dispute whether the term "GOTO statement," which likewise only appears in the preamble, is limiting and, if so, its proper construction as found in Claim 1 of the '841 patent. See '841 patent, col. 62:63.

For the reasons stated by Synopsys, the Court finds "GOTO statement" is not a limitation, and, accordingly, said term is not construed herein.

8. "Operational Characteristics of Said Logic Network" ('318 Patent, Claim 25)

The parties dispute the proper construction of "operational characteristics of said logic network" as found in Claim 25 of the '318 patent. See '318 patent, col. 65:55-56. Synopsys contends the term should be given its plain and ordinary meaning, which, according to Synopsys, is "a user description of the desired operation of the logic network, independent of the specific hardware for implementing the logic network." Mentor proposes the term be construed as "a user description of the desired operation of a logic circuit containing only signal levels in a logic network and the conditions under which those signal levels are generated, without describing the logical elements, design entities, components or other structures for implementing the logic circuit."

The Court, for the reasons stated by Mentor, hereby construes "operational characteristics of said logic network" as "a user description of the desired operation of a logic circuit containing only signals in a logic network and the conditions under which those signals are generated."[6]

9. "Inferring" ('420 Patent, Claims 1, 10, 11, and 20)

The parties dispute the proper construction of "inferring" as found, for example, in

[6] The Court's construction substitutes "signals" for "signal levels," consistent with the Summary of the Invention, on which Mentor relies, see '318 patent, col. 2:25-29, and the balance of Mentor's construction does not address what "operational characteristics" are, but, rather, what Mentor contends they are not.

Claim 1 of the '420 patent. See '420 patent, col. 9:49. Synopsys contends "inferring" should be given its plain and ordinary meaning, which, according to Synopsys, is "deducing [e.g., the existence of a resetable memory from a behavioral or RTL level description of a semiconductor circuit]." Mentor proposes the term be construed as "recognizing that a portion of circuit design corresponds to a specific hardware structure or class of structures."

The Court, for the reasons stated by Synopsys, hereby construes "inferring" in accordance with its plain and ordinary meaning, which is "deducing."

10. "Resetable Memory" ('420 Patent, Claims 1-3, 10-13, and 20)

The parties dispute the proper construction of "resetable memory" as found, for example, in Claim 1 of the '420 patent. See '420 patent, col. 9:49. Synopsys contends "resetable memory" should be construed as "a memory unit with a plurality of cells, each cell associated with a unique address that provides access to that storage cell, where the memory unit can be reset to a particular value." Mentor proposes the term be construed as "a unit comprising one or more storage cells that can set the read value of each storage cell in the unit to '0' in a single step."

The Court, for the reasons stated by Synopsys, hereby construes "resetable memory" as "a memory unit with a plurality of cells, each cell associated with a unique address that provides access to that storage cell, where the memory unit can be reset to a particular value."

11. "Level Sensitive Latch" ('841 Patent, Claim 1)

The parties do not dispute that Synopsys, as set forth in the prosecution history of the '841 patent, requested Claim 1 be amended to substitute "flow through latch" for "level sensitive latch," and it is the Court's understanding that both parties, at the hearing, were in agreement that, although the patent was issued without the requested amendment, acceptance thereof by the Patent and Trademark Office is ministerial in nature. Under such circumstances, the Court finds "level sensitive latch" as it appears in Claim 1 of the '841 patent is, in actuality, "flow through latch," a term neither party requested be

construed. Moreover, even if a dispute exists as to the proper construction of "flow through latch," the parties were limited to "a maximum of 10" terms to be construed in connection to the above-referenced briefing and hearing. See Patent L.R. 4-3(c).[7]

IT IS SO ORDERED.

Dated: November 7, 2013

MAXINE M. CHESNEY
United States District Judge

[7] Recently, on November 6, 2013, Synopsys filed a "Motion for Leave to File a Proposed Construction for 'Flow Through Latch,'" in which Synopsys states the parties have not been able to agree on a construction for "flow through latch," and submits a proposed construction to be used "[i]f the Court decides that a construction is desirable." (See Motion 2.) Said motion is not addressed herein.