IN THE UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

SYNOPSYS, INC.,

Plaintiff,

v.

ATOPTECH, INC.,

Defendant.

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No. C-13-2965 MMC

ORDER CONSTRUING CLAIMS

Before the Court is the parties' dispute regarding the proper construction of ten terms in four patents, specifically, U.S. Patent No. 6,567,967 ("'967 Patent"), U.S. Patent No. 6,507,941 ("'941 Patent"), U.S. Patent No. 6,237,127 ("'127 Patent"), and U.S. Patent No. 6,405,348 ("'348 Patent"). The matter came on regularly for hearing on November 30, 2015. Patrick T. Michael and Krista S. Schwartz of Jones Day appeared on behalf of Synopsys, Inc. ("Synopsys"). Philip W. Marsh and Willow Noonan of Arnold & Porter LLP appeared on behalf of ATopTech, Inc. ("ATopTech"). At the hearing, the Court afforded the parties leave to file supplemental briefing, upon receipt of which the Court took the matter under submission.

Having considered the parties' written submissions, and the arguments of counsel at the hearing, the Court rules as follows.

1. "Block"/"Blocks" (Claims 1, 5, 7, 10, 32-36 of the '967 Patent)

Synopsys contends the term "block"/"blocks" should be given its "plain and ordinary meaning" and, consequently, that no construction is required.[1] ATopTech proposes the term be construed as "a small portion of a design, above the cell level, that is designed and/or laid out separately comprising cells."

The Court, for the reasons stated by ATopTech,[2] construes the term "block"/"blocks" as "a portion of a design that is designed and/or laid out separately and comprising one or more cells." For the reasons stated by Synopsys, the Court's construction omits the word "small" and the phrase "above the cell level."

2. "Subgrid"/"Subgrids" (Claims 1, 17, 21, 26 of the '941 Patent)

Although the parties, in their Joint Claim Construction and Prehearing Statement, proposed differing constructions for the term "subgrid"/"subgrids," the parties agreed at the hearing, and the Court finds, "subgrid"/"subgrids" is properly construed as "a finer resolution grid."

3. "Tag" (Claim 1 of the '127 Patent)

Synopsys contends the term "tag" should be given its "plain and ordinary meaning" and, consequently, that no construction is required. ATopTech proposes the term be construed as "a data structure pointed to by an RF timing table which has two parts: i) a first part which is loaded with a unique identifier for the clock driving the flip flop for which the RF timing table was created, and ii) a second part which can contain a variety of labels."

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[1]Unless otherwise stated, the parties' respective constructions as set forth herein are taken from their "Joint Claim Construction and Prehearing Statement Under Patent Local Rule 4-3," filed August 31, 2015.

[2]Reference herein to a party's "reasons" includes, unless otherwise stated, the reasons provided in said party's written submissions and by counsel for said party at the hearing.

The Court, for the reasons stated by ATopTech, construes the term "tag" as "a data structure pointed to by an RF timing table which has two parts: i) a first part which is loaded with a unique identifier for the clock driving the flip flop for which the RF timing table was created, and ii) a second part which can contain a variety of labels."

To the extent Synopsys argued at the hearing that the term is broad enough to encompass circuit elements other than flip flops, the Court is not persuaded. See '127 Patent, at 2:1-4 (explaining "[t]he static timing analysis of the present invention is performed upon units of the circuit . . . which comprise a set of 'launch' flip flops, non-cyclic combinational circuitry and a set of 'capture' flip flops").

4. "Timing table" (Claims 1, 4 of the '127 Patent)

Synopsys contends the term "timing table" should be given its "plain and ordinary meaning" and, consequently, that no construction is required. ATopTech proposes the term be construed as "a table comprised of the following four values: minimum rise time (minRT), maximum rise time (maxRT), minimum fall time (minFT) and maximum fall time (maxFT); and having its own tag."

The Court, for the reasons stated by ATopTech, construes the term "timing table" as "a table comprised of the following four values: minimum rise time (minRT), maximum rise time (maxRT), minimum fall time (minFT) and maximum fall time (maxFT); and having its own tag."

5. "A bump-envelope waveform" (Claims 1, 8, 15, 22 of the '348 Patent)

Synopsys proposes the term "bump-envelope waveform" be construed as "a waveform encapsulating a response of the primary net." ATopTech proposes the term be construed as "the waveform obtained by stretching a bump-like waveform for the size of the aggressor switching window where 'bump-like waveform' is 'a waveform of the voltage fluctuation on the output of the primary net caused by switching of the input of the aggressor net.'"

The Court construes the term "bump-envelope waveform" as "a waveform encompassing, for the size of the aggressor timing window, the responses of a primary net caused by the switching of the input of an aggressor net."

In adopting the above construction, the Court considered both parties' proposals and, while the Court agrees with ATopTech that Synopsys's definition is too general to be meaningful, the Court also agrees with Synopsys that the claim is not limited to the embodiment on which ATopTech's construction is based.

6. "Means for identifying a cross-coupled circuit contained within said netlist, wherein said cross-coupled circuit includes a primary net and an aggressor net" (Claim 15 of the '348 Patent)

The parties agree that the term should be construed as a means-plus-function limitation pursuant to 35 U.S.C. § 112(f), and that the function is "identifying a cross-coupled circuit contained within said netlist, wherein said cross-coupled circuit includes a primary net and an aggressor net." Synopsys's proposed structure is a "general purpose computer system 112 configured to identify primary and aggressor nets of a cross-coupled circuit model of an interconnect stage based on primary/aggressor grouping information created based on coupling capacitor connectivity, and equivalents thereof." ATopTech contends the term is indefinite and, in the alternative, proposes as the structure a "computer program static timing analysis tool capable of reading a netlist in Verilog, VHDL, Epic, or SPICE formats, and capable of reading parasitic component lists in DSPF, SPEF or SPICE formats."

The Court, for the reasons stated by ATopTech in its supplemental brief, finds the term is indefinite.

7. "First simulation means for generating a primary waveform of said cross-coupled circuit" (Claims 15, 19 of the '348 Patent)

The parties agree that the term should be construed as a means-plus-function limitation pursuant to 35 U.S.C. § 112(f), and that the function is "generating a primary waveform of said cross-coupled circuit." Synopsys's proposed structure is a "general purpose computer system 112 configured to generate a primary waveform by applying a

single switching input to a primary net without switching the input of the aggressor net." ATopTech's proposed structure is a "circuit simulation program that applies a single switching input to a primary net without switching the input of a cross-coupled aggressor net to cause the primary waveform to be output."

The Court construes the structure as "a static timing analysis program configured to generate a primary waveform by applying a single switching input to a primary net without switching the input of the aggressor net."

At the hearing, the parties agreed on the phrase "static timing analysis program," and, with two exceptions, essentially agreed on the balance of the Court's construction. As to the two points of disagreement, specifically, ATopTech's proposal to further specify the aggressor net and method of generating the waveform, the Court, for the reasons stated by Synopsys, finds such limitations are not appropriate.

8. "Second simulation means for generating a bump-envelope waveform of said cross-coupled circuit" (Claim 15 of the '348 Patent)

The parties agree that the term should be construed as a means-plus-function limitation pursuant to 35 U.S.C. § 112(f), and that the function is "generating a bump-envelope waveform of said cross-coupled circuit." Synopsys's proposed structure is a "general purpose computer system 112 configured to generate responses of the primary net caused by switching of the input of an aggressor net and encapsulating the waveform response to form a bump-envelope waveform, and equivalents thereof." ATopTech contends the term is indefinite and, in the alternative, proposes as the structure a "circuit simulation program that generates a bump-like waveform by switching the input of the aggressor net, and stretches the bump-like waveform for the size of a switching window that corresponds to switching an input on an aggressor net."

The Court construes the structure as "a static timing analysis program that generates a bump-like waveform by switching the input of the aggressor net, and stretches the bump-like waveform for the size of a switching window that corresponds to switching the input of the aggressor net."

Contrary to ATopTech's argument, the Court, for the reasons stated by Synopsys, finds the term is not indefinite, and, at the hearing, the parties, in the event of such finding, agreed upon the phrase "static timing analysis program." With respect to the remainder of the construction, the Court, for the reasons stated by ATopTech, adopts, in essence, ATopTech's alternative construction. See '348 Patent, at 11:32-57 (describing generation of bump-envelope waveform by first generating "bump-like waveform on the primary net by switching the input of the aggressor net," and then "stretching the bump-like waveform . . . for the size of the switching window"); 35 U.S.C. § 112(f) (providing means-plus-function term "shall be construed to cover the corresponding structure, material, or acts described in the specification").

9. "First calculation means for determining a threshold voltage crossing point of said composite waveform" (Claim 15 of the '348 Patent)

The parties agree that the term should be construed as a means-plus-function limitation pursuant to 35 U.S.C. § 112(f), and that the function is "determining a threshold voltage crossing point of said composite waveform." Although the parties, in their Joint Claim Construction and Prehearing Statement, proposed differing constructions, the parties agreed at the hearing, and the Court finds, that the structure is properly construed as "a static timing analysis program configured to identify the time at which the composite waveform crosses a threshold voltage."

10. "Second calculation means for determining a worst case aggressor switching time based on said threshold voltage crossing point" (Claim 15 of the '348 Patent)

The parties agree that the term should be construed as a means-plus-function limitation pursuant to 35 U.S.C. § 112(f), and that the function is "determining a worst case aggressor switching time based on said threshold voltage crossing point." Although the parties, in their Joint Claim Construction and Prehearing Statement, proposed differing constructions, the parties agreed at the hearing, and the Court finds, that the structure is properly construed as "a static timing analysis program that subtracts the times needed for

each aggressor response to reach its peak voltage point from the time at which the composite waveform voltage crosses a threshold voltage."

IT IS SO ORDERED.

Dated: January 19, 2016

MAXINE M. CHESNEY
United States District Judge