UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

INTEL CORPORATION,

Plaintiff,

v.

TELA INNOVATIONS, INC.,

Defendant.

Case No. 3:18-cv-02848-WHO

CLAIM CONSTRUCTION ORDER

Re: Dkt. No. 163

Before me are six patents from the same patent family, all assigned to declaratory judgment defendant Tela Innovations, Inc., and all asserted against plaintiff Intel Corporation. The patented technology aims to improve the design and manufacturability of integrated circuits by ameliorating difficulties associated with the lithographic gap, or the size difference between ever-shrinking semiconductor features and the wavelength of light used to fabricate them. The parties have asked me to construe seven terms from the asserted claims. My constructions are below.

BACKGROUND

Between November 4, 2008 and January 22, 2019, the United States Patent and Trademark Office ("PTO") issued United States Patent Nos. 7,446,352 ("the '352 Patent"), 7,943,966 ("the '966 Patent"), 7,948,012 ("the '012 Patent"), 10,141,334 ("the '334 Patent"), 10,141,335 ("the '335 Patent"), and 10,186,523 ("the '523 Patent") (collectively, the "patents in suit"). *See* Declaration of Frank Liu ("Liu Decl."), Exs. 1-6 [Dkt. Nos. 166-2, 166-3, 166-4, 166-5, 166-6, 166-7]. All of the patents in suit are part of the same patent family, all claim priority to Provisional Application No. 60/781,288, filed on March 9, 2006, and all list Tela as the sole assignee.

Intel filed this declaratory judgment action on May 15, 2018.[1] Dkt. No. 1. Since that time, I have resolved a motion to transfer, several motions to dismiss and strike, a disputed motion for a protective order, and several discovery disputes. *See* Dkt. Nos. 64, 70, 86, 162. The parties briefed claim construction starting on June 13, 2019, and each submitted an electronic technology tutorial in advance of the claim construction hearing. *See* Dkt. Nos. 163, 173. After providing the parties with my tentative opinions, I heard argument on September 27, 2019. Dkt. Nos. 172, 173.

LEGAL STANDARD

Claim construction is a matter of law. *See Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 372 (1996); *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). "Generally, a claim term is given its ordinary and customary meaning—the meaning that a term would have to a person of ordinary skill in the art in question at the time of the invention." *Howmedica Osteonics Corp. v. Zimmer, Inc.*, 822 F.3d 1312, 1320 (Fed. Cir. 2016) (internal quotation marks and citation omitted). In determining the proper construction of a claim, a court begins with the intrinsic evidence of record, consisting of the claim language, the patent specification, and, if in evidence, the prosecution history. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005); *see also Vitronics*, 90 F.3d at 1582. "A claim term used in multiple claims should be construed consistently . . . ." *Inverness Med. Switzerland GmbH v. Princeton Biomeditech Corp.*, 309 F.3d 1365, 1371 (Fed. Cir. 2002).

"The appropriate starting point . . . is always with the language of the asserted claim itself." *Comark Commc'ns, Inc. v. Harris Corp.*, 156 F.3d 1182, 1186 (Fed. Cir. 1998). "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Phillips*, 415 F.3d at 1312. "There are only two exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution." *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012).

[1] The patents at issue in the case have evolved since it was initiated.

Such redefinition or disavowal need not be express to be clear. *Trustees of Columbia Univ. in City of New York v. Symantec Corp.*, 811 F.3d 1359, 1364 (Fed. Cir. 2016).

Courts read terms in the context of the claim and of the entire patent, including the specification. *Phillips*, 415 F.3d at 1313. The specification is "the single best guide to the meaning of a disputed term." *Vitronics*, 90 F.3d at 1582. "The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction." *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998). The court may also consider the prosecution history of the patent, if in evidence. *Markman*, 52 F.3d at 980. The prosecution history may "inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be." *Phillips*, 415 F.3d at 1317 (citing *Vitronics*, 90 F.3d at 1582-83); *see also Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005) ("The purpose of consulting the prosecution history in construing a claim is to exclude any interpretation that was disclaimed during prosecution.") (internal quotations omitted).

In most situations, analysis of the intrinsic evidence alone will resolve claim construction disputes, *Vitronics*, 90 F.3d at 1583; however, a court can further consult "trustworthy extrinsic evidence" to compare its construction to "widely held understandings in the pertinent technical field," *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1309 (Fed. Cir. 1999). Extrinsic evidence "consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises." *Markman*, 52 F.3d at 980. All extrinsic evidence should be evaluated in light of the intrinsic evidence, *Phillips*, 415 F.3d at 1319, and courts should not rely on extrinsic evidence in claim construction to contradict the meaning of claims discernible from examination of the claims, the written description, and the prosecution history, *Pitney Bowes*, 182 F.3d at 1308 (citing *Vitronics*, 90 F.3d at 1583).

DISCUSSION

I. THE TECHNOLOGY

The patents at issue aim to improve the design and manufacturability of integrated circuits by creating solutions to manage the lithographic gap. '352 Patent 1:49-51. Integrated circuit chips are the building blocks of devices like computers, smart phones, and tablets, and transistors are the building blocks of integrated circuit chips. Today, a single integrated circuit chip includes billions of transistors, which form the bottom layer of the chip, connected to the layers above by metal interconnects. Transistors are effectively switches that control the flow of electrical current through a circuit.

Transistors are made up of a substrate, a source region, a drain region, and a gate. A semiconductor material forms the substrate. The source and drain regions have the same charge, either positive or negative, which is created by introducing impurities during the fabrication process. The transistor gate can be made of metal or polysilicon. Voltage applied to the transistor gate determines whether a channel forms underneath the gate, allowing charge to flow between the source and drain regions. When the opposite charge is applied to the gate, a current begins to flow through the substrate between the source and drain regions (i.e., the transistor is "on").

Fabrication of integrated circuits occurs one layer at a time, beginning with the bottom transistor layer, known as the front end. To fabricate transistors, different materials are added, altered, and removed until the desired features are present. The Asserted Patents are primarily directed to one tool used during fabrication, called photolithography, or lithography. Lithography is used to create a specific pattern of gates on the substrate. Once the gate material has been deposited onto the substrate, a material called photoresist, which is sensitive to light, is placed on top.[2] A light is shone through a patterned mask, altering the chemical nature of the photoresist that it reaches and creating the desired pattern. When the photoresist is developed, depending on what type of photoresist was used, either the parts that were exposed to light or the parts that were not exposed to light will remain. The exposed gate material, i.e. without photoresist on top, is

[2] This account given in this Order does not detail every step involved in semiconductor fabrication.

chemically etched away, leaving the desired gate pattern. Finally, ashing removes the remaining photoresist.

When transistors are too close, they can electrically interfere with one another. With up to billions of transistors on a single chip, they might be separated by only the space of only one one-hundredth of a human hair. Despite this proximity, there are a few ways to prevent transistors from interfering with one another. Dummy gates, which lack source and drain regions, can separate transistors. In addition, field oxide can be used as an insulator to cover the portions of the substrate that do not have active transistors, and gates can be formed on top of the field oxide.

At the time of the '352 Patent, transistor feature sizes had decreased and were approaching 45 nm (nanometers).[3] '352 Patent 1:27-30. Because those feature sizes are smaller than the wavelength of light, unintended interactions can occur between neighboring features during lithography. *See id.* at 1:24-27. Specifically, unwanted shapes may be created (constructive interference) or desired shapes may be removed (destructive interference). *Id.* 1:35-41. The patented technology aims to create a solution "for managing lithographic gap issues as technology continues to progress toward smaller semiconductor device features sizes." *Id.* at 1:49-51.

II. CLAIM CONSTRUCTION

The parties agree on the construction of the following two terms:

Claim Term	Agreed Construction
"diffusion region"	selected portions of the substrate within which impurities have been introduced to form the source or drain of a transistor
"a lithography process"	plain and ordinary meaning, *i.e.*, a process by which a pattern is imprinted on a resist or semiconductor wafer using light using a mask

Joint Claim Construction and Prehearing Statement [Dkt. No. 163] 2. The parties dispute seven terms, and I construe them as follows.

[3] Also at the time of the '352 Patent, improvement in chemical mechanical polishing (CMP) allowed more interconnect layers to be stacked together. *Id.* at 1:21-23. The topology of the different interconnect layers can limit how many layers can be stacked together because "islands, ridges, and troughs can cause breaks in the interconnect lines that cross them." *Id.* at 17:13-22. CMP can help flatten the surface of the semiconductor wafer to facilitate stacking. *Id.* at 17:23-28.

A. "linear gate electrode segment, linear conductor segment(s), linear conductive segment(s), and (interconnect) linear conductive structures"

Tela's Proposal	Intel's Proposal	Court's Ruling
a 3D conductive structure having a rectangular shape of a given width defined in a plane parallel to a top surface of the substrate and defined to have a length that extends in one direction	having a consistent vertical cross-section shape and extending in a single direction over the substrate	extending in a single direction over the substrate
'352: 1, 17; **'966**: 2, 31, 33; **'012**: 2, 8, 11, 13, 28		

The parties first dispute the term "linear," which is found in the '352, '966, and '012 Patents. Tela argues that "linear" is to be defined and understood from the top-down view, while Intel counters that it should be understood in terms of a cross-section view. Because the claims themselves do not support the limitation Intel seeks to place on the term, nor does the specification clearly do so, I agree with Tela's position on the term "linear."

1. The plain and ordinary meaning of the claim language

I begin by analyzing the language of the claims themselves. Claim 2 of the '966 Patent reads in part, "wherein the gate electrode level region includes a plurality of linear conductive segments each formed to have a respective length and a respective width as measured parallel to the substrate region . . . ." '966 Patent 27:45-48. Claim 2 of the '012 Patent reads, "wherein the gate electrode level region includes a plurality of linear conductive segments each formed to have a respective length and a respective width as measured parallel to the substrate region . . . ." '012 Patent 33:3–6.

This language shows—and the parties agree—that "linear" at the very least means free of bends on the x-y axis. Op'g 10; Resp. 11. Indeed, that is the plain and ordinary meaning of the term: a straight line. According to Tela, this understanding is enough to construe the term because "linear" is properly understood according to the x-y axis, from the top-down view. Because the patents are directed to layout files, and features in a layout file are defined from a top view, this term too should be understood from the top view. *See* Liu Decl. Ex. 7, Declaration of Daniel Foty ("Foty Decl.") [Dkt. No. 166-8] ¶ 83 (asserting that the patentee used "linear" from

the top view).

The difficulty with construing this term arises from the fact that—despite the patents' focus on the x- and y-axes rather than the z-axis—"linear features" are three-dimensional. The specifications of the Asserted Patents do not describe or represent linear features only from the top view, although Tela rightly points out that most figures show that perspective. *See* Reply 3. But the patents do include and describe some three-dimensional figures. Because the claim language does not expressly address the z-axis of linear-shaped features, it is necessary to review the intrinsic evidence to determine whether it clearly communications anything about the z-axis. My review of the intrinsic evidence is guided by this admonition from the Federal Circuit:

> [E]ven where a particular structure makes it 'particularly difficult' to obtain certain benefits of the claimed invention, this does not rise to the level of disavowal of the structure. It is likewise not enough that the only embodiments, or all of the embodiments, contain a particular limitation. We do not read limitations from the specification into claims; we do not redefine words. Only the patentee can do that. To constitute disclaimer, there must be a clear and unmistakable disclaimer.

Thorner v. Sony Computer Entm't Am. LLC, 669 F.3d 1362, 1366–67 (Fed. Cir. 2012) (internal citation omitted).

2. The intrinsic evidence

The specification serves as "the single best guide to the meaning of a disputed term." *See Phillips*, 415 F.3d at 1315. The specification of the patents at issue primarily discusses linear features by reference to the x and y directions. For example, the '352 Patent reads, "It should be appreciated that the linear-shaped feature may be oriented to have its length 305 extend in either the first reference direction (x), the second reference direction (y), or in diagonal direction defined relative to the first and second reference directions (x) and (y). . . . Also, it should be understood that the linear-shaped feature is free of bends, i.e., change in direction, in the plane defined by the first and second reference directions." '352 Patent 9:4–9, 14–17.

One part of the specification of the '352 Patent provides:

> The dynamic array is defined such that layers (other than the diffusion region layer 203) are restricted with regard to layout feature shapes that can be defined therein. Specifically, in each layer other than the diffusion region layer 203, only linear-shaped layout features are allowed. **A linear-shaped layout feature in a given layer is characterized as having a consistent vertical cross-section shape and extending in a single common direction over the substrate.** Thus, the linear-shaped layout features define structures that are on-dimensionally varying.

'352 Patent 7:1–10 (emphasis added). Although Intel relies on this language to support its proposed construction, the language does not carry the dispositive weight Intel assigns to it. First, it is telling that the description specifically omits the diffusion region from the requirement that only linear-shaped features are allowed. The arrows below point to the diffusion region.

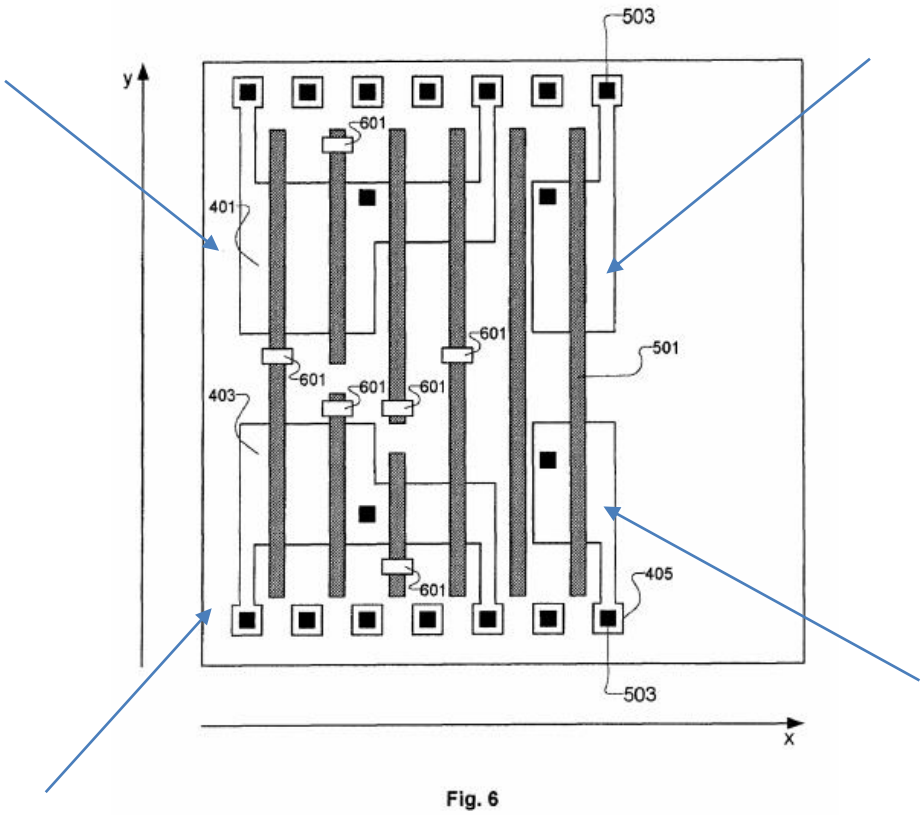


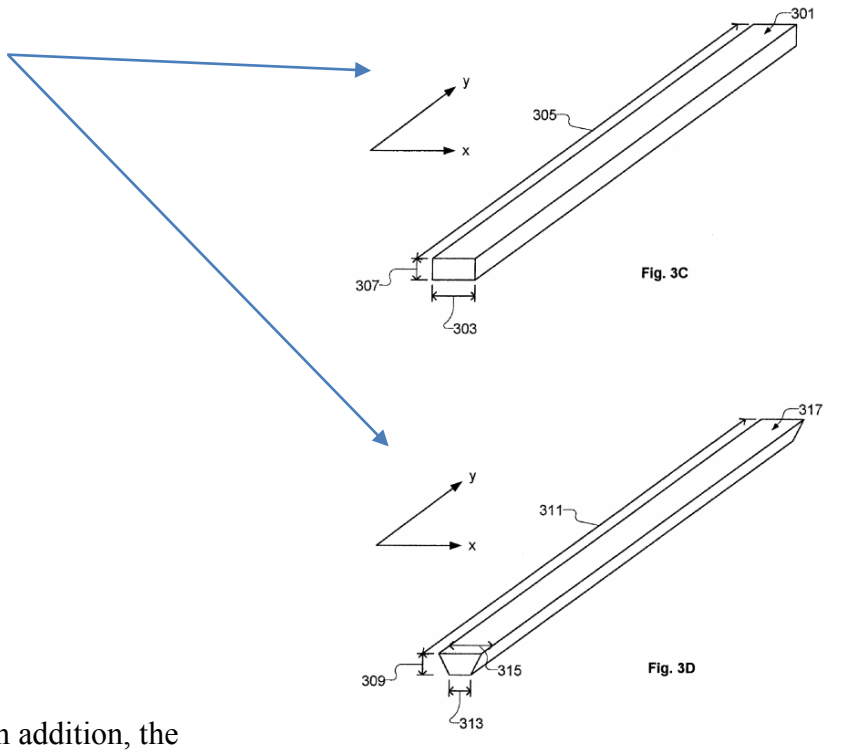
Fig. 6

'352 Patent, Figure 6. As is clear in the image above, the diffusion region does not run in a straight line on the x-y axis; instead, it has bends and direction changes. By contrast, the darker gate electrode features are linear—they run in straight, parallel lines.

It is not completely clear that the consistent-cross-section description above is limited to

just one embodiment, and Intel argues that following language shows that it applies broadly to all linear-shaped features: "The specific configurations and associated requirements of the linear-shaped features in the various layers 207-223 are discussed further with regard to FIGS. 3-15C." '352 Patent 7:23-26. Intel argues that with this language, the specification expands the cross-sectional definition to apply to all of the figures. I disagree. That language instead serves to clarify that other embodiments of linear-shaped features will have different "associated requirements"; they will not necessarily be required to have a consistent cross-sectional shape.

Next Intel contends that Figures 3C and 3D support its construction because those figures show three-dimensional features with consistent cross-sectional shapes. But the specification describes these figures as "exemplary linear-shaped feature[s]" that are "defined to be compatible with the dynamic array, in accordance with one embodiment of the present invention." '352 Patent 8:58–60, 9:18–20. Accordingly, the figures are limited to just one embodiment.



In addition, the specification clarifies that while Figures 3C and 3D have rectangular and trapezoidal cross-sections, "it should be understood that the linear shaped features having other types of cross-sections can be defined within the dynamic array." *Id.* at 9:45–49 (emphasis added). Indeed, "essentially any suitable cross-sectional shape of the linear-shaped feature can be utilized **so long as the linear-shaped feature**

is defined to have a length that extends in one direction . . . ." *Id.* at 9: 49–52 (emphasis added). I agree with Tela that this language shows that "irrespective of the cross-sectional shape, the defining characteristic of a linear feature is whether its length extends in one direction in an x-y plane and has consistent width (*i.e.*, free of bends)." *See* Op'g 13–14. While all linear features in that embodiment must have a consistent cross-sectional shape, that shape is not limited to a rectangle or a trapezoid as long as it is consistent across the feature. Figures 3C and 3D are accompanied by arrows that point in the x and y directions rather than the z direction, confirming that the x-y plane is the focus.

Figures 101A, 101B, and 101C, while showing rectangular shapes, do not support Intel's construction for a two reasons. First, they are limited to a single embodiment. *See* '966 Patent 11:28-31 ("FIG. 1 is an illustration showing a number of neighboring layout features and a representation of light intensity used to render each of the layout features, in accordance with one embodiment of the present invention."). Second, they are layout features in a mask used during the lithography process rather than three-dimensional conductive structures. *See id.* at 11:31-34 ("Specifically, three neighboring linear-shaped layout features (101A-101C) are depicted as being disposed in a substantially parallel relationship within a given mask layer."). These figures do not support Intel's argument that all linear features necessarily have consistent cross-sections.

The patents' description of some benefits of the dynamic array, on the other hand, do seem to favor Intel's proposed construction. The dynamic array architecture aims in part to achieve substantially uniform topologies in order to facilitate the stacking of more interconnect layers, to improve the effectiveness of the CMP procedure, and to reduce the unpredictability of light interaction during lithography. '352 Patent 17:13-18:49; *see* Foty Decl. ¶¶ 75-77. As the specification lays out the difficulties of these processes, widely varying topologies would prevent the realization of these benefits.[4] But this is not enough to support the narrowing of the claim language that Intel proposes. *See Thorner*, 669 F.3d at 1366–67 ("[E]ven where a particular

[4] Tela notes the difficulty of achieving a uniform topology: "A skilled artisan would understand that, in such a standard CMOS process, as features traverse across the substrate, there will be variations in the cross-sectional shape, particularly when traversing across shallow trench isolation regions." Reply 4.

structure makes it 'particularly difficult' to obtain certain benefits of the claimed invention, this does not rise to the level of disavowal of the structure."). As Tela argued at the hearing, the primary benefit of the technology is related to lithography, and those benefits are realized by placing layout features in a mask in a way that makes light interactions more predictable. *See* '352 Patent 18:32-35 ("The regular architecture implemented within the dynamic array allows the light interaction unpredictability in the via lithography to be removed . . . .").

The plain meaning of "linear" is a straight line. As Tela argued at the hearing, depth is simply not a defining characteristic of the technology claimed in the patents. Intel's proposed construction would improperly limit otherwise broad claim language. Because Tela indicated at the hearing that it was comfortable with the second half of Intel's proposal, and because I conclude that its wording would be more helpful to the jury, I adopt the following construction of linear: "extending in a single direction over the substrate."

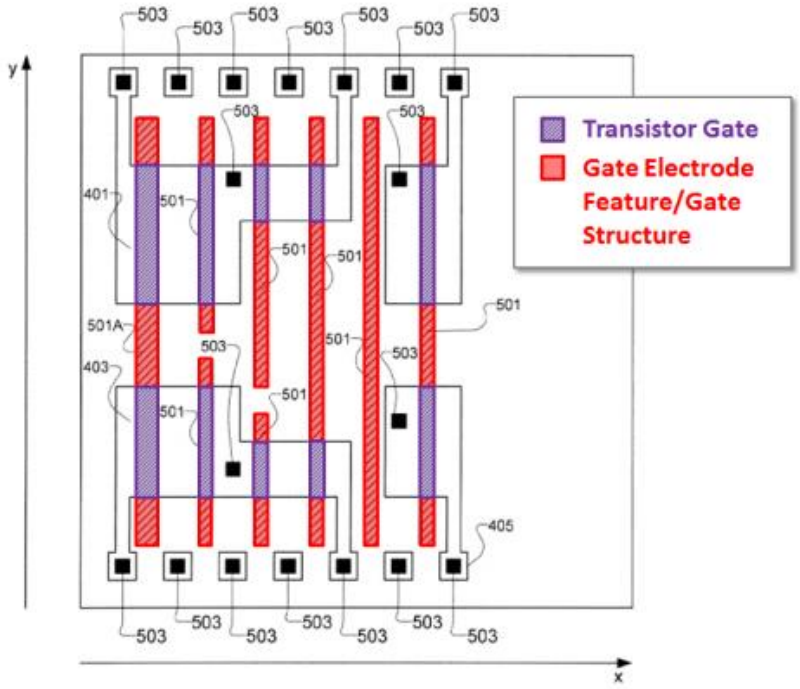
B. "gate structure(s) and gate electrode feature(s)"

Tela's Proposal	Intel's Proposal	Court's Ruling
feature that can form a gate(s) of a transistor(s) defined below the gate contact	linear-shaped feature comprising a gate(s) of a transistor(s) or a dummy gate	feature comprising a gate(s) of a transistor(s) or a dummy gate
'334: 1, 2, 4, 10, 20, 22; **'335**: 1, 2, 4, 10, 20, 22; **'523**: 1, 2, 4, 10, 18, 22, 26		

The parties next dispute the terms "gate structure" and "gate electrode feature," which are found in the '334, '335, and '523 Patents. There are three main disputes here. First is the question of whether to define these terms as being "linear-shaped features." To support its proposal that the structures should be construed as linear, Intel relies on specification language that describes a "rectangular shape," arguing that the specification was referring to rectangular cross-sections. Resp. 14-15. I cannot agree. Not only does Intel's argument depend on my acceptance of its construction of linear—which I rejected—but the claims themselves provide no indication that gate structures/ gate electrode features must be linear. It would be improper to impose this new requirement during claim construction.

The parties next dispute how to communicate the fact that gate structures/electrode features can, but may not necessarily, form the gate of a transistor. If gate structures/electrode features do not cross an active portion of the substrate, no transistor is formed; in other words, the gate is a

dummy gate. Below is Figure 5 from the '334 Patent, which Tela excerpts and annotates in its Opening Brief.



The parties substantially agree, but I will adopt Intel's proposal for three reasons. First, I agree with Intel that the language "comprising" is more accurate. A single gate structure can form one or more transistor gates without its entirety being a transistor gate, as Tela's annotations above acknowledge. Second, I agree with Intel's critique that Tela's language improperly suggests that dummy gates "can form a gate(s) of a transistor(s)." *See* Resp. 16. Instead, dummy gates are incapable of forming the gate of a transistor because they lack a source or drain.[5] In addition, even within the same gate electrode feature/ gate structure, some parts are not capable of forming a transistor because they are not above diffusion regions. Third, importantly, Tela does not dispute that the term "dummy gate" is an inaccurate way to describe the portions of a gate structure/ gate electrode contact that do not form transistor gates.

Finally, Tela seeks a construction that would require gate electrode features / gate

[5] Intel further notes, "To the extent Tela's construction means '[does or does not] form a gate of a transistor,' this language is meaningless and imposes no limitation at all—everything on earth does or does not form a gate of a transistor." Resp. 16.

structures to be defined below the gate contact, while Intel argues that dummy gates are generally not defined below a gate contact. I agree with Intel. Figure 6 of the '352 Patent shows two dummy gates (the dark rectangles on the right-hand side), neither of which is below a gate contact (labeled as 601).

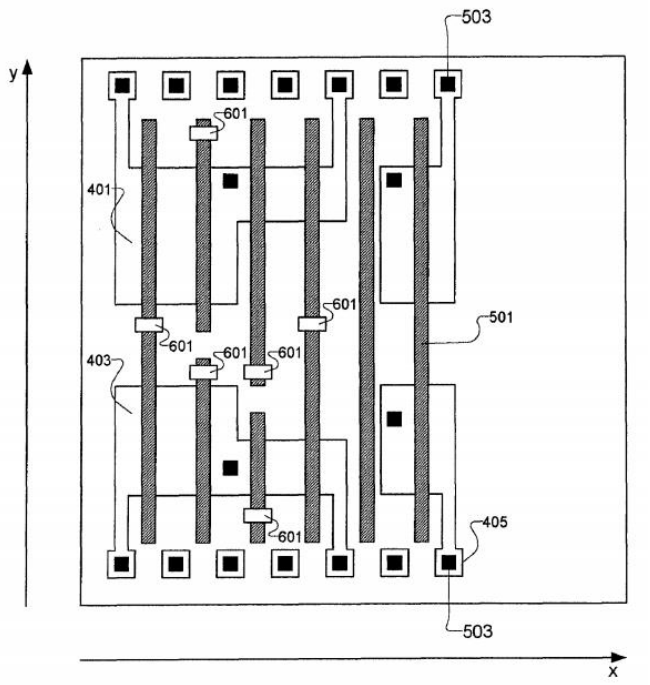


Fig. 6

To the extent that there *is* a contact gate, it should be defined as above the gate it contacts—but because some gate structures/ gate electrode features do not have associated gate contacts, it does not make sense to include that requirement as part of their construction.[6] *See* Resp. 16 ("Thus, while it makes sense to define a gate contact as above the gate that it contacts—as Intel does in Section III.D—it does not make sense to define a gate structure as below a contact that may or may not exist.").

[6] If Tela's proposal defined gate structures/ gate electrode features as below the *layer* of gate contacts, perhaps its construction would be appropriate. But given the singular construction—"**the** gate contact"—despite the absence of gate contacts with some gate structures/ gate electrode features, Tela's proposal is not precise.

C. "gate electrode"

Tela's Proposal	Intel's Proposal	Court's Ruling
portion of the [linear gate electrode segment ('352 Patent) / linear conductive segment ('966 and '012 Patents) / gate structure ('334 and '335 Patents) / gate electrode feature ('523 Patent)] used to control the flow of electrical current between the source and drain regions of a transistor	a portion of the conductive shape in the gate layer that extends over and parallel with a diffusion region to form a transistor gate	a portion of the conductive shape that extends over the diffusion region and is used to control the flow of electrical current between the source and drain regions of a transistor
'352: 1, 16, 17; **'966**: 2; **'012**: 2 , 8, 11, 13; **'334**: 1, 4, 22; **'335**: 1, 4, 22; **'523**: 1, 4, 22, 26		

The parties next dispute the term "gate electrode," which is found in all six patents at issue. The parties dispute (i) whether to construe gate electrode as extending over and parallel with a diffusion region and (ii) whether to describe its structure (as forming a transistor gate) or its function (as controlling the flow of electrical current).[7]

At the hearing, Tela generally expressed agreement that the gate electrode extends over the diffusion region, and language in the patents supports this understanding. *See* '352 Patent at Abstract ("Each linear gate electrode track . . . extends over . . . a diffusion region . . . ."); '966 Patent at Abstract (providing that the "diffusion region layout shapes to be formed within a portion of a substrate . . . a gate electrode level above the portion of the substrate"); *id.* at 8:20-29 (describing "gate electrode portions which extend over one or more of the [p/n]-type diffusion regions to form respective [P/N]MOS transistor devices"); *id.* at 12:38-40 (providing that "gate electrode features 207 are defined above the diffusion regions 203 to form transistor gates"); Op'g 14 (noting "the gate of a transistor is formed by the portion of the gate electrode feature or gate structure that extends over the active portions of the substrate"). Tela raised at the hearing its concern that because there must be a channel between a transistor's source and drain region, a literal understanding of Intel's proposal would prevent a transistor from being formed on a physical chip.[8] With the caveat that I do not construe this term in a way that would prevent the

[7] Intel argues that its proposal is substantially the same as a construction for gate electrode Tela agreed to adopt in a different case. According to Tela, different patents were at issue in that case.

[8] Tela has no concerns with this aspect of the construction with respect to the layout view.

formation of a transistor, I will adopt the construction that the gate electrode extends over a diffusion region.[9]

The parties next dispute whether the gate electrode should be defined as being parallel to the diffusion region. Neither the claim language nor the intrinsic record supports the addition of this requirement. Although Intel is right that the patent claims and specifications use the word parallel, the intrinsic evidence Intel points to does not specifically address the relationship between the gate electrode and the diffusion region, instead talking more generally about the substrate.[10] *See* '012 Patent 32:63-33:2 (providing, "a gate electrode level region . . . formed above and over the Substrate region . . . oriented substantially parallel to the Substrate region"); '352 Patent 7:21-23 (providing, "the linear-shaped layout features in a given layer extend in a common direction over the substrate and parallel with the substrate").

Finally, the parties dispute the appropriateness of a construction that describes the function the gate electrode performs. Intel argues that Tela is improperly inserting a functional requirement into a feature that the patents define only by its structure. Resp. 19. Tela counters that a person of ordinary skill in the art ("POSITA") would understand that the gate electrode controls the flow of electrical current. Reply 9-10. I agree, and the addition would aid the fact finder. For these reasons, and drawing from each party's proposal in a way that would be most helpful to the jury, I will construe gate electrode as "a portion of the conductive shape in the gate layer that extends over the diffusion region and is used to control the flow of electrical current between the source and drain regions of a transistor."

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[9] At the hearing, Intel clarified that it will not argue that complete overlap is necessary in order to "extend over." It understands "extend over" to mean in the vertical direction.

[10] Intel's reliance on Figure 2 of the '966 Patent is not persuasive because it is "an illustration showing a generalized stack of layers used to define a dynamic array architecture, in accordance with one embodiment of the present invention." '352 Patent 6:15-17.

D. "gate electrode contact, gate contact structure(s), contact structure"

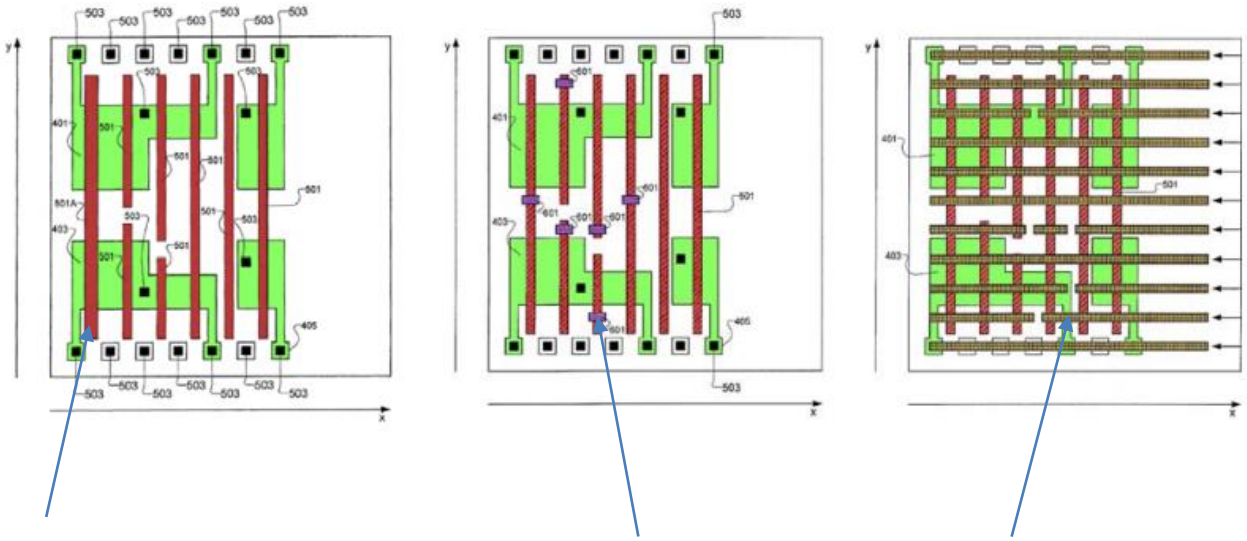
Tela's Proposal	Intel's Proposal	Court's Ruling
a structure that passes through an insulator to enable connection of the gate electrode feature to the overlying metal conduction lines	conductive structure(s) in a gate contact layer above and separate from the gate layer and below and separate from interconnect layers	conductive structure(s) in a gate contact layer above and separate from the gate layer and below and separate from interconnect layers
'352: 17, 19; **'334**: 1, 5, 22; **'335**: 1, 5, 22; **'523**: 1, 22, 26		

The parties next dispute the term "gate contact" and "gate contact structure," which is found in the '352, '334,'335, and '523 Patents. Intel argues that gate contacts "are their own distinct structure in a separate layer," while Tela argues that "some level of physical overlap" is necessary between the contact and the gate and interconnects in order for an electrical connection. *See* Op'g 19-21; Resp. 19-21.

The intrinsic evidence shows that the gate contact structures are a separate structure in a layer that is distinct from the gate layer and the interconnect layer. First, the patents separately name and describe gate structures, contact structures, and interconnects, which "strongly implies that the named entities are not one and the same structure." *See HTC Corp. v. Cellular Commc'ns Equip., LLC*, 701 F. App'x 978, 982 (Fed. Cir. 2017). The Patents further describe the relationship between the different structures, which would not be necessary if they were part of the same structure. *See* '334 Patent 30:63-65 (describing "contact structures positioned and sized to overlap both edges of the top surface of the gate structure to which it is in physical and electrical contact"), 30:31-32 (describing "a first-metal layer formed above top surfaces of the gate structures"). The specification language confirms this understanding. *See* '966 Patent 9:15-18 ("FIG. 6 is an illustration showing a gate electrode contact layer defined above and adjacent to the gate electrode layer of FIG. 5, in accordance with one embodiment of the present invention."), 12:40-42 ("Gate electrode contacts 209 are defined to enable connection between the gate electrode features 207 and the conductor lines."), 12:45-46 ("Interconnect layers are defined above the diffusion contact 205 layer and the gate electrode contact layer 209."), 18:34-37 ("In the gate electrode contat layer, gate electrode contacts 601 are drawn to enable connection of the gate electrode features 501 to the overlying metal conduction lines."), 18:44-48 ("Also, it should be

appreciated that in the present invention, the gate electrode contact 601 is oversized in the direction perpendicular to the gate electrode contact features 501 to ensure overlap between the gate electrode contact 601 and the gate electrode feature 501.").

Figures 5, 6, and 8A from the '966 Patent, shown here with colors added by Intel in its responsive brief, show three distinct stacked layers. Resp. 20 (showing the gate electrode in red, the contact in purple, and the metal interconnect in orange).



gate electrode gate contact interconnect

All of this evidence is sufficient to establish that the gate contact is positioned in a separate layer above the gate and below the interconnect.

Tela critiques Intel's proposal by arguing that "[o]ne of ordinary skill in the art would understand that to form the contacts described in the patent would require some level of physical overlap between the contact and the gate and interconnects to enable the electrical connection between the gate and interconnect features through the contact structure." Op'g 20-21. But Intel's proposal does not eliminate the possibility of physical contact; indeed, claim 1 of the '334 Patent expressly provides that the gate structures "have a respective top surface in physical and electrical contact with a corresponding one of the at least six contact structures." '334 Patent 30:55-58; *see also id.* at 11:34-38 ("Gate electrode contacts 209 are defined to enable connection between the gate electrode features 207 and conductor lines. For example, the gate electrode contacts 209 are

defined to enable connection between transistor gates and their respective conductor nets."), 17:39-43 (describing Figure 6) ("In the gate electrode contact layer, gate electrode contacts 601 are drawn to enable connection of the gate electrode features 501 to the underlying metal conduction lines."). The construction adopted here does not eliminate physical contact but rather clarifies that the gate contact is a separate structure in a separate layer from the gate and the interconnects.

E. "interconnect level region"

Tela's Proposal	Intel's Proposal	Court's Ruling
area within a layer having metal and/or via conductive structures where the layer is located above the diffusion contact layer/gate electrode contact layer and enables definition of the desired circuit connectivity	an area of a layer with conductive structures that traverse over the substrate to enable desired routing and connectivity	an area within a layer having conductive structures where the layer is located above the diffusion contact layer/gate electrode contact layer and enables definition of the desired circuit connectivity
'966: 31, 33, 35; **'012**: 26, 28, 30		

The parties next dispute the term "interconnect level region," which is found in the '966 and '012 Patents. Dependent claim 31 of the '966 Patent reads in part, "An integrated circuit device as recited in claim 2, further comprising: a first interconnect level region that forms part of an overall first interconnect level of the integrated circuit device." '966 Patent 30:45-53. The parties disagree over whether the interconnect level region should be construed as located above the diffusion contact layer and gate contact layer. Intel argues that Tela's proposal improperly adds a "contact layer" requirement even though the claims at issue here do not include language about a contact layer—while other, unasserted claims do. Resp. 22. Tela counters that its proposal is consistent with the specification, that Intel agreed that contact structures are located below the interconnect level in the context of other claims, and that claim terms in the same patent family should be read consistently with one another. Reply 12.

I agree with Tela that the construction of this term should specify the location of the interconnect level region relative to other levels in order to be consistent with the specification and aid the fact finder. *See* '966 Patent 12:45-46 ("Interconnect layers are defined above the diffusion contact 205 layer and the gate electrode contact layer 209."). Accordingly, to the extent that the

various layers are described in a claim,[11] the interconnect level region is defined above the diffusion contact layer and the gate electrode contact layer. I will construe "interconnect level region" as above the gate contacts. I also note that the parties agree that this term not cover the gate electrode layer, which is a distinct claim term and thus a distinct level. *See* Resp. 22 (laying out reasons why Tela is incorrect that Intel's construction would improperly encompass the gate electrode level).

Finally, Intel criticizes Tela's narrow construction of interconnects as metal and via structures, arguing that those materials are listed only in specific embodiments of the invention. I agree. The claim language does not support this narrower understanding of the materials that can form interconnects. For these reasons, I will adopt a modified version of Tela's proposed construction.

F. "[gate / metal / contact] gridline(s)"

Tela's Proposal	Intel's Proposal	Court's Ruling
virtual projected lines along which [gate /metal / contact] features are defined	gridline(s) along which [gate / metal / contact] structures are formed	virtual projected lines along which [gate /metal / contact] features are positioned
'334: 1, 2, 5, 10, 18, 20, 22; **'335**: 1, 2, 5, 10, 18, 20; **'523**: 1, 2, 6, 8, 10, 16-19, 22, 23		

The parties next dispute the term "grideline(s)," which is found in the '334, '335, and '523 Patents. The parties are in substantive agreement on this term and only dispute the accuracy of one another's choice of words. It is clear from the intrinsic evidence, and the parties agree, that the gate/ metal/ contact structures are positioned on a chip along virtual gridlines. *See* Resp. 23 ("Tela's only criticism of Intel's construction is based on the misapprehension that it requires gridlines to be a 'physical construct.' It does not."). Tela criticizes Intel's use of the word "formed," arguing that the features are defined and positioned on the gridlines during the layout process, not the fabrication process. Reply 13. Instead, "There is no need for the gridlines to be used to form the features, because the features were positioned prior to the lithography process." *Id.* at 14.

[11] Intel does not actually dispute the accuracy of this description of the layers' relative orientations. With the clarification that I recognize some claims may omit contact layers, I aim to assuage Intel's concerns that the requirement of such a layer will be improperly added into some claims.

Using the word "positioned" resolves the dispute between "defined" and "formed." Indeed, as the claim language shows, the gate/ metal/ contact structures are *defined* along virtual gridlines during the layout process in preparation for lithography. *See* '335 Patent 30:5-8 (providing, "gate structure layout shapes used as an input to a lithography process, the gate structure layout shapes positioned in accordance with a gate horizontal grid"). They are then *formed* on a chip in positions that are also along a virtual grid as predetermined during the layout process. *See* '334 Patent 30:3-6 (providing, ". . . gate structures formed within a region of a semiconductor chip, the gate structures positioned in accordance with a gate horizontal grid that includes at least seven gate gridlines"), 30:8-12 (providing, "each gate structure in the region . . . positioned to extend lengthwise in a y-direction in a substantially centered manner along an associated gate gridline"). At the hearing, both parties agreed with the tentative after clarifying their views.[12]

G. "physically and electrically separated by a [conductor] line end spacing of minimum size"

Tela's Proposal	Intel's Proposal	Court's Ruling
Plain and ordinary meaning. Not indefinite.	Indefinite.	Indefinite.
'352: 1		

Finally, the parties dispute the term "physically and electrically separated by a [conductor] line end spacing of minimum size," which is found in claim 1 of the '352 Patent. Intel argues that the term is indefinite because the specification fails to provide an objective boundary for determining "how much spacing between gate segments is permitted before it is no longer considered 'minimum.'" Resp. 23–24. Tela counters that the intrinsic evidence gives a POSITA enough information to understand this term with reasonable certainty. Op'g 23-24.

"[A] patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572

[12] Specifically, Intel confirmed that structures are positioned on virtual gridlines on the chip itself, and Tela confirmed that the positioning of the structures along gridlines is determined during the layout process.

U.S. 898, 901 (2014). While "absolute precision is unattainable," the claim language must be "precise enough to afford clear notice of what is claimed, thereby apprising the public of what is still open to them." *Id.* at 901, 910. Terms of degree must have objective boundaries. *Berkheimer v. HP Inc.*, 881 F.3d 1360, 1363–64 (Fed. Cir. 2018). "Because the claims of a patent are afforded a statutory presumption of validity, overcoming the presumption of validity requires that any facts supporting a holding of invalidity must be proved by clear and convincing evidence." *Budde v. Harley-Davidson, Inc.*, 250 F.3d 1369, 1376 (Fed. Cir. 2001).

The claim language surrounding this term reads:

> at least one of the linear gate electrode tracks having multiple linear gate electrode segments adjacently defined thereover in an end-to-end manner such that facing ends of adjacent linear gate electrode segments are physically and electrically separated by a line end spacing of minimum size, wherein a size of each line end spacing within a window of lithographic influence is substantially the same, wherein the minimum size of the line end spacing corresponds to a substantially full occupancy of the at least one linear gate electrode track by the multiple linear gate electrode segments . . .

'352 Patent 21:23-35. The specification devotes little attention to defining "spacing of minimum size." It provides,

> When a given gate electrode track is required to be interrupted, the separation between ends of the gate electrode track segments at the point of interruption is minimized to the extent possible taking into consideration the manufacturing capability and electrical effects. . . . Minimizing the separation between ends of the gate electrode track segments at the points of interruption serves to maximize the lithographic reinforcement, and uniformity thereof, provided from neighboring gate electrode tracks.

Tela argues that these descriptions are sufficient to allow one of ordinary skill in the art to understand "that the line-end spacing is placed and sized in a manner to maximize lithographic reinforcement of neighboring gate electrode segments while taking into consideration electrical effects." Op'g 25.

I disagree. The intrinsic evidence reveals *where* "line end spacing" is located and *why* "minimum size" is desirable,[13] but it provides no objective way to determine *what* "minimum size" means. Because the intrinsic evidence does not provide an objective boundary, it is

[13] As articulated by Tela, "the minimum size allows for substantially full occupancy of the gate electrode track." Op'g 24.

appropriate to consider extrinsic evidence. *See Berkheimer*, 881 F.3d at 1364 (noting that without "objective boundary or specific examples of what constitute[d] 'minimal' in the claims, specification, and prosecution history, the district court [had] properly considered and relied on extrinsic evidence").

According to Intel's expert, by requiring consideration of both "manufacturing capability" and "electrical effects," the specification introduces two measures that are inherently subjective. *See* Subramanian Decl. ¶¶ 92-96. In the semiconductor industry, "manufacturability involves a yield tradeoff." *Id.* ¶ 93; *see* '352 Patent 4:50-67 (acknowledging that products are "manufacturable with a specified probability"). Where there is more space between features, the manufacturing yield might approach 100%, but as the space decreases, the yield will similarly decrease. *See* Subramanian Decl. ¶ 94. As Intel points out, whether any given manufacturing yield is acceptable will depend on a subjective determination based on the manufacturer's goals—"*e.g.*, research (low yield acceptable); small-scale production (medium yield acceptable); mass production (only very high yield acceptable)." Resp. 24. The same is true for electrical effects: smaller spacing will increase the potential for undesirable electrical effects like interference, parasitic capacitance, or cross-talk. Subramanian Decl. ¶¶ 95-96. Whether or not these effects are acceptable depends on a subjective determination of the tradeoffs. The '352 Patent provides no line by which to measure "minimum space," instead explicitly inviting these subjective considerations to guide the determination of what that spacing should be.

Tela asserts that a POSITA would understand minimum size "to refer to the minimum spacings set forth in the design rules," which account for the lithographic concerns referred to in claim 1 of the '352 Patent. Reply 15. Because "[t]he design rules are set before the claimed semiconductor device is manufactured," according to Tela using the design rules to define the spacing is not subjective. *Id.* This argument is unpersuasive. The design rules for any given semiconductor device cannot serve as the objective bounds for determining minimum size; the patent must do that. *See Power Integrations, Inc. v. ON Semiconductor Corp.*, No. 16-CV-06371-BLF, 2018 WL 5603631, at *12-13 (N.D. Cal. Oct. 26, 2018) (finding "maximum period of time" indefinite even though the user "predefined" the value for maximum time value before beginning

the power discharge); *compare id.* at 12 ("Under the claim, 'you have to choose a value, and once you've chosen a value, you have to meet it. And if you do that, you meet the claim.'") *with* Reply 15 ("If that semiconductor device has line-end spacing that is no larger than the minimum allowed by the design rules, then it meets that claim element.").

Tela argues that numerical precision is not required; the patentee intentionally chose to claim "minimum" feature sizes rather than a specific value in order to account for advancements that would allow for smaller feature sizes. Reply 14. While Tela may be right on both counts, the law requires an objective boundary. The '352 Patent provides none; this term is indefinite.

CONCLUSION

For the reasons set forth above, the disputed terms are construed as follows:

Term	Court's Ruling
"linear gate electrode segment, linear conductor segment(s), linear conductive segment(s), and (interconnect) linear conductive structures"	extending in a single direction over the substrate
"gate structure(s) and gate electrode feature(s)"	feature comprising a gate(s) of a transistor(s) or a dummy gate
"gate electrode"	a portion of the conductive shape in the gate layer that extends over the diffusion region and is used to control the flow of electrical current between the source and drain regions of a transistor
"gate electrode contact, gate contact structure(s), contact structure"	conductive structure(s) in a gate contact layer above and separate from the gate layer and below and separate from interconnect layers
"interconnect level region"	an area within a layer having conductive structures where the layer is located above the diffusion contact layer/gate electrode contact layer and enables definition of the desired circuit connectivity
"[gate / metal / contact] gridline(s)"	virtual projected lines along which [gate /metal / contact] features are positioned
"physically and electrically separated by a [conductor] line end spacing of minimum size"	Indefinite

IT IS SO ORDERED.

Dated: November 4, 2019

William H. Orrick
United States District Judge