Exhibit F

JEDEC STANDARD

FBDIMM
Advanced Memory Buffer (AMB)

JESD82-20A

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13 AMB Quad Rank Support

13.1 Background

FB-DIMM supports 2 ranks per DIMM in the Architecture and Protocol spec, the AMB implementations, and the Host Controller designs.

This specification describes the implementation to achieve 4 ranks per DIMM. This is accomplished by making the DIMM appear to have the next higher density DRAMs installed, such that 2 ranks appear to the host controller as 1 rank. Quad Rank Mode A is also included in the AMB, allowing the host controller to utilize that mode of operation. The AMB must support both modes. The difference is in how the Rank Select 1 is determined.

13.2 AMB Signal Changes and DRAM Connections

13.2.1 Quad Rank Signal Requirements

Additional control signals (chip select and ODT) are required for quad rank operation. The Quad rank requirements are as follows:

Table 51 — Function Mapping Legend

Signal	Existing (SR & DR)	Quad Rank Requirement
Chip Select (CS#)	Two chip selects provided, with A and B copies.	Chip Selects are independent per rank, requiring 4 independently controlled Chip Selects. There are not separate A and B signals provided. One signal from the AMB drives both sides, and is terminated on each end.
ODT	One ODT provided, with A & B copies. Both ranks controlled by the one ODT signal.	The original ODT with A and B copies are maintained. Optionally, two more ODT signals are provided that are used for two new ranks. ODT usage is raw card dependent.
CKE	Two CKE signals provided, with A and B copies. AMB (and host) has individual control of CKE on each rank.	For raw cards that require 4 ODT signals, two CKE signals provided, but only the "A" copies, which drive both sides. For raw cards that require only 2 ODT signals, both the A and B copies of the CKE signals are available. CKE0 drives ranks 0 & 2, while CKE1 drives ranks 1 & 3. The AMB (and host) can control the CKE for rank pairs.
DRAM Address	A[15:0] provided with A and B copies.	A15 is not required, as 4Gbit devices are not supported by this quad rank spec. They are reused as ECCA2 and ECCA6, which are separately controlled copies of A2 and A6 sent only to the ECC DRAMs. Normally they are exact copies of A2 and A6, but during MRS commands, can be controlled separately by the AMB via the DCALADDR register.

13.2 AMB Signal Changes and DRAM Connections (cont'd)

13.2.2 Address and Control Signal Reuse

The existing AMB address and control signals are re-used for quad rank by:

- Reassigning an address bit not required by 2Gbit and below DRAMs
- Providing only one copy of chip selects, rather than an "A" and "B" copy.
- Optionally providing only one copy of the CKE signals, rather than an "A" and "B" copy.

13.2.2.1 Reassigning Address Bits

An AMB provides A0 through A15, and BA0 through BA2 signals to the DRAMs, but lower density DRAMs do not require all of these address signals. Specifically, A15 is not used until 4Gbit DRAMs which are not likely to be available in DDR2, and are not supported by this quad rank spec.

13.2.2.2 One Copy of Chip Select and (optionally) CKE Signals

The AMB has two copies of all DDR interface address, command, and control signals, one for the DRAMs on the left side of the DIMM and one for the DRAMs on the right side of the DIMM. These are labeled "A" and "B" at the end of the signal names. Each signal is terminated to Vtt via a resistor at the physical end of the DIMM.

For quad rank x8 DIMMs, the chip select signals are routed to only 9 DRAMs each, allowing one chip select signal to drive both sides for each rank. A dual termination scheme is used, providing a termination resistor on each end of the DIMM. Quad rank x4 would route each chip select and to 18 DRAMs each.

Optionally, the CKE0A and CKE1A signals also drive both the left and right sides for quad rank, with a dual termination scheme.

13.2.2.3 ODT Requirements of Quad Rank

There are two options for the ODT signals for quad rank operation. Option 1 provides two additional ODT signals that are used for ranks 2 and 3. Option 2 uses only the two original ODT signals.

In both cases the ODT for the rank 0 and 1 DRAMs are identical for quad rank as for single and dual rank DIMMs with 2 physical copies provided (ODT0A and ODT0B) to minimize the loading and/or simplify the routing.

In option 1, ranks 2 and 3 are controlled by the two new ODT signals, ODT1 and ODT2 respectively. This scheme requires a total of 4 ODT pins.

The ODT functionality is programmable, and it will depend on particular DIMM implementation.

Note that the functionality of original ODTA/B signals for rank 0 and rank 1 is completely unchanged, including the register programming.

13.2.2.4 ECCA2 and ECCA6

The signal routing topology of the ECC DRAMs may require different strength of ODT on the ECC DRAMs from the data DRAMs. The ODT strength is programmed through MRS commands, which will program all DRAMs of a rank with the same value via the DRAM address bus. The ODT strength is programmed via EMRS1 bits A6 and A2.

To allow the ECC DRAMs to have their ODT strength programmed separately, the AMB creates a separate A2 and A6 for the ECC DRAMs. These signals normally follow the A2 and A6 functionality, but on all MRS cycles, AMB can send out separate values.

ECCA2 and ECCA6 are connected to all 4 rank's ECC bits. ECCA2 and ECCA6 are non-inverted outputs when address inversion is enabled.

13.2 AMB Signal Changes and DRAM Connections (cont'd)

13.2.3 Quad Rank Signal Mapping

The following table shows the mapping of the chip select, ODT, and CKE signals to each rank. The Signal name is the logical signal. The mapping to physical AMB balls is listed in a follow on table.

Table 52 — Quad Rank Signal mapping per rank, ODT Option 1

Signal	Rank0	Rank1	Rank2	Rank3
CS0#	CS			
CS1#		CS		
CS2#			CS	
CS3#				CS
ODTA		ODT		
ODTB	ODT			
ODT1			ODT	
ODT2				ODT
CKE0	CKE		CKE	
CKE1		CKE		CKE

Table 53 — Quad Rank Signal mapping per rank, ODT Option 2

Signal	Rank0	Rank1	Rank2	Rank3
CS0#	CS			
CS1#		CS		
CS2#			CS	
CS3#				CS
ODT0A/B[a]	ODT	ODT		
VSS			ODT	ODT
CKE0A/B[1]	CKE		CKE	
CKE1A/B[1]		CKE		CKE

NOTES:
a. For ODT Option 2, CKE and ODT A and B copies are routed to the left and right sides of the DIMM in the same manner as dual rank DIMMs

13.2 AMB Signal Changes and DRAM Connections (cont'd)

13.2.4 Mapping to AMB Balls

The following table shows the mapping between the existing AMB balls and the quad rank signals.

Table 54 — AMB Pin usage for each DIMM type

AMB Ball	Non-QR (SR or DR)	Quad Rank ODT Opt 1	Quad Rank ODT Opt 2	Quad Rank Comment
CS0#A	CS0#A	CS0#[a]	CS0#[1]	Rank 0
CS0#B	CS0#B	CS2#[1]	CS2#[1]	Rank 1
CS1#A	CS1#A	CS1#[1]	CS1#[1]	Rank 2
CS1#B	CS1#B	CS3#[1]	CS3#[1]	Rank 3
ODTA	ODTA	ODTA[b]	ODTA[2]	First ODT
ODTB	ODTB	ODTB[2]	ODTB[2]	Second ODT
A15A	A15A	ECCA2	ECCA2	A2 for the ECC DRAMs
A15B	A15B	ECCA6	ECCA6	A6 for the ECC DRAMs
CKE0A	CKE0A	CKE0	CKE0A	Ranks 0&2
CKE0B	CKE0B	ODT1	CKE0B	Optional third ODT, or CKE0B for Ranks 0&2
CKE1A	CKE1A	CKE1	CKE1A	Ranks 1&3
CKE1B	CKE1B	ODT2	CKE1B	Optional third ODT, or CKE1B for Ranks 1&3

NOTES:
a. There are no separate A & B copies for the CS# signals in Quad Rank
b. Logically identical

13.2.5 Signal State at Reset

CKE and ODT signals must be low during the DRAM power ramp. Since CKE signals are muxed with ODT signals, there is no power up difference. On a quad rank DIMM, the BIOS should set the register bit to configure the CKE0B & CKE1B signals to the ODT functionality (if applicable) prior to taking CKE high.

13.3 Rank Decode

FBD Quad Rank allows two addressing modes for the additional ranks. The AMB must implement both modes. The host may choose which mode to implement.

Mode C is specific to FBD and uses a bank or row address bit as the additional rank select bit. This mode allows for the full 8 DIMMs per channel. This mode appears to the host controller as a dual rank DIMM.

Mode A uses DS2 as the additional rank select bit. It limits the number of DIMMs per channel to 4 when quad rank is being used.

13.3 Rank Decode (cont'd)

13.3.1 Quad Rank Mode C

Quad rank mode C operates by making two physical ranks show up as one logical rank. A bank address bit as well as the existing RS bit determines which rank the AMB will access. The host controller will see the DIMM as dual rank, with each rank being one density higher than the physical DRAMs.

The host controller sends one Rank Select bit with the DRAM commands that are rank specific. This is called RS in the FBD spec, and will be called RS0 here. The AMB must create an RS1 bit internally to determine which of the 4 ranks to access. RS1 will be used to divide each logical rank into 2 physical ranks on the DIMM. Logical Rank 0 will be divided into physical ranks 0 and 2, while Logical Rank 1 will be divided into physical ranks 1 and 3.

Table 55 — RS1:0 to rank decode

RS1 (created inside the AMB from BA0)	RS0 (RS field in FBD commands)	Rank Accessed
0	0	0
0	1	1
1	0	2
1	1	3

In the AMB the BA0 bit from the host controller is used to create RS1. This places the even numbered banks in one physical rank, and the odd numbered banks in the other physical rank.

The AMB must recreate the BA0 signal to the DRAMs (called dBA0 here), which is done differently depending on the DRAM density.

Table 56 — dBA0 (DRAM BA0) Selection by DRAM density

DRAM Density	dBA0 (DRAM BA0) bit:
512Mbit	Host BA2
1Gbit	Host Row A14
2Gbit	Host Row A15

The following table shows the physical layout of each DRAM type, and how the host controller will view the DIMM.

Table 57 — DIMM addressing

Physical x8 DRAMs on DIMM					Host Controller View				
Rank	Density	Banks	Row Bits	Col Bits	Rank	Density	Banks	Row Bits	Col Bits
4	512Mbit	4	14	10	2	1Gbit	***8***	14	10
4	1Gbit	8	14	10	2	2Gbit	8	***15***	10
4	2Gbit*	8	15	10	2	4Gbit	8	***16***	10

* Some QR DIMMs may not support 2Gbit DRAMs

13.3 Rank Decode (cont'd)

13.3.1 Quad Rank Mode C (cont'd)

512Mbit QR DIMMs appear to the host controller logically as Dual Rank 1Gbit DIMMs. The difference between 512Mbit parts and 1Gbit parts is the addition of BA2 (Bank Address 2) for both row and column commands. The AMB will use BA2 in the FBD command as dBA0 to the DRAMs. Note that BA2 is sent on both row and column commands to the DRAMs so this is a simple mapping.

1Gbit QR DIMMs appear to the host controller logically as Dual Rank 2Gbit DIMMs. The difference between a 1Gbit part and 2Gbit parts is the addition of A14 for the Activate Command. The AMB will use Row address A14 in the FBD command as dBA0 to the DRAMs.

2Gbit QR DIMMs appear to the host controller logically as Dual Rank 4Gbit DIMMs. The difference between a 2Gbit part and 4Gbit parts is the addition of A15 for the Activate Command. The AMB will use Row address A15 in the FBD command as dBA0 to the DRAMs.

For 512Mbit parts, the dBA0 bit is created from BA2, which is sent for all commands which are rank specific, so this is a simple mapping. For 1Gbit and 2Gbit DRAMs, a Row Address is used to create the DRAM dBA0. This bit is ONLY sent during activate commands. This requires the AMB to remember the dBA0 bit from the last activate and use it for subsequent Read, Write, and Precharge Single commands. The DRAM's BA0 essentially becomes a row address in Quad Rank Mode C.

The AMB must store the dBA0 bit separately for each combination of BA2:0 and RS0 from the host controller. This is required because the host could have sent a different dBA0 for each possible open bank. This requires 16 dBA0s to be stored in the AMB, corresponding to the 16 banks that could be open at one time by the host controller. The dBA0 is stored when it is sent with the Activate Command, and used for any subsequent read, write, and precharge command to the same bank of the same logical rank.

On each activate, the AMB stores the value being sent on dBA0 in one of 16 locations selected by the host RS bit and BA[2:0] bits. This represents each different bank that the host controller could consider opened.

One each read, write, or precharge single command the AMB selects the proper stored value by using the RS bit and BA[2:0] bits send by the host in the read, write, or precharge command.

Table 58 — Activate Command mapping

Host (FBD channel) bit	512Mbit DRAM	1Gbit DRAM	2Gbit DRAM	All other modes
BA0	(RS1)	(RS1)	(RS1)	BA0
BA1	BA1	BA1	BA1	BA1
BA2	BA0	BA2	BA2	BA2
A[13:0]	A[13:0]	A[13:0]	A[13:0]	A[13:0]
A14	(A14)	BA0	A14	A14
A15	(not used)	(not used)	BA0	A15
RS	selects ranks	selects ranks	selects ranks	selects ranks

13.3 Rank Decode (cont'd)

13.3.1 Quad Rank Mode C (cont'd)

Table 59 — Read, Write & Precharge Single Command mapping

Host (FBD channel) bit	512Mbit DRAM	1Gbit DRAM	2Gbit DRAM	All other modes
BA0	(RS1)	(RS1)	(RS1)	BA0
BA1	BA1	BA1	BA1	BA1
BA2	BA0	BA2	BA2	BA2
A[13:0]	A[13:0]	A[13:0]	A[13:0]	A[13:0]
RS	selects ranks	selects ranks	selects ranks	selects ranks
Stored BA0 bit from the activate	(not used)	BA0	BA0	(not used)

Table 60 — Rank Selection and dBA0 generation for each command type

Command	Rank Decoding	DRAM BA0
Activate	Uses Host BA0	512Mbit: Host BA2 used 1Gbit: Host A14 used 2Gbit: Host A15 used
Read	Uses Host BA0	512Mbit: Host BA2 used For 1Gbit and 2Gbit parts this is a stored value from the last activate command to the same bank and rank. Which stored bit is determined by the host BA[2:0] & RS bits. Which stored bit is used is determined by the host BA[2:0] & RS bits
Write	Uses Host BA0	512Mbit: Host BA2 used For 1Gbit and 2Gbit parts this is a stored value from the last activate command to the same bank and rank. Which stored bit is used is determined by the host BA[2:0] & RS bits.
Precharge Single	Uses Host BA0	512Mbit: Host BA2 used For 1Gbit and 2Gbit parts this is a stored value from the last activate command to the same bank and rank. Which stored bit is used is determined by the host BA[2:0] & RS bits.
Auto Refresh	Command is sent to two ranks. RS bit determines whether it is sent to Ranks 0 & 2 or Ranks 1 & 3.	N/A
Precharge All	Command is sent to two ranks. RS bit determines whether it is sent to Ranks 0 & 2 or Ranks 1 & 3.	N/A

Table 60 — Rank Selection and dBA0 generation for each command type

Command	Rank Decoding	DRAM BA0
Enter Self Refresh	Command is sent to two ranks. RS bit determines whether it is sent to Ranks 0 & 2 or Ranks 1 & 3.	N/A
Exit Self Refresh / power down	Command is sent to two ranks. RS bit determines whether it is sent to Ranks 0 & 2 or Ranks 1 & 3. Note that this command only involves the CKE signals which are physically shared by Ranks 0 & 2, and by Ranks 1 & 3.	N/A
Enter Power Down	Command is sent to two ranks. RS bit determines whether it is sent to Ranks 0 and 2 or Ranks 1 and 3. Note that this command only involves the CKE signals which are physically shared by Ranks 0 & 2, and by Ranks 1 & 3	N/A
CKE per DIMM	Sent to all ranks on the DIMM	N/A
CKE per rank	Command is sent to two ranks. The appropriate RS bit determines whether it is sent to Ranks 0 and 2 or Ranks 1 and 3. Note that this command only involves the CKE signals which are physically shared by Ranks 0 & 2, and by Ranks 1 & 3.	N/A

13.3.1.1 Host responsibilities for read timing

The host controller is responsible for assuring that there is a turnaround cycle between reads to the same DIMM but different ranks. This includes switching between physical ranks that appear as one logical rank in the Mode C addressing mode.

13.3.2 FBD2 Mode A Rank Decode

Mode A uses DS2 (DIMM Select 2) as the additional rank decode. This limits the total number of DIMMs to 4 per channel, as decoded by DS[1:0]. For Mode A, the host controller knows about the 4 individual ranks, and addresses them directly.

The decode for DS[2:0] within the AMB normally comes from the strapping signals SA[2:0], which provides the physical DIMM number, setting the address for the SPD and AMB. This DIMM number is compared to the DS[2:0] in the command frames. In Quad Rank Mode A, a quad rank DIMM decode ignores the DS2 bit, using it as Rank Select 1. By the same token, in Quad Rank Mode A, a quad rank DIMM decode will also ignore the WS2 bit which was used by the AMB on the DIMM to determine if it should write the Wdata into its write FIFO. Single and dual rank DIMMs will continue to decode DS2 as a DIMM select bit.

Table 61 — Quad Rank Mode A DS[2:0] and RS mapping

DIMM Type	DS2 (RS1)	DS1	DS0	RS
Quad Rank DIMM	Rank Select 1	DIMM Decode	DIMM Decode	Rank Select 0
Dual Rank DIMM	DIMM Decode	DIMM Decode	DIMM Decode	Rank Select
Single Rank DIMM	DIMM Decode	DIMM Decode	DIMM Decode	Not Used

13.3 Rank Decode (cont'd)

13.3.2 FBD2 Mode A Rank Decode (cont'd)

In Mode A, the AMB need not store the rank information for each bank, since the rank select is sent with all DRAM commands for all densities.

Operations other than DRAM commands operate in the same manner as a single or dual rank DIMM.

A quad rank DIMM responds to configuration read and write cycles at its selected DIMM number, decoding DS[2:0]. It does not respond to configuration read and write cycles at the alternate address with DS2=1.

A quad rank DIMM sends status frames providing data only on the lane selected by SA[2:0]. It does NOT repeat the status information on the additional lane selected when DS2=1.

The following example is for a quad rank DIMM with the strapping of SA[2:0] = 001 (DIMM 1).

Table 62 — AMB response to commands

Command	**AMB response, when SA[2:0]=001**
Activate Write Read Precharge All Precharge Single Auto Refresh	Responds to DS[2:0]=001 (Ranks 0 and 1) Responds to DS[2:0]=101 (Ranks 2 and 3) Commands are sent to a single rank.
Enter Self Refresh Exit Self Refresh/Exit Power Down Enter Power Down	Responds to DS2:0]=x01 Since CKE is shared between ranks 0&2 and ranks 1&3, these commands target 2 ranks at a time, based on the RS bit. RS=0 targets command to ranks 0 & 2. RS=1 targets command to ranks 1 & 3.
Channel commands Config read and write CKE per DIMM CKE per Rank	Responds to DS[2:0]=001 only
Status Packet	Drives data onto logical lane 1 only

13.4 ODT timing on reads

The read timing for ODT is basically the same as the write timing. The ODT is enabled for the DQS preamble, and remains active for 3.5 clocks for BL=4 and 5.5 clocks for BL=8. The equation for the DRAM ODT signals is:

Turn on: RL - 3 clocks from the read command

Turn off: RL - 2 + (BL/2) clocks from the read command

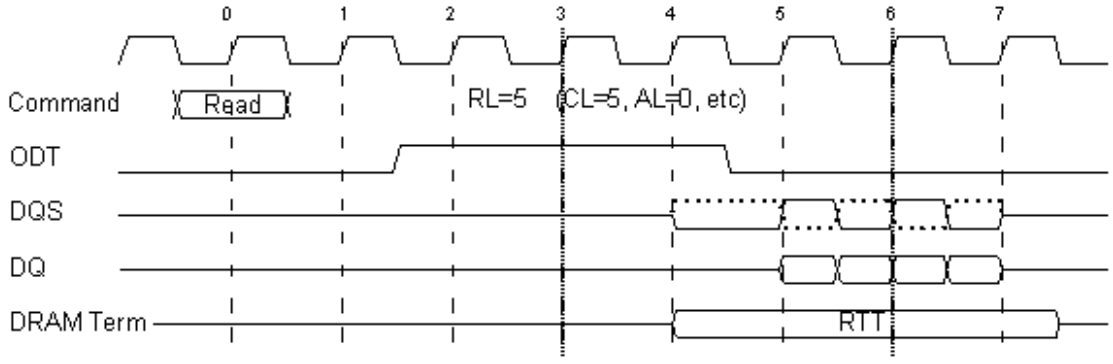

Figure 26 — DRAM ODT TIming during Reads

13.4.1 AMB data bus termination

The AMB data bus termination remains at 65 ohms nominal.

13.5 Registers

DDR2ODTC: DDR2 DRAM On-Die Termination Control

NOTE This is an existing register, in which previously only 8 bits were used. In reality, since the AMB only has one ODT pin set for ranks 0 and rank 1, only 4 of the 8 bits have any function. These original 8 bits are not changed.

For the quad rank option using 4 ODT signals, 8 more bits are added for control of the ODT1 and ODT2 signals for reads. There is one bit for each rank reads.

Device: NodeID **Function: 4** **Offset: FCh**			
Bit	**Attr**	**Default**	**Description**
15	RWST	0	ODT2 control during reads from CS3
14	RWST	0	ODT1 control during reads from CS3
13	RWST	0	ODT2 control during reads from CS2
12	RWST	0	ODT1 control during reads from CS2
11	RWST	0	ODT2 control during reads from CS1
10	RWST	0	ODT1 control during reads from CS1
9	RWST	0	ODT2 control during reads from CS0
8	RWST	0	ODT1 control during reads from CS0 1: ODT pin will drive high 0: ODT pin will drive low
Note that bits 7:0 below do not change from the current spec			
7:6	RWST	0h	R1ODTWR: ODT control during writes to CS1 & CS3 x1: ODT0A/B, ODT1, & ODT2 pins will drive high x0: ODT0A/B, ODT1, & ODT2 pins will drive low Note: Must always be set to 01 for SR and DR DIMMs
5:4	RWST	0h	R1ODTRD: ODT0 control during reads to CS1 & CS3 x1: ODT0A/B pins will drive high x0: ODT0A/B pins will drive low Note: Must always be set to 00
3:2	RWST	0h	R0ODTWR: ODT control during writes to CS0 & CS2 x1: ODT0A/B, ODT1, & ODT2 pins will drive high x0: ODT0A/B, ODT1, & ODT2 pins will drive low Note: Must always be set to 01 for SR and DR DIMMs
1:0	RWST	0h	R0ODTRD: ODT0 control during reads to CS0 & CS2 x1: ODT0A/B pins will drive high x0: ODT0A/B pins will drive low Note: Must always be set to 00

13.5 Registers (cont'd)

Quad Rank control register

Device: NodeID Function: 3 Offset: 88h			
Bit	**Attr**	**Default**	**Description**
5	RWST	0	A15A and A15B pin muxing 0 = A15A and A15B functionality 1 = ECCA2 and ECCA6 functionality. Only permitted when the Quad Rank Enable bit is set to a 1.
4	RWST	0	CKE0B and CKE1B pin muxing 0 = CKE0B and CKE1B functionality 1 = ODT1 and ODT2 functionality. Only permitted when the Quad Rank Enable bit is set to a 1.
3:2	RWST	00	RS1 Select. This field determines what the AMB uses for the dBA0 (DRAM BA0) 00 = BA2 used for dBA0 01 = Row Address 14 used for dBA0 10 = Row Address 15 used for dBA0 11 = DS2 (Quad Rank Mode A)
1			Reserved
0	RWST	0	Quad Rank Enable 0 = normal single or dual rank operation 1 = Quad Rank DIMM

DCALCSR

Bits 23 and 24 added to support the additional ranks.

Device: NodeID Function: 4 Offset: 40h			
Bit	**Attr**	**Default**	**Description**
24:21	RW	0000	This field corresponds to the chip select outputs: CS[3:0]. Setting a bit in this field will cause the corresponding CS pin to drive low when commands are issued on the DDR bus. This field Applies to NOP, Refresh, Precharge all, and MRS/ EMRS commands. Bit 21 is for CS0, Bit 22 if for CS1, Bit 23 is for CS2, and bit 24 is for CS3.

13.5 Registers (cont'd)

DCALADDR: DCAL Address Register

Bits 5:4 are added to XOR with ECCA2 and ECCA6

Device: NodeID **Function: 4** **Offset: 44h**	
Bit	**Description**
31:16	DRAM Address Bus 15:0
15:6	Reserved
5	XOR for ECCA6. This bit is set to a 1 to have the ECC A6 bit the opposite of A6. Only used if quad rank and A15A/B pin muxing enabled (function 3 offset 0x88 bits 0 and 5), otherwise ignored.
4	XOR for ECCA2. This bit is set to a 1 to have the ECC A2 bit the opposite of A2. Only used if quad rank and A15A/B pin muxing enabled (function 3 offset 0x88 bits 0 and 5), otherwise ignored.
3	Reserved
2:0	DRAM Bank Address bus 2:0

Shaded rows are unchanged.

A6/A2 and ECCA6/ECCA2 functionality of DCALADDR if Quad rank mode and A15A/B pin muxing enabled (function 3 offset 0x88 bits 0 and 5).

Signal	**DCALADDR bits**
A6A, A6B	Bit 22 (existing definition)
ECCA6	Bit 22 XOR Bit 5
A2A, A2B	Bit 18 (existing definition)
ECCA2	Bit 18 XOR Bit 4

MEMBIST register change

13.5 Registers (cont'd)

Only the two bits within the register that change are shown. Changes are shown in bold.

Device: NodeID **Function: 3** **Offset: 40h**			
Bit	**Attr**	**Default**	**Description**
21:20	RW	00	CS: CS[3:0] selection in MemBIST mode 01: Select Rank 0 10: Select Rank 1 00: Select Rank 2 11: Select Rank 3

NOTE The encoding of this register is based on the existing definition.

13.6 Fast Reset

During a fast reset, the AMB performs a set of operations to close all pages and put the DRAMs into self refresh. The AMB will access two ranks in parallel for all commands during this time.

NOTE For QRx8 this will be activating the same number of DRAMs at a time as is already done for DRx4 DIMMs.

For Quad Rank FB-DIMM MEMBIST and Transparent Mode support, please refer to JESD82-28A "Fully Buffered DIMM Design for Test, Design for Validation (DFx)".


JEDEC