Google Inc. v. Netlist, Inc.
Doc. 158 Att. 3

Exhibit L

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Minutes of Meeting No. 15
JC-45 Module Committee

June 6-7, 2007 — **Seattle, WA**

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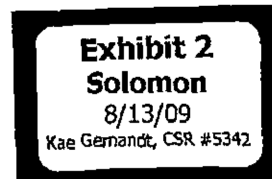
Exhibit 2
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1.0 Introduction

The JC-45 Plenary meeting opened at 10:18 AM on June 6, 2007. Mr. Quddus led the discussion of this group.

Self-introductions were completed by the attendees.

The meeting introduction was read.

1.1.0 Patent Policy

The patent policy was reviewed.

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1.2.0 Minutes

The minutes for the March 2007 meeting were reviewed and approved, with the modifications shown below, on a motion from Samsung and seconded by Netlist.

Add approval to ballot 72 SO DIMM bit extensions to SPD (Item #2161.00, section 2.4.4.0 of March '07 minutes). The addition to the minutes was requested by US Modular.

The motion passed by acclamation.

1.3.0 Meeting Rotation

Mr. Quddus announced that the meeting rotation for JC-45 would be as follows: 45.2, 45.3, 45.4, 45.5 then 45.1. *(Note: the minutes record the sub-committees in normal sequence.)*

1.4.0 Agenda

The agenda was reviewed and updated.

1.5.0 Awards

Chairman's Awards were given to Takao Ono (Elpida), David Chan (Qimonda) and Joseph Tsang (Intel). Their contributions to recent standardization efforts were acknowledged recognized by applause by the committee.

1.6.0 Elections

Mr. Quddus indicated that the JC-45.2 (UDIMM) vice-chair has resigned, and requested nominations for this position from the floor:
Nominations included:
- Yongshin Kim

Nominations were closed due to no further nominations.
Mr. Kim was elected by acclamation.

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response.

The motion passed with a vote count of 3 opposed and 6 in favor.

1.9.2.0 #2065.17 HP Total Module Power in DDR3 SPD

HP proposed the addition of two SPD bytes to the DDR3 SPD spec, to indicate DIMM power utilization:
1st byte: Minimum power utilization (idle condition)
2nd byte: Maximum power (max/worst case conditions)

An example was shown. HP indicated that two bytes may or may not be enough – prefer to have the TG consider the topic.

Discussion:
- Concerns were raised in earlier discussions – may wish to consider delta power, etc.

1.9.3.0 #2151.01 Tyco Folded Fin Heat Sink Comparison Study for DIMM Applications

Tyco made an informational showing the committee.

The presentation is intended to provide an introduction to folded fin technology, in addition to thermal studies and attachment methods.

A folded fin heat sink is a corrugated pattern of metal - example tooling was shown. A variety of folded fin heat sinks were shown as well as the folding design parameters, compressed/uncompressed versions, radial folded versions, etc.

The thermal study objectives and conditions were shown, including various (air) bypass versions and other boundary cases. Model parameters were shown for each case studied, as well as the wind tunnel environment. A mix of calculated and measured results was shown, showing the temperature rise as compared to the incoming air. Images were also shown for some heat sink configurations showing air velocity in and around the subject heat sinks.

Attachment methods were summarized, including clips and 2-sided tape. Tape thermal resistance was covered.

Work that still needs to be done was summarized, including shock and

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vibration testing.

Discussion:
- In response to a request from the secretary, the Tyco representative indicated no known IP with the material shown.

1.9.4.0 #2003.11 Intel FBDIMM1 Quad Rank SPD

Intel proposed a series of changes to accommodate quad rank FB DIMMs. The affected bytes were summarized, with changes identified on a per SPD byte basis. Bytes affected included 7 (changed), 75 – 78 (new bytes).

Intel indicated that this is a first showing of material, for consideration by the committee.

1.9.5.0 #2065.18 US Modular DDR3 SPD Register Mfg ID

US Modular indicated that a request was made in March to add a register manufacturer field in the DDR3 SPD. At this point, the manufacturer ID is optional in DDR3 SPD.

The showing summarized what the proposed SPD information might look like, based on the DRAM ID field, which includes two bytes for inclusion in Registered DIMM SPDs.

Discussion:
- May also need a DIMM manufacturer ID.
- Why use bytes 63 and 64? Response: Location is not important, concept is.
- Allows modules to be easily sorted when problems exist with register devices (mfg test, field, etc).
- Feel that the register specification should ensure functionality – this should not be needed.

Motion by US Modular and seconded by Sun to elevate the material to a second showing.
The motion failed with at least one company opposed.

The topic will be discussed in the SPD TG.

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1.9.6.0 #2075.03 Intel DDR3 SPD Thermal Bytes

Intel proposed a series of three SPD bytes to accommodate the possible use of a thermal sensor, including:
- Is a thermal sensor installed
- Accuracy of sensor
- Heat spreader details (if installed)
- SDRAM device type

The SPD TG chairman indicated that this material should be considered as a second showing based on an earlier showing on similar material.

Motion by Intel and seconded by US Modular to empower the SPD TG to issue one or more bytes on this material
The motion passed by acclamation.

2.0 JC45.1 Registered DIMMs

The meeting opened at 9:30 AM on June 7, 2007. Mr. Kiehl led the discussions of this group.

2.1.0 Agenda

The agenda was reviewed and updated.

2.2.0 BoD Ballot Review

The following BoD ballots were previously returned to the committee due to unresolved IP concerns:
- JCB-06-72 (#2119.01)
- JCB-06-73 (#2119.02)
- JCB-06-70 (#2129.01)

No action taken on the above items at the outset of the meeting.

The committee returned to the above items upon completion of the successful motion on related committee ballot JC-45.1-07-154 (item #2119.03):

Motion by Staktek and seconded US Modular to move item #2119.01 (JCB-

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5.5.0 First Presentations

5.5.1.0 #2171.01 Qimonda 4R x 8 FBDIMM (1Gb)

The maximum DRAM outline supported by the design is 9 mm wide x 13 mm high. The planned design schedule was shown, which lagged the 512Mb design. Several layer plots were shown. This card is not based on an existing design – it is a new design.

5.5.2.0 #2171.02 Qimonda 4R x 4 FBDIMM Stack

The design supports 36 stacked dual die devices. The maximum DRAM outline is 13 mm high x 9.1 mm wide. The card has 10 layers, with a stack-up identical to R/C V (2Rx4). Blind via usage was summarized. The high speed routing is fundamentally identical to R/C V – so no simulation of the high speed bus should be needed. The design schedule was also shown.

The addressing, command, control and DQ wiring was summarized. The component placements were shown, in addition to the net topologies and the routing layers.

Discussion:
- Clarification questions were covered on the material shown.
- Three raw cards were shown – Is Qimonda willing to allow other companies to sponsor any of the designs? Response: Can discuss in TG.
- The DRAM size is quite small – are many DRAM devices expected, in the industry, that will meet this size (especially when stacked)?
- In response to a question, Qimonda indicated no knowledge of IP associated with the designs.

5.5.3.0 #2171.03 Qimonda 4R x 8 FBDIMM (512 Mb)

The design is a 10 layer design, with a stack-up the same as R/C H. The maximum DRAM outline is 11 mm wide x 10.5 mm high. The design uses blind vias and micro vias.

Focus has been placed on power delivery, especially for the AMB – key elements of the design were summarized.

The design schedule was shown, with Rev 0.5 planned for August '07.
A layout was shown, with rank distributions identified. The net topologies were also shown, as well as the layer plots. Simulation plots were included, but not shown. The VCC resistance was shown, which is very close to the

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existing specification.

5.5.4.0 #103.46 Intel AMB Quad Rank Support

An FYI showing was made using a JC-40 item number.

Currently the AMB does not support 4 rank DIMMs; however 4 rank DIMMs are now being requested. With existing experience, it has been determined that 4 rank DIMMs are possible, given some changes to the AMB.

The proposed changes will not affect existing systems – e.g. in regard to the architecture and protocol. The AMB pkg and pinout will also not change. The objective is to "trick" the host into thinking that the DIMM is a 2-rank DIMM, using 2X device densities.

An extensive presentation was made, covering the fundamentals associated with the proposal. The quad rank signal requirements were summarized - with CS, ODT, Address and CKE signals and/or functions being affected.

Tables were shown indicating the mapping of CS, ODT, CKE signals, with two ODT-based options shown. Newly assigned (re-assigned) signals (e.g. ODT1 and ODT2) were identified.

The means by which the different ranks were selected, using existing signals, was summarized. The additional address for each DRAM density increment was summarized, in conjunction with the means for providing that address.

Intel noted that by enabling the use of Quad Rank DIMMs, the total number of DIMMs on a channel would be reduced (e.g. from 8 FB DIMMs to 4 FB DIMMs max). The AMB control register implications/changes were also summarized.

Discussion:
- In response to a question by the secretary, Mr. Tsang (Intel) indicated that IP filings are likely and he will pursue this information. He further indicated that he felt that Intel would likely be willing to meet the JEDEC RAND terms for any such IP.

6.0 JC45.5 Module Interconnect

The meeting opened at 8:55 AM on June 7, 2007. Mr. McGrath led the

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discussions of this group.

6.1.0 Agenda

No agenda was shown.

6.2.0 BoD Ballot Review

There were no BoD ballots for review in this sub-committee.

6.3.0 Ballot Review

There were no ballots for review in this sub committee.

6.4.0 Second Presentations

There were no second presentations for this sub-committee.

6.5.0 First Presentations

6.5.1.0 #2170.00 Intel Proposed Connector Specification for Outlines of Solid State and Related Components.

The connector outline was shown – the committee needs to develop accurate modeling parameters and techniques. A table of proposed connector S-parameter requirements were shown, including insertion loss, return loss, far end crosstalk and near-end cross-talk. Proposed "pass' criteria was shown, in addition to proposed measurement procedures.

An example of a frequency domain measurement was shown using a test board. Appendix A covered the proposed equipment, test fixtures and samples, etc.

Discussion:
- JC-45.5 is working with the Link Signaling TG (JC-16) to do channel modeling using the results of this TG.

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