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FBDIMM:
Architecture and Protocol

JESD206

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(From JEDEC Board Ballot, JCB-06-49, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Document Organization

The next four chapters of the FBD Channel Specification cover Channel Overview (Chapter 2), Initialization (Chapter 3), Channel Protocol (Chapter 4) and Reliability, Availability, and Serviceability (RAS) (Chapter 5).

1.1 List of Terms and Abbreviations

This document uses the following terms and abbreviations:

Note that the terms chipset and memory controller are used interchangeably throughout the rest of this document. The term *motherboard is used as a generic term* to describe the PCB onto which the memory controller is mounted. Actual implementations could have distributed memory controllers mounted on separate memory boards.

Table 1-1 — Terms and Definitions

TERM	Definition
AMB	Advanced Memory Buffer
Chip disable	An ECC encoding specifically tailored for memory such that the data from any defective memory device can be reconstructed from some aggregate of surviving memory devices. Corrects data from failed device.
Bit Lane	A differential pair of signals in one direction.
D+ and D-	The D+ and D- terms used in this document are used to indicate the two conductors or signals of a differential signaling pair.
DDR	Double Data Rate (SDRAM)
DDR Branch	The minimum aggregation of DDR channels which operate in lock-step to support error correction. Two channels per branch supports x8 chip disable ECC. A rank spans a branch.
DDR Channel	A DDR channel consists of a data channel with 72 bits of data and an addr/cntrl channel
DDR Data channel	A DDR data channel consists of 72 bits of data, divided into 18 data groups
DDR Data group	Each data group consists of 4 data signals and a differential strobe pair
DIMM	Dual In-Line Memory Module. A packaging arrangement of memory devices on a socketable substrate.
DIMM Slot	Receptacle (socket) for a DIMM. Also, the relative physical location of a specific DIMM on a DDR Channel.
DIMM Stack	Dual-ranked x4 DRAM DIMM physical topology: refers to two physical rows of DRAM "stacked" one above another
DRAM Page (Row)	The DRAM cells selected by the Row Address
DPM	Defects per million
DRAM	Dynamic Random Access Memory
ECC	Error Correction Code.
EMI	Electro-magnetic interference
FBD	Fully Buffered DIMM

Table 1-1 — Terms and Definitions (Cont'd)

TERM	Definition
Frame	Group of bits containing commands or data
HCSL	High-speed Current Steering Logic
Host	Memory controller agent on an FBD channel
ISI	Inter Symbol Interference
JEDEC	JEDEC Solid State Technology Association (once known as the Joint Electron Device Engineering Council)
JESD79	JEDEC Standard 79, DDR SDRAM Specification
Link	A dual-simplex communications path between two components. The collection of two Ports and their interconnecting bit lanes.
Mesochronous	Same frequency with unknown (but fixed) phase relation.
NB	Northbound
Northbound	The direction of signals running from the farthest DIMM toward the host.
Page Replace a.k.a. Page Miss, Row Hit / Page Miss	An access to a row that has another page open. The page must be transferred back from the sense amps to the array, and the bank must be pre-charged.
Page Hit	An access to an open page, or DRAM row. The data can be supplied from the sense amps at low latency.
Page Miss (Empty Page)	An access to a page that is not buffered in sense amps and must be fetched from DRAM array.
PLL	Phase Locked Loop
Port	In physical terms, a group of transmitters and receivers physically located on the same chip that define one end of a Link.
PTH	Plated Through-Hole
PVT	Process, Voltage and Temperature
Rank	A DIMM is organized as one or two physical sets of memory, called ranks. Note that single rank or dual rank is different from single-sided or double-sided, e.g. a single rank DIMM build from x4 DRAM devices is actually double-sided. It is also common practice to distribute the 9 devices of an x8 DIMM between both sides of the DIMM to enhance the thermal performance of the module.
Resample	A resampler repeater is a serial data in and serial data out node that attenuates jitter by re-generating the serial data using a clock recovered from the incoming data stream derived from a common reference clock. It also resets the voltage budget of the re-transmitted data.
Resync	A resync repeater is a serial data in and serial data out node that re-synchronizes data to a local clock after it has been sampled with a recovered clock derived from a common reference clock. The local clock is also generated from the same reference clock by a PLL multiplier. A drift compensation buffer is inserted between the two clock domains which absorbs the maximum link delay change over worst case voltage and temperature changes. Both the jitter and voltage budgets for the re-transmitted data are reset.
RPD	Return Path Discontinuity
SB	Southbound
SDRAM	Synchronous Dynamic Random Access Memory
SI	Signal Integrity
Serial Present Detect (aka SMBus protocol)	A 2-signal serial bus used to read and write control registers in the AMB and SDRAM

Table 1-1 — Terms and Definitions (Cont'd)

TERM	Definition
SMBus	System Management Bus. Mastered by a system management controller to read and write configuration registers. Limited to 100KHz.
Southbound	The direction of signals running from the host controller toward the DIMMs.
SSC	Spread Spectrum Clocking. Utilized to lower EMI
SSO	Simultaneously Switching Outputs
SSTL_18	Series Stub Terminated Logic for 1.8V
Throttled	Temporarily prohibiting memory accesses when a thermal or electrical limit has been reached.
Unit Interval	Average time interval between voltage transitions of a signal
Vss	Ground (0V)
Vddq	I/O buffer voltage for DDR-II buffers. Nominally 1.8V

1.2 Revision History

This document has been released in the following revisions:

Table 1-2 — Revision History

Version	Date	Changes
0.0	12/3/2003	Original revision
0.1	2/13/2004	Revision of all chapters to incorporate feedback
0.1a	5/3/2004	Added JEDEC Ballot Comments 2.1.3: added detail to SMBus addressing 3. Increased calibration time 3.1.2: added detail on determining clock train violaiton 3.3.3: Tx termination to remain on in disable state 3.3.3: Clarified disable state actions by reording table 3-8 3.3.4 & 3.3.5: Command to data fraction delay added in. 3.3.5 & 3.3.7: AMB with Last_AMB flag set loops back data 3.3.6: specified host operation in sending TS2 patterns 3.3.6: Clarified Mege_Disable bit funtionality 3.3.9.1: De-Emphasis disabled during calibrate 4.2.5 Table 4-41: corrected ERC and EL0s duration
	3/16/2005	Added Editorial changes from September 2004 JEDEC meeting Added Ballot changes from March 2005 JEDEC meeting

1.3 Related Documents

Table 1-3 — Related Documents

Document	Revision	Description
FBD Connector Specification	Na	Connector physical parameters: pinout, footprint, mechanical drawing, and requirements
FBD Signaling Specification		PTP link parameters: signaling, I/O, and AC and DC parameters
FBD AMB Specification	Na	AMB Characteristics: pinout, package type, mechanical outline, footprint, AC/DC specs, power/thermal requirements, buffer TPT, special feature requirements (e.g. thermal sensor), & basics DFT
FBD DIMM Specification	Na	FBD DIMM module parameters: multiple raw card designs, block diagrams, net topologies, routing details, timing budget, pin out, mech. Outline, stack up, and SPD requirements
SMBus	2.0	System Management Bus Specification http://smbus.org/specs/smbus20.pdf
DDRII JEDEC Spec		JEDEC DDR II SDRAM Data Sheet JC-42.3

2 Fully Buffered DIMM Overview

Higher CPU speeds are driving the need for higher memory bandwidth. Looking beyond DDR2-533, the existing "stub bus" architecture becomes unworkable. The number of DRAM devices per channel has been trending toward fewer devices per channel. This reduction in capacity reduces performance. Platform cost restrictions limit DRAM pin count increases, routing restrictions limits adding channels to maintain capacity, and differing DRAM interfaces require unique motherboard developments and products.

Fully Buffered DIMM (FBD) addresses these requirements by providing a high-bandwidth, large capacity channel solution that has a narrow host interface. Fully Buffered DIMMs use commodity DRAMs isolated from the channel behind a buffer on the DIMM that creates a pay-as-you-go cost structure. Memory device capacity remains high and total memory capacity scales with DRAM bit density.

This chapter describes the FBD Channel topology, physical signaling, clocking and data flow.

2.1 Memory Channel

The FBD channel provides a communication path from a host controller to an array of DRAM devices. The DRAM devices are buffered behind one or more Advanced Memory Buffer (AMB) devices. The physical isolation of the DRAM devices from the channel enables the flexibility to enhance the communication path to significantly increase the reliability and availability of the memory subsystem.

2.1.1 Link Widths

Figure 2-1 shows a logical diagram of the FBD channel's southbound and northbound data paths. The channel interconnect actually consists of two unidirectional links: one in the southbound direction and the other in the northbound direction. The southbound data path running from the host to the DIMMs is 10 logical signals wide, and the northbound data path running from the DIMMs back to the host is 14, 13, or 12 logical signals wide. The width of the northbound link is application dependent. The host may support the link width or widths needed to provide the appropriate error detection coverage needed for the intended application. An AMB device on a non-ECC DIMM must support the 12 logical signal width. An AMB device on an ECC DIMM must support the 13 and 14 bit widths.

The southbound link may be operated in fail-over mode to map out a bad bit lane if supported by the host. The 14 or 13 bit width northbound link may be operated in fail-over mode to map out a bad bit lane if supported by the host. An AMB is required to support fail-over on the southbound link, and is required to support fail-over on the northbound link if ECC mode is supported (14 and 13 bit widths).

Other Restrictions

Only one outstanding configuration read or write register transaction is allowed on the channel. A configuration register read begins with the command and ends with the data being returned to the host. A configuration write begins with the command and ends when the read data would have been returned if the command were a Read Config Reg. This is the same point that an Alert Frame would be generated if there were a CRC error on the Write Config Reg command. Allowing only one outstanding configuration transaction on the bus allows for proper replay of the Write Config Reg command following an Alert Frame.

A Soft Channel Reset requires NOP commands in all other command slots in the previous DRAM clock, the current DRAM clock, and the next 4 DRAM clocks.

Only one In-band Debug event may be sent within a DRAM clock.

The host controller is responsible for state and timing of the CKE pins vs. DRAM commands based on the DRAM specifications. A DRAM command and CKE command may target the same DIMM on the same DRAM clock provided that the DRAM specifications are met.

Examples:

A DRAM command may be issued to rank 1 on the same DRAM clock as a DRAM CKE per Rank command that changes the CKE of rank 0 while retaining a 1 on the CKE of rank 1.

A DRAM command may be issued to DIMM 2 on the same DRAM clock as a DRAM CKE Command per DIMM that targets all DIMMs, but retains the state the CKEs of DIMM 2 as 1.

4.2.3 Command Encoding

Commands are encoded into the 24 bit C[23:0] fields of Command frames. Table 4-39 defines the bit mapping of an example DRAM configuration and the channel commands into the C[23:0] field.

Table 4-39 — Command Encoding

DRAM Cmnds	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Activate	DS2	DS1	DS0	1	DRAM Addr		RS	DRAM Bank & Address																
Write	DS2	DS1	DS0	0	1	1	RS	DRAM Bank & Address																
Read	DS2	DS1	DS0	0	1	0	RS	DRAM Bank & Address																
Precharge All	DS2	DS1	DS0	0	0	1	RS	X	X	X	X	1	1	1	X	X	X	X	X	X	X	X	X	X
Precharge Single	DS2	DS1	DS0	0	0	1	RS	DRAM Bank				1	1	0	X	X	X	X	X	X	X	X	X	X
Auto (CBR) Refresh	DS2	DS1	DS0	0	0	1	RS	X	X	X	X	1	0	1	X	X	X	X	X	X	X	X	X	X
Enter Self Refresh	DS2	DS1	DS0	0	0	1	RS	X	X	X	X	1	0	0	X	X	X	X	X	X	X	X	X	X
Exit Self Refresh / Exit Power Down	DS2	DS1	DS0	0	0	1	RS	X	X	X	X	0	1	1	X	X	X	X	X	X	X	X	X	X
Enter Power Down	DS2	DS1	DS0	0	0	1	RS	X	X	X	X	0	1	0	X	X	X	X	X	X	X	X	X	X
reserved	X	X	X	0	0	1	X	X	X	X	X	0	0	X	X	X	X	X	X	X	X	X	X	X

Note: The values in "X" fields in non-reserved commands above may be driven onto the DRAM device pins.

Channel Cmnds							OP3	OP2	OP1	OP0														
Debug: In-band Events	EV7	EV6	EV5	0	0	0	1	1	1	1	1	EV4	EV3	EV2	EV1	EV0	PV7	PV6	PV5	PV4	PV3	PV2	PV1	PV0
Debug: Relative Timing	PH5	PH4	PH3	0	0	0	1	1	1	1	0	PH2	PH1	PH0	RT9	RT8	RT7	RT6	RT5	RT4	RT3	RT2	RT1	RT0
Debug: Exposed Info	EX18	EX15	EX14	0	0	0	1	1	1	0	EX13	EX12	EX11	EX10	EX9	EX8	EX7	EX6	EX5	EX4	EX3	EX2	EX1	EX0
reserved	X	X	X	0	0	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
reserved	X	X	X	0	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
DRAM CKE per DIMM	DS2	DS1	DS0	0	0	0	0	1	1	1	BCST	X	X	X	X	X	DE7	DE6	DE5	DE4	DE3	DE2	DE1	DE0
DRAM CKE per Rank	DS2	DS1	DS0	0	0	0	0	1	1	0	BCST	X	X	X	X	X	D3 R1	D3 R0	D2 R1	D2 R0	D1 R1	D1 R0	D0 R1	D0 R0
Write Config Reg	DS2	DS1	DS0	0	0	0	0	1	0	1	DS3	TID	X	A10	A9	A8	A7	A6	A5	A4	A3	A2	0	0
Read Config Reg	DS2	DS1	DS0	0	0	0	0	1	0	0	DS3	X	X	A10	A9	A8	A7	A6	A5	A4	A3	A2	0	0
reserved	X	X	X	0	0	0	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Soft Channel Reset	X	X	X	0	0	0	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Sync	X	X	X	0	0	0	0	0	0	1	X	SD1	SD0	X	X	X	X	IER	ERC	ELOs	X	X	R1	R0
Channel NOP	X	X	X	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Note: All unused encodings are reserved. "X" values should be driven by the host to zero and ignored by the AMB.

4.2.4 DRAM Commands

DRAM commands are generated by the host to access the DRAM devices behind each AMB buffer. The host has access to the DRAM devices as if the devices were directly connected to the host. The DS[2:0] field directs the command to one of the eight possible DRAM DIMMs on the FBD channel. The AMB decodes the DRAM commands and generates the control signals to the DRAM devices. The command delivery on the DRAM address and control signals (excluding CKE) use 1n command timing. 1n command timing means that the commands are present on the DRAM pins for a single clock cycle. The exact mapping of the control signals delivered to the DRAM devices are defined in the *FBD AMB Specification.*

AMB buffers may support more than one DRAM technology. The details of the mapping of bank and address bits from the commands to the DRAM devices are specified in the *FBD AMB Specification.* An example mapping is shown in Table 4-40. For complete details of the DRAM command encoding refer to the JEDEC SDRAM data sheets.

In the following table, the RS (Rank Select) bit specifies to the AMB which memory ranks located behind the buffer should be accessed. The other labels correspond to the familiar labels in the SDRAM data sheets. Rows labeled with an "*" are speculative and may change as the JEDEC SDRAM data sheets mature.

Bit position 10 is used in the command encoding of the Precharge Single and Precharge All commands to allow the command bit to be mapped directly onto the DRAM address bit 10 to match the DRAM AP bit usage.

Table 4-40 — DRAM Command Mapping Examples

DDR2 Config		20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
256Mb (64Mbx4) 1KB page	Row	1	X	X	RS	X	X	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	X	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
512Mb (128Mbx4) 1KB page	Row	1	X	X	RS	A13	X	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	X	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1Gb (256Mbx4) 1KB page	Row	1	X	X	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	B2	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
2Gb (512Mbx4) 1KB page	Row	1	X	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	B2	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4Gb (1Gbx4) * 1KB page	Row	1	A15	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	B2	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4Gb (1Gbx4) * 2KB page	Row	1	X	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	B2	B1	B0	A12	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

DRAM Read and Write commands always transfer complete bursts of data determined by the Burst Length field programmed into the DRAM MRS registers. A burst length of 4 will transfer 36 bytes and a burst length of 8 will transfer 72 bytes to/from each ECC DIMM. Non-ECC memory DIMMs support the Data Mask function.

Write accesses transfer the data from the write data FIFO located inside the AMB device on the DIMM. A register instructs the AMB when to drive the data after the Write command. The DDR2 specific Off-Chip Driver (OCD) Impedance Adjust command (EMRS access with A[9:7] = 100) also transfers data from the write data FIFO to the DRAM devices.

The host is responsible for memory ordering, FBD channel scheduling, and error handling.

4.2.5 Channel Commands

Channel commands include the Sync command, miscellaneous DRAM commands, configuration register read and write commands, and miscellaneous maintenance commands. Channel commands may include a DS[2:0] field to specify which DIMM the command is addressing, a 4-bit operation code field to define the command type, and an 11-bit address field. Table 4-41 defines the encoding of the Channel commands. The individual configuration registers are defined in the *FBD AMB Specification* Register chapter.