EXHIBIT Y

JEDEC STANDARD

FBDIMM
Advanced Memory Buffer (AMB)

JESD82-20A
(Revision of JESD82-20, March 2007)

SPECIAL DISCLAIMER: JEDEC has received information that certain patents or patent applications may be relevant to this standard, and, as of the publication date of this standard, no statements regarding an assurance or refusal to license such patents or patent applications have been provided.

http://www.jedec.org/download/search/FBDIMM/Patents.xls

JEDEC does not make any determination as to the validity or relevancy of such patents or patent applications. Prospective users of the standard should act accordingly.

MARCH 2009

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

JEDEC

EXHIBIT
//

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or call (703) 907-7559 or www.jedec.org

Published by
©JEDEC Solid State Technology Association 2009
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

PRICE: Please refer to the current
Catalog of JEDEC Engineering Standards and Publications online at
http://www.jedec.org/Catalog/catalog.cfm

Special Disclaimer

JEDEC has received information that certain patents or patent applications may be relevant to this standard, and, as of the publication date of this standard, no statements regarding an assurance or refusal to license such patents or patent applications have been provided.

http://www.jedec.org/download/search/FBDIMM/Patents.xls

JEDEC does not make any determination as to the validity or relevancy of such patents or patent applications. Prospective users of the standard should act accordingly.

FBDIMM: Advanced Memory Buffer (AMB)

Contents

FBDIMM: Advanced Memory Buffer (AMB)

Contents (cont'd)

FBDIMM: Advanced Memory Buffer (AMB)

Contents (cont'd)

FBDIMM: Advanced Memory Buffer (AMB)

Contents (cont'd)

Contents (cont'd)

Tables

Contents (cont'd)

Figures

FBDIMM: Advanced Memory Buffer (AMB)

Contents (cont'd)

FBDIMM: Advanced Memory Buffer (AMB)

(From JEDEC Board ballot JCB-06-42 and JCB-08-75, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Introduction

This document is a core specification for a Fully Buffered DIMM (FBD) memory system. This document, along with the other core specifications, must be treated as a whole. Information critical to a Advanced Memory Buffer design appears in the other specifications, with specific cross-references provided.

1.1 Advanced Memory Buffer Overview

The Advanced Memory Buffer (AMB) reference design complies with the *FB-DIMM Architecture and Protocol Specification* . It supports DDR2 SDRAM main memory. The Advanced Memory Buffer allows buffering of memory traffic to support large memory capacities. All memory control for the DRAM resides in the host, including memory request initiation, timing, refresh, scrubbing, sparing, configuration access, and power management. The Advanced Memory Buffer interface is responsible for handling FBD channel and memory requests to and from the local DIMM and for forwarding requests to other DIMMs on the FBD channel.

Fully Buffered DIMM (FBD) provides a high memory bandwidth, large capacity channel solution that has a narrow host interface. Fully Buffered DIMMs use commodity DRAMs isolated from the channel behind a buffer on the DIMM. The memory capacity is 288 devices per channel and total memory capacity scales with DRAM bit density. The Advanced Memory Buffer is the buffer that isolates the DRAMs from the channel.

1.2 Advanced Memory Buffer Functionality

1.2.1 Advanced Memory Buffer

The Advanced Memory Buffer will perform the following FBD channel functions:

- Supports channel initialization procedures as defined in the initialization chapter of the *FB-DIMM Architecture and Protocol Specification* to align the clocks and the frame boundaries, verify channel connectivity, and identify AMB DIMM position.
- Supports the forwarding of southbound and northbound frames, servicing requests directed to a specific AMB or DIMM, as defined in the protocol chapter, and merging the return data into the northbound frames.
- If the AMB resides on the last DIMM in the channel, the AMB initializes northbound frames.
- Detects errors on the channel and reports them to the host memory controller.
- Support the FBD configuration register set as defined in the register chapters.
- Acts as DRAM memory buffer for all read, write, and configuration accesses addressed to the DIMM.
- Provides a read buffer FIFO and a write buffer FIFO.
- Supports an SMBus protocol interface for access to the AMB configuration registers.
- Provides logic to support MEMBIST and IBIST Design for Test functions.
- Provides a register interface for the thermal sensor and status indicator.
- Functions as a repeater to extend the maximum length of FBD Links.

2.3 Channel Protocol (cont'd)

2.3.4 Address Mapping of DDR Commands to DRAMs

DDR2 x4 Config		20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
256Mb (64Mbx4) 1KB page	Row	1	X	X	RS	X	X	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	X	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
512Mb (128Mbx4) 1KB page	Row	1	X	X	RS	A13	X	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	X	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1Gb (256Mbx4) 1KB page	Row	1	X	X	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	B2	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
2Gb (512Mbx4) 1KB page	Row	1	X	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	B2	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4Gb (1Gbx4) * 1KB page	Row	1	A15	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	B2	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4Gb (1Gbx4) * 2KB page	Row	1	X	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	B2	B1	B0	A12	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

DDR2 x8 Config		20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
256Mb (32Mbx8) 1KB page	Row	1	X	X	RS	X	X	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	X	B1	B0	X	X	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
512Mb (64Mbx8) 1KB page	Row	1	X	X	RS	A13	X	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	X	B1	B0	X	X	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1Gb (128Mbx8) 1KB page	Row	1	X	X	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	B2	B1	B0	X	X	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
2Gb (256Mbx8) 1KB page	Row	1	X	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	B2	B1	B0	X	X	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4Gb (512Mbx8) * 1KB page	Row	1	A15	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	B2	B1	B0	X	X	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4Gb (512Mbx8) * 2KB page	Row	1	X	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	B2	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

2.3.5 FBD L0s State

The L0s state provides a low latency power down state for the FBD channel. The L0s state will nominally last for 41 frame times such that no sync packets are missed. The actual amount of time is programmable in the AMB. Times greater than 41 frames are not supported at this time. The L0s state may be used when the memory controller is throttling, and producing no transfers.

The duration of the L0s state is pre-programmed into the MC and AMB registers, and is triggered by a sync command with the L0s command indicated. The basic sequence is:

L0 to L0s Transition

- MC issues L0s command in the SYNC command.
- The MC continues sending one additional command, which is a NOP.
- AMB must gate its inputs and stop accepting commands following the NOP. It need not accept and decode the NOP itself.
- Southbound output drivers and input receivers are disabled following the NOP. The turnoff may be staggered for power supply di/dt reduction.
- Northbound channels are shut down following the status packet corresponding to the sync command.
- AMB takes CKE low to all DRAMs and floats the commands and address bus to the DRAMS (all signals except clock, CKE, and ODT).
- The PLL is never powered down before, during, or after the transition.

13.3 Rank Decode (cont'd)

13.3.1 Quad Rank Mode C

Quad rank mode C operates by making two physical ranks show up as one logical rank. A bank address bit as well as the existing RS bit determines which rank the AMB will access. The host controller will see the DIMM as dual rank, with each rank being one density higher than the physical DRAMs.

The host controller sends one Rank Select bit with the DRAM commands that are rank specific. This is called RS in the FBD spec, and will be called RS0 here. The AMB must create an RS1 bit internally to determine which of the 4 ranks to access. RS1 will be used to divide each logical rank into 2 physical ranks on the DIMM. Logical Rank 0 will be divided into physical ranks 0 and 2, while Logical Rank 1 will be divided into physical ranks 1 and 3.

Table 55 — RS1:0 to rank decode

RS1 (created inside the AMB from BA0)	*RS0* (RS field in FBD commands)	Rank Accessed
0	0	0
0	1	1
1	0	2
1	1	3

In the AMB the BA0 bit from the host controller is used to create RS1. This places the even numbered banks in one physical rank, and the odd numbered banks in the other physical rank.

The AMB must recreate the BA0 signal to the DRAMs (called dBA0 here), which is done differently depending on the DRAM density.

Table 56 — dBA0 (DRAM BA0) Selection by DRAM density

DRAM Density	dBA0 (DRAM BA0) bit:
512Mbit	Host BA2
1Gbit	Host Row A14
2Gbit	Host Row A15

The following table shows the physical layout of each DRAM type, and how the host controller will view the DIMM.

Table 57 — DIMM addressing

Physical x8 DRAMs on DIMM					Host Controller View				
Rank	Density	Banks	Row Bits	Col Bits	Rank	Density	Banks	Row Bits	Col Bits
4	512Mbit	4	14	10	2	1Gbit	*8*	14	10
4	1Gbit	8	14	10	2	2Gbit	8	*15*	10
4	2Gbit*	8	15	10	2	4Gbit	8	*16*	10

* Some QR DIMMs may not support 2Gbit DRAMs