

# EXHIBIT Y

# JEDEC STANDARD

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## FBDIMM Advanced Memory Buffer (AMB)

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### JESD82-20A

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## FBDIMM: Advanced Memory Buffer (AMB)

### Contents

---

Contents .....	i
List of Tables .....	v
List of Figures .....	vi
<b>1 Introduction.....</b>	<b>1</b>
1.1 Advanced Memory Buffer Overview .....	1
1.2 Advanced Memory Buffer Functionality .....	1
1.2.1 Advanced Memory Buffer .....	1
1.2.2 Transparent Mode for DRAM Test Support.....	2
1.2.3 Debug and Logic Analyzer Interface .....	2
1.2.4 DDR SDRAM.....	2
1.3 Advanced Memory Buffer Block Diagram.....	3
1.4 Interfaces .....	4
1.4.1 FBD High-Speed Differential Point-to-Point Link (at 1.5 V) Interfaces .....	4
1.4.2 DDR2 Channel .....	4
1.4.3 SMBus Slave Interface .....	5
1.5 References .....	5
1.6 Glossary .....	5
<b>2 FBD Channel Interface .....</b>	<b>8</b>
2.1 Advanced Memory Buffer Support for FBD Operating Modes .....	8
2.2 Channel Initialization .....	8
2.3 Channel Protocol .....	8
2.3.1 General.....	8
2.3.2 Timeouts during TSO .....	8
2.3.3 Recalibrate state considerations .....	9
2.3.4 Address Mapping of DDR Commands to DRAMs .....	10
2.3.5 FBD L0s State .....	10
2.4 Reliability, Availability, and Serviceability .....	11
2.4.1 General .....	11
2.4.2 Channel Error Detection and Logging .....	11
2.5 Channel Configuration.....	11
2.5.1 Re-sync and Resample Modes .....	11
2.5.2 Other Channel Configuration Modes .....	12
2.5.3 Lane to Lane Skew on a Channel .....	12
2.6 Repeater Mode .....	13
2.7 Performance .....	13
2.7.1 Idle Memory Read Latency.....	13
2.8 AMB Components of Channel Latency .....	14
2.8.1 Command to Data Delay Calculation .....	15
2.8.2 Channel Throughput.....	17
<b>3 DDR Interface .....</b>	<b>18</b>
3.1 Advanced Memory Buffer DDR Interface Overview .....	18
3.2 Data Mapping .....	18
3.2.1 Data Mask .....	18
3.3 Command / Address Outputs .....	19
3.3.1 CKE Output Control.....	20

**FBDIMM: Advanced Memory Buffer (AMB)****Contents (cont'd)**


---

3.3.2	Memory Controller / BIOS requirements .....	20
3.4	DQS I/O and DM Outputs .....	21
3.5	Refresh .....	22
3.5.1	Self-Refresh During Channel Reset .....	22
3.5.2	Automatic Refresh .....	22
3.6	Back to Back Turnaround Time .....	23
3.7	DDR Calibration .....	23
3.7.1	DRAM Initialization and (E)MRS .....	24
3.7.2	Automatic DDR Bus Calibration .....	24
3.7.3	S3 Recovery Configuration Registers .....	25
3.7.4	Receive Enable Calibration .....	25
3.7.5	DQS Delay Calibration .....	25
3.8	DDR MEMBIST .....	25
3.8.1	MEMBIST Features .....	26
3.9	DIMM Organization .....	28
<b>4</b>	<b>Electrical, Power, and Thermal .....</b>	<b>29</b>
4.1	Electrical DC Parameters .....	29
4.1.1	Absolute maximum ratings .....	29
4.1.2	Normal Mode .....	30
4.1.3	S3 current Specification .....	37
4.2	FBD Channel Interface .....	37
4.2.1	FBD Electrical Timing Specifications .....	37
4.2.2	AMB Latency Parameters .....	38
4.3	DDR2 DRAM Interface Electrical Specifications .....	42
4.4	DDR2 Electrical Output Timing Specifications .....	43
4.4.1	Description of DQ/DQS Alignment .....	43
4.4.2	Description of ADD/CMD/CNTL Outputs .....	43
4.4.3	Test Load Specification .....	43
4.4.4	tDVA and tDVB Parameter Description .....	43
4.4.5	tjit and tjitHP Parameter Description .....	44
4.4.6	tCVA, tCVB, tECVA and tECVB Parameter Description .....	44
4.4.7	tDQSCK Timing Parameter Description .....	45
4.4.8	DQ and CB (ECC) Setup/Hold Relationships to/from DQS (Read Operation) .....	45
4.4.9	Write Preamble Duration .....	46
4.4.10	Write Postamble Duration .....	46
4.4.11	Advance Memory Buffer Component Electrical Timing Summary .....	47
4.4.12	Reference DDR2 Interface Package Trace Lengths .....	48
4.5	SMBUS Interface .....	49
4.6	Misc I/O (1.5 CMOS Driver) .....	49
4.7	Thermal Diode and Analog to Digital Converter (ADC) .....	50
4.7.1	Thermal Sensor Effects on the Advanced Memory Buffer's Functional Behavior .....	50
<b>5</b>	<b>Error Handling .....</b>	<b>51</b>
5.1	Types of Errors and Responses .....	51
5.1.1	FBD Link Errors .....	51
5.1.2	DDR Errors .....	52
5.1.3	Host Protocol Errors .....	53
5.1.4	Other Errors .....	53

**FBDIMM: Advanced Memory Buffer (AMB)**

**Contents (cont'd)**

---

5.2	Error Logging .....	54
5.2.1	Error Logging Procedure .....	54
5.3	Fail Over Mode Support .....	54
5.4	Fallback to Pass-Thru.....	54
<b>6</b>	<b>Transparent Mode .....</b>	<b>55</b>
6.1	Transparent Mode .....	55
6.1.1	Block Diagram .....	55
6.1.2	Transparent Mode Signal Definitions .....	56
6.1.3	Transparent Mode to FBD Pin Mapping .....	57
6.1.4	Clock Frequency and Core Timing .....	57
6.1.5	Transparent mode timing .....	58
6.1.6	Error reporting .....	62
6.1.7	Transparent mode I/O specifications.....	64
6.1.8	I/O implementation guidellnes .....	65
6.2	Transparent Mode Control and Status Registers .....	66
<b>7</b>	<b>SMBus Interface .....</b>	<b>67</b>
7.1	System Management Access .....	67
7.1.1	SMBus 2.0 Specification Compatibility .....	67
7.1.2	Supported SMBus Commands .....	67
7.1.3	FBD AMB Register Access Protocols.....	68
7.1.4	SMBus Error Handling.....	71
7.1.5	SMBus Resets.....	72
<b>8</b>	<b>Clocking .....</b>	<b>73</b>
8.1	Advanced Memory Buffer Clock Domains.....	73
8.2	PLL Clocks .....	73
8.3	Reference Clock .....	73
8.4	FBD Lane Frame Clocks .....	73
8.5	Clock Ratios .....	74
8.6	DDR DRAM Clock Support.....	74
8.7	Clock Pins.....	74
8.8	PLL Requirements.....	75
8.8.1	Jitter.....	75
8.8.2	PLL Bandwidth Reqlirements .....	75
8.8.3	External Reference.....	75
8.8.4	Spread Spectrum Support .....	75
8.9	Analog Power Supply Pins .....	75
<b>9</b>	<b>Pin Descriptions .....</b>	<b>76</b>
9.1	Pin Description .....	76
<b>10</b>	<b>Reset.....</b>	<b>79</b>
10.1	Introduction.....	79
10.2	Platform Reset Functionality.....	79
10.2.1	Platform RESET# Requirements .....	79
10.2.2	Advanced Memory Buffer RESET# Requirements.....	79
10.2.3	Power-Up and Suspend-to-RAM Considerations .....	80
10.3	Reset Types .....	80



**FBDIMM: Advanced Memory Buffer (AMB)****Contents (cont'd)**


---

10.4	Pads Controlling Reset .....	80
10.4.1	RESET# Pad .....	80
10.4.2	Primary FBD Link .....	80
10.5	Details.....	81
10.5.1	Cold Power-Up Reset Sequence.....	81
10.6	Timing Diagrams .....	82
10.7	I/O Initialization .....	82
10.7.1	FBD Channel Initialization .....	82
<b>11</b>	<b>Registers .....</b>	<b>83</b>
11.1	Access Mechanisms .....	83
11.1.1	Conflict Resolution and Usage Model Limitations .....	83
11.1.2	FBD Data on Configuration Read Returns .....	83
11.1.3	Non-Existent Register Bits.....	83
11.1.4	Register Attribute Definition.....	84
11.1.5	Binary Number Notation .....	84
11.1.6	Function Mapping .....	84
11.2	PCI Standard Header Identification Registers (Function 0).....	94
11.2.1	VID: Vendor Identification Register .....	94
11.2.2	DID: Device Identification Register .....	94
11.2.3	RID: Revision Identification Register .....	94
11.2.4	CCR: Class Code Register.....	95
11.2.5	HDR: Header Type Register.....	95
11.3	FBD Link Registers (Function 1) .....	96
11.3.1	FBD Link Control and Status .....	96
11.3.2	Error Registers .....	109
11.3.3	PERSONALITY BYTES loaded from the SPD .....	111
11.3.4	Advanced Memory Buffer Hardware Configuration Registers .....	112
11.4	Implementation Specific FBD Registers (Function 2).....	114
11.5	DDR and Miscellaneous Registers (Function 3).....	115
11.5.1	Memory BIST Registers .....	115
11.5.2	Memory Registers .....	123
11.5.3	Thermal Sensor Registers.....	128
11.6	Implementation Specific DDR Initialization and Calibration Registers (Function 4) .....	131
11.6.1	DDR Calibration.....	131
11.7	DFX Registers (Function 5).....	134
11.7.1	Transparent Mode Registers .....	134
11.7.2	Logic Analyzer Interface (LAI) Registers .....	136
11.7.3	Error Injection Registers.....	156
11.8	Bring-up and Debug Registers (Function 6).....	147
11.8.1	Southbound FBD IBIST registers .....	147
11.8.2	Northbound FBD IBIST registers.....	153
<b>12</b>	<b>Ballout and Package Information.....</b>	<b>159</b>
12.1	655-ball FBGA, Pin configuration .....	159
12.2	Pin Assignments for the Advanced Memory Buffer (AMB).....	160
12.3	Package Information.....	168

## FBDIMM: Advanced Memory Buffer (AMB)

## Contents (cont'd)

13	AMB Quad Rank Support.....	169
13.1	Background .....	169
13.2	AMB signal changes and DRAM connections .....	169
13.2.1	Quad Rank Signal Requirements .....	169
13.2.2	Address and Control signal reuse .....	170
13.2.3	Quad Rank Signal Mapping.....	171
13.2.4	Mapping to AMB balls.....	172
13.2.5	Signal state at reset.....	172
13.3	Rank Decode.....	172
13.3.1	Quad Rank Mode C.....	173
13.3.2	FBD2 Mode A Rank Decode .....	176
13.4	ODT timing on reads .....	178
13.4.1	AMB data bus termination .....	178
13.5	Registers .....	179
13.6	Fast Reset .....	182

## Tables

1	Example FBD-667 Channel Idle Memory Read Latencies.....	14
2	DQS association with DQ/CB pins in x8 and x4 mode .....	21
3	MEMBIST Feature Summary .....	27
4	Absolute maximum ratings over operating free-air temperature range (see Note 1) .....	29
5	Advanced Memory Buffer Normal Mode DC Electrical Parameters.....	30
5A	Advanced Memory Buffer Normal Mode DC+AC Electrical Parameters.....	30
6	AMB Power Specification Parameters and Test Conditions .....	30
6A	Table 6 values for x8 DIMMs .....	32
6B	Table 6 values for x4 DIMMs .....	32
7	Advanced Memory Buffer FBD Timing/Electrical .....	37
8	Recommended operating conditions for DRAM Interface .....	42
9	Advanced Memory Buffer Component DDR2 Electrical Timing Specifications.....	47
10	Advanced Memory Buffer DDR2 Package Lengths .....	48
11	Recommended operating conditions for SMBUS Interface.....	49
12	Recommended operating conditions for RESET and BFUNC pins.....	49
13	Link Errors In Initialization .....	51
14	Link Errors in Normal Operation.....	51
15	DDR Errors.....	52
16	Host Protocol Errors .....	53
17	Other Errors .....	53
18	Additional Signals In Transparent Mode .....	56
19	Mapping of FBD Pins In Transparent Mode .....	57
20	Mapping of burst position bits to error capture .....	63
21	Selection of 8 bit data paths when ENDOUT is set.....	64
22	Transparent mode FB-DIMM interface signaling specifications.....	64
23	SMBus command Encoding.....	68
24	SMBus Protocol Addressing fields .....	68
25	Status Field Encoding for SMBus Reads .....	69
26	Advanced Memory Buffer Clock Ratios.....	74
27	Clock Pins .....	74
28	Buffer Signal Types .....	76
29	Pin Descriptions .....	76

**FBDIMM: Advanced Memory Buffer (AMB)**

**Contents (cont'd)**

---

30	Access to "Non-existent" Register Bits.....	83
31	Register Attributes Definitions.....	84
32	Function Mapping Legend.....	85
33	Function 0: PCI Standard Header Identification Registers.....	86
34	Function 1: FBD Link Registers.....	87
35	Function 2: Implementation Specific FBD Registers.....	88
36	Function 3: DDR and Miscellaneous Registers.....	89
37	Function 4: Implementation Specific DDR Initialization and Calibration Registers.....	90
38	Function 5: DFX Registers.....	91
39	Function 6: IBIST, Bring-up and Debug Registers.....	92
40	Functions 7: FBD DFX/Defeature Registers.....	93
41	Functional mapping of MemBIST data fields by test mode.....	119
42	MBDATA Failure Address register correspondence to DRAM address.....	120
43	BL4 Column and Chunk correspondence to DRAM address.....	120
44	BL8 Column and Chunk correspondence to DRAM address.....	120
45	Functional Characteristics of DCALADDR.....	132
46	Bit Locations for SB Match and Mask.....	137
47	Local Mask and Match Events selected by MMEVENTnSEL fields.....	140
48	655-Ball FBGA - Left Side.....	160
49	655-Ball FBGA - Right Side.....	161
50	Advanced Memory Buffer Signals by Ball Number.....	162
51	Function Mapping Legend.....	169
52	Quad Rank Signal mapping per rank, ODT Option 1.....	171
53	Quad Rank Signal mapping per rank, ODT Option 2.....	171
54	AMB Pin usage for each DIMM type.....	172
55	RS1:0 to rank decode.....	173
56	dBA0 (DRAM BA0) Selection by DRAM density.....	173
57	DIMM addressing.....	173
58	Activate Command mapping.....	174
59	Read, Write & Precharge Single Command mapping.....	175
60	Rank Selection and dBA0 generation for each command type.....	175
61	Quad Rank Mode A DS[2:0] and RS mapping.....	176
62	AMB response to commands.....	177

**Figures**

1	Advanced Memory Buffer Block Diagram.....	3
2	Advanced Memory Buffer Interfaces.....	4
3	Delays Through an AMB.....	15
4	Command to Data Delay timing.....	16
5	Nominal Turnaround Time Timing Diagram.....	23
6	tDVA and tDVB Timing Diagram.....	44
7	tjit and tjitHP Timing Diagram.....	44
8	tCVA and tCVB Timing Diagram.....	44
9	tECVA and tECVB Timing Diagram.....	45
10	TDQSCK Timing Diagram.....	45
11	DQ and CB (ECC) Setup/Hold Relationship to/from DQS Timing Diagram.....	46
12	Write Preamble Duration Timing Diagram.....	46
13	Write Postamble Duration Timing Diagram.....	46
14	Transparent Mode Simplified Block Diagram.....	55
15	Transparent Mode Timing.....	59
16	Transparent mode write timing.....	60
17	Transparent mode read timing.....	61

FBDIMM: Advanced Memory Buffer (AMB)

Contents (cont'd)

---

18	BL=8 Read timing.....	62
19	SMBus Configuration Read (Block Write / Block Read, PEC enabled).....	69
20	SMBus Configuration Read (Write Bytes / Read Bytes, PEC enabled).....	70
21	SMBus Configuration Double Word Write (Block Write, PEC enabled).....	70
22	SMBus Configuration Double Word Write (Write Bytes, PEC enabled).....	71
23	SMBus Configuration Word Write (Block Write, PEC disabled).....	71
24	SMBus Configuration Byte Write (Write Bytes, PEC disabled).....	71
25	Pinout Configuration.....	159
26	DRAM ODT Timing during Reads.....	178



## FBDIMM: Advanced Memory Buffer (AMB)

(From JEDEC Board ballot JCB-06-42 and JCB-08-75, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

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### 1 Introduction

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This document is a core specification for a Fully Buffered DIMM (FBD) memory system. This document, along with the other core specifications, must be treated as a whole. Information critical to an Advanced Memory Buffer design appears in the other specifications, with specific cross-references provided.

#### 1.1 Advanced Memory Buffer Overview

The Advanced Memory Buffer (AMB) reference design complies with the *FB-DIMM Architecture and Protocol Specification*. It supports DDR2 SDRAM main memory. The Advanced Memory Buffer allows buffering of memory traffic to support large memory capacities. All memory control for the DRAM resides in the host, including memory request initiation, timing, refresh, scrubbing, sparing, configuration access, and power management. The Advanced Memory Buffer interface is responsible for handling FBD channel and memory requests to and from the local DIMM and for forwarding requests to other DIMMs on the FBD channel.

Fully Buffered DIMM (FBD) provides a high memory bandwidth, large capacity channel solution that has a narrow host interface. Fully Buffered DIMMs use commodity DRAMs isolated from the channel behind a buffer on the DIMM. The memory capacity is 288 devices per channel and total memory capacity scales with DRAM bit density. The Advanced Memory Buffer is the buffer that isolates the DRAMs from the channel.

#### 1.2 Advanced Memory Buffer Functionality

##### 1.2.1 Advanced Memory Buffer

The Advanced Memory Buffer will perform the following FBD channel functions:

- Supports channel initialization procedures as defined in the initialization chapter of the *FB-DIMM Architecture and Protocol Specification* to align the clocks and the frame boundaries, verify channel connectivity, and identify AMB DIMM position.
- Supports the forwarding of southbound and northbound frames, servicing requests directed to a specific AMB or DIMM, as defined in the protocol chapter, and merging the return data into the northbound frames.
- If the AMB resides on the last DIMM in the channel, the AMB initializes northbound frames.
- Detects errors on the channel and reports them to the host memory controller.
- Support the FBD configuration register set as defined in the register chapters.
- Acts as DRAM memory buffer for all read, write, and configuration accesses addressed to the DIMM.
- Provides a read buffer FIFO and a write buffer FIFO.
- Supports an SMBus protocol interface for access to the AMB configuration registers.
- Provides logic to support MEMBIST and IBIST Design for Test functions.
- Provides a register interface for the thermal sensor and status indicator.
- Functions as a repeater to extend the maximum length of FBD Links.

2.3 Channel Protocol (cont'd)

2.3.4 Address Mapping of DDR Commands to DRAMs

DDR2 x4 Config		20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
256Mb (64Mbx4) 1KB page	Row	1	X	X	RS	X	X	B1	B0	A2	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	X	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
512Mb (128Mbx4) 1KB page	Row	1	X	X	RS	A3	X	B1	B0	A2	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	X	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1Gb (256Mbx4) 1KB page	Row	1	X	X	RS	A3	B2	B1	B0	A2	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	B2	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
2Gb (512Mbx4) 1KB page	Row	1	X	A14	RS	A3	B2	B1	B0	A2	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	B2	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4Gb (1Gbx4) 1KB page	Row	1	A5	A14	RS	A3	B2	B1	B0	A2	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	B2	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4Gb (1Gbx4) 2KB page	Row	1	X	A14	RS	A3	B2	B1	B0	A2	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	B2	B1	B0	A2	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
DDR2 x8 Config		20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
256Mb (32Mbx8) 1KB page	Row	1	X	X	RS	X	X	B1	B0	A2	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	X	B1	B0	X	X	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
512Mb (64Mbx8) 1KB page	Row	1	X	X	RS	A3	X	B1	B0	A2	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	X	B1	B0	X	X	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1Gb (128Mbx8) 1KB page	Row	1	X	X	RS	A3	B2	B1	B0	A2	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	B2	B1	B0	X	X	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
2Gb (256Mbx8) 1KB page	Row	1	X	A14	RS	A3	B2	B1	B0	A2	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	B2	B1	B0	X	X	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4Gb (512Mbx8) 1KB page	Row	1	A5	A14	RS	A3	B2	B1	B0	A2	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	B2	B1	B0	X	X	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4Gb (512Mbx8) 2KB page	Row	1	X	A14	RS	A3	B2	B1	B0	A2	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	Col	0	1	r/w	RS	X	B2	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

2.3.5 FBD L0s State

The L0s state provides a low latency power down state for the FBD channel. The L0s state will nominally last for 41 frame times such that no sync packets are missed. The actual amount of time is programmable in the AMB. Times greater than 41 frames are not supported at this time. The L0s state may be used when the memory controller is throttling, and producing no transfers.

The duration of the L0s state is pre-programmed into the MC and AMB registers, and is triggered by a sync command with the L0s command indicated. The basic sequence is:

L0 to L0s Transition

- MC issues L0s command in the SYNC command.
- The MC continues sending one additional command, which is a NOP.
- AMB must gate its inputs and stop accepting commands following the NOP. It need not accept and decode the NOP itself.
- Southbound output drivers and input receivers are disabled following the NOP. The turnoff may be staggered for power supply di/dt reduction.
- Northbound channels are shut down following the status packet corresponding to the sync command.
- AMB takes CKE low to all DRAMs and floats the commands and address bus to the DRAMs (all signals except clock, CKB, and ODT).
- The PLL is never powered down before, during, or after the transition.

### 13.3 Rank Decode (cont'd)

#### 13.3.1 Quad Rank Mode C

Quad rank mode C operates by making two physical ranks show up as one logical rank. A bank address bit as well as the existing RS bit determines which rank the AMB will access. The host controller will see the DIMM as dual rank, with each rank being one density higher than the physical DRAMs.

The host controller sends one Rank Select bit with the DRAM commands that are rank specific. This is called RS in the FBD spec, and will be called RS0 here. The AMB must create an RS1 bit internally to determine which of the 4 ranks to access. RS1 will be used to divide each logical rank into 2 physical ranks on the DIMM. Logical Rank 0 will be divided into physical ranks 0 and 2, while Logical Rank 1 will be divided into physical ranks 1 and 3.

Table 55 — RS1:0 to rank decode

RS1 (created inside the AMB from BA0)	RS0 (RS field in FBD commands)	Rank Accessed
0	0	0
0	1	1
1	0	2
1	1	3

In the AMB the BA0 bit from the host controller is used to create RS1. This places the even numbered banks in one physical rank, and the odd numbered banks in the other physical rank.

The AMB must recreate the BA0 signal to the DRAMs (called dBA0 here), which is done differently depending on the DRAM density.

Table 56 — dBA0 (DRAM BA0) Selection by DRAM density

DRAM Density	dBA0 (DRAM BA0) bit:
512Mbit	Host BA2
1Gbit	Host Row A14
2Gbit	Host Row A15

The following table shows the physical layout of each DRAM type, and how the host controller will view the DIMM.

Table 57 — DIMM addressing

Physical x8 DRAMs on DIMM					Host Controller View				
Rank	Density	Banks	Row Bits	Col Bits	Rank	Density	Banks	Row Bits	Col Bits
4	512Mbit	4	14	10	2	1Gbit	8	14	10
4	1Gbit	8	14	10	2	2Gbit	8	15	10
4	2Gbit*	8	15	10	2	4Gbit	8	16	10

\* Some QR DIMMs may not support 2Gbit DRAMs