Exhibit 2

CERTIFICATE OF MAILING BY EXPRESS MAIL
Express Mail Label No. EV584756268US
Date of Deposit: May 11, 2010

PTO/SB/58 (02-09)
Approved for use through 08/31/2010. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

(Also referred to as FORM PTO-1465)

REQUEST FOR *INTER PARTES* REEXAMINATION TRANSMITTAL FORM

Address to:
Mail Stop *Inter Partes* Reexam
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attorney Docket No.: 19473-0052RX1

Date: May 11, 2010

1. ☒ This is a request for *inter partes* reexamination pursuant to 37 CFR 1.913 of patent number 7,289,386 issued 10/30/2007. The request is made by a third party requester, identified herein below.

2. ☒ a. The name and address of the person requesting reexamination is:
Hans R. Troesch, Fish & Richardson P.C.
500 Arguello Street, Suite 500
Redwood City, CA 94063-1526

b. The real party in interest (37 CFR 1.915(b)(8)) is: Google Inc.

3. ☐ a. A check in the amount of $_____ is enclosed to cover the reexamination fee, 37 CFR 1.20(c)(2);

☒ b. The Director is hereby authorized to charge the fee as set forth in 37 CFR 1.20(c)(2) to Deposit Account No. 06-1050; **or**

☐ c. Payment by credit card. Form PTO-2038 is attached.

4. ☒ Any refund should be made by ☐ check or ☒ credit to Deposit Account No. 06-1050 37 CFR 1.26(c). If payment is made by credit card, refund must be to credit card account.

5. ☒ A copy of the patent to be reexamined having a double column format on one side of a separate paper is enclosed. 37 CFR 1.915(b)(5)

6. ☐ CD-ROM or CD-R in duplicate, Computer Program (Appendix) or large table
☐ Landscape Table on CD

7. ☐ Nucleotide and/or Amino Acid Sequence Submission
If applicable, items a. – c. are required.
a. ☐ Computer Readable Form (CRF)
b. Specification Sequence Listing on:
i. ☐ CD-ROM (2 copies) or CD-R (2 copies); **or**
ii. ☐ paper
c. ☐ Statements verifying identity of above copies

8. ☒ A copy of any disclaimer, certificate of correction or reexamination certificate issued in the patent is included.

9. ☒ Reexamination of claim(s) 1-12 is requested.

10. ☒ A copy of every patent or printed publication relied upon is submitted herewith including a listing thereof on Form PTO/SB/08, PTO-1449, or equivalent.

11. ☐ An English language translation of all necessary and pertinent non-English language patents and/or printed publications is included.

CERTIFICATE OF MAILING BY EXPRESS MAIL
Express Mail Label No. EV584756268US
Date of Deposit: May 11, 2010

PTO/SB/58 (02-09)
Approved for use through 08/31/2010. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

12. [X] The attached detailed request includes at least the following items:

a. A statement identifying each substantial new question of patentability based on prior patents and printed publications. 37 CFR 1.915(b)(3)
b. An identification of every claim for which reexamination is requested, and a detailed explanation of the pertinency and manner of applying the cited art to every claim for which reexamination is requested. 37 CFR 1.915(b)(1) & (3).

13. [X] It is certified that the estoppel provisions of 37 CFR 1.907 do not prohibit this reexamination. 37 CFR 1.915(b)(7)

14. [X] a. It is certified that a copy of this request has been served in its entirety on the patent owner as provided in 37 CFR 1.33(c).
The name and address of the party served and the date of service are:

Bruce S. Itchkawitz, KNOBBE MARTENS OLSON & BEAR LLP

2040 Main Street, Fourteenth Floor

Irvine, CA 92614

Date of Service: May 11, 2010 ; **or**

[ ] b. A duplicate copy is enclosed because service on patent owner was not possible. An explanation of the efforts made to serve patent owner **is attached**. See MPEP 2620.

15. Third Party Requester Correspondence Address: Direct all communications about the reexamination to:

[X] The address associated with Customer Number: 26192

OR

[ ] Firm or Individual Name

Address

City | State | Zip

Country

Telephone | Email

16. [X] The patent is currently the subject of the following concurrent proceeding(s):

[ ] a. Copending reissue Application No.
[ ] b. Copending reexamination Control No.
[ ] c. Copending Interference No.
[X] d. Copending litigation styled:

Google Inc. vs. Netlist, Inc., Northern District of California,

Civil Action No. ~~C 08-04144~~

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

Authorized Signature — Date: 05/11/2010

Hans R. Troesch — Typed/Printed Name

36,950 — Registration No., if applicable

CERTIFICATE OF MAILING BY EXPRESS MAIL
Express Mail Label No. EV584756268US
Date of Deposit: May 11, 2010

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of Bhakta *et al.*

U.S. Patent No.:	7,289,386
Issue Date:	October 30, 2007
Application No.:	11/173,175
Filing Date:	July 1, 2005
Title:	Memory Module Decoder

Mail Stop Inter Partes Reexam
Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR INTER PARTES REEXAMINATION UNDER 35 U.S.C. § 311 AND 37 C.F.R. § 1.913

In accordance with 35 U.S.C. § 311 and 37 C.F.R. § 1.913, inter partes reexamination of claims 1-12 of U.S. Patent No. 7,289,386 (the '386 patent) is requested.

The application for the '386 patent was filed on or after November 29, 1999; the '386 patent is therefore eligible for inter partes reexamination.

The '386 patent has not yet been adjudged invalid or unenforceable.

This request is submitted by the undersigned on behalf of the Requester. The undersigned is acting in a representative capacity in accordance with 37 C.F.R. § 1.34(a).

CERTIFICATE OF MAILING BY EXPRESS MAIL

Express Mail Label No. EV584756268US

May 11, 2010
Date of Deposit

TABLE OF CONTENTS

LIST OF APPENDICES

APPENDIX A - U.S. Patent 7,289,386 to Bhakta *et al.* including certificate of correction

APPENDIX B - Relevant portions of the prosecution history of the '386 patent

APPENDIX C - U.S. Patent No. 6,209,074 ("Dell")

APPENDIX D - U.S. Patent No. 6,414,868 ("Wong")

APPENDIX E - U.S. Patent No. 4,368,515 ("Nielsen")

APPENDIX F - U.S. Patent Publication No. 2006/0117152 ("Amidi")

APPENDIX G - Barr, Michael, "Programmable Logic: What's it to Ya?," Embedded Systems Programming, June 1999, pp. 75-84 ("Barr")

APPENDIX H - Claims chart applying principally Dell to the claims.

APPENDIX I - Claims chart applying principally Wong to the claims.

APPENDIX J - Claims chart applying principally Nielsen to the claims.

APPENDIX K - Claims chart applying Amidi to the claims.

I. SUMMARY OF REQUEST

A. Identification of Claims

This reexamination request is directed to claims 1-12 of the '386 patent.

A copy of the patent is attached as Appendix A of this request, including a certificate of correction; and copies of the relevant portions of the '386 patent prosecution history are attached as Appendix B.

The Requester (Google Inc.) is not aware of any disclaimers or reexamination certificates for the '386 patent. A certificate of correction was issued that is not material to the present request. The Requester is aware of the assertion of the '386 patent in a now-terminated action in the United States District Court for the District of Delaware, Civil Action No. 09-cv-165, styled *Netlist, Inc., vs. MetaRAM, Inc.*, and a pending action in the Northern District of California, Civil Action No. C 08-04144, styled *Google Inc. vs. Netlist, Inc.*

B. Identification of Prior Art

1. Priority Date

The earliest priority date to which the claims of the '386 patent could be entitled is March 5, 2004, the filing date of U.S. patent application no. 60/550,668. This request relies on art that is earlier than this date, but the Requester does not concede that the '386 patent is entitled to any priority date earlier than its actual filing date, July 1, 2005.

2. Publications and Substantial New Questions of Patentability

The following documents, which are listed on the form PTO/SB/08 filed with this request, raise substantial new questions of patentability for claims of the '386 patent.

(a) Dell – U.S. Patent No. 6,209,074

Dell was filed on April 28, 1998, issued on March 27, 2001, and is prior art under 35 U.S.C. § 102(b).

Dell was not cited in the record of the '386 patent.

The substantial new question of patentability raised by Dell is described on page 13, below.

(b) **Wong – U.S. Patent No. 6,414,868**

Wong was filed on June 7, 1999, issued on July 2, 2002, and is prior art under 35 U.S.C. § 102(b).

Wong was not cited in the record of the '386 patent.

The substantial new question of patentability raised by Wong is described on page 16, below.

(c) **Nielsen – U.S. Patent No. 4,368,515**

Nielsen was filed on May 7, 1981, issued on January 11, 1983, and is prior art under 35 U.S.C. § 102(b).

Nielsen was not cited in the record of the '386 patent.

The substantial new question of patentability raised by Nielsen is described on page 18, below.

(d) **Amidi – U.S. Patent Publication No. 2006/0117152**

Amidi was filed on January 5, 2004, published June 1, 2006, and is prior art under 35 U.S.C. § 102(e). The Requester submits that the '386 patent is not entitled to any claim of priority to its provisional applications and that Amidi should therefore be considered to be prior art under 35 U.S.C. § 102(b).

Amidi was not cited in the record of the '386 patent.

The substantial new question of patentability raised by Amidi is described on page 20, below.

(e) **Barr – "Programmable Logic: What's it to Ya?"**

Barr has a publication date of June 1999, and is prior art under 35 U.S.C. § 102(b). Barr was cited in the record in the '386 patent and was relied on in combination in rejecting

dependent claims 5-8. This request relies on Barr in the same way, with the same grounds for combining Barr with the principal references, and for the same purpose.

C. Substantial New Questions of Patentability

This request presents questions of patentability that have not been decided by the Office in a previous examination, nor in a final holding of invalidity by a court.

As described more specifically below in connection with the individual references, this request presents substantial new questions of patentability because the stated reason for allowance and the Examiner's comments on the art indicate that the Examiner had not considered the question of the patentability in light of pre-priority date art teaching the generation of more rank selecting signals from fewer rank selecting signals. As described more specifically below, each of the principal references relied on in this request – Dell, Wong, Nielsen and Amidi – teach just this feature.

In short, the references being relied upon present teachings that were "not previously considered and discussed on the record during the prosecution of" the '386 patent or any part application. (See, e.g., MPEP 2616)

Consequently, it is respectfully submitted that:

1. Dell raises a substantial new question of patentability for claims 1-5, 7, and 9-13 of the '386 patent.
2. Dell in combination with Barr raises a substantial new question of patentability for claims 6 and 8 of the '386 patent.
3. Wong raises a substantial new question of patentability for claims 1-4, 10 and 12 of the '386 patent.
4. Wong in combination with Barr raises a substantial new question of patentability for claims 5-8 of the '386 patent.
5. Nielsen raises a substantial new question of patentability for claims 1, 3, 10, and 12 of the '386 patent.
6. Nielsen in combination with Barr raises a substantial new question of patentability for claims 5-8 of the '386 patent.

7. Amidi raises a substantial new question of patentability for claims 1-9 and 11-13 of the '386 patent.

II. DESCRIPTION OF THE '386 PATENT

A. The '386 Patent

The '386 patent is directed to techniques that allow a memory module to be used in a system, where the memory module has a higher density or a larger number of rows of memory devices than the system supports: "Most computer and server systems support one-rank and two-rank memory modules. By only supporting one-rank and two-rank memory modules, the memory density that can be incorporated in each memory slot is limited." (2:38-42) The techniques described in the '386 patent purportedly can be used to increase the memory capacity or memory density per memory slot or socket of a system, allowing for a higher memory capacity in systems with limited memory slots. They purportedly can also be used to reduce the cost of memory modules by substituting pairs of lower cost-per-bit lower-density memory devices for individual higher-density memory devices. (32:58-33:16)

The one independent claim recites a memory module that can be connected to a system and, furthermore, that has a printed circuit board. Coupled to the printed circuit board are multiple memory devices and a logic element. The logic element performs the actions of (i) receiving, from the system, input control signals that correspond to a system number of memory devices, which is smaller than the actual number of memory devices actually on the printed circuit board, and (ii) generating, in response to the input control signals, output control signals that correspond to the actual number of memory devices. The claim further recites: (i) that the actual memory devices on the printed circuit board are arranged in an actual number of ranks; (ii) that the input control signals (e.g., rank select signals) correspond to a system number of ranks, which is less than the actual number of ranks; (iii) that the logic element responds to a first command signal (e.g., read or write from a rank) from the system by generating a second command signal (e.g., read or write from a rank) transmitted to the actual memory devices; and (iv) and that the first command signal corresponds to the system number of ranks and the second command signal corresponds to the actual number of ranks. In claim 10, the '386 patent recites

the particular example where the actual number of ranks is two and the system number of ranks is one.

III. THE SPECIFICATION, CLAIMS, AND PROSECUTION HISTORY OF THE '386 PATENT

A. Prosecution History of the '386 Patent

1. Prosecution history

The '386 patent issued October 30, 2007, from an application filed July 1, 2005. The patent describes itself as "a continuation-in-part of U.S. patent application Ser. No. 11/075,395, filed Mar. 7, 2005, [which issued as U.S. Patent No. 7,286,436 on October 23, 2007] which claims the benefit of U.S. Provisional Application No. 60/550,668, filed Mar. 5, 2004 and U.S. Provisional Application No. 60/575,595, filed May 28, 2004. The present application also claims the benefit of U.S. Provisional Application No. 60/588,244, filed Jul. 15, 2004 . . . ."

The application for the '386 patent was filed with 20 claims. In response to a restriction requirement, the applicant elected claims 1-15 without traverse. The restriction requirement described these claims as follows: "Claims 1-15, drawn to memory with address decoder, classified in class 365, subclass 230.06." (Action with notification date of January 26, 2007, pages 2-3) (the "first action") The claims themselves, however, are directed to a "memory module connectable to a computer system" (preamble of claim 1) that includes a printed circuit board, multiple memory devices, and a logic element.

In the first action, claims 1-11 and 14-15 were rejected under 35 U.S.C. § 103. In response, the applicant cancelled these claims without addressing the merits of the prior art based rejections.

In the first action, the Examiner stated that claims 12 and 13 contained allowable subject matter but objected to them as depending from a rejected base claim.

In response, the applicant amended claim 12 to incorporate the limitations of its rejected base claims – claims 1 and 8 – and added new claims 21-31, corresponding to other rejected claims, as claims depending from claim 12. Claim 13 had already depended from claim 12. (Amendment And Response To January 26, 2007 Office Action, dated June 19, 2007)

"Applicants submit that the limitations of Claims 21-31 generally correspond to those of Claims 2-7, 9-11, 14, and 15, respectively . . . ." (*Id.*, p. 6)

The next action was a notice of allowance and notice of allowability, dated July 30, 2007.

Thus, claim 1 of the '386 patent is a combination of originally filed claims 1, 8 and 12. The Examiner found that the art did not teach the features of claim 12, as is clear from the Examiner's stated reasons for allowance, set forth below.

2. Stated Reasons for Allowance

The Examiner's statement of reasons for allowance read as follows:

> **With respect to independent claim 12**, there is no teaching, suggestion, or motivation for combination in the prior art to the logic element generating a second command signal, corresponding to a first number of ranks, based on the first command signal, corresponding to a second number of ranks, wherein the second number of ranks is less than the first number of ranks (i.e., the logic element generates more rank select signals from a number of rank select signals). (Notice of Allowability, p. 2) (underlining added)

This statement tracked the features recited in original claim 12; in the first action, the Examiner had stated that claim 12 contained allowable subject matter. Claim 12 had read as follows:

> 12. The memory module of Claim 8, wherein the logic element further responds to a first command signal from the computer system by generating a second command signal transmitted to the plurality of memory devices, the first command signal corresponding to the second number of ranks and the second command signal corresponding to the first number of ranks.

The applicant replied with a purported disagreement with the Examiner's reasons for allowance with the following boilerplate remark, which does not actually challenge the Examiner's stated reason:

> Applicants respectfully disagree with the Examiner's Statement of Reasons for Allowance to the extent that the limitations recited by the Examiner are not present in all of the claims. (COMMENTS ON EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE, dated Sept. 19, 2007)

The Examiner also commented on the art, as follows:

> The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Sakurai (U.S. Patent 5,959,930), Kinsley et al. (U.S. Patent 7,046,538), Raghuram (U.S. Patent 7,200,021), and Raghuram (U.S. Patent Application Publication 200610129755).
>
> Sakurai teach a bank address decoder that takes two bank signals and generates 4 bank select signals to select each of the memory arrays (banks are different than ranks).
>
> Kinsley et al., filed after instant application's provisional applications, teach a three rank memory module.
>
> Raghuram '021, filed after instant application's provisional applications, teach 2 rank select signals input to a decoder that outputs 4 rank select signals.
>
> Raghuram '755, filed after instant application's provisional applications, teach 3 rank select signals input to a decoder that outputs 8 rank select signals.

The Examiner's comments about the two Raghuram references, along with the Examiner's stated reason for allowance that "the [claimed] logic element generates more rank select signals from a number of rank select signals," clearly indicates the Examiner had not considered the question of patentability in light of pre-priority date art teaching the generation of more rank selecting signals from fewer rank selecting signals. The Examiner's comments also indicates that the Examiner had not considered the question of the relevance of teachings about the multiplication of bank select signals to the patentability of the claims under 35 U.S.C. § 103.

3. Prosecution History and Allowances in Parent Applications

The '386 patent claims priority to U.S. Patent No. 7,286,436 (application no. 11/075,395) (the " '436 patent ") as a continuation-in-part.

Its abstract describes the '436 patent as being directed to a "memory module that comprises a plurality of memory components. Each memory component has a first bit width. The plurality of memory components are configured as one or more pairs of memory components. Each pair of memory components simulates a single virtual memory component having a second bit width which is twice the first bit width." (Abstract)

Claims 34-45 of the application were allowed in a first action. The Examiner's reasons for allowance read as follows. (Pages 4-5 of action having a notification date of Jan. 2, 2007):

The following is a statement of reasons for the indication of allowable subject matter:

The prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Pax, Doblar et al. (US 6,996,686), and Anglada et al. (US 5,805,520) taken individually or in combination, do not teach the claimed invention having the following limitations, in combination with the remaining claimed limitations:

- **As in claim 34-39**: wherein the first termination circuit selectively electrically terminates the first data strobe pin and the at least one data pin of the first memory component in response to a first signal received by the first termination signal pin from the termination bus; or
- **As in claims 40-45**: further comprising a serial-presence-detect (SPD) device comprising data that characterizes each pair of memory components as a virtual memory component having a second bit width equal to twice the first bit width, a second number of banks of memory locations equal to the first number of banks, a second number of row address bits equal to the first number of row address bits, and a second number of column address bits equal to the first number of column address bits.

These reasons for allowance are not germane to the allowance of the '386 patent.

B. Analysis and Interpretation of Claims

1. Claims in Reexamination Must Be Given the Broadest Reasonable Interpretation

During a reexamination proceeding, claims must be interpreted according to the "broadest reasonable interpretation" standard. MPEP § 2258(I)(G); *see also* MPEP § 2658. This "broadest reasonable interpretation" standard is different from the claim construction standards applied in a litigation context. Federal Circuit law mandates this difference in how claims are interpreted. *Atlantic Thermoplastics Co. v. Faytex Corp.*, 970 F.2d 834, 846 (Fed. Cir. 1992) (stating that the PTO gives claims their "broadest reasonable meaning when determining patentability" but that "this approach is inapplicable" during litigation determining validity or infringement). Therefore, claim interpretations in this request are provided in accordance with the "broadest reasonable interpretation" standard to be used by the PTO during reexamination and do not reflect the claim constructions that the Requester believes should be used by a court

in litigation. By interpreting the claims in this manner, the Requester neither admits nor acquiesces as to any construction of any claim.

The following analyses of claim 1 are made with these rules in mind.

2. Claim 1

The claim reads as follows:

> 1. A memory module connectable to a computer system, the memory module comprising:
>
> a printed circuit board;
>
> a plurality of memory devices coupled to the printed circuit board, the plurality of memory devices having a first number of memory devices; and
>
> a logic element coupled to the printed circuit board, the logic element receiving a set of input control signals from the computer system, the set of input control signals corresponding to a second number of memory devices smaller than the first number of memory devices, the logic element generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of memory devices, wherein the plurality of memory devices are arranged in a first number of ranks, and the set of input control signals corresponds to a second number of ranks of memory modules, the second number of ranks less than the first number of ranks, wherein the logic element further responds to a first command signal from the computer system by generating a second command signal transmitted to the plurality of memory devices, the first command signal corresponding to the second number of ranks and the second command signal corresponding to the first number of ranks.

The Requester makes the following observations on terms appearing in claim 1.

First and second and corresponding signals. There are many relationships defined in claim 1 among first and second numbers of things and the signals that correspond to them. It may be useful to tabulate the relationships:

Memory devices:

First number – the actual number of devices on the module.

Corresponds to output control signals generated by logic element.

Second command signal is transmitted to plurality (equal to first number) of actual devices.

Second number – a number smaller than the first number.

Corresponds to input control signals from the computer system.

Ranks:

First number – the actual number of ranks on the module.

Corresponds to second command signal

Second number – a number less than the first number.

Corresponds to input control signals from the computer system.

Corresponds to first command signal from the computer system.

One can make things a bit easier to follow by referring to each first number of things as the actual number, and each second number, as the system number; and by referring to signals that are received by the logic element from the computer system as system (command or control) signals, and to signals generated by the logic element for the actual memory devices as actual signals. Table 1 summarizes the foregoing information.

	System	Actual
Number of things	What the system thinks is on the module (fewer than the actual number) • second number of ranks • second number of devices	What is actually on the module • first number of ranks • first number of devices
Signals	Signals received by the logic element from the computer system; corresponds to the system number of things • first command signal • input control signals	Signals the logic element generates for the actual number of things; corresponds to the actual number of things • second command signals • output control signals

Table 1

The limitations of claim 1 can then be more recast for easier understanding as follows:

- the logic element receives system control signals
- the system control signals correspond to a system number of memory devices
- the system number is smaller than the actual number of memory devices
- the logic element generates actual control signals in response to the system control signals

- the actual control signals correspond to the actual number of memory devices
- the actual memory devices are arranged in the actual number of ranks
- the system control signals correspond to a system number of ranks
- the system number of ranks is less than the actual number of ranks
- the logic element receives a system command signal
- the system command signal corresponds to the system number of ranks
- the logic element generates an actual command signal, transmitted to the actual number of memory devices
- the actual command signal corresponds to the actual number of ranks.

In short, the logic element receives system signals that correspond to system numbers of memory devices and ranks, and generates actual signals that correspond to actual numbers of memory devices and ranks. The systems numbers are smaller than the corresponding actual numbers.

Corresponding. The '386 patent does not explain or define what it means for a signal to correspond to a number. Under the broadest reasonable interpretation, then, any correspondence of any kind between a signal and a number of ranks or devices, or the ranks or devices themselves, will be considered to meet the limitation.

Logic element. Claim 1 does not limit the recited logic element except as to the functions it can perform (receiving signals from the computer system and generating and transmitting signals to the memory devices) and that it is coupled to the printed circuit. Under the broadest reasonable interpretation, it can therefore be implemented in any form of logic that is coupled to the printed circuit board directly or indirectly.

Smaller system numbers of devices and ranks. Under the broadest reasonable interpretation, the claim limitations reciting the smaller numbers of system ranks and memory devices than actual ranks and memory devices will be considered to be met without limitation as to how the counting is done and without avoiding double counting, e.g., where a consequence of a greater actual number of ranks is the presence on the module of a greater actual number of memory devices.

IV. INVALIDITY ANALYSIS

A. Claims 1-5, 7, and 9-12 are Obvious in View of Dell; Claims 6 and 8 are Obvious in View of Dell and Barr

Claims 1-5, 7, and 9-12 are unpatentable because they are obvious in view of Dell. Claims 6 and 8 are unpatentable because they are obvious in view of Dell and Barr.

1. Summary of the Application of Dell

Dell discloses a memory module that has a logic circuit and multiple memory devices that are each configured in M banks. The logic circuit receives from a memory controller a number of address inputs and a number of bank address signals. The received address inputs and bank address input signals correspond to N-bank memory devices. The logic circuit re-maps at least one of the address inputs as an additional bank address signal to the memory device having M banks. (Abstract) This remapping allows a system that expects a module with N banks to use a module that actually has 2N banks. (8:15-28, 52-61)

The remapping of the "banks" in Dell corresponds directly to the remapping of the "ranks" that are remapped in the '386 patent, and all the features of the remapping claimed in claim 1 and many of the dependent claims are described in Dell in reference to remapping banks.

Very specifically, and exactly parallel to the '386 patent, Dell notes an application in which a "system may need a two bank memory chip, but the memory module may include a memory device that is a four bank device." (2:29-31)

The problem Dell addressed, how to use more or cheaper memory in systems that support a limited number of banks, is simply and directly analogous to the problem of how to use more or cheaper memory that exists relative to systems that support a limited number of ranks. The motivations for applying the teachings of Dell to a system with a limited number of ranks include enabling the use of higher-density or lower-cost memory modules, by using a larger number of ranks, just as Dell had used a larger number of banks, than the system knows about.

As noted by the Supreme Court in *KSR*, "if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond

his or her skill." *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1740 (2007). The person of skill would have recognized that the technique used to improve the bank-limited memory architecture of Dell could equally well be used to improve the rank-limited memory architecture addressed in the '386 patent. The straightforward and legally obvious use of the technique in the context of the '386 patent is shown in the claim chart of Appendix H, which applies Dell to the claims.

2. Summary of the Application of Dell and Barr

The Barr reference was of record during the prosecution of the '386 patent. Barr was applied to reject dependent claims 4-7 of the application, which recite the same limitations as do dependent claims 5-8 of the '386 patent. Barr is applied in the claim chart in the same way it was applied by the Examiner during the original prosecution.

This Request applies Barr to dependent claims 6 and 8 in combination with the principal reference in the same way Barr was applied during the prosecution of the '386 patent.

As noted by the Examiner in combining Barr with a different principal reference and applying the combination to claims corresponding to claims 5-8, "it would have been obvious to one of ordinary skill in the art at the time of the invention to use an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device for the logic device such that the memory module would be programmable. Barr further supports that ASICs, FPGAs, CPLDs are commonly used in memory circuitry as address decoders." This observation applies directly to claims 5-8.

3. Substantial New Question of Patentability

Because these teachings of Dell were not provided by the art considered by the Examiner during the prosecution of the '386 patent, the teachings of Dell raise a substantial new question of patentability.

In particular, the Examiner's comments on the art upon allowance of the '386 patent – "banks are different than ranks" – indicates that the Examiner had not considered the question of how banks are analogous to ranks and the relevance of teachings about the multiplication of bank select signals to the obviousness of the claims. For this additional reason, this request presents a substantial new question of patentability.

4. Claim Chart Applying Dell to Claims 1-5, 7, and 9-12

Claims 1-5, 7, and 9-12 of the '386 patent are unpatentable under 35 U.S.C. §§ 103 and 102(b) as being obvious in view of Dell, as shown by the claim chart attached as Appendix H.

5. Claim Chart Applying Dell and Barr to Claims 6 and 8

Claims 6 and 8 of the '386 patent are unpatentable under 35 U.S.C. §§ 103 and 102(b) as being obvious in view of the combination of Dell and Barr, as also shown by the claim chart attached as Appendix H.

B. Claims 1-4, 10 and 12 are Anticipated by Wong; Claims 5-8 are Obvious in View of Wong and Barr

Claims 1-4, 10, and 12 are unpatentable because they are anticipated by Wong. Claims 5-8 are unpatentable because they are obvious in view of Wong and Barr.

1. Summary of the Application of Wong

Wong discloses a memory module that has a logic circuit (made up of a buffer and a bank control circuit) and multiple memory devices. Multiple memory devices are organized into ranks on the module. In Wong, in accordance with usage at the time Wong was filed, the word "bank" was used to refer to what the '386 patent refers to as ranks.

The logic circuit receives from a memory controller a number of address inputs and a number of rank select signals (these are signals selecting what are called "banks" in Wong). The received address input signals and rank select input signals correspond to that number of ranks (called "banks" in Wong). The logic circuit re-maps at least one of the address input signals and the rank address signals into more rank address signals than were received from the memory controller. This remapping allows a system that expects a module with one rank, for example, to use a module that actually has two ranks. (See, e.g., Figs. 4A and 4B, showing the mapping of one rank select input signal RAS0 and one address input signal A13 into two rank select output signals RASUX and RASLX, which select two different ranks.)

Moreover, the problem Wong addressed is the same problem addressed by the '386 patent:

> It would be desirable to increase the memory capacity for such a computer system by adding extra banks of memory [called "ranks" of memory in the '386 patent] without having to change the type of memory chip employed. However, the number of address inputs to the system's memory chips limits the ability to do this. Furthermore, the presence of only one RAS and one CAS signal also limits the ability to expand system memory, as a separate bank of memory [called a "rank" of memory in the '386 patent] typically requires at minimum either a unique RAS or unique CAS signal for each bank. As such, it would be desirable to overcome the limitations described above in order to allow extra banks of memory [called "ranks" of memory in the '386 patent] to be added to a computer system, thereby expanding system memory capacity. (Wong, 1:62 – 2:10, emphasis added)

2. Summary of the Application of Wong and Barr

The Barr reference was of record during the prosecution of the '386 patent. Barr was applied to reject dependent claims 4-7 of the application, which recite the same limitations as do dependent claims 5-8 of the '386 patent. Barr is applied in the claim chart in the same way it was applied by the Examiner during the original prosecution.

This Request applies Barr to dependent claims 6 and 8 in combination with the principal reference in the same way Barr was applied during the prosecution of the '386 patent.

As noted by the Examiner in combining Barr with a different principal reference and applying the combination to claims corresponding to claims 5-8, "it would have been obvious to one of ordinary skill in the art at the time of the invention to use an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device for the logic device such that the memory module would be programmable. Barr further supports that ASICs, FPGAs, CPLDs are commonly used in memory circuitry as address decoders." This observation applies directly to claims 5-8.

3. Substantial New Question of Patentability

Because these teachings of Wong were not provided by the art considered by the Examiner during the prosecution of the '386 patent, the teachings of Wong raise a substantial new question of patentability.

In particular, the Examiner's specific reason for allowance of the '386 patent – "the logic element [of claim 1] generates more rank select signals from a number of rank select signals" – shows that the application of a reference like Wong that teaches just such logic raises a substantial new question of patentability.

Similarly, the Examiner's indication of the materiality of the two Raghuram references, which the Examiner considered to have been filed too late to apply, supports that same conclusion:

> Raghuram '021, filed after instant application's provisional applications, teach 2 rank select signals input to a decoder that outputs 4 rank select signals.
>
> Raghuram '755, filed after instant application's provisional applications, teach 3 rank select signals input to a decoder that outputs 8 rank select signals.

For each of these reasons, this request presents a substantial new question of patentability.

4. Claim Chart Applying Wong to Claims 1-4, 10, and 12

Claims 1-4, 10, and 12 of the '386 patent are unpatentable under 35 U.S.C. § 102(b) as being anticipated by Wong, as shown by the claim chart attached as Appendix I.

5. Claim Chart Applying Wong and Barr to Claims 5-8

Claims 5-8 of the '386 patent are unpatentable under 35 U.S.C. §§ 103 and 102(b) as being obvious in view of the combination of Wong and Barr, as also shown by the claim chart attached as Appendix I.

C. Claims 1, 10, and 12 are Anticipated by Nielsen; Claim 3 is Obvious in View of Nielsen; Claims 5-8 are Obvious in View of Nielsen and Barr

Claims 1, 10, and 12 are unpatentable because they are anticipated by Nielsen. Claim 3 is unpatentable because it is obvious in view of Nielsen. Claims 5-8 are unpatentable because they are obvious in view of Nielsen and Barr.

1. Summary of the Application of Nielsen

Nielsen discloses a memory module that has a logic circuit, which includes address decode logic, and multiple memory devices. The multiple memory devices are each activated by a separate chip select (CS) signal and thus each memory device is a rank on the module. A chip select is not a necessary input into the module; however, a single rank can be addressed from the computer side without necessarily using a chip select signal.

The address lines for the module provide signal lines for only a single memory. The logic circuit generates more chip select signals than it receives (which could be zero) in order to address more ranks and increase the number of addressable memory locations. (2:3-5; Fig. 4)

The logic circuit detects certain preprogrammed addresses appearing on the address signal lines from the computer (the game console) and switches the active rank that responds to general addresses accordingly. (5:54-66)

Absent the use of and response to the preprogrammed switching addresses, the memory module would provide in effect a single rank of memory. The logic circuit converts a sequence of address signals for one rank into signals that address multiple ranks. (See, e.g., Figs. 3 and 4, showing the generation of multiple chip select (CS) signals.)

2. Summary of the Application of Nielsen and Barr

The Barr reference was of record during the prosecution of the '386 patent. Barr was applied to reject dependent claims 4-7 of the application, which recite the same limitations as do dependent claims 5-8 of the '386 patent. Barr is applied in the claim chart in the same way it was applied by the Examiner during the original prosecution.

This Request applies Barr to dependent claims 5-8 in combination with the principal reference in the same way Barr was applied during the prosecution of the '386 patent.

As noted by the Examiner in combining Barr with a different principal reference and applying the combination to claims corresponding to claims 5-8, "it would have been obvious to one of ordinary skill in the art at the time of the invention to use an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device for the logic device such that the memory module would be programmable. Barr further supports that ASICs, FPGAs, CPLDs are commonly used in memory circuitry as address decoders." This observation applies directly to claims 5-8.

3. Substantial New Question of Patentability

Because these teachings of Nielsen were not provided by the art considered by the Examiner during the prosecution of the '386 patent, the teachings of Nielsen raise a substantial new question of patentability.

In particular, the Examiner's specific reason for allowance of the '386 patent – "the logic element [of claim 1] generates more rank select signals from a number of rank select signals" – shows that the application of a reference like Nielsen that teaches just such logic raises a substantial new question of patentability.

Similarly, the Examiner's indication of the materiality of the two Raghuram references, which the Examiner considered to have been filed too late to apply, supports that same conclusion:

> Raghuram '021, filed after instant application's provisional applications, teach 2 rank select signals input to a decoder that outputs 4 rank select signals.
>
> Raghuram '755, filed after instant application's provisional applications, teach 3 rank select signals input to a decoder that outputs 8 rank select signals.

For each of these reasons, this request presents a substantial new question of patentability.

4. Claim Chart Applying Nielsen to Claims 1, 3, 10, and 12

Claims 1, 10, and 12 of the '386 patent are unpatentable under 35 U.S.C. § 102(b) as being anticipated by Nielsen, as shown by the claim chart attached as Appendix J. Claim 3 is unpatentable because it is obvious in view of Nielsen, as shown by the claim chart attached as Appendix J.

5. Claim Chart Applying Nielsen and Barr to Claims 5-8

Claims 5-8 of the '386 patent are unpatentable under 35 U.S.C. §§ 103 and 102(b) as being obvious in view of the combination of Nielsen and Barr, as also shown by the claim chart attached as Appendix J.

D. Claims 1-9 and 11-12 are Anticipated by Amidi; Claim 10 is Obvious in View of Amidi

Claims 1-9 and 11-12 are unpatentable because they are anticipated by Amidi. Claim 10 is unpatentable because it is obvious in view of Amidi.

1. Summary of the Application of Amidi

Amidi discloses a memory module that has a logic circuit, which includes a CPLD (complex programmable logic device) and register circuitry, and multiple DRAM memory devices organized into ranks. The ranks of memory devices are each activated by one of a larger number of output chip select (CS) signals, e.g., one of four signals rcs0, rcs1, rcs2 or rcs3, that are generated from a smaller number of input chip select signals, e.g., one of two signals cs0 or cs1, and an address signal. (See, e.g., Fig. 6A)

The memory module of Amidi is designed with the same technical backdrop and the same goals. The results achieved according to the '386 patent were already anticipated by Amidi. Consider this passage from the '386 patent:

> In certain embodiments, the memory density of a memory module is advantageously doubled by providing twice as many memory devices as would otherwise be provided. For example, pairs of lower-density memory devices can be substituted for individual higher-density memory devices to reduce costs or to increase performance. As another example, twice the

> number of memory devices can be used to produce a higher-density memory configuration of the memory module. Each of these examples can be limited by the number of chip select signals which are available from the memory controller or by the size of the memory devices. Certain embodiments described herein advantageously provide a logic mechanism to overcome such limitations. ('386 patent, 33:4-16)

The following paragraphs from Amidi describe the same issues and goals, and reference the same solutions:

> [0008] Because memory devices with lower densities are cheaper and more readily available, it may be advantageous to build the above same density memory module using lower densities devices. However, in order to [do so], the memory module needs four ranks . . . .
>
> [0010] The only solution would be, to stack two memory devices together to achieve an extra rank on the same placement space. Although this would solve the placement problem . . ., the memory module would still possess four memory ranks. As explained earlier, all standard memory modules have only two chip select signals per memory socket routed. Therefore, such memory module would not be viable.
>
> [0011] A need therefore exists for a transparent four rank memory module fitting into a memory socket having two chip select signals routed. A primary purpose of the present invention is to solve these needs and provide further, related advantages. (Amidi, paragraphs 8-11)

2. Substantial New Question of Patentability

Because these teachings of Amidi were not provided by the art considered by the Examiner during the prosecution of the '386 patent, the teachings of Amidi raise a substantial new question of patentability.

In particular, the Examiner's specific reason for allowance of the '386 patent – "the logic element [of claim 1] generates more rank select signals from a number of rank select signals" – shows that the application of a reference like Amidi that teaches just such logic raises a substantial new question of patentability.

Similarly, the Examiner's indication of the materiality of the two Raghuram references, which the Examiner considered to have been filed too late to apply, supports that same conclusion:

Raghuram '021, filed after instant application's provisional applications, teach 2 rank select signals input to a decoder that outputs 4 rank select signals.

Raghuram '755, filed after instant application's provisional applications, teach 3 rank select signals input to a decoder that outputs 8 rank select signals.

For each of these reasons, this request presents a substantial new question of patentability.

3. Claim Chart Applying Amidi to Claims 1-12

Claims 1-9 and 11-12 of the '386 patent are unpatentable under 35 U.S.C. § 102(b) as being anticipated by Amidi, as shown by the claim chart attached as Appendix K. Claim 10 is unpatentable because it is obvious in view of Amidi, as shown by the claim chart attached as Appendix K.

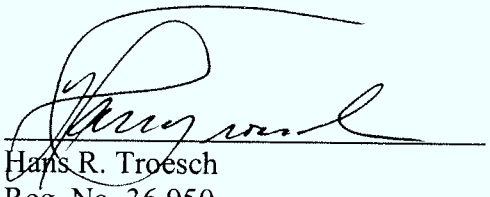
CONCLUSION

For the foregoing reasons, substantial and new questions of patentability exist with respect to claims 1-12 of the '386 patent. The references cited above render claims 1-13 of the '386 patent unpatentable as set forth above. Reexamination of these claims is therefore requested.

Please apply any required charges not otherwise paid or any credits to our Deposit Account No. 06-1050.

Respectfully submitted,

Dated: 11 May 10



Hans R. Troesch
Reg. No. 36,950

Fish & Richardson P.C.
Telephone: (650) 839-5070
Facsimile: (650) 839-5071

50703549.doc

CERTIFICATE OF SERVICE

I hereby certify, pursuant to 37 C.F.R. §1. 915(b)(6), that on May 11, 2010, I caused a true and correct copy of the foregoing REQUEST FOR INTER PARTES REEXAMINATION UNDER 35 U.S.C. § 311 AND 37 C.F.R. § 1.913 to be served by First Class U.S. Mail on the following attorney of record for the purported patent owner:

Bruce S. Itchkawitz
KNOBBE MARTENS OLSON & BEAR LLP
2040 Main Street
Fourteenth Floor
Irvine, CA 92614

Date: 11 May 10

Hans R. Troesch
Reg. No. 36,950

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet | | of | |

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Jayesh R. Bhakta
Art Unit	
Examiner Name	
Attorney Docket Number	19473-0052RX1

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 7,289,386	10/30/2007	Bhakta et al.	
		US- 6,209,074	03/27/2001	Dell et al.	
		US- 6,414,868	07/02/2002	Wong et al.	
		US- 4,368,515	01/11/1983	Nielsen	
		US- 2006/0117152	06/01/2006	Amidi et al.	
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/08b (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet | | of | |

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Jayesh R. Bhakta
Art Unit	
Examiner Name	
Attorney Docket Number	19473-0052RX1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Barr, Michael, "Programmable Logic: What's it to Ya?," Embedded Systems Programming, June 1999, pp. 75-84.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

APPENDIX A

US007289386B2

(12) United States Patent
Bhakta et al.

(10) Patent No.: US 7,289,386 B2
(45) Date of Patent: Oct. 30, 2007

(54) **MEMORY MODULE DECODER**

(75) Inventors: **Jayesh R. Bhakta**, Cerritos, CA (US); **Jeffrey C. Solomon**, Irvine, CA (US)

(73) Assignee: **Netlist, Inc.**, Irvine, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 21 days.

(21) Appl. No.: **11/173,175**

(22) Filed: **Jul. 1, 2005**

(65) **Prior Publication Data**

US 2006/0062047 A1 Mar. 23, 2006

Related U.S. Application Data

(63) Continuation-in-part of application No. 11/075,395, filed on Mar. 7, 2005.

(60) Provisional application No. 60/588,244, filed on Jul. 15, 2004, provisional application No. 60/575,595, filed on May 28, 2004, provisional application No. 60/550,668, filed on Mar. 5, 2004.

(51) **Int. Cl.**
G11C 8/00 (2006.01)

(52) **U.S. Cl.** **365/230.06**; 365/51; 365/230.08

(58) **Field of Classification Search** 326/105; 365/230.06, 51, 52, 230.01, 230.03, 230.08; 711/5, 211
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,392,212 A * 7/1983 Miyasaka et al. 365/230.06
5,247,643 A 9/1993 Shottan
5,426,753 A * 6/1995 Moon 711/5
5,703,826 A 12/1997 Hush et al.
5,805,520 A 9/1998 Anglada et al.
5,959,930 A * 9/1999 Sakurai 365/230.03
6,154,418 A 11/2000 Li
6,453,381 B1 9/2002 Yuan et al.
6,518,794 B2 2/2003 Coteus et al.
6,681,301 B1 1/2004 Mehta et al.
6,785,189 B2 8/2004 Jacobs et al.
6,807,125 B2 10/2004 Coteus et al.
6,813,196 B2 11/2004 Park et al.

(Continued)

OTHER PUBLICATIONS

Barr, Michael. "Programmable Logic: What's it to Ya?," Embedded Systems Programming, Jun. 1999, pp. 75-84. Retrieved by Examiner from http://www.netrino.com/Articles/ProgrammableLogic/index.php.*

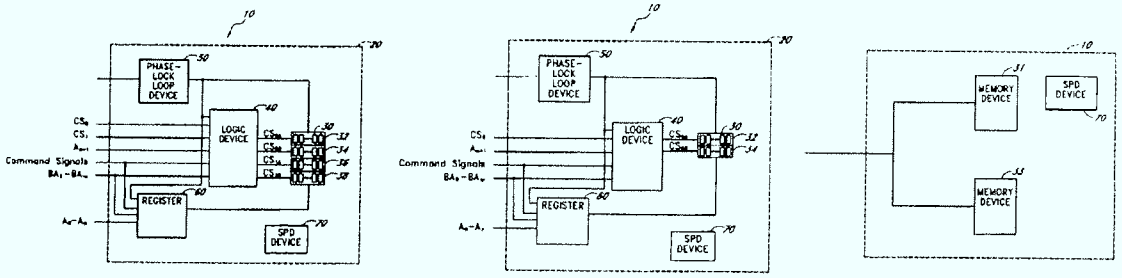
(Continued)

Primary Examiner—Son Dinh
Assistant Examiner—Alexander Sofocleous
(74) *Attorney, Agent, or Firm*– Knobbe Martens Olson & Bear LLP

(57) **ABSTRACT**

A memory module connectable to a computer system includes a printed circuit board, a plurality of memory devices coupled to the printed circuit board, and a logic element coupled to the printed circuit board. The plurality of memory devices has a first number of memory devices. The logic element receives a set of input control signals from the computer system. The set of input control signals corresponds to a second number of memory devices smaller than the first number of memory devices. The logic element generates a set of output control signals in response to the set of input control signals. The set of output control signals corresponds to the first number of memory devices.

13 Claims, 18 Drawing Sheets



U.S. PATENT DOCUMENTS

6,944,694	B2	9/2005	Pax	
6,981,089	B2 *	12/2005	Dodd et al.	710/308
6,982,893	B2 *	1/2006	Jakobs	365/63
6,996,686	B2	2/2006	Doblar et al.	
7,046,538	B2 *	5/2006	Kinsley et al.	365/52
7,120,727	B2 *	10/2006	Lee et al.	711/5
7,200,021	B2 *	4/2007	Raghuram	365/51
2001/0052057	A1	12/2001	Lai et al.	
2002/0088633	A1	7/2002	Kong et al.	
2003/0063514	A1	4/2003	Faue	
2003/0191995	A1	10/2003	Abrosimov et al.	
2003/0210575	A1	11/2003	Seo et al.	
2004/0037158	A1	2/2004	Coteus et al.	
2005/0036378	A1	2/2005	Kawaguchi et al.	
2005/0281096	A1	12/2005	Bhakta et al.	
2006/0126369	A1 *	6/2006	Raghuram	365/51
2006/0129755	A1 *	6/2006	Raghuram	711/105

OTHER PUBLICATIONS

Cuppu, Vinodh, et al., "A Performance Comparison of Contemporary DRAM Architectures," *IEEE Proceedings of the 26th International Symposium on Computer Architecture*, May 2-4, 1999, Atlanta, Georgia, pp. 1-12.

JEDEC Standard No. 21-C, 4.20-2—168 Pin, PC133 SDRAM Registered Design Specification, Revision 1.4, Release 11a, Feb. 2002.

JEDEC Standard No. 21-C, 4.20-3—144 Pin, PC133 SDRAM Unbuffered SO-DIMM, Reference Design Specification, Revision 1.02, Release 11.

JEDEC Standard No. 21-C, DDR SDRAM PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification, Revision 1.3, Release 11b, Jan. 2002.

JEDEC Standard No. 21-C, 4.20.5—184 Pin, PC1600/2100 DDR SDRAM Unbuffered DIMM Design Specification, Revision 1.1, Release 11b.

JEDEC Standard No. 21-C, 4.20.6—200 Pin, PC2700/PC2100/PC1600 DDR SDRAM Unbuffered SO-DIMM Reference Design Specification, Revision 1.1, Release 11b, Apr. 26, 2002.

JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification," published Feb. 2004.

Intel Corporation, PC SDRAM Registered DIMM Design Support Document, Revision 1.2, Oct. 1998.

Intel Corporation, 66/100 MHz PC SDRAM 64-Bit Non-ECC/Parity 144 Pin Unbuffered SO-DIMM Specification, Revision 1.0, Feb. 1999.

U.S. Appl. No. 11/173,175, filed Jul. 1, 2005, Bhakta et al.

* cited by examiner

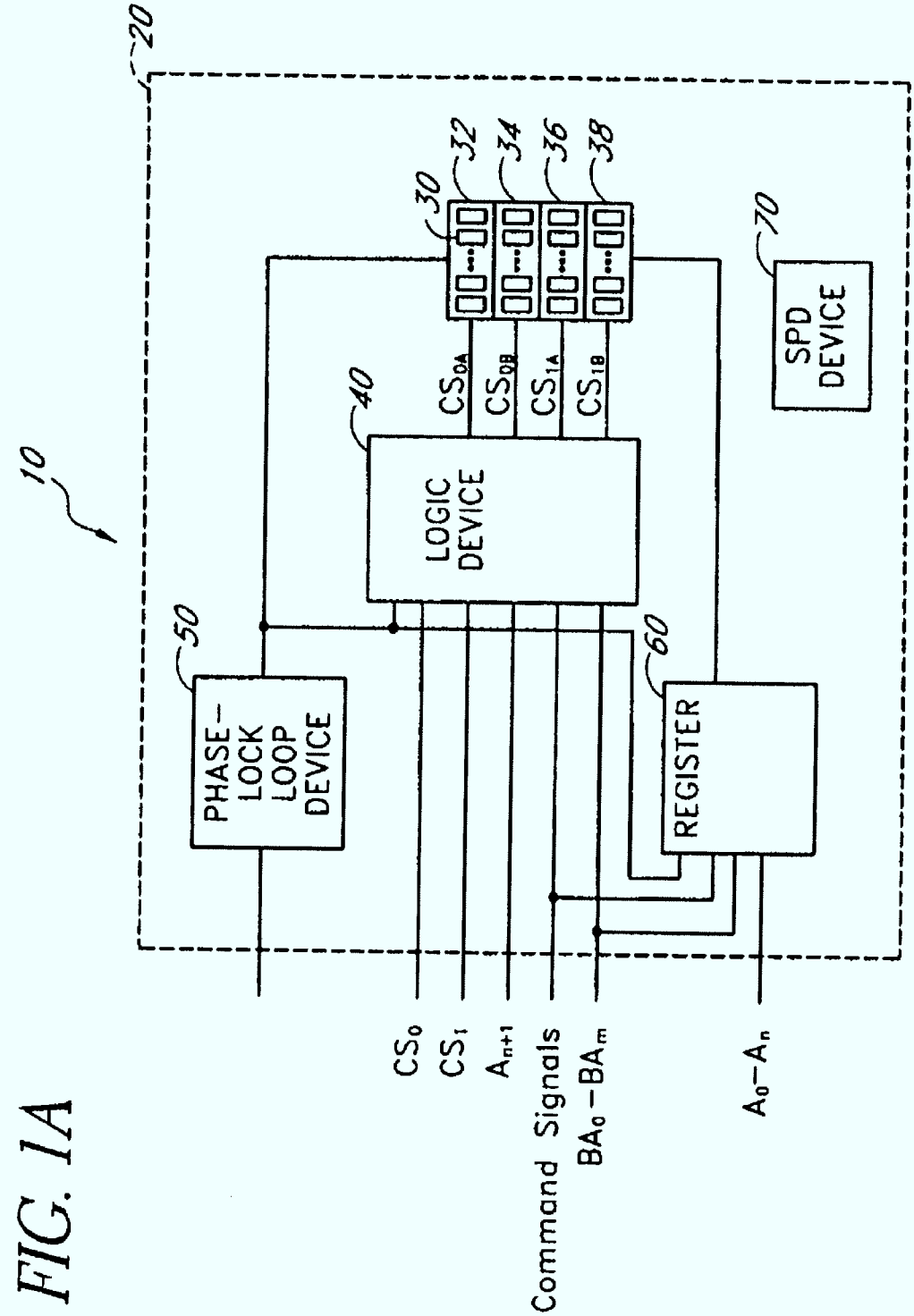

10
20
30
32
34
36
38
40
50
60
70
LOGIC DEVICE
PHASE-LOCK LOOP DEVICE
REGISTER
SPD DEVICE
CS_{0A}
CS_{0B}
CS_{1A}
CS_{1B}
CS_0
CS_1
A_{n+1}
Command Signals
$BA_0 - BA_m$
$A_0 - A_n$

FIG. 1A

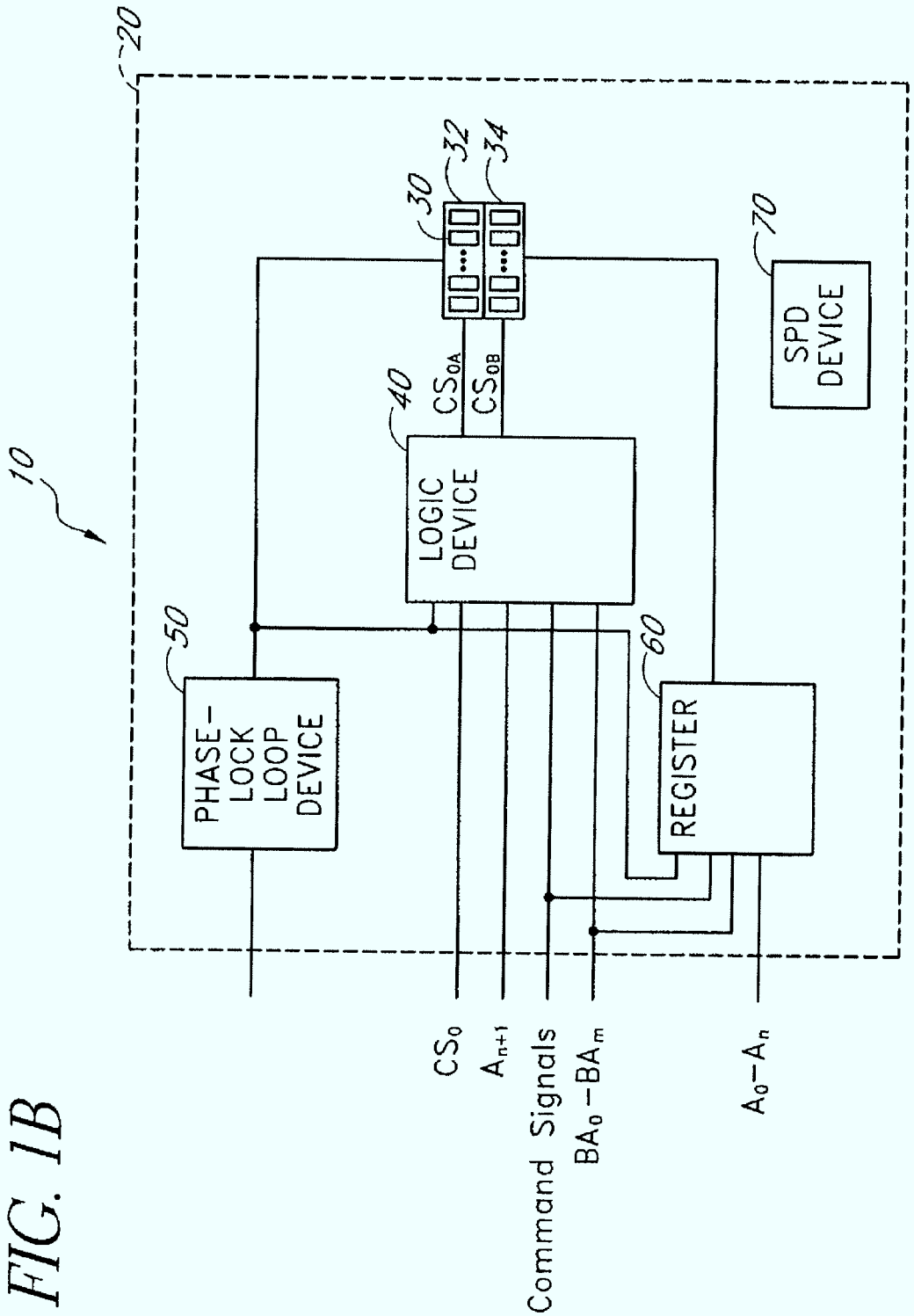

10
20
30
32
34
40
CS_{0A}
CS_{0B}
LOGIC DEVICE
50
PHASE-LOCK LOOP DEVICE
60
REGISTER
70
SPD DEVICE
CS_0
A_{n+1}
Command Signals
$BA_0 - BA_m$
$A_0 - A_n$

FIG. 1B

FIG. 1C

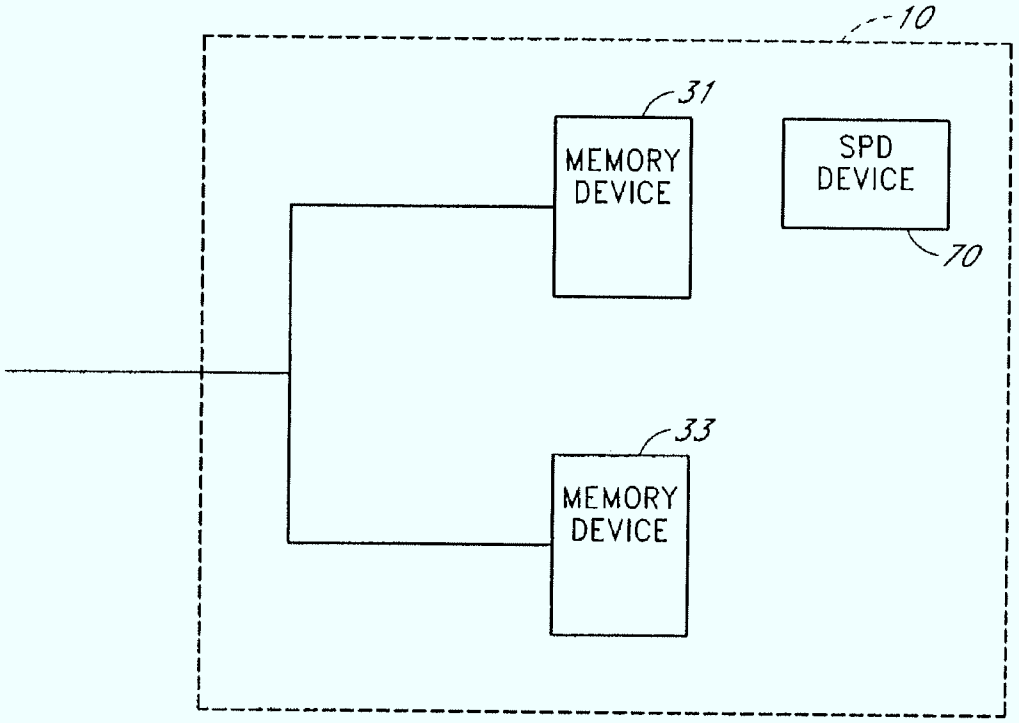


FIG. 2A

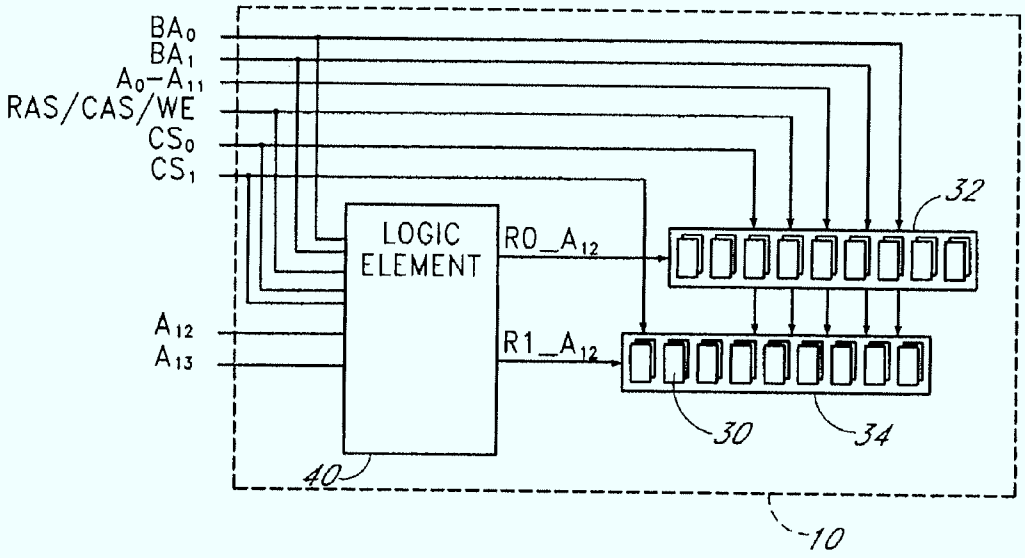

BA0
BA1
A0–A11
RAS/CAS/WE
CS0
CS1
A12
A13
LOGIC ELEMENT
R0_A12
R1_A12
32
30
34
40
10

FIG. 2B

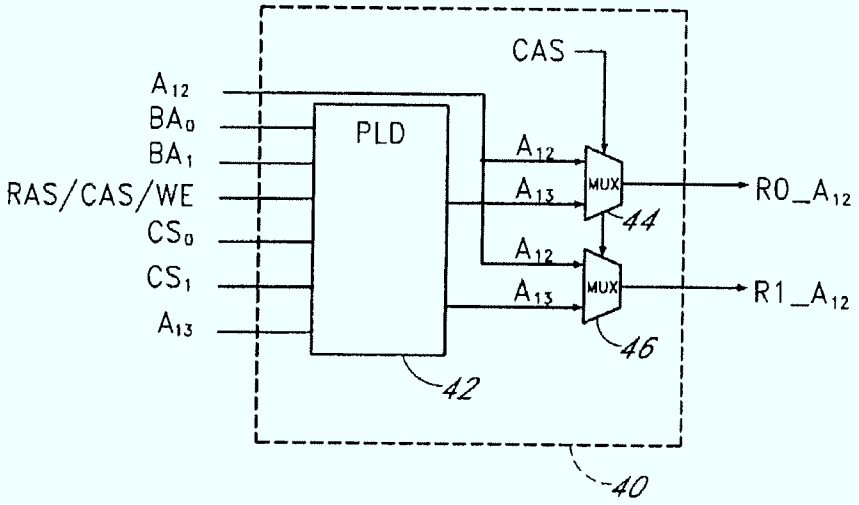

CAS
A12
BA0
BA1
RAS/CAS/WE
CS0
CS1
A13
PLD
A12
A13
MUX
44
A12
A13
MUX
46
R0_A12
R1_A12
42
40

FIG. 3A

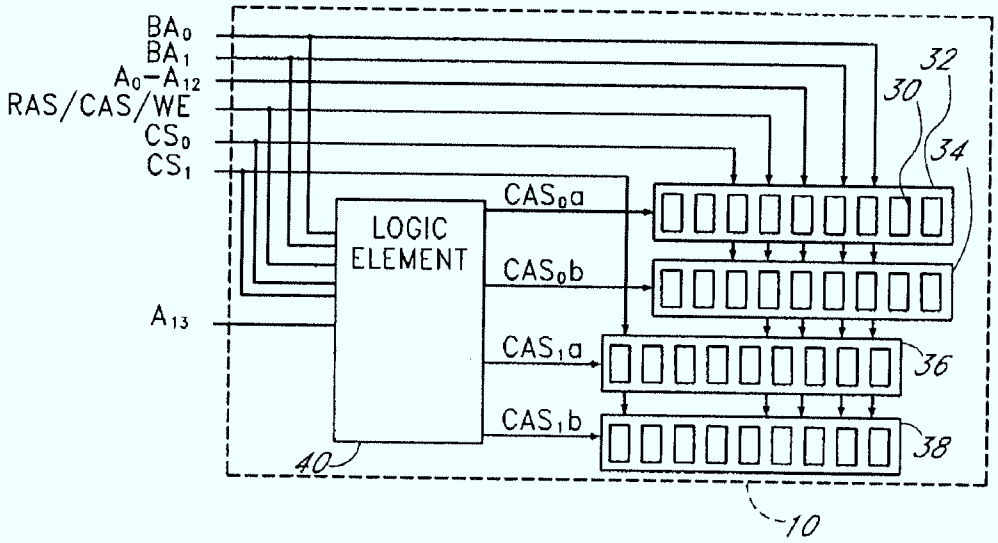
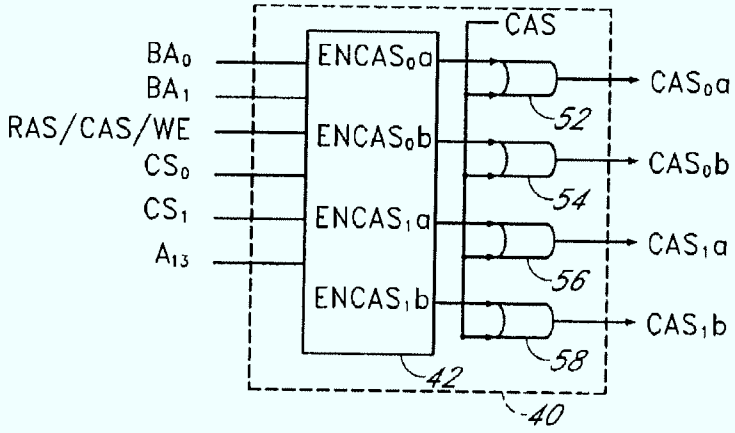

BA0
BA1
A0–A12
RAS/CAS/WE
CS0
CS1
A13
LOGIC ELEMENT
CAS0a
CAS0b
CAS1a
CAS1b
32
30
34
36
38
40
10

FIG. 3B


BA0
BA1
RAS/CAS/WE
CS0
CS1
A13
ENCAS0a
ENCAS0b
ENCAS1a
ENCAS1b
CAS
CAS0a
CAS0b
CAS1a
CAS1b
52
54
56
58
42
40

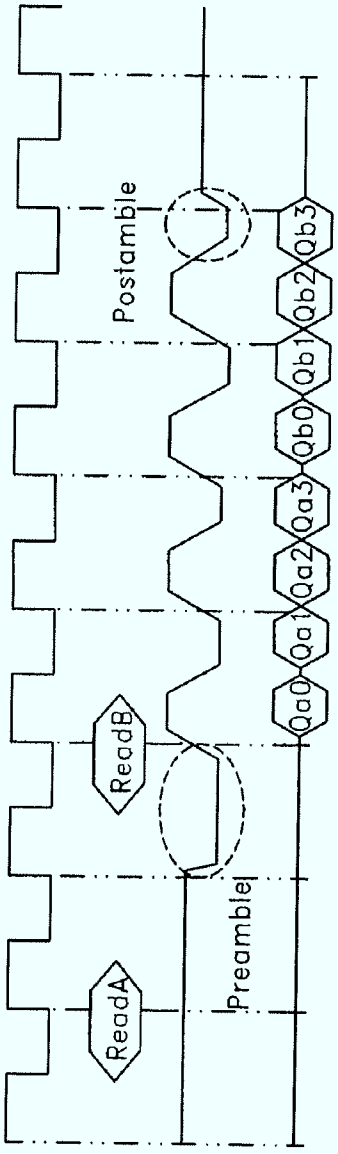

CK
Command
DQS
DQs
ReadA
ReadB
Preamble
Postamble
Qa0
Qa1
Qa2
Qa3
Qb0
Qb1
Qb2
Qb3

FIG. 4A

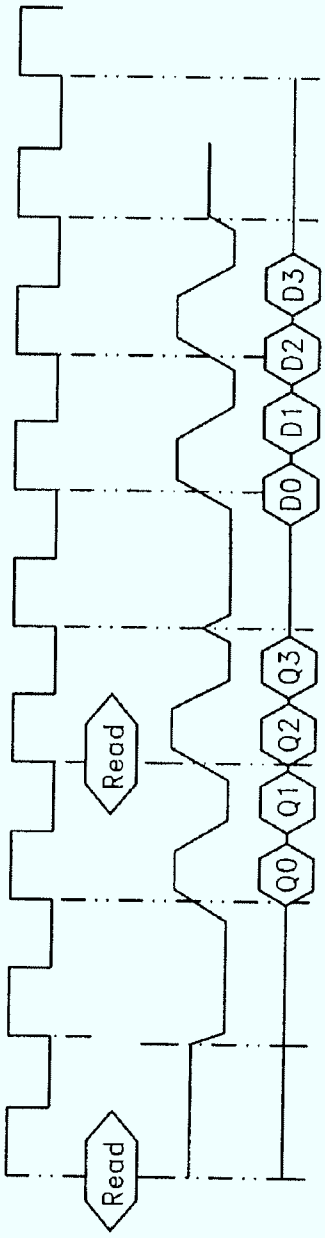

CK
Command
DQS
DQs
Read
Read
Q0
Q1
Q2
Q3
D0
D1
D2
D3

FIG. 4B

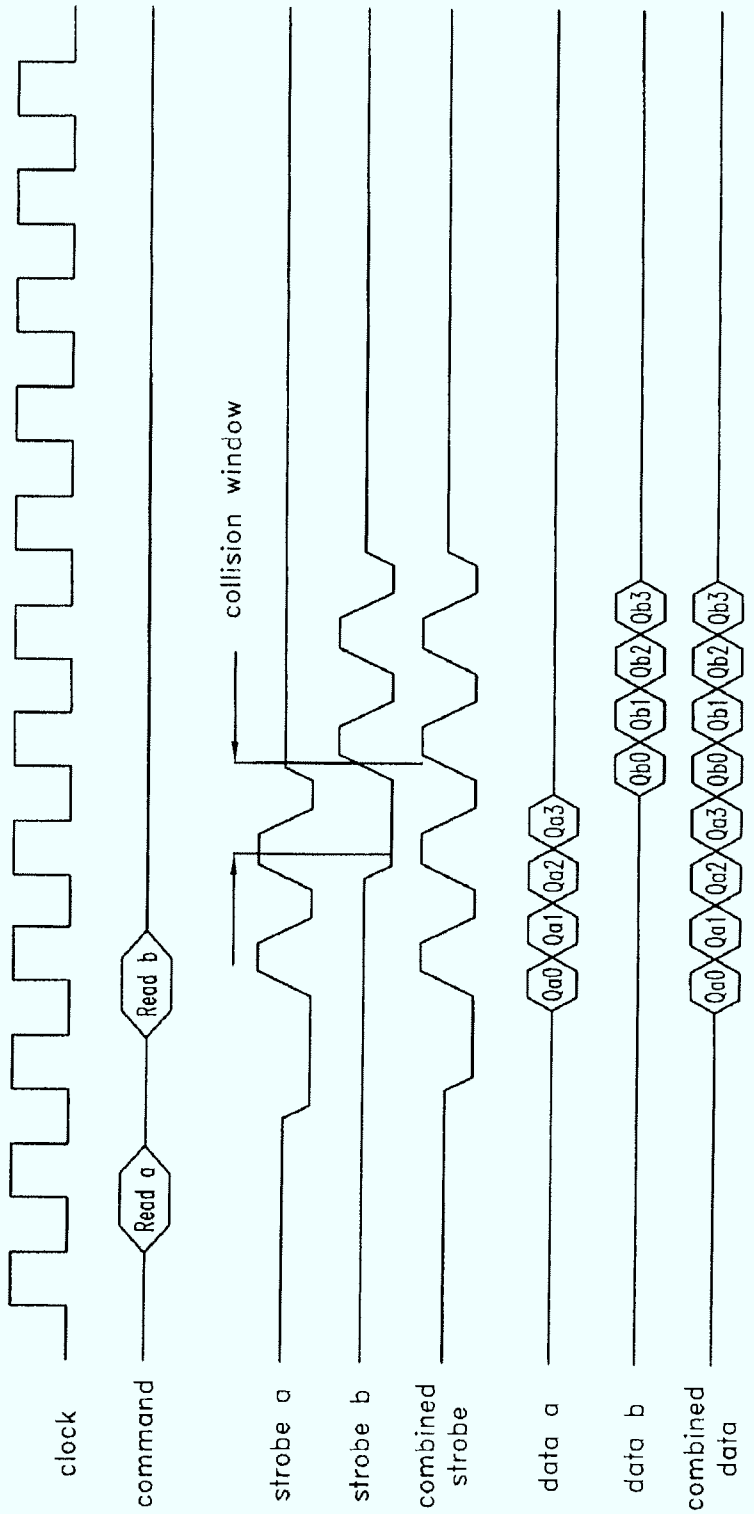

clock
command
Read a
Read b
collision window
strobe a
strobe b
combined strobe
data a
Qa0
Qa1
Qa2
Qa3
data b
Qb0
Qb1
Qb2
Qb3
combined data

FIG. 5

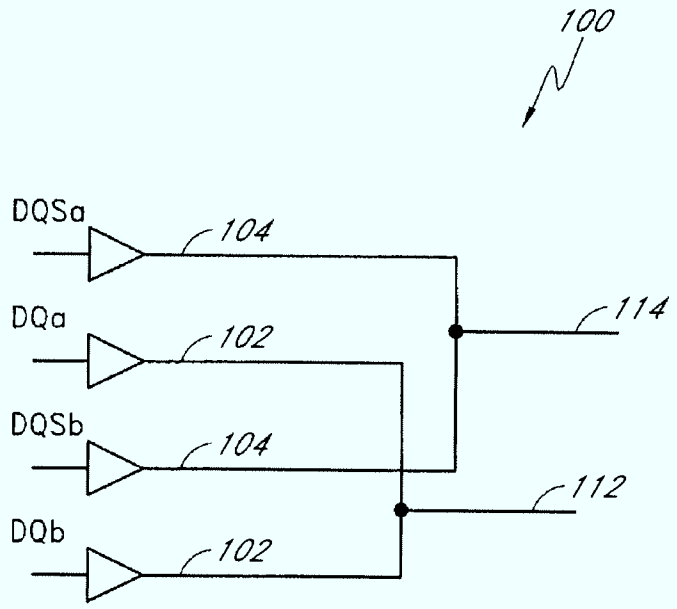

100
DQSa
104
DQa
102
DQSb
104
DQb
102
114
112

FIG. 6A

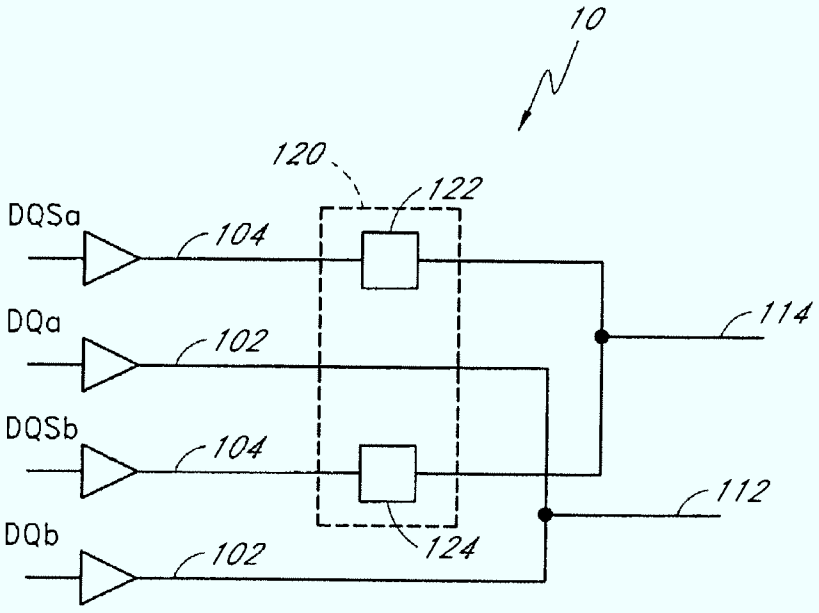

10
120
122
DQSa
104
DQa
102
DQSb
104
DQb
102
114
112
124

FIG. 6B

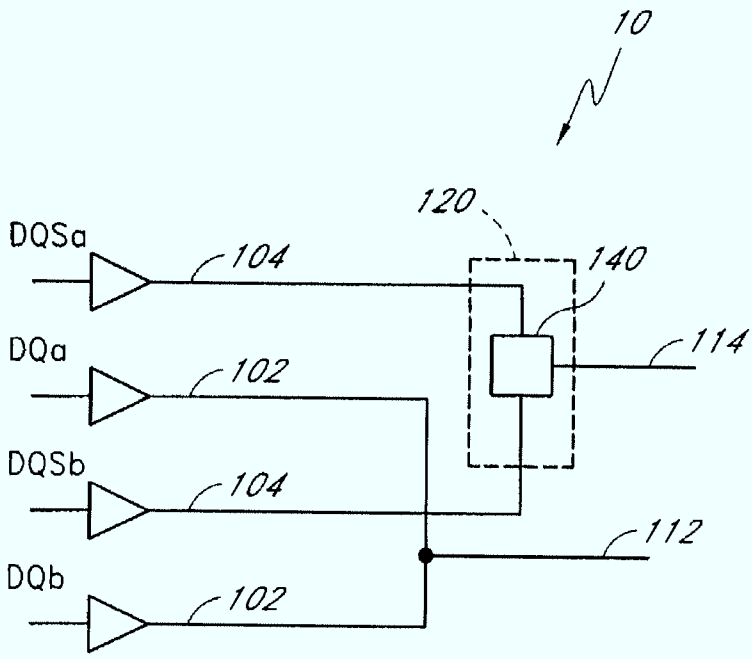

10
120
DQSa
104
140
DQa
102
114
DQSb
104
112
DQb
102

FIG. 6C

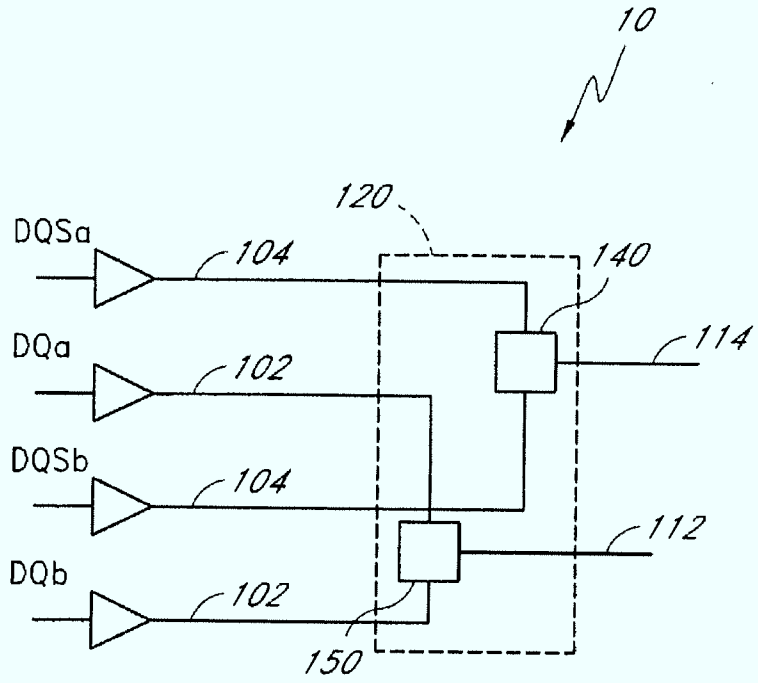

10
120
DQSa
104
140
DQa
102
114
DQSb
104
112
DQb
102
150

FIG. 6D

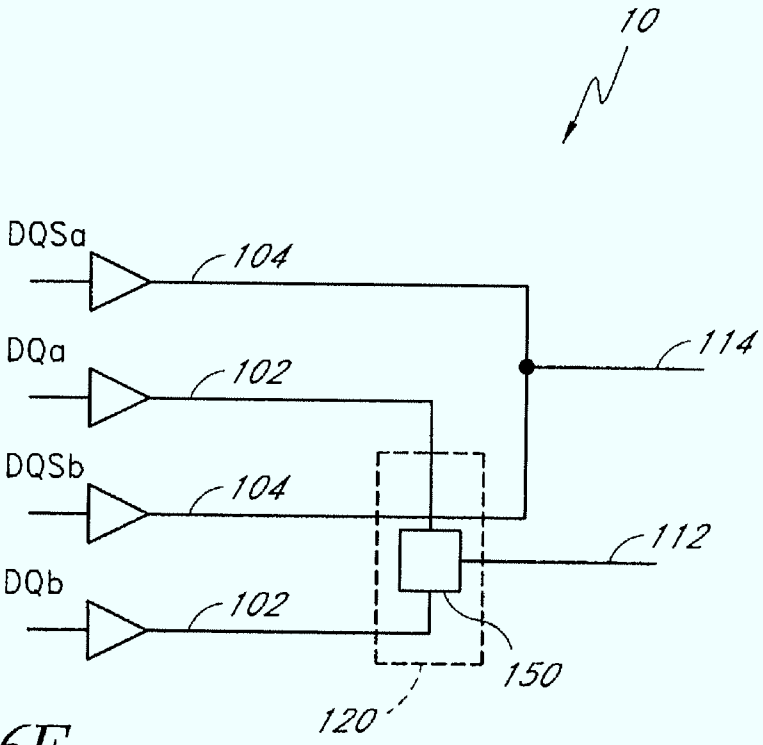


FIG. 6E

FIG. 7

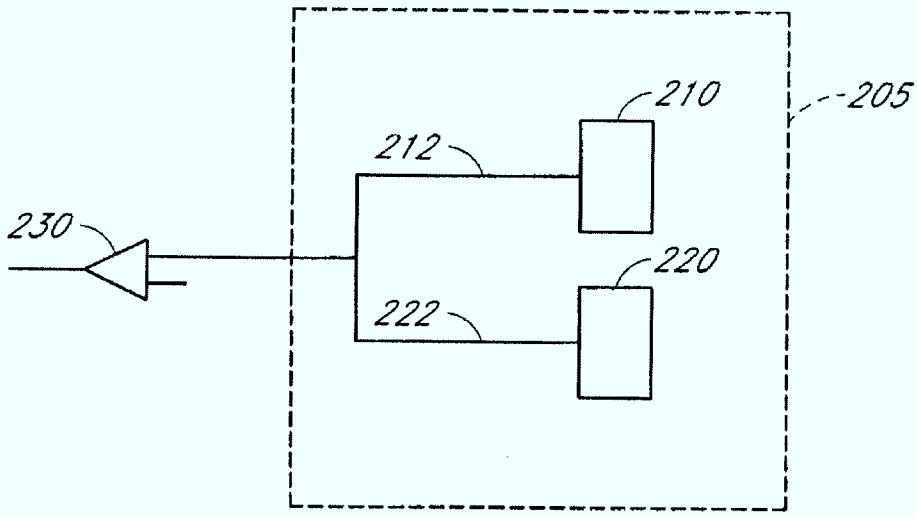


FIG. 8

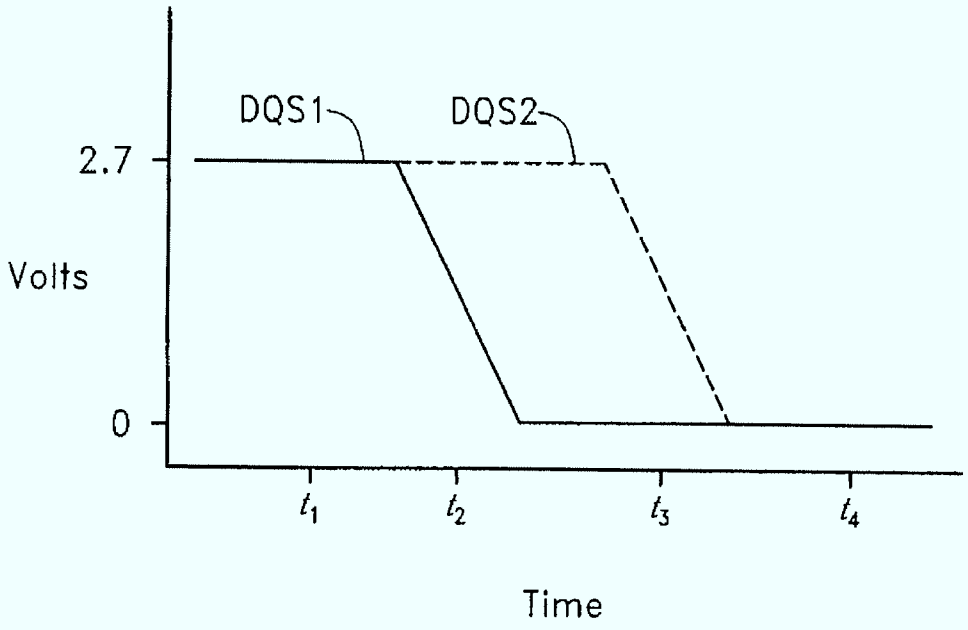


FIG. 9

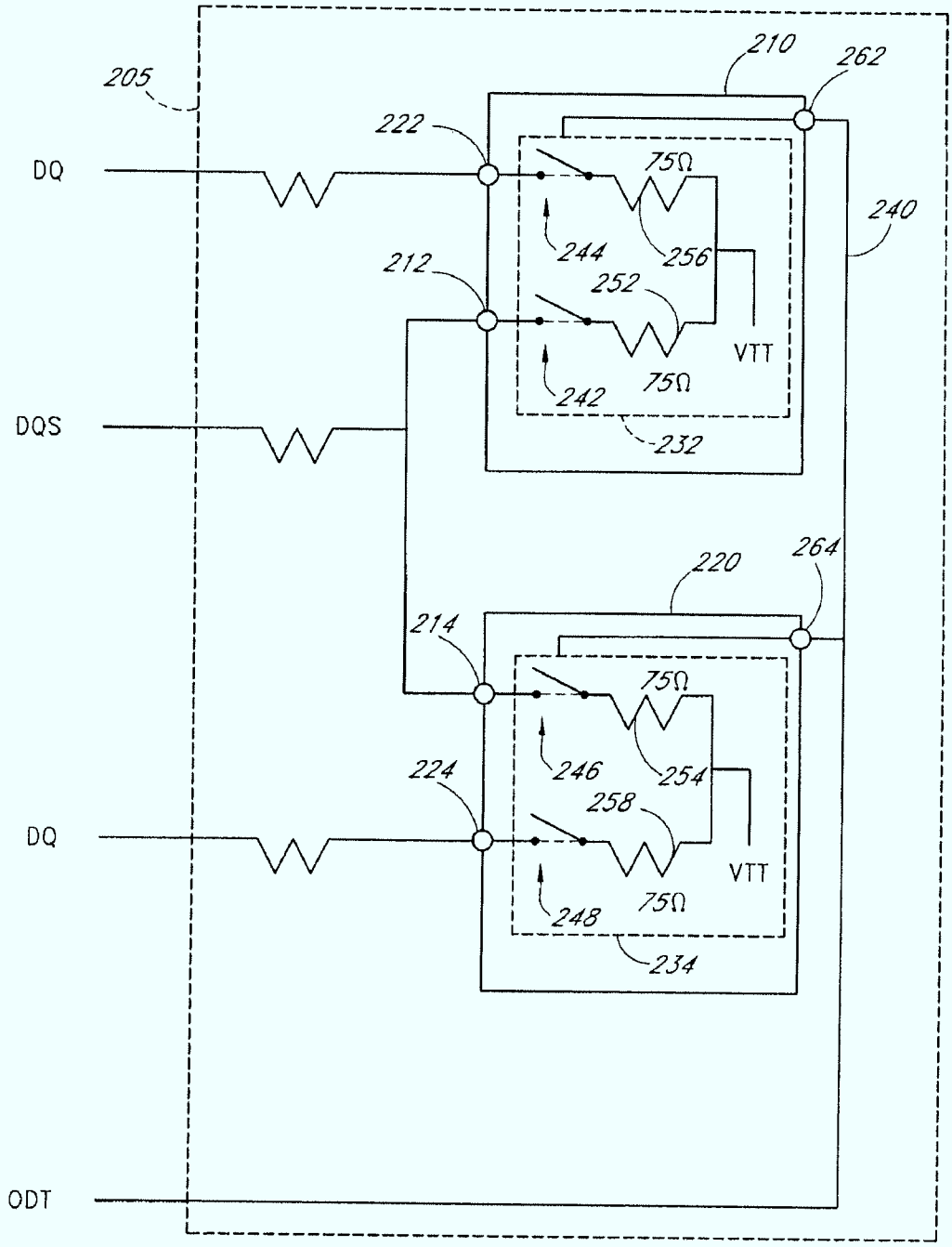

205
210
262
222
DQ
75Ω
240
244
256
212
252
VTT
DQS
242
75Ω
232
220
264
214
75Ω
246
254
224
258
DQ
VTT
75Ω
248
234
ODT

FIG. 10

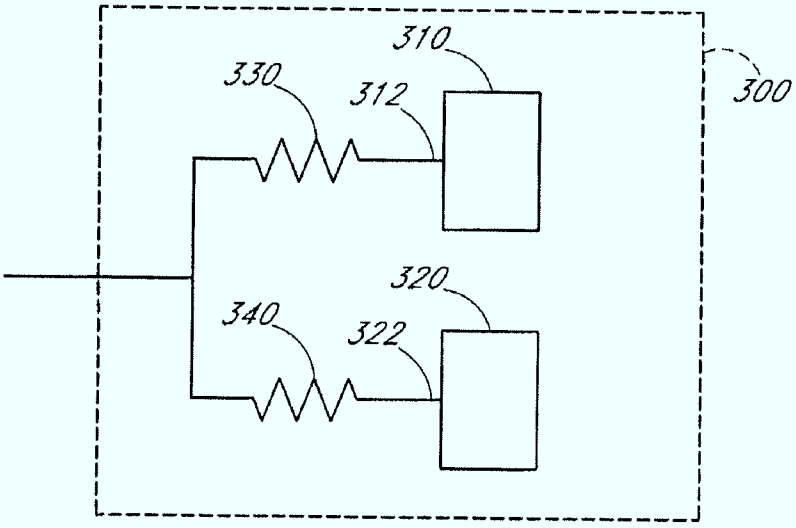


FIG. 11A

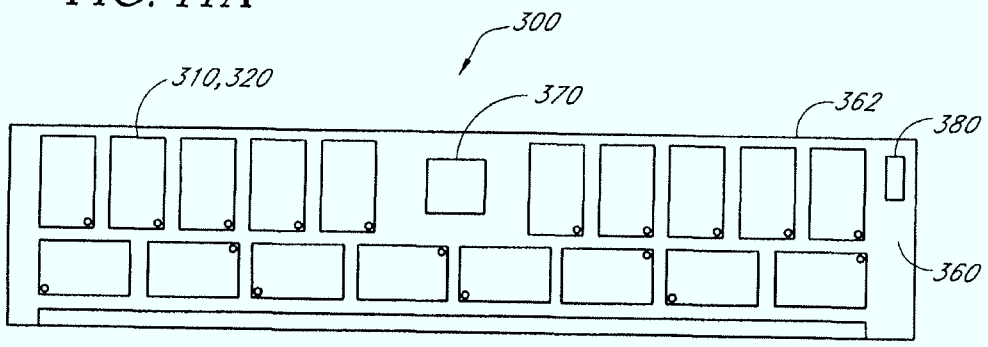


FIG. 11B

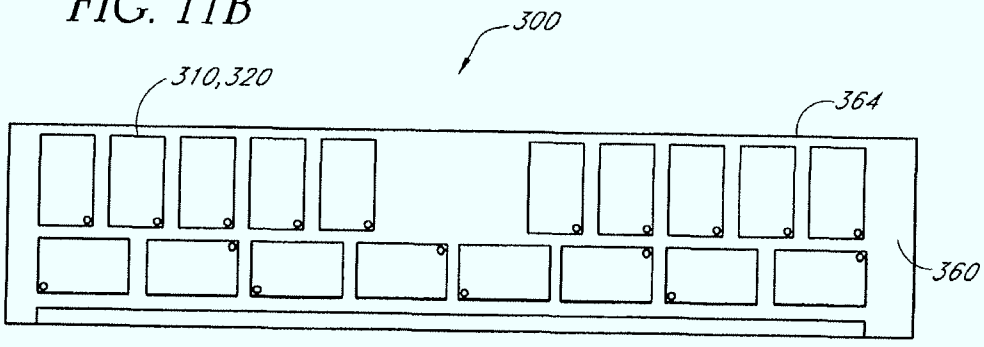


FIG. 12A

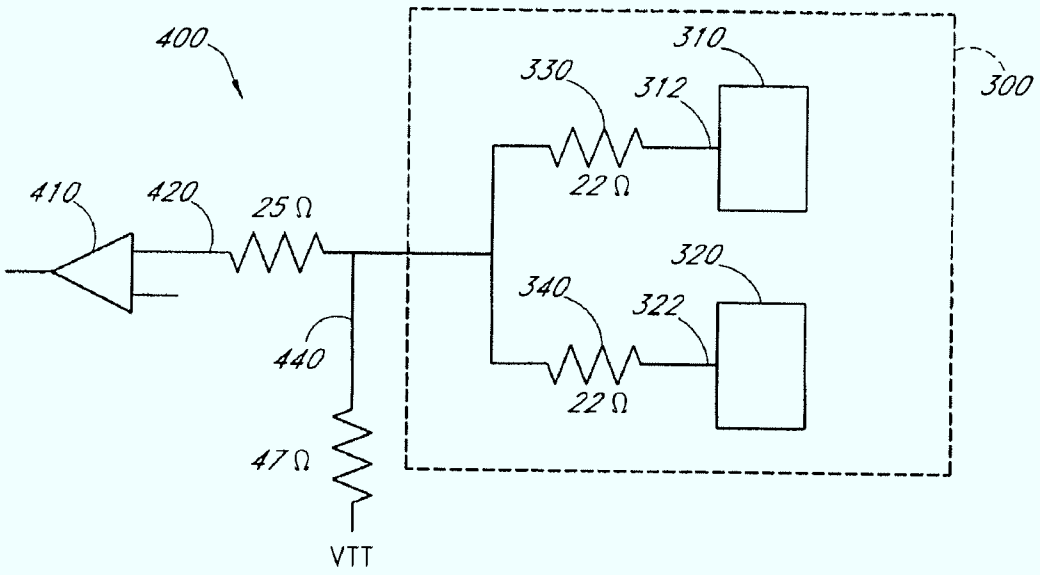


FIG. 12B

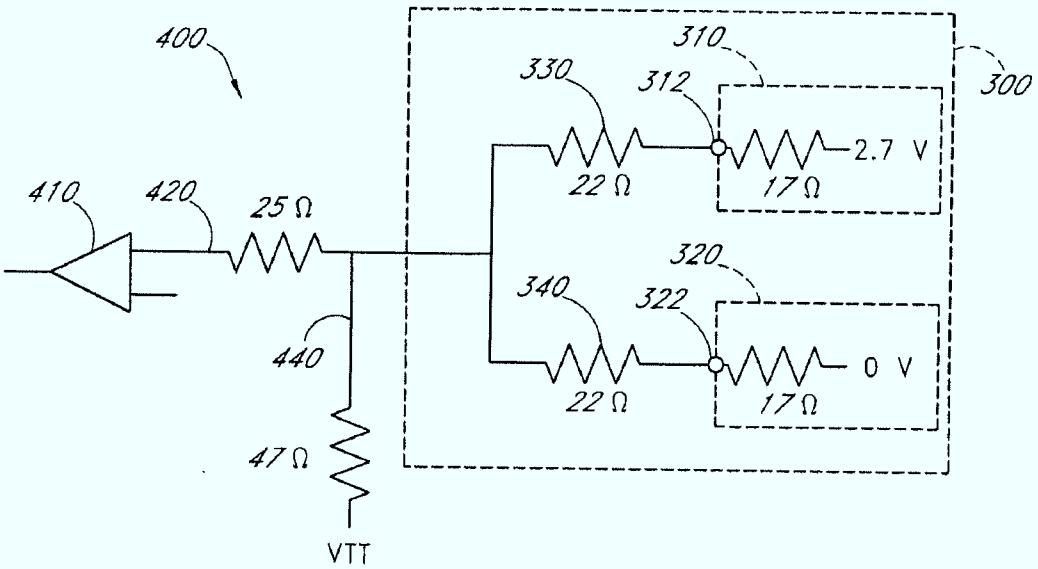


FIG. 13

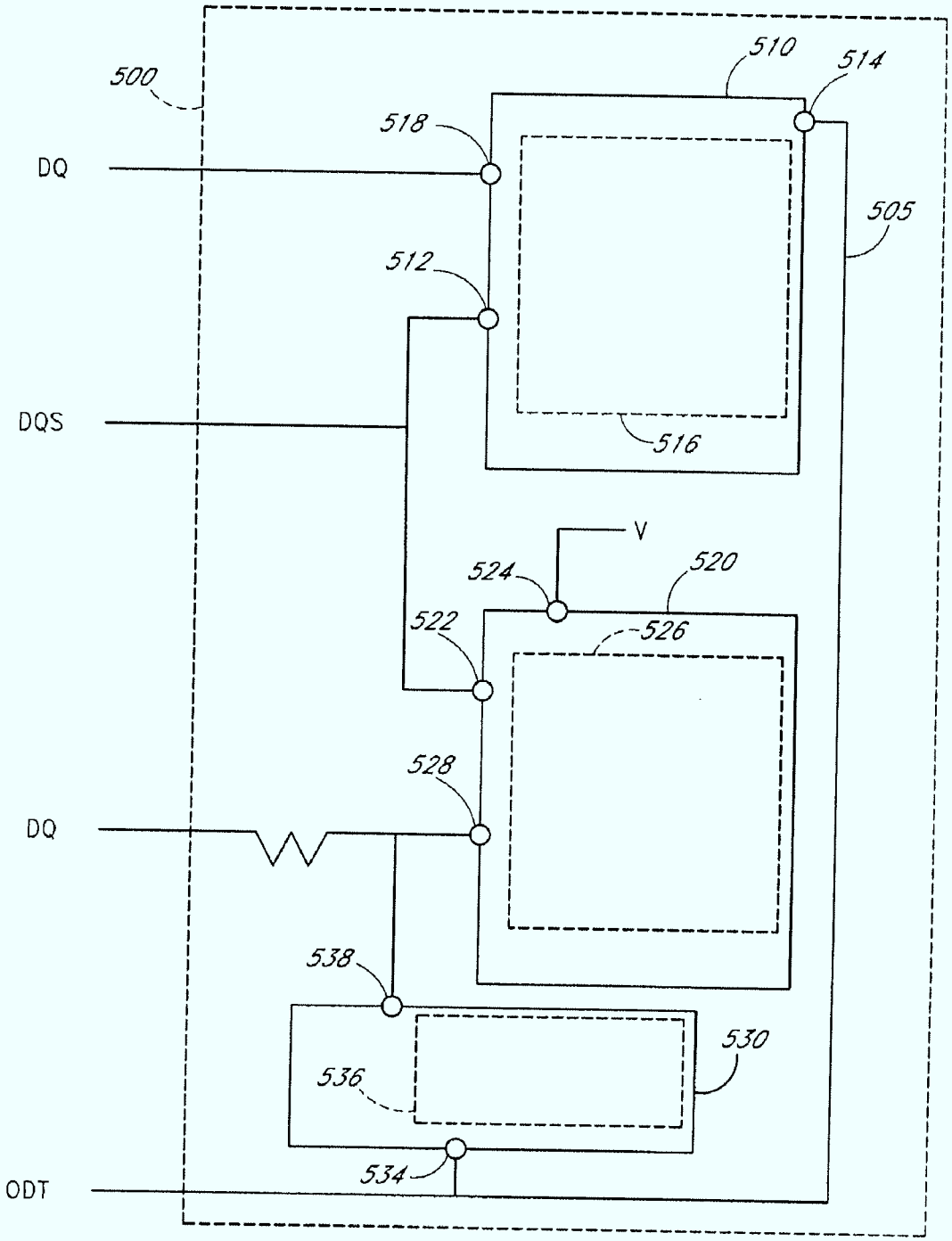
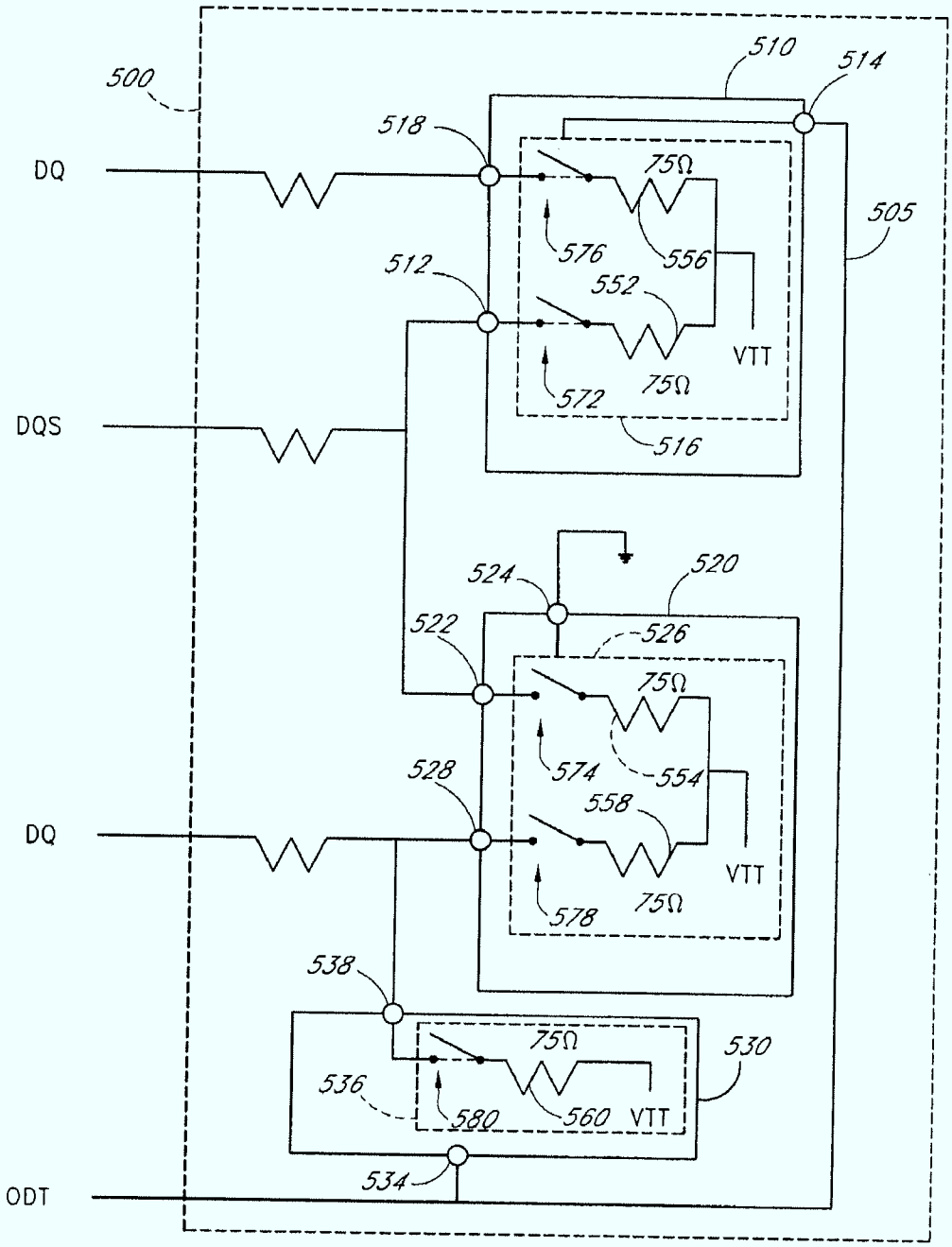

500
510
514
518
DQ
505
512
DQS
516
V
524
520
522
526
528
DQ
538
530
536
534
ODT

FIG. 14


500
510
514
518
DQ
75Ω
505
576
556
512
552
VTT
572
75Ω
DQS
516
524
520
522
526
75Ω
574
554
528
558
DQ
VTT
578
75Ω
538
75Ω
530
536
580
560
VTT
534
ODT

MEMORY MODULE DECODER

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application is a continuation-in-part of U.S. patent application Ser. No. 11/075,395, filed Mar. 7, 2005, which claims the benefit of U.S. Provisional Application No. 60/550,668, filed Mar. 5, 2004 and U.S. Provisional Application No. 60/575,595, filed May 28, 2004. The present application also claims the benefit of U.S. Provisional Application No. 60/588,244, filed Jul. 15, 2004, which is incorporated in its entirety by reference herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to memory modules of a computer system, and more specifically to devices and methods for improving the performance, the memory capacity, or both, of memory modules.

2. Description of the Related Art

Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the processor of the computer system. Memory modules typically have a memory configuration with a unique combination of rows, columns, and banks which result in a total memory capacity for the memory module.

For example, a 512-Megabyte memory module (termed a "512-MB" memory module, which actually has 2^{29} or 536,870,912 bytes of capacity) will typically utilize eight 512-Megabit DRAM devices (each identified as a "512-Mb" DRAM device, each actually having 2^{29} or 536,870,912 bits of capacity). The memory cells (or memory locations) of each 512-Mb DRAM device can be arranged in four banks, with each bank having an array of 2^{24} (or 16,777,216) memory locations arranged as 2^{13} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 64M 8-bit-wide memory locations (actually with four banks of 2^{27} or 134,217,728 one-bit memory cells arranged to provide a total of 2^{26} or 67,108,864 memory locations with 8 bits each) are identified as having a "64 Mb×8" or "64M×8-bit" configuration, or as having a depth of 64M and a bit width of 8. Furthermore, certain commercially-available 512-MB memory modules are termed to have a "64M×8-byte" configuration or a "64M×64-bit" configuration with a depth of 64M and a width of 8 bytes or 64 bits.

Similarly, a 1-Gigabyte memory module (termed a "1-GB" memory module, which actually has 2^{30} or 1,073,741,824 bytes of capacity) can utilize eight 1-Gigabit DRAM devices (each identified as a "1-Gb" DRAM device, each actually having 2^{30} or 1,073,741,824 bits of capacity). The memory locations of each 1-Gb DRAM device can be arranged in four banks, with each bank having an array of memory locations with 2^{14} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 128M 8-bit-wide memory locations (actually with a total of 2^{27} or 134,217,728 memory locations with 8 bits each) are identified as having a "128 Mb×8" or "128M×8-bit" configuration, or as having a depth of 128M and a bit width of 8. Furthermore, certain commercially-available 1-GB memory modules are identified as having a "128M×8-byte" configuration or a "128M×64-bit" configuration with a depth of 128M and a width of 8 bytes or 64 bits.

The commercially-available 512-MB (64M×8-byte) memory modules and the 1-GB (128M×8-byte) memory modules described above are typically used in computer systems (e.g., personal computers) which perform graphics applications since such "×8" configurations are compatible with data mask capabilities often used in such graphics applications. Conversely, memory modules with "×4" configurations are typically used in computer systems such as servers which are not as graphics-intensive. Examples of such commercially available "×4" memory modules include, but are not limited to, 512-MB (128M×4-byte) memory modules comprising eight 512-Mb (128 Mb×4) memory devices.

The DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width. For example, a memory module in which each rank of the memory module is 64 bits wide is described as having an "×64" organization. Similarly, a memory module having 72-bit-wide ranks is described as having an "×72" organization.

The memory capacity of a memory module increases with the number of memory devices. The number of memory devices of a memory module can be increased by increasing the number of memory devices per rank or by increasing the number of ranks. For example, a memory module with four ranks has double the memory capacity of a memory module with two ranks and four times the memory capacity of a memory module with one rank. Rather than referring to the memory capacity of the memory module, in certain circumstances, the memory density of the memory module is referred to instead.

During operation, the ranks of a memory module are selected or activated by control signals that are received from the processor. Examples of such control signals include, but are not limited to, rank-select signals, also called chip-select signals. Most computer and server systems support one-rank and two-rank memory modules. By only supporting one-rank and two-rank memory modules, the memory density that can be incorporated in each memory slot is limited.

SUMMARY OF THE INVENTION

In certain embodiments, a memory module is connectable to a computer system. The memory module comprises a printed circuit board, a plurality of memory devices coupled to the printed circuit board, and a logic element coupled to the printed circuit board. The plurality of memory devices has a first number of memory devices. The logic element receives a set of input control signals from the computer system. The set of input control signals corresponds to a second number of memory devices smaller than the first number of memory devices. The logic element generates a set of output control signals in response to the set of input control signals. The set of output control signals corresponds to the first number of memory devices.

In certain embodiments, a method utilizes a memory module in a computer system. The method comprises coupling the memory module to the computer system. The memory module comprises a plurality of memory devices arranged in a first number of ranks. The method further comprises inputting a first set of control signals to the memory module. The first set of control signals corresponds to a second number of ranks smaller than the first number of ranks. The method further comprises generating a second set

of control signals in response to the first set of control signals. The second set of control signals corresponds to the first number of ranks.

In certain embodiments, a memory module is connectable to a computer system. The memory module comprises a plurality of memory devices arranged in a first number of ranks. The memory module comprises means for coupling the memory module to the computer system. The memory module further comprises means for inputting a first set of control signals to the memory module. The first set of control signals corresponds to a second number of ranks smaller than the first number of ranks. The memory module further comprises means for generating a second set of control signals in response to the first set of control signals. The second set of control signals corresponds to the first number of ranks.

In certain embodiments, a memory module is connectable to a computer system. The memory module comprises a first memory device having a first data signal line and a first data strobe signal line. The memory module further comprises a second memory device having a second data signal line and a second data strobe signal line. The memory module further comprises a common data signal line connectable to the computer system. The memory module further comprises an isolation device electrically coupled to the first data signal line, to the second data signal line, and to the common data signal line. The isolation device selectively alternates between electrically coupling the first data signal line to the common data signal line and electrically coupling the second data signal line to the common data signal line.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1**A schematically illustrates an exemplary memory module with four ranks of memory devices compatible with certain embodiments described herein.

FIG. **1**B schematically illustrates an exemplary memory module with two ranks of memory devices compatible with certain embodiments described herein.

FIG. **1**C schematically illustrates another exemplary memory module in accordance with certain embodiments described herein.

FIG. **2**A schematically illustrates an exemplary memory module which doubles the rank density in accordance with certain embodiments described herein.

FIG. **2**B schematically illustrates an exemplary logic element compatible with embodiments described herein.

FIG. **3**A schematically illustrates an exemplary memory module which doubles number of ranks in accordance with certain embodiments described herein.

FIG. **3**B schematically illustrates an exemplary logic element compatible with embodiments described herein.

FIG. **4**A shows an exemplary timing diagram of a gapless read burst for a back-to-back adjacent read condition from one memory device.

FIG. **4**B shows an exemplary timing diagram with an extra clock cycle between successive read commands issued to different memory devices for successive read accesses from different memory devices.

FIG. **5** shows an exemplary timing diagram in which the last data strobe of memory device "a" collides with the pre-amble time interval of the data strobe of memory device "b."

FIG. **6**A schematically illustrates a circuit diagram of a conventional memory module showing the interconnections between the DQ data signal lines of two memory devices and their DQS data strobe signal lines.

FIG. **6**B schematically illustrates a circuit diagram of an exemplary memory module comprising an isolation device in accordance with certain embodiments described herein.

FIG. **6**C schematically illustrates an isolation device comprising a logic element which multiplexes the DQS data strobe signal lines from one another.

FIG. **6**D schematically illustrates an isolation device which multiplexes the DQS data strobe signal lines from one another and which multiplexes the DQ data signal lines from one another.

FIG. **6**E schematically illustrates an isolation device which comprises the logic element on the DQ data signal lines but not a corresponding logic element on the DQS data strobe signal lines.

FIG. **7** schematically illustrates an exemplary memory module in which a data strobe (DQS) pin of a first memory device is electrically connected to a DQS pin of a second memory device while both DQS pins are active.

FIG. **8** is an exemplary timing diagram of the voltages applied to the two DQS pins due to non-simultaneous switching.

FIG. **9** schematically illustrates another exemplary memory module in which a DQS pin of a first memory device is connected to a DQS pin of a second memory device.

FIG. **10** schematically illustrates an exemplary memory module in accordance with certain embodiments described herein.

FIGS. **11**A and **11**B schematically illustrate a first side and a second side, respectively, of a memory module with eighteen 64Mx4 bit, DDR-I SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board.

FIGS. **12**A and **12**B schematically illustrate an exemplary embodiment of a memory module in which a first resistor and a second resistor are used to reduce the current flow between the first DQS pin and the second DQS pin.

FIG. **13** schematically illustrates another exemplary memory module compatible with certain embodiments described herein.

FIG. **14** schematically illustrates a particular embodiment of the memory module schematically illustrated by FIG. **13**.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

Most high-density memory modules are currently built with 512-Megabit ("512-Mb") memory devices wherein each memory device has a 64Mx8-bit configuration. For example, a 1-Gigabyte ("1-GB") memory module with error checking capabilities can be fabricated using eighteen such 512-Mb memory devices. Alternatively, it can be economically advantageous to fabricate a 1-GB memory module using lower-density memory devices and doubling the number of memory devices used to produce the desired word width. For example, by fabricating a 1-GB memory module using thirty-six 256-Mb memory devices with 64Mx4-bit configuration, the cost of the resulting 1-GB memory module can be reduced since the unit cost of each 256-Mb memory device is typically lower than one-half the unit cost of each 512-Mb memory device. The cost savings can be significant, even though twice as many 256-Mb memory devices are used in place of the 512-Mb memory devices.

Market pricing factors for DRAM devices are such that higher-density DRAM devices (e.g., 1-Gb DRAM devices) are much more than twice the price of lower-density DRAM devices (e.g., 512-Mb DRAM devices). In other words, the

price per bit ratio of the higher-density DRAM devices is greater than that of the lower-density DRAM devices. This pricing difference often lasts for months or even years after the introduction of the higher-density DRAM devices, until volume production factors reduce the costs of the newer higher-density DRAM devices. Thus, when the cost of a higher-density DRAM device is more than the cost of two lower-density DRAM devices, there is an economic incentive for utilizing pairs of the lower-density DRAM devices to replace individual higher-density DRAM devices.

FIG. **1**A schematically illustrates an exemplary memory module **10** compatible with certain embodiments described herein. The memory module **10** is connectable to a computer system (not shown). The memory module **10** comprises a printed circuit board **20** and a plurality of memory devices **30** coupled to the printed circuit board **20**. The plurality of memory devices **30** has a first number of memory devices. The memory module **10** further comprises a logic element **40** coupled to the printed circuit board **20**. The logic element **40** receives a set of input control signals from the computer system. The set of input control signals correspond to a second number of memory devices smaller than the first number of memory devices. The logic element **40** generates a set of output control signals in response to the set of input control signals. The set of output control signals corresponds to the first number of memory devices.

In certain embodiments, as schematically illustrated in FIG. **1**A, the memory module **10** further comprises a phase-lock loop device **50** coupled to the printed circuit board **20** and a register **60** coupled to the printed circuit board **20**. In certain embodiments, the phase-lock loop device **50** and the register **60** are each mounted on the printed circuit board **20**. In response to signals received from the computer system, the phase-lock loop device **50** transmits clock signals to the plurality of memory devices **30**, the logic element **40**, and the register **60**. The register **60** receives and buffers a plurality of control signals, including address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals), and transmits corresponding signals to the appropriate memory devices **30**. In certain embodiments, the register **60** comprises a plurality of register devices. While the phase-lock loop device **50**, the register **60**, and the logic element **40** are described herein in certain embodiments as being separate components, in certain other embodiments, two or more of the phase-lock loop device **50**, the register **60**, and the logic element **40** are portions of a single component. Persons skilled in the art are able to select a phase-lock loop device **50** and a register **60** compatible with embodiments described herein.

In certain embodiments, the memory module **10** further comprises electrical components which are electrically coupled to one another and are surface-mounted or embedded on the printed circuit board **20**. These electrical components can include, but are not limited to, electrical conduits, resistors, capacitors, inductors, and transistors. In certain embodiments, at least some of these electrical components are discrete, while in other certain embodiments, at least some of these electrical components are constituents of one or more integrated circuits.

Various types of memory modules **10** are compatible with embodiments described herein. For example, memory modules **10** having memory capacities of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, as well as other capacities, are compatible with embodiments described herein. In addition, memory modules **10** having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. Furthermore, memory modules **10** compatible with embodiments described herein include, but are not limited to, single in-line memory modules (SIMMs), dual in-line memory modules (DIMMs), small-outline DIMMs (SO-DIMMs), unbuffered DIMMs (UDIMMs), registered DIMMs (RDIMMs), fully-buffered DIMM (FB-DIMM), mini-DIMMs, and micro-DIMMs.

In certain embodiments, the printed circuit board **20** is mountable in a module slot of the computer system. The printed circuit board **20** of certain such embodiments has a plurality of edge connections electrically coupled to corresponding contacts of the module slot and to the various components of the memory module **10**, thereby providing electrical connections between the computer system and the components of the memory module **10**.

Memory devices **30** compatible with embodiments described herein include, but are not limited to, random-access memory (RAM), dynamic random-access memory (DRAM), synchronous DRAM (SDRAM), and double-data-rate DRAM (e.g., DDR-1, DDR-2, DDR-3). In addition, memory devices **30** having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with embodiments described herein. Memory devices **30** compatible with embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μBGA), mini-BGA (mBGA), and chip-scale packaging (CSP). Memory devices **30** compatible with embodiments described herein are available from a number of sources, including but not limited to, Samsung Semiconductor, Inc. of San Jose, Calif., Infineon Technologies AG of San Jose, Calif., and Micron Technology, Inc. of Boise, Id. Persons skilled in the art can select appropriate memory devices **30** in accordance with certain embodiments described herein.

In certain embodiments, the plurality of memory devices **30** are arranged in a first number of ranks. For example, in certain embodiments, the memory devices **30** are arranged in four ranks, as schematically illustrated by FIG. **1**A. In other embodiments, the memory devices **30** are arranged in two ranks, as schematically illustrated by FIG. **1**B. Other numbers of ranks of the memory devices **30** are also compatible with embodiments described herein.

In certain embodiments, the logic element **40** comprises a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, or a complex programmable-logic device (CPLD). In certain embodiments, the logic element **40** is a custom device. Sources of logic elements **40** compatible with embodiments described herein include, but are not limited to, Lattice Semiconductor Corporation of Hillsboro, Oreg., Altera Corporation of San Jose, Calif., and Xilinx Incorporated of San Jose, Calif. In certain embodiments, the logic element **40** comprises various discrete electrical elements, while in certain other embodiments, the logic element **40** comprises one or more integrated circuits. Persons skilled in the art can select an appropriate logic element **40** in accordance with certain embodiments described herein.

As schematically illustrated by FIGS. **1**A and **1**B, in certain embodiments, the logic element **40** receives a set of input control signals, which includes address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select

signals) and command signals (e.g., refresh, precharge) from the computer system. In response to the set of input control signals, the logic element **40** generates a set of output control signals which includes address signals and command signals.

In certain embodiments, the set of output control signals corresponds to a first number of ranks in which the plurality of memory devices **30** of the memory module **10** are arranged, and the set of input control signals corresponds to a second number of ranks per memory module for which the computer system is configured. The second number of ranks in certain embodiments is smaller than the first number of ranks. For example, in the exemplary embodiment as schematically illustrated by FIG. **1**A, the first number of ranks is four while the second number of ranks is two. In the exemplary embodiment of FIG. **1**B, the first number of ranks is two while the second number of ranks is one. Thus, in certain embodiments, even though the memory module **10** actually has the first number of ranks of memory devices **30**, the memory module **10** simulates a virtual memory module by operating as having the second number of ranks of memory devices **30**. In certain embodiments, the memory module **10** simulates a virtual memory module when the number of memory devices **30** of the memory module **10** is larger than the number of memory devices **30** per memory module for which the computer system is configured to utilize.

In certain embodiments, the computer system is configured for a number of ranks per memory module which is smaller than the number of ranks in which the memory devices **30** of the memory module **10** are arranged. In certain such embodiments, the computer system is configured for two ranks of memory per memory module (providing two chip-select signals CS_0, CS_1) and the plurality of memory modules **30** of the memory module **10** are arranged in four ranks, as schematically illustrated by FIG. **1**A. In certain other such embodiments, the computer system is configured for one rank of memory per memory module (providing one chip-select signal CS_0) and the plurality of memory modules **30** of the memory module **10** are arranged in two ranks, as schematically illustrated by FIG. **1**B.

In the exemplary embodiment schematically illustrated by FIG. **1**A, the memory module **10** has four ranks of memory devices **30** and the computer system is configured for two ranks of memory devices per memory module. The memory module **10** receives row/column address signals or signal bits (A_0-A_{n+1}), bank address signals (BA_0-BA_m), chip-select signals (CS_0 and CS_1), and command signals (e.g., refresh, precharge, etc.) from the computer system. The A_0-A_n row/column address signals are received by the register **60**, which buffers these address signals and sends these address signals to the appropriate ranks of memory devices **30**. The logic element **40** receives the two chip-select signals (CS_0, CS_1) and one row/column address signal (A_{n+1}) from the computer system. Both the logic element **40** and the register **60** receive the bank address signals (BA_0-BA_m) and at least one command signal (e.g., refresh, precharge, etc.) from the computer system.

Logic Tables

Table 1 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices **30** using chip-select signals.

TABLE 1

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

Note:

1. Cs_0, CS_1, CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are active low signals.
2. A_{n+1} is an active high signal.
3. 'x' is a Don't Care condition.
4. Command involves a number of command signals that define operations such as refresh, precharge, and other operations.

In Logic State 1: CS_0 is active low, A_{n+1} is non-active, and Command is active. CS_{0A} is pulled low, thereby selecting Rank 0.

In Logic State 2: CS_0 is active low, A_{n+1} is active, and Command is active. CS_{0B} is pulled low, thereby selecting Rank 1.

In Logic State 3: CS_0 is active low, A_{n+1} is Don't Care, and Command is active high. CS_{0A} and CS_{0B} are pulled low, thereby selecting Ranks 0 and 1.

In Logic State 4: CS_1 is active low, A_{n+1} is non-active, and Command is active. CS_{1A} is pulled low, thereby selecting Rank 2.

In Logic State 5: CS_1 is active low, A_{n+1} is active, and Command is active. CS_{1B} is pulled low, thereby selecting Rank 3.

In Logic State 6: CS_1 is active low, A_{n+1} is Don't Care, and Command is active. CS_{1A} and CS_{1B} are pulled low, thereby selecting Ranks 2 and 3.

In Logic State 7: CS_0 and CS_1 are pulled non-active high, which deselects all ranks, i.e., CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are pulled high.

The "Command" column of Table 1 represents the various commands that a memory device (e.g., a DRAM device) can execute, examples of which include, but are not limited to, activation, read, write, precharge, and refresh. In certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of Table 1). In such embodiments, the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both associated ranks (e.g., state 6 of Table 1). In such embodiments, the command signal (e.g., refresh) is sent to both memory devices to ensure that the memory content of the memory devices remains valid over time. Certain embodiments utilize a logic table such as that of Table 1 to simulate a single memory device from two memory devices by selecting two ranks concurrently.

Table 2 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices **30** using gated CAS signals.

TABLE 2

CS*	RAS*	CAS*	WE*	Density Bit	A_{10}	Command	CAS0*	CAS1*
1	x	x	x	x	x	NOP	x	x
0	1	1	1	x	x	NOP	1	1
0	0	1	1	0	x	ACTIVATE	1	1
0	0	1	1	1	x	ACTIVATE	1	1
0	1	0	1	0	x	READ	0	1
0	1	0	1	1	x	READ	1	0
0	1	0	0	0	x	WRITE	0	1
0	1	0	0	1	x	WRITE	1	0
0	0	1	0	0	0	PRECHARGE	1	1
0	0	1	0	1	0	PRECHARGE	1	1
0	0	1	0	x	1	PRECHARGE	1	1
0	0	0	0	x	x	MODE REG SET	0	0
0	0	0	1	x	x	REFRESH	0	0

In certain embodiments in which the density bit is a row address bit, for read/write commands, the density bit is the value latched during the activate command for the selected bank.

Serial-Presence-Detect Device

Memory modules typically include a serial-presence detect (SPD) device **70** (e.g., an electrically-erasable-programmable read-only memory or EEPROM device) comprising data which characterize various attributes of the memory module, including but not limited to, the number of row addresses the number of column addresses, the data width of the memory devices, the number of ranks, the memory density per rank, the number of memory devices, and the memory density per memory device. The SPD device **70** communicates this data to the basic input/output system (BIOS) of the computer system so that the computer system is informed of the memory capacity and the memory configuration available for use and can configure the memory controller properly for maximum reliability and performance.

For example, for a commercially-available 512-MB (64M×8-byte) memory module utilizing eight 512-Mb memory devices each with a 64M×8-bit configuration, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

Byte **3**: Defines the number of row address bits in the DRAM device in the memory module [13 for the 512-Mb memory device].

Byte **4**: Defines the number of column address bits in the DRAM device in the memory module [11 for the 512-Mb memory device].

Byte **13**: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 512-Mb (64M×8-bit) memory device].

Byte **14**: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 512-Mb (64M×8-bit) memory device].

Byte **17**: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 512-Mb memory device].

In a further example, for a commercially-available 1-GB (128M×8-byte) memory module utilizing eight 1-Gb memory devices each with a 128M×8-bit configuration, as described above, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

Byte **3**: Defines the number of row address bits in the DRAM device in the memory module [14 for the 1-Gb memory device].

Byte **4**: Defines the number of column address bits in the DRAM device in the memory module [11 for the 1-Gb memory device].

Byte **13**: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 1-Gb (128M×8-bit) memory device].

Byte **14**: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 1-Gb (128M×8-bit) memory device].

Byte **17**: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 1-Gb memory device].

In certain embodiments, the SPD device **70** comprises data which characterize the memory module **10** as having fewer ranks of memory devices than the memory module **10** actually has, with each of these ranks having more memory density. For example, for a memory module **10** compatible with certain embodiments described herein having two ranks of memory devices **30**, the SPD device **70** comprises data which characterizes the memory module **10** as having one rank of memory devices with twice the memory density per rank. Similarly, for a memory module **10** compatible with certain embodiments described herein having four ranks of memory devices **30**, the SPD device **70** comprises data which characterizes the memory module **10** as having two ranks of memory devices with twice the memory density per rank. In addition, in certain embodiments, the SPD device **70** comprises data which characterize the memory module **10** as having fewer memory devices than the memory module **10** actually has, with each of these memory devices having more memory density per memory device. For example, for a memory module **10** compatible with certain embodiments described herein, the SPD device **70** comprises data which characterizes the memory module **10** as having one-half the number of memory devices that the memory module **10** actually has, with each of these memory devices having twice the memory density per memory device.

FIG. **1C** schematically illustrates an exemplary memory module **10** in accordance with certain embodiments described herein. The memory module **10** comprises a pair of substantially identical memory devices **31**, **33**. Each memory device **31**, **33** has a first bit width, a first number of banks of memory locations, a first number of rows of memory locations, and a first number of columns of memory locations. The memory module **10** further comprises an SPD device **70** comprising data that characterizes the pair of memory devices **31**, **33**. The data characterize the pair of memory devices **31**, **33** as a virtual memory device having a second bit width equal to twice the first bit width, a second

number of banks of memory locations equal to the first number of banks, a second number of rows of memory locations equal to the first number of rows, and a second number of columns of memory locations equal to the first number of columns.

In certain such embodiments, the SPD device **70** of the memory module **10** is programmed to describe the combined pair of lower-density memory devices **31**, **33** as one virtual or pseudo-higher-density memory device. In an exemplary embodiment, two 512-Mb memory devices, each with a 128Mx4-bit configuration, are used to simulate one 1-Gb memory device having a 128Mx8-bit configuration. The SPD device **70** of the memory module **10** is programmed to describe the pair of 512-Mb memory devices as one virtual or pseudo-1-Gb memory device.

For example, to fabricate a 1-GB (128Mx8-byte) memory module, sixteen 512-Mb (128Mx4-bit) memory devices can be used. The sixteen 512-Mb (128Mx4-bit) memory devices are combined in eight pairs, with each pair serving as a virtual or pseudo-1-Gb (128Mx8-bit) memory device. In certain such embodiments, the SPD device **70** contains the following SPD data (in appropriate bit fields of these bytes):

Byte **3**: 13 row address bits.

Byte **4**: 12 column address bits.

Byte **13**: 8 bits wide for the primary virtual 1-Gb (128Mx 8-bit) memory device.

Byte **14**: 8 bits wide for the error checking virtual 1-Gb (128Mx8-bit) memory device.

Byte **17**: 4 banks.

In this exemplary embodiment, bytes **3**, **4**, and **17** are programmed to have the same values as they would have for a 512-MB (128Mx4-byte) memory module utilizing 512-Mb (128Mx4-bit) memory devices. However, bytes **13** and **14** of the SPD data are programmed to be equal to 8, corresponding to the bit width of the virtual or pseudo-higher-density 1-Gb (128Mx8-bit) memory device, for a total capacity of 1-GB. Thus, the SPD data does not describe the actual-lower-density memory devices, but instead describes the virtual or pseudo-higher-density memory devices. The BIOS accesses the SPD data and recognizes the memory module as having 4 banks of memory locations arranged in 2^{13} rows and 2^{12} columns, with each memory location having a width of 8 bits rather than 4 bits.

In certain embodiments, when such a memory module **10** is inserted in a computer system, the computer system's memory controller then provides to the memory module **10** a set of input control signals which correspond to the number of ranks or the number of memory devices reported by the SPD device **70**. For example, placing a two-rank memory module **10** compatible with certain embodiments described herein in a computer system compatible with one-rank memory modules, the SPD device **70** reports to the computer system that the memory module **10** only has one rank. The logic element **40** then receives a set of input control signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output control signals corresponding to two ranks to the appropriate memory devices **30** of the memory module **10**. Similarly, when a two-rank memory module **10** compatible with certain embodiments described herein is placed in a computer system compatible with either one- or two-rank memory modules, the SPD device **70** reports to the computer system that the memory module **10** only has one rank. The logic element **40** then receives a set of input control signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output control signals corresponding to two ranks to the appropriate memory devices **30** of the memory module **10**. Furthermore, a four-rank memory module **10** compatible with certain embodiments described herein simulates a two-rank memory module whether the memory module **10** is inserted in a computer system compatible with two-rank memory modules or with two- or four-rank memory modules. Thus, by placing a four-rank memory module **10** compatible with certain embodiments described herein in a module slot that is four-rank-ready, the computer system provides four chip-select signals, but the memory module **10** only uses two of the chip-select signals.

Memory Density Multiplication

In certain embodiments, two memory devices having a memory density are used to simulate a single memory device having twice the memory density, and an additional address signal bit is used to access the additional memory. Similarly, in certain embodiments, two ranks of memory devices having a memory density are used to simulate a single rank of memory devices having twice the memory density, and an additional address signal bit is used to access the additional memory. As used herein, such simulations of memory devices or ranks of memory devices are termed as "memory density multiplication," and the term "density transition bit" is used to refer to the additional address signal bit which is used to access the additional memory.

In certain embodiments utilizing memory density multiplication embodiments, the memory module **10** can have various types of memory devices **30** (e.g., DDR1, DDR2, DDR3, and beyond). The logic element **40** of certain such embodiments utilizes implied translation logic equations having variations depending on whether the density transition bit is a row, column, or internal bank address bit. In addition, the translation logic equations of certain embodiments vary depending on the type of memory module **10** (e.g., UDIMM, RDIMM, FBDIMM, etc.). Furthermore, in certain embodiments, the translation logic equations vary depending on whether the implementation multiplies memory devices per rank or multiplies the number of ranks per memory module.

Table 3A provides the numbers of rows and columns for DDR-1 memory devices, as specified by JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification," published February 2004, and incorporated in its entirety by reference herein.

TABLE 3A

	128-Mb	256-Mb	512-Mb	1-Gb
Number of banks	4	4	4	4
Number of row address bits	12	13	13	14
Number of column address bits for "x4" configuration	11	11	12	12
Number of column address bits for "x8" configuration	10	10	11	11
Number of column address bits for "x16" configuration	9	9	10	10

As described by Table 3A, 512-Mb (128Mx4-bit) DRAM devices have 2^{13} rows and 2^{12} columns of memory locations, while 1-Gb (128Mx8-bit) DRAM devices have 2^{14} rows and 2^{11} columns of memory locations. Because of the differences in the number of rows and the number of columns for the two types of memory devices, complex address translation procedures and structures would typically be needed to fabricate a 1-GB (128Mx8-byte) memory module using sixteen 512-Mb (128Mx4-bit) DRAM devices.

Table 3B shows the device configurations as a function of memory density for DDR2 memory devices.

TABLE 3B

	Number of Rows	Number of Columns	Number of Internal Banks	Page Size (×4s or ×8s)
256 Mb	13	10	4	1 KB
512 Mb	14	10	4	1 KB
1 Gb	14	10	8	1 KB
2 Gb	15	10	8	1 KB
4 Gb	to be determined	to be determined	8	1 KB

Table 4 lists the corresponding density transition bit for the density transitions between the DDR2 memory densities of Table 3B.

TABLE 4

Density Transition	Density Transition Bit
256 Mb to 512 Mb	A_{13}
512 Mb to 1 Gb	BA_2
1 Gb to 2 Gb	A_{14}
2 Gb to 4 Gb	to be determined

Because the standard memory configuration of 4-Gb DDR2 SDRAM modules is not yet determined by the appropriate standards-setting organization, Tables 3B and 4 have "to be determined" in the appropriate table entries.

In certain embodiments, the logic translation equations are programmed in the logic element **40** by hardware, while in certain other embodiments, the logic translation equations are programmed in the logic element **40** by software. Examples 1 and 2 provide exemplary sections of Verilog code compatible with certain embodiments described herein. As described more fully below, the code of Examples 1 and 2 includes logic to reduce potential problems due to "back-to-back adjacent read commands which cross memory device boundaries or "BBARX." Persons skilled in the art are able to provide additional logic translation equations compatible with embodiments described herein.

An exemplary section of Verilog code compatible with memory density multiplication from 512 Mb to 1 Gb using DDR2 memory devices with the BA_2 density transition bit is listed below in Example 1. The exemplary code of Example 1 corresponds to a logic element **40** which receives one chip-select signal from the computer system and which generates two chip-select signals.

EXAMPLE 1

```
always @(posedge clk_in)
  begin
    rs0N_R <= rs0_in_N;      // cs0
    rasN_R <= ras_in_N;
    casN_R <= cas_in_N;
    weN_R <= we_in_N;
  end
// Gated Chip Selects
assign   pcs0a_1 = (~rs0_in_N & ~ras_in_N & ~cas_in_N)                          // ref,rnd reg set
         | (~rs0_in_N & ras_in_N & cas_in_N)                                    // ref exit, pwr dn
         | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in)               // pchg all
         | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ~ba2_in)// pchg single bnk
         | (~rs0_in_N & ~ras_in_N & cas_in_N & we_in_N      & ~ba2_in) // activate
         | (~rs0_in_N & ras_in_N & ~cas_in_N      & ~ba2_in)                    // xfr
         ;
assign   pcs0b_1 = (~rs0_in_N & ~ras_in_N & ~cas_in_N)                          // ref,rnd reg set
         | (~rs0_in_N & ras_in_N & cas_in_N)                                    // ref exit, pwr dn
         | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in)               // pchg all
         | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ba2_in)// pchg single bnk
         | (~rs0_in_N & ~ras_in_N & cas_in_N & we_in_N      & ba2_in)  // activate
         | (~rs0_in_N & ras_in_N & ~cas_in_N      & ba2_in)                     // xfr
         ;
//-------------------------------------
 always @(posedge_clk_in)
  begin
    a4_r <= a4_in ;
    a5_r <= a5_in ;
    a6_r <= a6_in ;
    a10_r <= a10_in ;
    ba0_r <= ba0 _in ;
    ba1_r <= ba1_in ;
    ba2_r <= ba2_in ;
    q_mrs_cmd_cyc1 <= q_mrs_cmd ;
  end
////////////////////////////////////////////////////////////////
// determine the cas latency
////////////////////////////////////////////////////////////////
assign q_mrs_cmd_r = (!rasN_R & !casN_R & !weN_R)
    & !rs0N_R
```

-continued

```
    & (!ba0_r & !ba1_r)
    ;       // md reg set cmd
  always @(posedge clk_in)
   if (~reset_N)       // lmr
     cl3 <= 1 'b1 ;
   else if (q_mrs_cmd_cyc1)       // load mode reg cmd
   begin
     cl3 <= (~a6_r & a5_r & a4_r ) ;
   end
  always @(posedge clk_in)
   if (~reset_N)       // reset
     cl2 <= 1 'b0 ;
   else if (q_mrs_cmd_cyc1)       // load mode reg cmd
   begin
     cl2 <= (~a6_r & a5_r & ~a4_r ) ;
   end
 always @(posedge clk_in)
   if (~reset_N)       // reset
     cl4 <= 1 'b0 ;
   else if (q_mrs_cmd_cyc1)       // load mode reg cmd
   begin
     cl4 <= (a6_r & ~a5_r & ~a4_r ) ;
   end
 always @(posedge clk_in)
   if (~reset_N)       cl5 <= 1 'b0 ;
   else if (q_mrs_cmd_cyc1)       // load mode reg cmd
   begin
     cl5 <= (a6_r & ~a5_r & a4_r ) ;
   end
 assign    pre_cyc2_enfet = (wr_cmd_cyc1 & acs_cyc1 & cl3)   // wr brst cl3 preamble
               ;
 assign    pre_cyc3_enfet = (rd_cmd_cyc2 & cl3)              // rd brst cl3 preamble
               | (wr_cmd_cyc2 & cl3)                         // wr brst cl3 1st pair
               | (wr_cmd_cyc2 & cl4)                         // wr brst cl4 preamble
               ;
 assign    pre_cyc4_enfet = (wr_cmd_cyc3 & cl3)              // wr brst cl3 2nd pair
               | (wr_cmd_cyc3 & cl4)                         // wr brst cl4 1st pair
               | (rd_cmd_cyc3 & cl3)                         // rd brst cl3 1st pair
               | (rd_cmd_cyc3 & cl4)                         // rd brst cl4 preamble
               ;
 assign    pre_cyc5_enfet = (rd_cmd_cyc4 & cl3)              // rd brst cl3 2nd pair
               | (wr_cmd_cyc4 & cl4)                         // wr brst cl4 2nd pair
               | (rd_cmd_cyc4 & cl4)                         // rd brst cl4 1st pair
               ;
// dq
 assign    pre_dq_cyc = pre_cyc2_enfet
               | pre_cyc3_enfet
               | pre_cyc4_enfet
               | pre_cyc5_enfet
               ;
 assign    pre_dq_ncyc = enfet_cyc2
               | enfet_cyc3
               | enfet_cyc4
               | enfet_cyc5
               ;
// dqs
 assign    pre_dqsa_cyc = (pre_cyc2_enfet & ~ba2_r)
               | (pre_cyc3_enfet & ~ba2_cyc2)
               | (pre_cyc4_enfet & ~ba2_cyc3)
               | (pre_cyc5_enfet & ~ba2_cyc4)
               ;
 assign    pre_dqsb_cyc = (pre_cyc2_enfet & ba2_r)
               | (pre_cyc3_enfet & ba2_cyc2)
               | (pre_cyc4_enfet & ba2_cyc3)
               | (pre_cyc5_enfet & ba2_cyc4)
               ;
 assign    pre_dqsa_ncyc = (enfet_cyc2 & ~ba2_cyc2)
               | (enfet_cyc3 & ~ba2_cyc3)
               | (enfet_cyc4 & ~ba2_cyc4)
               | (enfet_cyc5 & ~ba2_cyc5)
               ;
 assign    pre_dqsb_ncyc = (enfet_cyc2 & ba2_cyc2)
               | (enfet_cyc3 & ba2_cyc3)
               | (enfet_cyc4 & ba2_cyc4)
               | (enfet_cyc5 & ba2_cyc5)
               ;
 always @(posedge clk_in)
   begin
     acs_cyc2 <= acs_cyc1 ;       // cs active
```

-continued

```
    ba2_cyc2 <= ba2_r ;
    ba2_cyc3 <= ba2_cyc2 ;
    ba2_cyc4 <= ba2_cyc3 ;
    ba2_cyc5 <= ba2_cyc4 ;
    rd_cmd_cyc2 <= rd_cmd_cyc1 & acs_cyc1;
    rd_cmd_cyc3 <= rd_cmd_cyc2 ;
    rd_cmd_cyc4 <= rd_cmd_cyc3 ;
    rd_cmd_cyc5 <= rd_cmd_cyc4 ;
    rd_cmd_cyc6 <= rd_cmd_cyc5 ;
    rd_cmd_cyc7 <= rd_cmd_cyc6 ;
    wr_cmd_cyc2 <= wr_cmd_cyc1 & acs_cyc1;
    wr_cmd_cyc3 <= wr_cmd_cyc2 ;
    wr_cmd_cyc4 <= wr_cmd_cyc3 ;
    wr_cmd_cyc5 <= wr_cmd_cyc4 ;
  end
 always @(negedge clk_in)
  begin
    dq_ncyc <= dq_cyc;
    dqs_ncyc_a <= dqs_cyc_a;
    dqs_ncyc_b <= dqs_cyc_b;
  end
// DQ FET enables
assign      enq_fet1 = dq_cyc | dq_ncyc              ;
assign      enq_fet2 = dq_cyc | dq_ncyc ;
assign      enq_fet3 = dq_cyc | dq_ncyc              ;
assign        enq_fet4 = dq_cyc | dq_ncyc ;
assign        enq_fet5 = dq_cyc | dq_ncyc ;
// DQS FET enables
assign        ens_fet1a = dqs_cyc_a | dqs_ncyc_a  ;
assign        ens_fet2a = dqs_cyc_a | dqs_ncyc_a  ;
assign        ens_fet3a = dqs_cyc_a | dqs_ncyc_a  ;
assign        ens_fet1b = dqs_cyc_b | dqs_ncyc_b  ;
assign        ens_fet2b = dqs_cyc_b | dqs_ncyc_b  ;
assign        ens_fet3b = dqs_cyc_b | dqs_ncyc_b  ;
```

Another exemplary section of Verilog code compatible with memory density multiplication from 256 Mb to 512 Mb using DDR2 memory devices and gated CAS signals with the row A_{13} density transition bit is listed below in Example 2. The exemplary code of Example 2 corresponds to a logic element **40** which receives one gated CAS signal from the computer system and which generates two gated CAS signals.

EXAMPLE 2

```
// latched a13 flags cs0, banks 0-3
 always @(posedge clk_in)
  if (actv_cmd_R & ~rs0N_R & ~bnk1_R & ~bnk0_R) // activate
  begin
        l_a13_00 <= a13_r ;
  end
 always @(posedge clk_in)
  if (actv_cmd_R & ~rs0N_R & ~bnk1_R & bnk0_R) // activate
  begin
        l_a13_01 <= a13_r ;
  end
 always @(posedge clk_in)
  if (actv_cmd_R & ~rs0N_R & bnk1_R & ~bnk0_R) // activate
  begin
        l_a13_10 <= a13_r ;
  end
 always @(posedge clk_in)
  if (actv_cmd_R & ~rs0N_R & bnk1_R & bnk0_R) // activate
  begin
        l_a13_11 <= a13_r ;
  end
// gated cas
assign cas_i = ~(casN_R);
assign cas0_o = ( ~rasN_R & cas_i)
```

-continued

```
        | ( rasN_R & ~l_a13_00 & ~bnk1_R & ~bnk0_R & cas_i)
        | ( rasN_R & ~l_a13_01 & ~bnk1_R & bnk0_R & cas_i)
        | ( rasN_R & ~l_a13_10 & bnk1_R & ~bnk0_R & cas_i)
        | ( rasN_R & ~l_a13_11 & bnk1_R & bnk0_R & cas_i)
        ;
assign cas1_o = ( ~rasN_R & cas_i)
        | ( rasN_R & l_a13_00      & ~bnk1_R & ~bnk0_R & cas_i)
        | ( rasN_R & l_a13_01      & ~bnk1_R & bnk0_R & cas_i)
        | ( rasN_R & l_a13_10      & bnk1_R & ~bnk0_R & cas_i)
        | (rasN_R & l_a13_11       & bnk1_R & bnk0_R & cas_i)
        ;
assign  pcas_0_N = ~cas0_o;
assign  pcas_1_N = ~cas1_o;
assign  rd0_o_R1 = rasN_R & cas0_o & weN_R & ~rs0N_R; // rnk0 rd cmd cyc
assign  rd1_o_R1 = rasN_R & cas1_o & weN_R & ~rs0N_R; // rnk1 rd cmd cyc
assign  wr0_o_R1 = rasN_R & cas0_o & ~weN_R & ~rs0N_R; // rnk0 wr cmd cyc
assign  wr1_o_R1 = rasN_R & cas1_o & ~weN_R & ~rs0N_R ; // rnk1 wr cmd cyc
 always @(posedge clk_in)
  begin
        rd0_o_R2 <= rd0_o_R1 ;
        rd0_o_R3 <= rd0_o_R2;
        rd0_o_R4 <= rd0_o_R3;
        rd0_o_R5 <= rd0_o_R4;
        rd1_o_R2 <= rd1_o_R1 ;
        rd1_o_R3 <= rd1_o_R2;
        rd1_o_R4 <= rd1_o_R3;
        rd1_o_R5 <= rd1_o_R4;
        wr0_o_R2 <= wr0_o_R1 ;
        wr0_o_R3 <= wr0_o_R2;
        wr0_o_R4 <= wr0_o_R3;
        wr1_o_R2 <= wr1_o_R1 ;
        wr1_o_R3 <= wr1_o_R2;
        wr1_o_R4 <= wr1_o_R3;
 end
 always @(posedge clk_in)
  begin
  if (
      (rd0_o_R2 & ~rd1_o_R4)                                  // pre-am rd if no ped on rnk 1
   | rd0_o_R3                                                 // 1st cyc of rd brst
   | rd0_o_R4                                                 // 2nd cyc of rd brst
   | (rd0_o_R5 & ~rd1_o_R2 & ~rd1_o_R3)                       // post-rd cyc if no ped on rnk 1
   | (wr0_o_R1)                                               // pre-am wr
   | wr0_o_R2 | wr0_o_R3                                      // wr brst 1st & 2nd cyc
   | (wr0_o_R4)                                               // post-wr cyc (chgef9)
   | wr1_o_R1 | wr1_o_R2 | wr1_o_R3 | wr1_o_R4 // rank 1 (chgef9)
   )
            en_fet_a <= 1'b1;                                 // enable fet
 else
            en_fet_a <= 1'b0;                                 // disable fet
 end
always @(posedge clk_in)
        begin
        if (
         (rd1_o_R2 & ~rd0_o_R4)
        | rd1_o_R3
        | rd1_o_R4
        | (rd1_o_R5 & ~rd0_o_R2 & ~rd0_o_R3)
     | (wr1_o_R1)                                             // (chgef8)
     | wr1_o_R2 | wr1_o_R3
     | (wr1_o_R4)                                             // post-wr cyc (chgef9)
     | wr0_o_R1 | wr0_o_R2 | wr0_o_R3 | wr0_o_R4              // rank 0 (chgef9)
        )
            en_fet_b <= 1'b1;                                 //
        else
            en_fet_b <= 1'b0;
        end
```

FIG. 2A schematically illustrates an exemplary memory module **10** which doubles the rank density in accordance with certain embodiments described herein. The memory module **10** has a first memory capacity. The memory module **10** comprises a plurality of substantially identical memory devices **30** configured as a first rank **32** and a second rank **34**. In certain embodiments, the memory devices **30** of the first rank **32** are configured in pairs, and the memory devices **30** of the second rank **34** are also configured in pairs. In certain embodiments, the memory devices **30** of the first rank **32** are configured with their respective DQS pins tied together and the memory devices **30** of the second rank **34** are configured with their respective DQS pins tied together, as described more fully below. The memory module **10** further comprises a logic element **40** which receives a first set of address and control signals from a memory controller (not shown) of the computer system. The first set of address and control signals is compatible with a second memory capacity substantially

equal to one-half of the first memory capacity. The logic element **40** translates the first set of address and control signals into a second set of address and control signals which is compatible with the first memory capacity of the memory module **10** and which is transmitted to the first rank **32** and the second rank **34**.

The first rank **32** of FIG. **2**A has 18 memory devices **30** and the second rank **34** of FIG. **2**A has 18 memory devices **30**. Other numbers of memory devices **30** in each of the ranks **32**, **34** are also compatible with embodiments described herein.

In the embodiment schematically illustrated by FIG. **2**A, the memory module **10** has a width of 8 bytes (or 64 bits) and each of the memory devices **30** of FIG. **2**A has a bit width of 4 bits. The 4-bit-wide ("×4") memory devices **30** of FIG. **2**A have one-half the width, but twice the depth of 8-bit-wide ("×8") memory devices. Thus, each pair of "×4" memory devices **30** has the same density as a single "×8" memory device, and pairs of "×4" memory devices **30** can be used instead of individual "×8" memory devices to provide the memory density of the memory module **10**. For example, a pair of 512-Mb 128M×4-bit memory devices has the same memory density as a 1-Gb 128M×8-bit memory device.

For two "×4" memory devices **30** to work in tandem to mimic a "×8" memory device, the relative DQS pins of the two memory devices **30** in certain embodiments are advantageously tied together, as described more fully below. In addition, to access the memory density of a high-density memory module **10** comprising pairs of "×4" memory devices **30**, an additional address line is used. While a high-density memory module comprising individual "×8" memory devices with the next-higher density would also utilize an additional address line, the additional address lines are different in the two memory module configurations.

For example, a 1-Gb 128M×8-bit DDR-1 DRAM memory device uses row addresses A_{13}-A_0 and column addresses A_{11} and A_9-A_0. A pair of 512-Mb 128M×4-bit DDR-1 DRAM memory devices uses row addresses A_{12}-A_0 and column addresses A_{12}, A_{11}, and A_9-A_0. In certain embodiments, a memory controller of a computer system utilizing a 1-GB 128M×8 memory module **10** comprising pairs of the 512-Mb 128M×4 memory devices **30** supplies the address and control signals including the extra row address (A_{13}) to the memory module **10**. The logic element **40** receives the address and control signals from the memory controller and converts the extra row address (A_{13}) into an extra column address (A_{12}).

FIG. **2**B schematically illustrates an exemplary logic element **40** compatible with embodiments described herein. The logic element **40** is used for a memory module **10** comprising pairs of "×4" memory devices **30** which mimic individual "×8" memory devices. In certain embodiments, each pair has the respective DQS pins of the memory devices **30** tied together. In certain embodiments, as schematically illustrated by FIG. **2**B, the logic element **40** comprises a programmable-logic device (PLD) **42**, a first multiplexer **44** electrically coupled to the first rank **32** of memory devices **30**, and a second multiplexer **46** electrically coupled to the second rank **34** of memory devices **30**. In certain embodiments, the PLD **42** and the first and second multiplexers **44**, **46** are discrete elements, while in, other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD **42**, first multiplexer **44**, and second multiplexer **46** in accordance with embodiments described herein.

In the exemplary logic element **40** of FIG. **2**B, during a row access procedure (CAS is high), the first multiplexer **44** passes the A_{12} address through to the first rank **32**, the second multiplexer **46** passes the A_{12} address through to the second rank **34**, and the PLD **42** saves or latches the A_{13} address from the memory controller. In certain embodiments, a copy of the A_{13} address is saved by the PLD **42** for each of the internal banks (e.g., 4 internal banks) per memory device **30**. During a subsequent column access procedure (CAS is low), the first multiplexer **44** passes the previously-saved A_{13} address through to the first rank **32** as the A_{12} address and the second multiplexer **46** passes the previously-saved A_{13} address through to the second rank **34** as the A_{12} address. The first rank **32** and the second rank **34** thus interpret the previously-saved A_{13} row address as the current A_{12} column address. In this way, in certain embodiments, the logic element **40** translates the extra row address into an extra column address in accordance with certain embodiments described herein.

Thus, by allowing two lower-density memory devices to be used rather than one higher-density memory device, certain embodiments described herein provide the advantage of using lower-cost, lower-density memory devices to build "next-generation" higher-density memory modules. Certain embodiments advantageously allow the use of lower-cost readily-available 512-Mb DDR-2 SDRAM devices to replace more expensive 1-Gb DDR-2 SDRAM devices. Certain embodiments advantageously reduce the total cost of the resultant memory module.

FIG. **3**A schematically illustrates an exemplary memory module **10** which doubles number of ranks in accordance with certain embodiments described herein. The memory module **10** has a first plurality of memory locations with a first memory density. The memory module **10** comprises a plurality of substantially identical memory devices **30** configured as a first rank **32**, a second rank **34**, a third rank **36**, and a fourth rank **38**. The memory module **10** further comprises a logic element **40** which receives a first set of address and control signals from a memory controller (not shown). The first set of address and control signals is compatible with a second plurality of memory locations having a second memory density. The second memory density is substantially equal to one-half of the first memory density. The logic element **40** translates the first set of address and control signals into a second set of address and control signals which is compatible with the first plurality of memory locations of the memory module **10** and which is transmitted to the first rank **32**, the second rank **34**, the third rank **36**, and the fourth rank **38**.

Each rank **32**, **34**, **36**, **38** of FIG. **3**A has 9 memory devices **30**. Other numbers of memory devices **30** in each of the ranks **32**, **34**, **36**, **38** are also compatible with embodiments described herein.

In the embodiment schematically illustrated by FIG. **3**A, the memory module **10** has a width of 8 bytes (or 64 bits) and each of the memory devices **30** of FIG. **3**A has a bit width of 8 bits. Because the memory module **10** has twice the number of 8-bit-wide ("×8") memory devices **30** as does a standard 8-byte-wide memory module, the memory module **10** has twice the density as does a standard 8-byte-wide memory module. For example, a 1-GB 128M×8-byte memory module with 36 512-Mb 128M×8-bit memory devices (arranged in four ranks) has twice the memory density as a 512-Mb 128M×8-byte memory module with 18 512-Mb 128M×8-bit memory devices (arranged in two ranks).

To access the additional memory density of the high-density memory module **10**, the two chip-select signals (CS_0, CS_1) are used with other address and control signals to gate a set of four gated CAS signals. For example, to access the additional ranks of four-rank 1-GB 128M×8-byte DDR-1 DRAM memory module, the CS_0 and CS_1 signals along with the other address and control signals are used to gate the CAS signal appropriately, as schematically illustrated by FIG. **3**A. FIG. **3**B schematically illustrates an exemplary logic element **40** compatible with embodiments described herein. In certain embodiments, the logic element **40** comprises a programmable-logic device (PLD) **42** and four "OR" logic elements **52**, **54**, **56**, **58** electrically coupled to corresponding ranks **32**, **34**, **36**, **38** of memory devices **30**.

In certain embodiments, the PLD **42** comprises an ASIC, an FPGA, a custom-designed semiconductor device, or a CPLD. In certain embodiments, the PLD **42** and the four "OR" logic elements **52**, **54**, **56**, **58** are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD **42** and appropriate "OR" logic elements **52**, **54**, **56**, **58** in accordance with embodiments described herein.

In the embodiment schematically illustrated by FIG. **3**B, the PLD **42** transmits each of the four "enabled CAS" ($ENCAS_0a$, $ENCAS_0b$, $ENCAS_1a$, $ENCAS_1b$) signals to a corresponding one of the "OR" logic elements **52**, **54**, **56**, **58**. The CAS signal is also transmitted to each of the four "OR" logic elements **52**, **54**, **56**, **58**. The CAS signal and the "enabled CAS" signals are "low" true signals. By selectively activating each of the four "enabled CAS" signals which are inputted into the four "OR" logic elements **52**, **54**, **56**, **58**, the PLD **42** is able to select which of the four ranks **32**, **34**, **36**, **38** is active.

In certain embodiments, the PLD **42** uses sequential and combinatorial logic procedures to produce the gated CAS signals which are each transmitted to a corresponding one of the four ranks **32**, **34**, **36**, **38**. In certain other embodiments, the PLD **42** instead uses sequential and combinatorial logic procedures to produce four gated chip-select signals (e.g., CS_0a, CS_0b, CS_1a, and CS_1b) which are each transmitted to a corresponding one of the four ranks **32**, **34**, **36**, **38**.

Back-to-Back Adjacent Read Commands

Due to their source synchronous nature, DDR SDRAM (e.g., DDR1, DDR2, DDR3) memory devices operate with a data transfer protocol which surrounds each burst of data strobes with a pre-amble time interval and a post-amble time interval. The pre-amble time interval provides a timing window for the receiving memory device to enable its data capture circuitry when a known valid level is present on the strobe signal to avoid false triggers of the memory device's capture circuit. The post-amble time interval provides extra time after the last strobe for this data capture to facilitate good signal integrity. In certain embodiments, when the computer system accesses two consecutive bursts of data from the same memory device, termed herein as a "back-to-back adjacent read," the post-amble time interval of the first read command and the pre-amble time interval of the second read command are skipped by design protocol to increase read efficiency. FIG. **4**A shows an exemplary timing diagram of this "gapless" read burst for a back-to-back adjacent read condition from one memory device.

In certain embodiments, when the second read command accesses data from a different memory device than does the first read command, there is at least one time interval (e.g., clock cycle) inserted between the data strobes of the two memory devices. This inserted time interval allows both read data bursts to occur without the post-amble time interval of the first read data burst colliding or otherwise interfering with the pre-amble time interval of the second read data burst. In certain embodiments, the memory controller of the computer system inserts an extra clock cycle between successive read commands issued to different memory devices, as shown in the exemplary timing diagram of FIG. **4**B for successive read accesses from different memory devices.

In typical computer systems, the memory controller is informed of the memory boundaries between the ranks of memory of the memory module prior to issuing read commands to the memory module. Such memory controllers can insert wait time intervals or clock cycles to avoid collisions or interference between back-to-back adjacent read commands which cross memory device boundaries, which are referred to herein as "BBARX."

In certain embodiments described herein in which the number of ranks of the memory module is doubled or quadrupled, the logic element **40** generates a set of output control signals so that the selection decoding is transparent to the computer system. However, in certain such embodiments, there are memory device boundaries of which the computer system is unaware, so there are occasions in which BBARX occurs without the cognizance of the memory controller of the computer system. As shown in FIG. **5**, the last data strobe of memory device "a" collides with the pre-amble time interval of the data strobe of memory device "b," resulting in a "collision window."

FIG. **6**A schematically illustrates a circuit diagram of a conventional memory module **100** showing the interconnections between the DQ data signal lines **102** of the memory devices "a" and "b" (not shown) and their DQS data strobe signal lines **104**. In certain embodiments, the electrical signal lines are etched on the printed circuit board. As shown in FIG. **6**A, each of the memory devices has their DQ data signal lines **102** electrically coupled to a common DQ line **112** and the DQS data strobe signal lines **104** electrically coupled to a common DQS line **114**.

In certain embodiments, BBARX collisions are avoided by a mechanism which electrically isolates the DQS data strobe signal lines **104** of the memory devices from one another during the transition from the first read data burst of one rank of memory devices to the second read data burst of another rank of memory devices. FIG. **6**B schematically illustrates a circuit diagram of an exemplary memory module **10** comprising an isolation device **120** in accordance with certain embodiments described herein. As shown in FIG. **6**B, each of the memory devices **30** otherwise involved in a BBARX collision have their DQS data strobe signal lines **104** electrically coupled to the common DQS line **114** through the isolation element **120**. The isolation device **120** of certain embodiments multiplexes the DQS data strobe signal lines **104** of the two ranks of memory devices **30** from one another to avoid a BBARX collision.

In certain embodiments, as schematically illustrated by FIG. **6**B, the isolation device **120** comprises a first switch **122** electrically coupled to a first data strobe signal line (e.g., DQSa) of a first memory device (not shown) and a second switch **124** electrically coupled to a second data strobe signal line (e.g., DQSb) of a second memory device (not shown). Exemplary switches compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex. In certain embodiments, the time

for switching the first switch **122** and the second switch **124** is between the two read data bursts (e.g., after the last DQS data strobe of the read data burst of the first memory device and before the first DQS data strobe of the read data burst of the second memory device). During the read data burst for a first memory device, the first switch **122** is enabled. After the last DQS data strobe of the first memory device and before the first DQS data strobe of the second memory device, the first switch **122** is disabled and the second switch **124** is enabled.

In certain embodiments, as schematically illustrated by FIG. **6**C, the isolation device **120** comprises a logic element **140** which multiplexes the DQS data strobe signal lines **104** from one another. Exemplary logic elements compatible with embodiments described herein include, but are not limited to multiplexers, such as the SN74AUC2G53 2:1 analog multiplexer/demultiplexer available from Texas Instruments, Inc. of Dallas, Tex. The logic element **140** receives a first DQS data strobe signal from the first memory device and a second DQS data strobe signal from a second memory device and selectively switches one of the first and second DQS data strobe signals to the common DQS data strobe signal line **114**. Persons skilled in the art can select other types of isolation devices **120** compatible with embodiments described herein.

In certain embodiments, as schematically illustrated by FIG. **6**D, the isolation device **120** also multiplexes the DQ data signal lines **102** of the two memory devices from one another. For example, in certain embodiments, the isolation device **120** comprises a pair of switches on the DQ data signal lines **102**, similar to the switches **122**, **124** on the DQS data strobe signal lines **104** schematically illustrated by FIG. **6**B. In certain other embodiments, the isolation device **120** comprises a logic element **150**, as schematically illustrated by FIG. **6**D. In certain embodiments, the same types of switches and/or logic elements are used for the DQ data signal lines **102** as for the DQS data strobe signal lines **104**. The logic element **150** receives a first DQ data signal from the first memory device and a second DQ data signal from the second memory device and selectively switches one of the first and second DQ data signals to the common DQ data signal line **112**. Persons skilled in the art can select other types of isolation devices **120** compatible with embodiments described herein.

In certain embodiments, the isolation device **120** advantageously adds propagation delays to the DQ data signals which match the DQS strobe signals being multiplexed by the isolation device **120**. In certain embodiments, the isolation device **120** advantageously presents a reduced impedance load to the computer system by selectively switching between the two ranks of memory devices to which it is coupled. This feature of the isolation device **120** is used in certain embodiments in which there is no memory density multiplication of the memory module (e.g., for a computer system with four chip-select signals), but where the impedance load of the memory module may otherwise limit the number of ranks or the number of memory devices per memory module. As schematically illustrated by FIG. **6**E, the isolation device **120** of certain such embodiments comprises the logic element **150** on the DQ data signal lines but not a corresponding logic element on the DQS data strobe signal lines.

In certain embodiments, the control and timing of the isolation device **120** is performed by an isolation-control logic element (e.g., application-specific integrated circuit, custom programmable logic device, field-programmable gate array, etc.) which is resident on the memory module **10**. In certain embodiments, the isolation-control logic element is the same logic element **40** as schematically illustrated in FIGS. **1**A and **1**B, is part of the isolation device **120** (e.g., logic element **140** or logic element **150** as schematically illustrated by FIG. **6**D), or is a separate component. The isolation-control logic element of certain embodiments controls the isolation device **120** by monitoring commands received by the memory module **10** from the computer system and producing "windows" of operation whereby the appropriate components of the isolation device **120** are switched to enable and disable the DQS data strobe signal lines **104** to mitigate BBARX collisions. In certain other embodiments, the isolation-control logic element monitors the commands received by the memory module from the computer system and selectively enables and disables the DQ data signal lines **102** to reduce the load impedance of the memory module **10** on the computer system. In still other embodiments, this logic element performs both of these functions together.

Tied Data Strobe Signal Pins

For proper operation, the computer system advantageously recognizes a 1-GB memory module comprising 256-Mb memory devices with 64M×4-bit configuration as a 1-GB memory module having 512-Mb memory devices with 64M×8-bit configuration (e.g., as a 1-GB memory module with 128M×8-byte configuration). This advantageous result is desirably achieved in certain embodiments by electrically connecting together two output signal pins (e.g., DQS or data strobe pins) of the two 256-Mb memory devices such that both output signal pins are concurrently active when the two memory devices are concurrently enabled. The DQS or data strobe is a bi-directional signal that is used during both read cycles and write cycles to validate or latch data. As used herein, the terms "tying together" or "tied together" refer to a configuration in which corresponding pins (e.g., DQS pins) of two memory devices are electrically connected together and are concurrently active when the two memory devices are concurrently enabled (e.g., by a common chip-select or CS signal). Such a configuration is different from standard memory module configurations in which the output signal pins (e.g., DQS pins) of two memory devices are electrically coupled to the same source, but these pins are not concurrently active since the memory devices are not concurrently enabled. However, a general guideline of memory module design warns against tying together two output signal pins in this way.

FIGS. **7** and **8** schematically illustrate a problem which may arise from tying together two output signal pins. FIG. **7** schematically illustrates an exemplary memory module **205** in which a first DQS pin **212** of a first memory device **210** is electrically connected to a second DQS pin **222** of a second memory device **220**. The two DQS pins **212**, **222** are both electrically connected to a memory controller **230**.

FIG. **8** is an exemplary timing diagram of the voltages applied to the two DQS pins **212**, **222** due to non-simultaneous switching. As illustrated by FIG. **8**, at time t_1, both the first DQS pin **212** and the second DQS pin **222** are high, so no current flows between them. Similarly, at time t_4, both the first DQS pin **212** and the second DQS pin **222** are low, so no current flows between them. However, for times between approximately t_2 and approximately t_3, the first DQS pin **212** is low while the second DQS pin **222** is high. Under such conditions, a current will flow between the two DQS pins **212**, **222**. This condition in which one DQS pin is low while the other DQS pin is high can occur for fractions of a second (e.g., 0.8 nanoseconds) during the dynamic random-access

memory (DRAM) read cycle. During such conditions, the current flowing between the two DQS pins **212**, **222** can be substantial, resulting in heating of the memory devices **210**, **220**, and contributing to the degradation of reliability and eventual failure of these memory devices.

A second problem may also arise from tying together two output signal pins. FIG. **9** schematically illustrates another exemplary memory module **205** in which a first DQS pin **212** of a first memory device **210** is electrically connected to a second DQS pin **214** of a second memory device **220**. The two DQS pins **212**, **214** of FIG. **9** are both electrically connected to a memory controller (not shown). The DQ (data input/output) pin **222** of the first memory device **210** and the corresponding DQ pin **224** of the second memory device **220** are each electrically connected to the memory controller by the DQ bus (not shown). Typically, each memory device **210**, **220** will have a plurality of DQ pins (e.g., eight DQ pins per memory device), but for simplicity, FIG. **9** only shows one DQ pin for each memory device **210**, **220**.

Each of the memory devices **210**, **220** of FIG. **9** utilizes a respective on-die termination or "ODT" circuit **232**, **234** which has termination resistors (e.g., 75 ohms) internal to the memory devices **210**, **220** to provide signal termination. Each memory device **210**, **220** has a corresponding ODT signal pin **262**, **264** which is electrically connected to the memory controller via an ODT bus **240**. The ODT signal pin **262** of the first memory device **210** receives a signal from the ODT bus **240** and provides the signal to the ODT circuit **232** of the first memory device **210**. The ODT circuit **232** responds to the signal by selectively enabling or disabling the internal termination resistors **252**, **256** of the first memory device **210**. This behavior is shown schematically in FIG. **9** by the switches **242**, **244** which are either closed (dash-dot line) or opened (solid line). The ODT signal pin **264** of the second memory device **220** receives a signal from the ODT bus **240** and provides the signal to the ODT circuit **234** of the second memory device **220**. The ODT circuit **234** responds to the signal by selectively enabling or disabling the internal termination resistors **254**, **258** of the second memory device **220**. This behavior is shown schematically in FIG. **9** by the switches **246**, **248** which are either closed (dash-dot line) or opened (solid line). The switches **242**, **244**, **246**, **248** of FIG. **9** are schematic representations of the operation of the ODT circuits **232**, **234**, and do not signify that the ODT circuits **232**, **234** necessarily include mechanical switches.

Examples of memory devices **210**, **220** which include such ODT circuits **232**, **234** include, but are not limited to, DDR2 memory devices. Such memory devices are configured to selectively enable or disable the termination of the memory device in this way in response to signals applied to the ODT signal pin of the memory device. For example, when the ODT signal pin **262** of the first memory device **210** is pulled high, the termination resistors **252**, **256** of the first memory device **210** are enabled. When the ODT signal pin **262** of the first memory device **210** is pulled low (e.g., grounded), the termination resistors **252**, **256** of the first memory device **210** are disabled. By selectively disabling the termination resistors of an active memory device, while leaving the termination resistors of inactive memory devices enabled, such configurations advantageously preserve signal strength on the active memory device while continuing to eliminate signal reflections at the bus-die interface of the inactive memory devices.

In certain configurations, as schematically illustrated by FIG. **9**, the DQS pins **212**, **214** of each memory device **210**, **220** are selectively connected to a voltage VTT through a corresponding termination resistor **252**, **254** internal to the corresponding memory device **210**, **220**. Similarly, in certain configurations, as schematically illustrated by FIG. **9**, the DQ pins **222**, **224** are selectively connected to a voltage VTT through a corresponding termination resistor **256**, **258** internal to the corresponding memory device **210**, **220**. In certain configurations, rather than being connected to a voltage VTT, the DQ pins **212**, **214** and/or the DQS pins **222**, **224** are selectively connected to ground through the corresponding termination resistors **252**, **254**, **256**, **258**. The resistances of the internal termination resistors **252**, **254**, **256**, **258** are selected to clamp the voltages so as to reduce the signal reflections from the corresponding pins. In the configuration schematically illustrated by FIG. **9**, each internal termination resistor **252**, **254**, **256**, **258** has a resistance of approximately 75 ohms.

When connecting the first memory device **210** and the second memory device **220** together to form a double word width, both the first memory device **210** and the second memory device **220** are enabled at the same time (e.g., by a common CS signal). Connecting the first memory device **210** and the second memory device **220** by tying the DQS pins **212**, **214** together, as shown in FIG. **9**, results in a reduced effective termination resistance for the DQS pins **212**, **214**. For example, for the exemplary configuration of FIG. **9**, the effective termination resistance for the DQS pins **212**, **214** is approximately 37.5 ohms, which is one-half the desired ODT resistance (for 75-ohm internal termination resistors) to reduce signal reflections since the internal termination resistors **252**, **254** of the two memory devices **210**, **220** are connected in parallel. This reduction in the termination resistance can result in signal reflections causing the memory device to malfunction.

FIG. **10** schematically illustrates an exemplary memory module **300** in accordance with certain embodiments described herein. The memory module **300** comprises a first memory device **310** having a first data strobe (DQS) pin **312** and a second memory device **320** having a second data strobe (DQS) pin **322**. The memory module **300** further comprises a first resistor **330** electrically coupled to the first DQS pin **312**. The memory module **300** further comprises a second resistor **340** electrically coupled to the second DQS pin **322** and to the first resistor **330**. The first DQS pin **312** is electrically coupled to the second DQS pin **322** through the first resistor **330** and through the second resistor **340**.

In certain embodiments, the memory module **300** is a 1-GB unbuffered Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) high-density dual in-line memory module (DIMM). FIGS. **11A** and **11B** schematically illustrate a first side **362** and a second side **364**, respectively, of such a memory module **300** with eighteen 64Mx4-bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board (PCB) **360**. In certain embodiments, the memory module **300** further comprises a phase-lock-loop (PLL) clock driver **370**, an EEPROM for serial-presence detect (SPD) data **380**, and decoupling capacitors (not shown) mounted on the PCB in parallel to suppress switching noise on VDD and VDDQ power supply for DDR-1 SDRAM. By using synchronous design, such memory modules **300** allow precise control of data transfer between the memory module **300** and the system controller. Data transfer can take place on both edges of the DQS signal at various operating frequencies and programming latencies. Therefore, certain such memory modules **300** are suitable for a variety of high-performance system applications.

In certain embodiments, the memory module **300** comprises a plurality of memory devices configured in pairs, each pair having a first memory device **310** and a second memory device **320**. For example, in certain embodiments, a 128M×72-bit DDR SDRAM high-density memory module **300** comprises thirty-six 64M×4-bit DDR-1 SDRAM integrated circuits in FBGA packages configured in eighteen pairs. The first memory device **310** of each pair has the first DQS pin **312** electrically coupled to the second DQS pin **322** of the second memory device **320** of the pair. In addition, the first DQS pin **312** and the second DQS pin **322** are concurrently active when the first memory device **310** and the second memory device **320** are concurrently enabled.

In certain embodiments, the first resistor **330** and the second resistor **340** each has a resistance advantageously selected to reduce the current flow between the first DQS pin **312** and the second DQS pin **322** while allowing signals to propagate between the memory controller and the DQS pins **312**, **322**. In certain embodiments, each of the first resistor **330** and the second resistor **340** has a resistance in a range between approximately 5 ohms and approximately 50 ohms. For example, in certain embodiments, each of the first resistor **330** and the second resistor **340** has a resistance of approximately 22 ohms. Other resistance values for the first resistor **330** and the second resistor **340** are also compatible with embodiments described herein. In certain embodiments, the first resistor **330** comprises a single resistor, while in other embodiments, the first resistor **330** comprises a plurality of resistors electrically coupled together in series and/or in parallel. Similarly, in certain embodiments, the second resistor **340** comprises a single resistor, while in other embodiments, the second resistor **340** comprises a plurality of resistors electrically coupled together in series and/or in parallel.

FIGS. **12**A and **12**B schematically illustrate an exemplary embodiment of a memory module **300** in which the first resistor **330** and the second resistor **340** are used to reduce the current flow between the first DQS pin **312** and the second DQS pin **322**. As schematically illustrated by FIG. **12**A, the memory module **300** is part of a computer system **400** having a memory controller **410**. The first resistor **330** has a resistance of approximately 22 ohms and the second resistor **340** has a resistance of approximately 22 ohms. The first resistor **330** and the second resistor **340** are electrically coupled in parallel to the memory controller **410** through a signal line **420** having a resistance of approximately 25 ohms. The first resistor **330** and the second resistor **340** are also electrically coupled in parallel to a source of a fixed termination voltage (identified by VTT in FIGS. **12**A and **12**B) by a signal line **440** having a resistance of approximately 47 ohms. Such an embodiment can advantageously be used to allow two memory devices having lower bit widths (e.g., 4-bit) to behave as a single virtual memory device having a higher bit width (e.g., 8-bit).

FIG. **12**B schematically illustrates exemplary current-limiting resistors **330**, **340** in conjunction with the impedances of the memory devices **310**, **320**. During an exemplary portion of a data read operation, the memory controller **410** is in a high-impedance condition, the first memory device **310** drives the first DQS pin **312** high (e.g., 2.7 volts), and the second memory device **320** drives the second DQS pin **322** low (e.g., 0 volts). The amount of time for which this condition occurs is approximated by the time between t_2 and t_3 of FIG. **8**, which in certain embodiments is approximately twice the tDQSQ (data strobe edge to output data edge skew time, e.g., approximately 0.8 nanoseconds). At least a portion of this time in certain embodiments is caused by simultaneous switching output (SSO) effects.

In certain embodiments, as schematically illustrated by FIG. **12**B, the DQS driver of the first memory device **310** has a driver impedance R_1 of approximately 17 ohms, and the DQS driver of the second memory device **320** has a driver impedance R_4 of approximately 17 ohms. Because the upper network of the first memory device **310** and the first resistor **330** (with a resistance R_2 of approximately 22 ohms) is approximately equal to the lower network of the second memory device **320** and the second resistor **340** (with a resistance R_3 of approximately 22 ohms), the voltage at the midpoint is approximately 0.5*(2.7−0)=1.35 volts, which equals VTT, such that the current flow across the 47-ohm resistor of FIG. **12**B is approximately zero.

The voltage at the second DQS pin **322** in FIG. **12**B is given by $V_{DQS2}=2.7*R_4/(R_1+R_2+R_3+R_4)=0.59$ volts and the current flowing through the second DQS pin **322** is given by $I_{DQS2}=0.59/R_4=34$ milliamps. The power dissipation in the DQS driver of the second memory device **320** is thus $P_{DQS2}=34$ mA*0.59 V=20 milliwatts. In contrast, without the first resistor **330** and the second resistor **340**, only the 17-ohm impedances of the two memory devices **310**, **320** would limit the current flow between the two DQS pins **312**, **322**, and the power dissipation in the DQS driver of the second memory device **320** would be approximately 107 milliwatts. Therefore, the first resistor **330** and the second resistor **340** of FIGS. **12**A and **12**B advantageously limit the current flowing between the two memory devices during the time that the DQS pin of one memory device is driven high and the DQS pin of the other memory device is driven low.

In certain embodiments in which there is overshoot or undershoot of the voltages, the amount of current flow can be higher than those expected for nominal voltage values. Therefore, in certain embodiments, the resistances of the first resistor **330** and the second resistor **340** are advantageously selected to account for such overshoot/undershoot of voltages.

For certain such embodiments in which the voltage at the second DQS pin **322** is $V_{DQS2}=0.59$ volts and the duration of the overdrive condition is approximately 0.8 nanoseconds at maximum, the total surge is approximately 0.59 V*1.2 ns=0.3 V-ns. For comparison, the JEDEC standard for overshoot/undershoot is 2.4 V-ns, so certain embodiments described herein advantageously keep the total surge within predetermined standards (e.g., JEDEC standards).

FIG. **13** schematically illustrates another exemplary memory module **500** compatible with certain embodiments described herein. The memory module **500** comprises a termination bus **505**. The memory module **500** further comprises a first memory device **510** having a first data strobe pin **512**, a first termination signal pin **514** electrically coupled to the termination bus **505**, a first termination circuit **516**, and at least one data pin **518**. The first termination circuit **516** selectively electrically terminating the first data strobe pin **512** and the first data pin **518** in response to a first signal received by the first termination signal pin **514** from the termination bus **505**. The memory module **500** further comprises a second memory device **520** having a second data strobe pin **522** electrically coupled to the first data strobe pin **512**, a second termination signal pin **524**, a second termination circuit **526**, and at least one data pin **528**. The second termination signal pin **524** is electrically coupled to a voltage, wherein the second termination circuit **526** is responsive to the voltage by not terminating the second data strobe pin **522** or the second data pin **528**. The memory module **500** further comprises at least one termination

assembly **530** having a third termination signal pin **534**, a third termination circuit **536**, and at least one termination pin **538** electrically coupled to the data pin **528** of the second memory device **520**. The third termination signal pin **534** is electrically coupled to the termination bus **505**. The third termination circuit **536** selectively electrically terminates the data pin **528** of the second memory device **520** through the termination pin **538** in response to a second signal received by the third termination signal pin **534** from the termination bus **505**.

FIG. **14** schematically illustrates a particular embodiment of the memory module **500** schematically illustrated by FIG. **13**. The memory module **500** comprises an on-die termination (ODT) bus **505**. The memory module **500** comprises a first memory device **510** having a first data strobe (DQS) pin **512**, a first ODT signal pin **514** electrically coupled to the ODT bus **505**, a first ODT circuit **516**, and at least one data (DQ) pin **518**. The first ODT circuit **516** selectively electrically terminates the first DQS pin **512** and the DQ pin **518** of the first memory device **510** in response to an ODT signal received by the first ODT signal pin **514** from the ODT bus **505**. This behavior of the first ODT circuit **516** is schematically illustrated in FIG. **14** by the switches **572**, **576** which are selectively closed (dash-dot line) or opened (solid line).

The memory module **500** further comprises a second memory device **520** having a second DQS pin **522** electrically coupled to the first DQS pin **512**, a second ODT signal pin **524**, a second ODT circuit **526**, and at least one DQ pin **528**. The first DQS pin **512** and the second DQS pin **522** are concurrently active when the first memory device **510** and the second memory device **520** are concurrently enabled. The second ODT signal pin **524** is electrically coupled to a voltage (e.g., ground), wherein the second ODT circuit **526** is responsive to the voltage by not terminating the second DQS pin **522** or the second DQ pin **524**. This behavior of the second ODT circuit **526** is schematically illustrated in FIG. **14** by the switches **574**, **578** which are opened.

The memory module **500** further comprises at least one termination assembly **530** having a third ODT signal pin **534** electrically coupled to the ODT bus **505**, a third ODT circuit **536**, and at least one termination pin **538** electrically coupled to the DQ pin **528** of the second memory device **520**. The third ODT circuit **536** selectively electrically terminates the DQ pin **528** of the second memory device **520** through the termination pin **538** in response to an ODT signal received by the third ODT signal pin **534** from the ODT bus **505**. This behavior of the third ODT circuit **536** is schematically illustrated in FIG. **14** by the switch **580** which is either closed (dash-dot line) or opened (solid line).

In certain embodiments, the termination assembly **530** comprises discrete electrical components which are surface-mounted or embedded on the printed-circuit board of the memory module **500**. In certain other embodiments, the termination assembly **530** comprises an integrated circuit mounted on the printed-circuit board of the memory module **500**. Persons skilled in the art can provide a termination assembly **530** in accordance with embodiments described herein.

Certain embodiments of the memory module **500** schematically illustrated by FIG. **14** advantageously avoid the problem schematically illustrated by FIG. **7** of electrically connecting the internal termination resistances of the DQS pins of the two memory devices in parallel. As described above in relation to FIG. **9**, FIGS. **13** and **14** only show one DQ pin for each memory device for simplicity. Other embodiments have a plurality of DQ pins for each memory device. In certain embodiments, each of the first ODT circuit **516**, the second ODT circuit **526**, and the third ODT circuit **536** are responsive to a high voltage or signal level by enabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by disabling the corresponding termination resistors. In other embodiments, each of the first ODT circuit **516**, the second ODT circuit **526**, and the third ODT circuit **536** are responsive to a high voltage or signal level by disabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by enabling the corresponding termination resistors. Furthermore, the switches **572**, **574**, **576**, **578**, **580** of FIG. **14** are schematic representations of the enabling and disabling operation of the ODT circuits **516**, **526**, **536** and do not signify that the ODT circuits **516**, **526**, **536** necessarily include mechanical switches.

The first ODT signal pin **514** of the first memory device **510** receives an ODT signal from the ODT bus **505**. In response to this ODT signal, the first ODT circuit **516** selectively enables or disables the termination resistance for both the first DQS pin **512** and the DQ pin **518** of the first memory device **510**. The second ODT signal pin **524** of the second memory device **520** is tied (e.g., directly hard-wired) to the voltage (e.g., ground), thereby disabling the internal termination resistors **554**, **558** on the second DQS pin **522** and the second DQ pin **528**, respectively, of the second memory device **520** (schematically shown by open switches **574**, **578** in FIG. **14**). The second DQS pin **522** is electrically coupled to the first DQS pin **512**, so the termination resistance for both the first DQS pin **512** and the second DQS pin **522** is provided by the termination resistor **552** internal to the first memory device **510**.

The termination resistor **556** of the DQ pin **518** of the first memory device **510** is enabled or disabled by the ODT signal received by the first ODT signal pin **514** of the first memory device **510** from the ODT bus **505**. The termination resistance of the DQ pin **528** of the second memory device **520** is enabled or disabled by the ODT signal received by the third ODT signal pin **534** of the termination assembly **530** which is external to the second memory device **520**. Thus, in certain embodiments, the first ODT signal pin **514** and the third ODT signal pin **534** receive the same ODT signal from the ODT bus **505**, and the termination resistances for both the first memory device **510** and the second memory device **520** are selectively enabled or disabled in response thereto when these memory devices are concurrently enabled. In this way, certain embodiments of the memory module **500** schematically illustrated by FIG. **14** provides external or off-chip termination of the second memory device **520**.

Certain embodiments of the memory module **500** schematically illustrated by FIG. **14** advantageously allow the use of two lower-cost readily-available 512-Mb DDR-2 SDRAM devices to provide the capabilities of a more expensive 1-GB DDR-2 SDRAM device. Certain such embodiments advantageously reduce the total cost of the resultant memory module **500**.

Certain embodiments described herein advantageously increase the memory capacity or memory density per memory slot or socket on the system board of the computer system. Certain embodiments advantageously allow for higher memory capacity in systems with limited memory slots. Certain embodiments advantageously allow for flexibility in system board design by allowing the memory module **10** to be used with computer systems designed for different numbers of ranks (e.g., either with computer systems designed for two-rank memory modules or with com-

puter systems designed for four-rank memory modules). Certain embodiments advantageously provide lower costs of board designs.

In certain embodiments, the memory density of a memory module is advantageously doubled by providing twice as many memory devices as would otherwise be provided. For example, pairs of lower-density memory devices can be substituted for individual higher-density memory devices to reduce costs or to increase performance. As another example, twice the number of memory devices can be used to produce a higher-density memory configuration of the memory module. Each of these examples can be limited by the number of chip select signals which are available from the memory controller or by the size of the memory devices. Certain embodiments described herein advantageously provide a logic mechanism to overcome such limitations.

Various embodiments of the present invention have been described above. Although this invention has been described with reference to these specific embodiments, the descriptions are intended to be illustrative of the invention and are not intended to be limiting. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention.

What is claimed is:

1. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of memory devices coupled to the printed circuit board, the plurality of memory devices having a first number of memory devices; and

a logic element coupled to the printed circuit board, the logic element receiving a set of input control signals from the computer system, the set of input control signals corresponding to a second number of memory devices smaller than the first number of memory devices, the logic element generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of memory devices, wherein the plurality of memory devices are arranged in a first number of ranks, and the set of input control signals corresponds to a second number of ranks of memory modules, the second number of ranks less than the first number of ranks, wherein the logic element further responds to a first command signal from the computer system by generating a second command signal transmitted to the plurality of memory devices, the first command signal corresponding to the second number of ranks and the second command signal corresponding to the first number of ranks.

2. The memory module of claim **1**, wherein the first command signal is a refresh signal or a precharge signal.

3. The memory module of claim **1**, wherein the memory devices comprise dynamic random-access memory (DRAM) devices.

4. The memory module of claim **1**, wherein the set of input control signals comprises a first number of chip-select signals and wherein the set of output control signals comprises a second number of chip-select signals, wherein the first number of chip-select signals is less than the second number of chip-select signals, the memory module simulating a virtual memory module having the second number of memory devices.

5. The memory module of claim **1**, wherein the logic element comprises an application-specific integrated circuit.

6. The memory module of claim **1**, wherein the logic element comprises a field-programmable gate array.

7. The memory module of claim **1**, wherein the logic element comprises a custom-designed semiconductor device.

8. The memory module of claim **1**, wherein the logic element comprises a complex programmable-logic device.

9. The memory module of claim **1**, wherein the first number of ranks is four, and the second number of ranks is two.

10. The memory module of claim **1**, wherein the first number of ranks is two, and the second number of ranks is one.

11. The memory module of claim **1**, wherein the set of input control signals comprises two chip-select signals and an address signal and the set of output control signals comprises four chip-select signals.

12. The memory module of claim **1**, wherein the printed circuit board is mountable in a module slot of the computer system, the printed circuit board having a plurality of edge connections electrically coupled to corresponding contacts of the module slot.

13. The memory module of claim **1**, wherein the plurality of memory devices are arranged to provide a first memory density per rank, and the set of output control signals corresponds to a second memory density per rank, the second memory density greater than the first memory density per rank.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,289,386 B2
APPLICATION NO. : 11/173175
DATED : October 30, 2007
INVENTOR(S) : Jayesh R. Bhakta et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

At Column 21, line 38, in the specification, please delete "A_0-A_0" and insert -- A_9-A_0 --, therefor.

At Column 28, line 9, in the specification, please delete "212, 214" and insert -- 222, 224 --, therefor.

At Column 28, line 9, in the specification, please delete "222, 224" and insert -- 212, 214 --, therefor.

Signed and Sealed this

Thirteenth Day of May, 2008

JON W. DUDAS
Director of the United States Patent and Trademark Office

APPENDIX B

AO 120 (Rev. 3/04)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Delaware on the following X Patents or ☐ Trademarks:

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
09cv165	3/12/09	DISTRICT OF DELAWARE

PLAINTIFF	DEFENDANT
Netlist, Inc.	MetaRAM, Inc.

	PATENT OR	DATE OF PATENT	HOLDER OF PATENT OR TRADEMARK
1	7,289,386 B2	10/30/07	Netlist, Inc.
2			
3			
4			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
PETER T. DALLEO, CLERK OF COURT		3/12/09

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,289,386 B2
APPLICATION NO. : 11/173175
DATED : October 30, 2007
INVENTOR(S) : Jayesh R. Bhakta et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

At Column 21, line 38, in the specification, please delete "A_0-A_0" and insert -- A_9-A_0 --, therefor.

At Column 28, line 9, in the specification, please delete "212, 214" and insert -- 222, 224 --, therefor.

At Column 28, line 9, in the specification, please delete "222, 224" and insert -- 212, 214 --, therefor.

Signed and Sealed this

Thirteenth Day of May, 2008

JON W. DUDAS
Director of the United States Patent and Trademark Office

Knobbe Martens Olson & Bear LLP
Intellectual Property Law

2040 Main Street
Fourteenth Floor
Irvine, CA 92614
Tel 949-760-0404
Fax 949-760-9502
www.kmob.com

Bruce S. Itchkawitz, Ph.D.
2bsi@kmob.com

January 18, 2008

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Re: Title: MEMORY MODULE DECODER
Letters Patent No.: 7,289,386
Issued: October 30, 2007
Our Reference No.: NETL.018CP1

Dear Sir:

Enclosed for filing is a Certificate of Correction in connection with the above-identified patent.

As the errors cited in the Certificate of Correction were incurred through the fault of the Applicant, the fee due in the amount of $100 will be paid through EFS Web. Please charge any additional fees to our Deposit Account No. 11-1410.

Respectfully submitted,

Knobbe, Martens, Olson & Bear, LLP

Bruce S. Itchkawitz
Registration No. 47,677
Customer No. 20995

Enclosures

4776277
011808

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.	: 7,289,386
APPLICATION NO.	: 11/173,175
ISSUE DATE	: October 30, 2007
INVENTOR(S)	: Jayesh R. Bhakta et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

At Column 21, line 38, in the specification, please delete "A_0-A_0" and insert - - A_9-A_0 - -, therefor.

At Column 28, line 9, in the specification, please delete "212, 214" and insert - - 222, 224 - - , therefor.

At Column 28, line 9, in the specification, please delete "222, 224" and insert - - 212, 214 - - , therefor.

4776184
011808

MAILING ADDRESS OF SENDER:

Bruce S. Itchkawitz
KNOBBE, MARTENS, OLSON & BEAR, LLP
2040 Main Street, 14th Floor
Irvine, California 92614

DOCKET NO. NETL.018CP1

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/173,175	10/30/2007	7289386	NETL.018CP1	6355

20995 7590 10/10/2007

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 21 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Jayesh R. Bhakta, Cerritos, CA;
Jeffrey C. Solomon, Irvine, CA;

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

20995 7590 07/30/2007

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/173,175	07/01/2005	Jayesh R. Bhakta	NETL.018CP1	6355

TITLE OF INVENTION: MEMORY MODULE DECODER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	10/30/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
SOFOCLEOUS, ALEXANDER	2824	365-063000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Knobbe Martens
2 Olson & Bear LLP
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Netlist, Inc.
(B) RESIDENCE: (CITY and STATE OR COUNTRY): Irvine, California

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☑ Issue Fee
☑ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 11-1410 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature Bruce S. Itchkawitz Date 9/19/07

Typed or printed name Bruce S. Itchkawitz Registration No. 47,677

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

NETL.018CP1 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jayesh R. Bhakta et al.	Group Art Unit 2824
App. No.	:	11/173,175	
Filed	:	July 1, 2005	
For	:	MEMORY MODULE DECODER	
Examiner	:	Alexander Sofocleous	

COMMENTS ON EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE

Mail Stop- ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Arlington, VA 22313-1450

Dear Sir:

Applicants respectfully disagree with the Examiner's Statement of Reasons for Allowance to the extent that the limitations recited by the Examiner are not present in all of the claims.

To the extent that there is any implication that the patentability of the claims rests on the recitation of a single feature, Applicants respectfully disagree with the Examiner's Statement because it is the combination of features that makes the claims patentable. Accordingly, Applicants submit that the claims of the present application are allowable because each of the claims recites a combination of features that are not taught or suggested by the prior art.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 9/19/07

By: _____

Bruce S. Itchkawitz
Registration No. 47,677
Attorney of Record
Customer No. 20,995
(949) 760-0404

4275327
091707

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

20995 7590 07/30/2007

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
SOFOCLEOUS, ALEXANDER	
ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 07/30/2007

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/173,175	07/01/2005	Jayesh R. Bhakta	NETL.018CP1	6355

TITLE OF INVENTION: MEMORY MODULE DECODER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	10/30/2007

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 07/07) Approved for use through 07/31/2007.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

20995 7590 07/30/2007

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/173,175	07/01/2005	Jayesh R. Bhakta	NETL.018CP1	6355

TITLE OF INVENTION: MEMORY MODULE DECODER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	10/30/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
SOFOCLEOUS, ALEXANDER	2824	365-063000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____ 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/173,175	07/01/2005	Jayesh R. Bhakta	NETL.018CP1	6355

20995 7590 07/30/2007

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
SOFOCLEOUS, ALEXANDER	
ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 07/30/2007

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 21 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 21 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 07/07) Approved for use through 07/31/2007.

EF

Notice of Allowability	Application No.	Applicant(s)	
	11/173,175	BHAKTA ET AL.	
	Examiner	Art Unit	
	Alexander Sofocleous	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed June 19, 2007*.

2. ☒ The allowed claim(s) is/are *12,13 and 21-31*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 7/20/2007
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

SON DINH
PRIMARY PATENT EXAMINER

DETAILED ACTION

1. This action is responsive to the following communication: the Amendment filed June 19, 2007.

2. Claims 12, 13, and 21-31 are pending in the case. Claims 1-11, and 14-20 are cancelled. Claim 12 is currently amended. Claims 21-31 are new claims. Claim 12 is independent.

Drawings

4. The proposed drawings corrections received on June 19, 2007 are approved.

Allowable Subject Matter

5. **Claims 12, 13, and 21-31 are allowed.**

6. The following is an examiner's statement of reasons for allowance:

With respect to independent claim 12, there is no teaching, suggestion, or motivation for combination in the prior art to the logic element generating a second command signal, corresponding to a first number of ranks, based on the first command signal, corresponding to a second number of ranks, wherein the second number of ranks is less than the first number of ranks (i.e., the logic element generates more rank select signals from a number of rank select signals).

Any comments considered necessary by applicant must be submitted no later

than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Sakurai (U.S. Patent 5,959,930), Kinsley et al. (U.S. Patent 7,046,538), Raghuram (U.S. Patent 7,200,021), and Raghuram (U.S. Patent Application Publication 2006/0129755).

Sakurai teach a bank address decoder that takes two bank signals and generates 4 bank select signals to select each of the memory arrays (banks are different than ranks).

Kinsley et al., filed after instant application's provisional applications, teach a three rank memory module.

Raghuram '021, filed after instant application's provisional applications, teach 2 rank select signals input to a decoder that outputs 4 rank select signals.

Raghuram '755, filed after instant application's provisional applications, teach 3 rank select signals input to a decoder that outputs 8 rank select signals.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Sofocleous whose telephone number is 571-272-0635. The examiner can normally be reached on M-F 7:00am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGS

SON DINH
PRIMARY PATENT EXAMINER

PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	11/173,175
	Filing Date	July 1, 2005
	First Named Inventor	Jayesh R. Bhakta
	Art Unit	2824
(Multiple sheets used when necessary)	Examiner	Alexander Sofocleous
SHEET 1 OF 1	Attorney Docket No.	NETL.018CP1

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number	Publication Date	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
/AGS/	1	5,805,520 A	09/1998	Anglada et al.	
/AGS/	2	6,944,694 B2	09/2005	Pax	
/AGS/	3	6,996,686 B2	02/2006	Doblar et al.	
/AGS/	4	App. No. 11/173175	07/01/2005	Bhakta et al.	
/AGS/	5	2005/0281096 A1	12/22/2005	Bhakta et al.	

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author, title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[1]

4033382
071807

Examiner Signature	/Alexander Sofocleous/	Date Considered	07/23/2007

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

T[1] - Place a check mark in this area when an English language Translation is attached.

Notice of References Cited	Application/Control No. 11/173,175	Applicant(s)/Patent Under Reexamination BHAKTA ET AL.	
	Examiner Alexander Sofocleous	Art Unit 2824	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,959,930	09-1999	Sakurai, Mikio	365/230.03
*	B	US-7,046,538	05-2006	Kinsley et al.	365/52
*	C	US-7,200,021	04-2007	Raghuram, Siva	365/51
*	D	US-2006/0129755	06-2006	Raghuram, Siva	711/105
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

Bib Data Sheet

CONFIRMATION NO. 6355

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/173,175	07/01/2005 RULE	365	2824	NETL.018CP1

APPLICANTS

Jayesh R. Bhakta, Cerritos, CA;
Jeffrey C. Solomon, Irvine, CA;

**** CONTINUING DATA ***************************

This application is a CIP of 11/075,395 03/07/2005 which claims benefit of 60/550,668 03/05/2004
and claims benefit of 60/575,595 05/28/2004
and claims benefit of 60/588,244 07/15/2004 OK. AGJ

**** FOREIGN APPLICATIONS *********************

NONE. AGJ

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 07/22/2005

		STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
Foreign Priority claimed	☐ yes ☒ no	CA	18	20 13	4 1
35 USC 119 (a-d) conditions met	☐ yes ☐ no ☐ Met after Allowance				
Verified and Acknowledged	Examiner's Signature / Initials AGJ				

ADDRESS
20995

TITLE
Memory module decoder

FILING FEE RECEIVED		
1330	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11173175	BHAKTA ET AL.
	Examiner	Art Unit
	Sofocleous, Alexander	2824

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	01/09/2007	01/12/2007	07/19/2007						
	1	+	✓	-						
	2	+	✓	-						
	3	+	✓	-						
	4	+	✓	-						
	5	+	✓	-						
	6	+	✓	-						
	7	+	✓	-						
	8	+	✓	-						
	9	+	✓	-						
	10	+	✓	-						
	11	+	✓	-						
	12	+	O	=						
	13	+	O	=						
	14	+	✓	-						
	15	+	✓	-						
	16	+	N	-						
	17	+	N	-						
	18	+	N	-						
	19	+	N	-						
	20	+	N	-						
	21			=						
	22			=						
	23			=						
	24			=						
	25			=						
	26			=						
	27			=						
	28			=						
	29			=						
	30			=						
	31			=						

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11173175	BHAKTA ET AL.
	Examiner	Art Unit
	Sofocleous, Alexander	2824

SEARCHED

Class	Subclass	Date	Examiner
326	105	01/09/2007	AGS
365	230.06	01/09/2007	AGS
711	5, 211	01/09/2007	AGS
365	51, 52, 230.01, 230.03, 230.06, 230.08	07/19/2007	AGS

SEARCH NOTES

Search Notes	Date	Examiner
see EAST search history	01/09/2007	AGS
consulted VanThu Nguyen (AU2824) regarding class 365	07/17/2007	AGS
see updated EAST search history	07/19/2007	AGS
reviewed parent case history (11/075395)	07/23/2007	AGS

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner
365	51, 230.06, 230.08	07/19/2007	AGS

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S3	3	(rank near2 decoder) (memory adj module)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 11:52
S4	1	(10/037436).APP.	USPAT; USOCR	AND	ON	2007/01/09 12:55
S5	1	(10/100312).APP.	USPAT; USOCR	AND	ON	2007/01/09 12:56
S6	1	(09/023170).APP.	USPAT; USOCR	AND	ON	2007/01/09 13:30
S8	1	S2 S7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 13:33
S7	4039	(365/230.06).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/09 13:33
S9	776	(rank) (memory adj module)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 13:35
S2	126	(rank with four) (memory adj module)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 13:35
S10	9	S7 S9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 13:40

EAST Search History

S1	1	11/173175.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 13:40
S16	6	S9 S15	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 13:41
S15	8638	"CS.sub."$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 13:41
S14	201	S9 S11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 13:41
S13	203	S9 S12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 13:41
S12	546176	CS$2 or "CS.sub."$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 13:41
S11	540234	CS$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 13:41
S17	1	(10/453466).APP.	USPAT; USOCR	AND	ON	2007/01/09 14:05

EAST Search History

S20	43	S9 S18	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 14:06
S18	5905	((326/105) or (365/230.06) or (711/5,211)).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/09 14:06
S19	18	S15 S18	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 14:21
S24	3	((SOLOMON-JEFF SOLOMON-JEFFREY SOLOMON-JEFFREY-C) and (BHAKTA-J BHAKTA-JAY BHAKTA-JAYESH-R BHAKTA-J-R)). in. and (memory)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/09 14:24
S23	44	((SOLOMON-JEFF SOLOMON-JEFFREY SOLOMON-JEFFREY-C) (BHAKTA-J BHAKTA-JAY BHAKTA-JAYESH-R BHAKTA-J-R)).in. and (memory)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/09 14:24
S21	56	((SOLOMON-JEFF SOLOMON-JEFFREY SOLOMON-JEFFREY-C) (BHAKTA-J BHAKTA-JAY BHAKTA-JAYESH-R BHAKTA-J-R)).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/09 14:24
S25	1	(11/217056).APP.	USPAT; USOCR	AND	ON	2007/01/09 14:33
S26	1	(10/037436).APP.	USPAT; USOCR	AND	ON	2007/01/09 14:37
S27	1	(10/601104).APP.	USPAT; USOCR	AND	ON	2007/01/09 14:47
S29	0	(11/010182).APP.	USPAT; USOCR	AND	ON	2007/07/19 12:25

EAST Search History

S28	32	multi$1rank (memory adj module)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/07/19 12:42
S30	203	multi$4rank or (multi$3 adj rank) (memory adj module)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/07/19 12:43
S31	1	(10/932834).APP.	USPAT; USOCR	AND	ON	2007/07/19 12:45
S32	10	("4884237" | "5963464" | "6278616" | "6298426" | "6404662" | "6633948" | "6683372" | "6765812" | "6771526" | "6961281").PN. OR ("7046538").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/19 12:46
S33	10	("20020002662" | "20030090879" | "5535169" | "5959930" | "6108745" | "6115314" | "6134168" | "6414868" | "6636957").PN. OR ("6961281").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/19 12:48
S35	2	("20020112119" | "6683372").PN. OR ("7200021").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/19 13:06
S34	1	(11/010942).APP.	USPAT; USOCR	AND	ON	2007/07/19 13:06
S36	11985	(365/51,52,230.01,230.03,230.08, 230.06).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/07/19 13:37
S37	10	S30 S36	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/07/19 13:38

EAST Search History

S39	16	S36 S38	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/07/19 13:44
S38	112	(rank (memory adj module)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/07/19 13:44
S40	1	(10/199857).APP.	USPAT; USOCR	AND	ON	2007/07/19 13:45
S41	1	(09/941649).APP.	USPAT; USOCR	AND	ON	2007/07/19 13:46
L2	4	(("5805520") or ("6944694") or ("6996686") or ("20050281096")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/07/23 15:32
L3	1	2 rank	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/07/23 15:33

INFORMATION DISCLOSURE STATEMENT

Applicants	:	Jayesh R. Bhakta et al.
App. No	:	11/173,175
Filed	:	July 1, 2005
For	:	MEMORY MODULE DECODER
Examiner	:	Alexander Sofocleous
Art Unit	:	2824

CERTIFICATE OF EFS WEB TRANSMISSION

I hereby certify that this correspondence, and any other attachment noted on the automated Acknowledgement Receipt, is being transmitted from within the Pacific Time zone to the Commissioner for Patents via the EFS Web server on:

7/20/07
(Date)

Bruce S. Itchkawitz, Reg. No. 47,677

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is an Information Disclosure Statement by Applicant (PTO/SB/08 equivalent) listing five (5) references to be considered by the Examiner. Copies of the references are not submitted pursuant to 37 C.F.R. § 1.98(d).

A first Office Action on the merits was mailed before the mailing date of this Statement, the Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 7/20/07

By: _____

Bruce S. Itchkawitz
Registration No. 47,677
Attorney of Record
Customer No. 20,995
(949) 760-0404

4033516
072007

PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	11/173,175
	Filing Date	July 1, 2005
	First Named Inventor	Jayesh R. Bhakta
	Art Unit	2824
(Multiple sheets used when necessary)	Examiner	Alexander Sofocleous
SHEET 1 OF 1	Attorney Docket No.	NETL.018CP1

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number	Publication Date	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	1	5,805,520 A	09/1998	Anglada et al.	
	2	6,944,694 B2	09/2005	Pax	
	3	6,996,686 B2	02/2006	Doblar et al.	
	4	App. No. 11/173175	07/01/2005	Bhakta et al.	
	5	2005/0281096 A1	12/22/2005	Bhakta et al.	

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author, title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city and/or country where published.	T^1

4033382
071807

Examiner Signature	Date Considered
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

T^1 - Place a check mark in this area when an English language Translation is attached.

NETL.018CP1 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jayesh R. Bhakta et al.	Group Art Unit 2824
Appl. No.	:	11/173,175	
Filed	:	July 1, 2005	
For	:	MEMORY MODULE DECODER	
Examiner	:	Alexander Sofocleous	

AMENDMENT AND RESPONSE TO JANUARY 26, 2007 OFFICE ACTION

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the January 26, 2007 Office Action, Applicants request the Examiner to reconsider the above-identified patent application in view of the following amendments and remarks.

Amendments to the Claims: Begin on page 2 of this Response.

Remarks: Begin on page 4 of this Response.

AMENDMENTS TO THE CLAIMS

Please cancel Claims 1-11 and 14-20 without prejudice, as indicated below.

Please add Claims 21-31, as indicated below.

Please amend Claim 12 as indicated below.

A complete listing of all claims is presented below with insertions underlined (e.g., insertion), and deletions struckthrough or in double brackets (e.g., ~~deletion~~ or [[deletion]]):

1.-11. (Cancelled)

12. (Currently Amended) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of memory devices coupled to the printed circuit board, the plurality of memory devices having a first number of memory devices; and

a logic element coupled to the printed circuit board, the logic element receiving a set of input control signals from the computer system, the set of input control signals corresponding to a second number of memory devices smaller than the first number of memory devices, the logic element generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of memory devices, wherein the plurality of memory devices are arranged in a first number of ranks, and the set of input control signals corresponds to a second number of ranks of memory modules, the second number of ranks less than the first number of ranks~~The memory module of Claim 8~~, wherein the logic element further responds to a first command signal from the computer system by generating a second command signal transmitted to the plurality of memory devices, the first command signal corresponding to the second number of ranks and the second command signal corresponding to the first number of ranks.

13. (Original) The memory module of Claim 12, wherein the first command signal is a refresh signal or a precharge signal.

14.-20. (Cancelled)

21. (New) The memory module of Claim 12, wherein the memory devices comprise dynamic random-access memory (DRAM) devices.

22. (New) The memory module of Claim 12, wherein the set of input control signals comprises a first number of chip-select signals and wherein the set of output control signals comprises a second number of chip-select signals, wherein the first number of chip-select signals is less than the second number of chip-select signals, the memory module simulating a virtual memory module having the second number of memory devices.

23. (New) The memory module of Claim 12, wherein the logic element comprises an application-specific integrated circuit.

24. (New) The memory module of Claim 12, wherein the logic element comprises a field-programmable gate array.

25. (New) The memory module of Claim 12, wherein the logic element comprises a custom-designed semiconductor device.

26. (New) The memory module of Claim 12, wherein the logic element comprises a complex programmable-logic device.

27. (New) The memory module of Claim 12, wherein the first number of ranks is four, and the second number of ranks is two.

28. (New) The memory module of Claim 12, wherein the first number of ranks is two, and the second number of ranks is one.

29. (New) The memory module of Claim 12, wherein the set of input control signals comprises two chip-select signals and an address signal and the set of output control signals comprises four chip-select signals.

30. (New) The memory module of Claim 12, wherein the printed circuit board is mountable in a module slot of the computer system, the printed circuit board having a plurality of edge connections electrically coupled to corresponding contacts of the module slot.

31. (New) The memory module of Claim 12, wherein the plurality of memory devices are arranged to provide a first memory density per rank, and the set of output control signals corresponds to a second memory density per rank, the second memory density greater than the first memory density per rank.

REMARKS

The foregoing amendments and the following remarks are responsive to the January 26, 2007 Office Action. Claims 1-11 and 14-20 are cancelled without prejudice, Claim 12 is amended, Claim 13 remains as originally filed, and new Claims 21-31 are added. Thus, Claims 12, 13, and 21-31 are presented for further consideration. Please enter the amendments and reconsider the claims in view of the following remarks.

Response to Objection to the Drawings

In the January 26, 2007 Office Action, the Examiner objects to Figures 1A-3A for having various unlabeled rectangular boxes, and suggests that these boxes be provided with descriptive text labels.

Applicants respectfully traverse this objection and assert that Figures 1A-3A as originally filed are sufficiently clear without these descriptive text labels. However, to expedite allowance of the present application, Applicants are submitting herewith amended drawings as replacement sheets (labeled "Replacement Sheet") in accordance with 37 C.F.R. § 1.121(d). In these replacement sheets, text labels are provided for the memory devices 31, 33, logic element 40, PLC 42, multiplexers 44, 46, phase-lock loop device 50, register 60, and SPD device 70 for Figures 1A-3A. Applicants submit that these amendments of the drawings do not add new matter to the present application. Applicants respectfully request that the Examiner withdraw the objection to the drawings.

Affirmation of Election Made in Response to Election/Restriction Requirement

In the January 26, 2007 Office Action, the Examiner requires Applicants to affirm a provisional election made without traverse to prosecute Claims 1-15 by Applicants' representative, Bruce S. Itchkawitz, in a telephone conversation with the Examiner on January 10, 2007. The Examiner indicates that Claims 16-20 are withdrawn from further consideration, as being drawn to a non-elected invention.

Applicants hereby affirm this election without traverse. To expedite allowance of the present application, Applicants have cancelled Claims 16-20 without prejudice, reserving the right to pursue allowance of these claims by continuation practice. Applicants respectfully request that the Examiner consider the patentability of the remaining pending claims.

Comments on Allowable Subject Matter

In the January 26, 2007 Office Action, the Examiner states that Claims 12 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As described herein, Applicants have amended Claim 12 to be in independent form including all of the limitations of the base claim and any intervening claims. Therefore, Applicants submit that Claim 12 is in condition for allowance. Claim 13 depends from Claim 12, so Applicants submit that Claim 13 is also in condition for allowance. Applicants respectfully request that the Examiner withdraw the objection of Claims 12 and 13 and pass these claims to allowance.

Response to Rejection of Claims 1, 2, 8-10, 14, and 15 Under 35 U.S.C. § 103(a)

In the January 26, 2007 Office Action, the Examiner rejects Claims 1, 2, 8-10, 14, and 15 as being unpatentable over U.S. Patent No. 7,120,727 issued to Lee et al. ("Lee"). Applicants respectfully traverse this rejection. However, in the interest of expediting allowance of the present application, Applicants have cancelled Claims 1, 2, 8-10, 14, and 15 without prejudice, reserving the right to pursue allowance of these claims by continuation practice. Applicants respectfully request that the Examiner consider the patentability of the remaining pending claims.

Response to Rejection of Claims 4-7 Under 35 U.S.C. § 103(a)

In the January 26, 2007 Office Action, the Examiner rejects Claims 4-7 as being unpatentable over Lee as supported by Barr (NPL "How Programmable Logic Works"). Applicants respectfully traverse this rejection. However, in the interest of expediting allowance of the present application, Applicants have cancelled Claims 4-7 without prejudice, reserving the right to pursue allowance of these claims by continuation practice. Applicants respectfully request that the Examiner consider the patentability of the remaining pending claims.

Response to Rejection of Claims 1-3, 8, 11, and 14 Under 35 U.S.C. § 103(a)

In the January 26, 2007 Office Action, the Examiner rejects Claims 1-3, 8, 11, and 14 as being unpatentable over U.S. Patent No. 4,392,212 issued to Miyasaka et al. ("Miyasaka"). Applicants respectfully traverse this rejection. However, in the interest of expediting allowance of the present application, Applicants have cancelled Claims 1-3, 8, 11, and 14 without prejudice, reserving the right to pursue allowance of these claims by continuation practice. Applicants respectfully request that the Examiner consider the patentability of the remaining pending claims.

Response to Rejection of Claims 4-7 Under 35 U.S.C. § 103(a)

In the January 26, 2007 Office Action, the Examiner rejects Claims 4-7 as being unpatentable over Miyasaka as supported by Barr. Applicants respectfully traverse this rejection. However, in the interest of expediting allowance of the present application, Applicants have cancelled Claims 4-7 without prejudice, reserving the right to pursue allowance of these claims by continuation practice. Applicants respectfully request that the Examiner consider the patentability of the remaining pending claims.

Comments on New Claims 21-31

Applicants have added new Claims 21-31, each of which depends from Claim 12. Applicants submit that the limitations of Claims 21-31 generally correspond to those of Claims 2-7, 9-11, 14, and 15, respectively, and that these new claims do not add new matter. Applicants respectfully request that the Examiner consider the patentability of new Claims 21-31 and pass these claims to allowance.

Summary

For the foregoing reasons, Applicants submit that Claims 12, 13, and 21-31 are in condition for allowance, and Applicants respectfully request such action.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

Dated: 6/19/07 By: _____

Bruce S. Itchkawitz
Registration No. 47,677
KNOBBE, MARTENS, OLSON & BEAR, LLP
Attorney of Record
2040 Main Street
Fourteenth Floor
Irvine, CA 92614
(949) 760-0404

3828455
053107

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/173,175	07/01/2005	Jayesh R. Bhakta	NETL.018CP1	6355

20995 7590 01/26/2007

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
SOFOCLEOUS, ALEXANDER	
ART UNIT	PAPER NUMBER
2824	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	01/26/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 01/26/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jcartee@kmob.com
eOAPilot@kmob.com

Office Action Summary	Application No.	Applicant(s)	
	11/173,175	BHAKTA ET AL.	
	Examiner	Art Unit	
	Alexander Sofocleous	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *16-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,14 and 15* is/are rejected.

7)☒ Claim(s) *12 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 July 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *20070111*.
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *EAST search history*.

DETAILED ACTION

1. This action is responsive to the following communications: the Application filed July 01, 2005, and the Information Disclosure Statement filed December 2, 2005.

2. Claims 1-15 are pending in the case. Claims 16-20 are withdrawn from consideration. Claim 1 is an independent claim.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-15, drawn to memory with address decoder, classified in class 365, subclass 230.06.

II. Claims 16-17, drawn to memory with ranks, classified in class 365, subclass 230.03.

III. Claims 18-20, drawn to memory with data strobe, classified in class 365, subclass 193.

Inventions Group I and Group II and Group III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination Group I has separate utility such as requiring a logic element coupled to the printed circuit board. See MPEP § 806.05(d).

The examiner has required restriction between subcombinations usable together. Where applicant elects a subcombination and claims thereto are subsequently found

allowable, any claim(s) depending from or otherwise requiring all the limitations of the allowable subcombination will be examined for patentability in accordance with 37 CFR 1.104. See MPEP § 821.04(a). Applicant is advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application.

Because these inventions are independent or distinct for the reasons given above and there would be a serious burden on the examiner if restriction is not required because the inventions have acquired a separate status in the art in view of their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Attorney Bruce Itchkawitz on January 10, 2007 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-15. Affirmation of this election must be made by applicant in replying to this Office action. Claims 16-20 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Information Disclosure Statement

3. Acknowledgment is made of Applicant's Information Disclosure Statement (IDS) Form PTO-1449 filed on December, 2, 2005. This IDS has been considered.

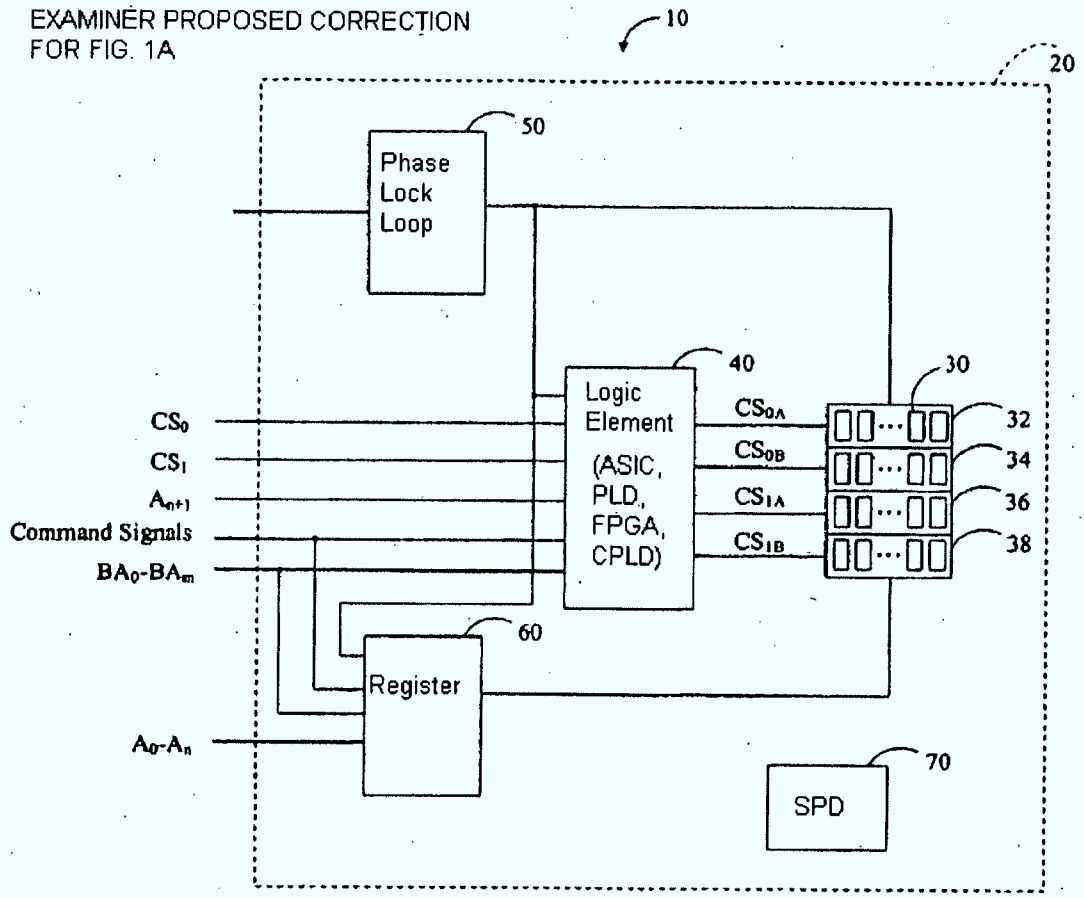
Examiner notes that the Non-Patent Literature (NPL) cited on this IDS (citations

17-25) were submitted with parent application 11/335875. These references have been considered.

Drawings

4. Figures 1A - 3A are objected to because the unlabeled rectangular box(es) shown in the Figures (Fig. 1A, Fig. 1B, Fig. 1C, Fig. 2A, Fig. 2B, Fig. 3A) should be provided with descriptive text labels. For clarity purposes, Examiner suggests the following proposed correction for Figure 1A:

Figure 1A:
EXAMINER PROPOSED CORRECTION FOR FIG. 1A



Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1, 2, 8-10, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (U.S. Patent 7,120,727).**

Regarding independent claim 1, Lee et al. teach a memory module (Fig. 5 [54a, 54b, 54n]) connectable to a computer system (see Fig. 5 [104, 108, 110, 112, 114, 118, 120, 124]), the memory module comprising:

a printed circuit board;

a plurality of memory devices (Fig. 5 [70]), the plurality of memory devices having a first number of memory devices (see Fig. 2 [74, 80, 86, 88]);

and a logic element (Fig. 2 [60]), the logic element receiving a set of input control signals from the computer system (see Fig. 2 [62]), the set of input control signals corresponding to a second number of memory devices (see Fig. 2 [74, 80, 86, 88]) smaller than the first number of memory devices, the logic element generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of memory devices (see column 4, lines 23-26 and 46-63).

Lee et al. are silent with respect to the provision of the memory module comprising a printed circuit board. However, it is well-known in the art to manufacture a memory on a printed circuit board so it may be used in a personal computer system.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to manufacture the memory modules of Lee et al. on a printed circuit board for the purposes of using the memory in a personal computer system.

Regarding dependent claim 2, Lee et al. teach the memory devices comprise dynamic random-access memory (DRAM) devices (see column 4, lines 4-5).

Regarding independent claim 8, Lee et al. teach the plurality of memory

devices are arranged in a first number of ranks (Fig. 2 [74, 80, 86, 88]), and the set of input control signals corresponds to a second number of ranks of memory modules, the second number of ranks less than the first number of ranks (see column 4, lines 23-26 and 46-63).

Regarding dependent claim 9 and 10, Lee et al. teach four ranks that are accessible as two ranks or as one rank (see column 4, lines 23-26 and 46-63).

Regarding dependent claim 14, Lee et al. are silent with respect to a printed circuit board mountable in a module slot of the computer system, the printed circuit board having a plurality of edge connections electrically coupled to corresponding contacts of the module slot. However, it is well-known in the art to manufacture a memory on a printed circuit board with edge connections so it may be used in a personal computer system (module slot on a motherboard).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to manufacture the memory modules of Lee et al. on a printed circuit board for the purposes of using the memory in a personal computer system.

Regarding dependent claim 15, Lee et al. disclose the plurality of memory devices are arranged to provide a first memory density per rank, and the set of output control signals corresponds to a second memory density per rank, the second memory density greater than the first memory density per rank (see column 4, lines 35-45). The indicated column directly teaches operating modes of the memory to allow different bandwidth rates; however, the bandwidth rate is determined by how many ranks connected to the memory hub are grouped together (accessible together) through link

58.

7. **Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (U.S. Patent 7,120,727) as supported by Barr (NPL "How Programmable Logic Works").**

Lee et al. are silent with respect to the logic element being an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device. However, Lee et al. teach the computer register programs the memory hub of each memory module.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device for the logic device such that the memory module would be programmable. Barr further supports that ASICs, FPGAs, CPLDs are commonly used in memory circuitry as address decoders.

8. **Claims 1-3, 8, 11, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyasaka et al. (U.S. Patent 4,392,212).**

Regarding independent claim 1, Miyasaka et al. teach a semiconductor memory comprising:

a plurality of memory devices (Fig. 2), the plurality of memory devices having a first number of memory devices (Fig. 2 [1, 1', 1",1"']);

and a logic element (Fig. 2 [6, 7, 8]) coupled to the semiconductor memory, the

logic element receiving a set of input control signals from the computer system (Fig. 4 [SEL_1, SEL_2]), the set of input control signals corresponding to a second number of memory devices smaller than the first number of memory devices, the logic element generating a set of output control signals (Fig. 4 [S_1, $/S_1$, S_2, $/S_2$]) in response to the set of input control signals, the set of output control signals corresponding to the first number of memory devices.

Miyasaka et al. are silent with respect to the memory being provided on a memory module that is on a printed circuit board. However, it is well-known in the art to manufacture a memory on a printed circuit board so it may be used in a personal computer system.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to manufacture the semiconductor memory of Miyasaka et al. on memory modules on a printed circuit board for the purposes of using the memory in a personal computer system.

Regarding dependent claim 2, Miyasaka et al. teach the memory to be RAM (see column 1, line 11). Miyasaka et al. are silent with respect to the memory being DRAM. However, it is well-known in the art to implement memory using DRAM because it is cost effective.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use DRAM for Miyasaka et al. RAM for the purposes of reducing the costs of the memory.

Regarding dependent claim 3, Miyasaka et al. teach the set of input control

signals comprises a first number of chip-select signals (see Fig. 4 [SEL_1, SEL_2]), and wherein the set of output control signals comprises a second number of chip-select signals (see Fig. 4 [S_1, $/S_1$, S_2, $/S_2$]), wherein the first number of chip-select signals is less than the second number of chip-select signals, the memory module simulating a virtual memory module having the second number of memory devices.

Regarding dependent claim 8, Miyasaka et al. teach the plurality of memory devices are arranged in a first number of ranks, and the set of input control signals Fig. 4 [SEL_1, SEL_2]) corresponds to a second number of ranks of memory modules (one), the second number of ranks less than the first number of ranks (four) (see Fig. 4[S_1, $/S_1$, S_2, $/S_2$, Cells No. 1- Cells No.4]).

Regarding dependent claim 11, Miyasaka et al. teach the set of input control signals comprises two chip-select signals (Fig. 4 [SEL_1, SEL_2]) and an address signal (see Fig. 1B [ADR]) and the set of output control signals comprises four chip-select signals (Fig. 4[S_1, $/S_1$, S_2, $/S_2$]).

Regarding dependent claim 14, Miyasaka et al. are silent with respect to the memory being provided on a memory module that is on a printed circuit board. However, it is well-known in the art to manufacture a memory on a printed circuit board with edge connections so it may be used in a personal computer system (module slot on a motherboard).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to manufacture the semiconductor memory of Miyasaka et al. on memory modules on a printed circuit board for the purposes of using the memory in a

personal computer system.

9. **Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyasaka et al. (U.S. Patent 4,392,212) as supported by Barr (NPL "How Programmable Logic Works").**

Miyasaka et al. are silent with respect to the logic element being an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device. However, Barr supports that ASICs, FPGAs, CPLDs are commonly used in memory circuitry as address decoders.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device for the logic device such that the memory module would be programmable in a commonly known fashion.

Allowable Subject Matter

10. **Claims 12-13 are objected to as being dependent upon a rejected base claim**, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject

matter:

With respect to dependent claim 12 (and claim 13 which depends therefrom), there is no teaching or suggestion in the prior art to the logic element generating a second command signal based on the first command signal, wherein the first command signal corresponds to the second number of ranks and the second command signal corresponds to the first number of ranks, and wherein the second number of ranks is less than the first number of ranks (as per dependent claim 8 from which this claim depends).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Raghuram (U.S. Patent Application Publication 2006/0126369), Raghuram (U.S. Patent Application 2006/0129755), Jakobs (U.S. Patent 6,982,893), Dodd et al. (U.S. Patent 6,981,089), and Moon (U.S. Patent 5,426753).

Raghuram '369 and '755, both filed after provisional application 60/588244, show a memory module with a decoder that receives N number of select signals that are inputted into a decoder and outputted as 2^N number of ranks select signals.

Jakobs shows a memory module receiving rank select signals (two) that correspond to the ranks (two).

Dodd et al. show a memory module receiving rank select signals (two) that correspond to the ranks (two).

Moon shows a memory with a decoder coupled to a microprocessor.

When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating appropriate paragraphs.

A shortened statutory period for response to this action is set to expire three months and zero days from the date of this letter. Failure to respond within the period for response will cause this application to become abandoned (see MPEP 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Sofocleous whose telephone number is 571-272-0635. The examiner can normally be reached on 7:00am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGS

SON DINH
PRIMARY PATENT EXAMINER

Interview Summary	Application No.	Applicant(s)	
	11/173,175	BHAKTA ET AL.	
	Examiner	Art Unit	
	Alexander Sofocleous	2824	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Alexander Sofocleous (PTO personnel)*. (3)_____.

(2) *Attorney Bruce Itchkawitz (App's rep; reg 47,677)*. (4)_____.

Date of Interview: *10 January 2007*.

Type: a)☒ Telephonic b)☐ Video Conference
c)☐ Personal [copy given to: 1)☐ applicant 2)☐ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☒ No.
If Yes, brief description: _____.

Claim(s) discussed: *1-20*.

Identification of prior art discussed: *none*.

Agreement with respect to the claims f)☒ was reached. g)☐ was not reached. h)☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *On 1/9/2007, Examiner contacted Attorney Itchkawitz regarding the following restriction: Group I claims 1-15 (subclass 230.06), Group II claims 16-17 (subIcass 230.03), and Group III claims 18-20 (subclass 193). On 1/10/2007, Attorney Itchkawitz contacted Examiner to elect Group I without traverse*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN A NON-EXTENDABLE PERIOD OF THE LONGER OF ONE MONTH OR THIRTY DAYS FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.

Examiner's signature, if required

PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Multiple sheets used when necessary)

SHEET 1 OF 2

Application No.	11/173,175
Filing Date	July 1, 2005
First Named Inventor	Jayesh R. Bhakta
Art Unit	2824
Examiner	Alexander Sofocleous
Attorney Docket No.	NETL.018CP1

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Publication Date	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
AGS	1	5,247,643	09/21/1993	Shottan	
	2	5,703,826	12/30/1997	Hush et al.	
	3	6,154,418	11/28/2000	Li	
	4	6,453,381 B1	09/17/2002	Yuan et al.	
	5	6,518,794 B2	02/11/2003	Coteus et al.	
	6	6,681,301 B1	01/20/2004	Mehta et al.	
	7	6,785,189 B2	08/31/2004	Jacobs et al.	
	8	6,807,125 B2	10/19/2004	Coteus et al.	
	9	6,813,196 B2	11/02/2004	Park et al.	
	10	2001/0052057 A1	12/13/2001	Lai et al.	
	11	2002/0088633 A1	07/11/2002	Kong et al.	
	12	2003/0063514 A1	04/03/2003	Faue	
	13	2003/0191995 A1	10/09/2003	Abrosimov et al.	
	14	2003/0210575 A1	11/13/2003	Seo et al.	
	15	2004/0037158 A1	02/26/2004	Coteus et al.	
AGS	16	2005/0036378 A1	02/17/2005	Kawaguchi et al.	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author, title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[1]
AGS	17	CUPPU, Vinodh, et al., "A Performance Comparison of Contemporary DRAM Architectures," IEEE Proceedings of the 26th International Symposium on Computer Architecture, May 2-4, 1999, Atlanta, Georgia, pp. 1-12.	
	18	JEDEC Standard No. 21-C, 4.20-2 – 168 Pin, PC133 SDRAM Registered Design Specification, Revision 1.4, Release 11a, February 2002.	
	19	JEDEC Standard No. 21-C, 4.20-3 – 144 Pin, PC133 SDRAM Unbuffered SO-DIMM, Reference Design Specification, Revision 1.02, Release 11.	
	20	JEDEC Standard No. 21-C, DDR SDRAM PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification, Revision 1.3, Release 11b, January 2002.	
	21	JEDEC Standard No. 21-C, 4.20.5 – 184 Pin, PC1600/2100 DDR SDRAM Unbuffered DIMM Design Specification, Revision 1.1, Release 11b.	
AGS	22	JEDEC Standard No. 21-C, 4.20.6 – 200 Pin, PC2700/PC2100/PC1600 DDR SDRAM Unbuffered SO-DIMM Reference Design Specification, Revision 1.1, Release 11b, April 26, 2002.	

Examiner Signature	/Alexander Sofocleous/	Date Considered	01/11/2007

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] - Place a check mark in this area when an English language Translation is attached.

PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT		
	Application No.	11/173,175
	Filing Date	July 1, 2005
	First Named Inventor	Jayesh R. Bhakta
	Art Unit	2824
(Multiple sheets used when necessary)	Examiner	Alexander Sofocleous
SHEET 2 OF 2	Attorney Docket No.	NETL.018CP1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author, title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[1]
AGS	23	JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification," published February 2004.	
↓	24	INTEL CORPORATION, PC SDRAM Registered DIMM Design Support Document, Revision 1.2, October 1998.	
AGS	25	INTEL CORPORATION, 66/100 MHz PC SDRAM 64-Bit Non-ECC/Parity 144 Pin Unbuffered SO-DIMM Specification, Revision 1.0, February 1999.	

2074187
113005

Examiner Signature	/Alexander Sofocleous/	Date Considered	01/11/2007

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] - Place a check mark in this area when an English language Translation is attached.

Notice of References Cited	Application/Control No. 11/173,175	Applicant(s)/Patent Under Reexamination BHAKTA ET AL.	
	Examiner Alexander Sofocleous	Art Unit 2824	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,120,727	10-2006	Lee et al.	711/5
*	B	US-4,392,212	07-1983	Miyasaka et al.	365/230.06
*	C	US-2006/0129755	06-2006	Raghuram, Siva	711/105
*	D	US-2006/0126369	06-2006	Raghuram, Siva	365/051
*	E	US-6,982,893	01-2006	Jakobs, Andreas	365/63
*	F	US-6,981,089	12-2005	Dodd et al.	710/308
*	G	US-5,426,753	06-1995	Moon, Sung W.	711/5
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Barr, Michael. "Programmable Logic: What's it to Ya?," Embedded Systems Programming, June 1999, pp75-84. Retrieved by Examiner from http://www.netrino.com/Articles/ProgrammableLogic/index.php
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

Bib Data Sheet

CONFIRMATION NO. 6355

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/173,175	07/01/2005 RULE	365	2824	NETL.018CP1

APPLICANTS

Jayesh R. Bhakta, Cerritos, CA;
Jeffrey C. Solomon, Irvine, CA;

**** CONTINUING DATA ***************************

This application is a CIP of 11/075,395 03/07/2005 which claims benefit of 60/550,668 03/05/2004
and claims benefit of 60/575,595 05/28/2004
and claims benefit of 60/588,244 07/15/2004 OK. AGJ

**** FOREIGN APPLICATIONS *********************

NONE. AGJ

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 07/22/2005

		STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
Foreign Priority claimed	☐ yes ☒ no	CA	18	20	4
35 USC 119 (a-d) conditions met	☐ yes ☐ no ☐ Met after Allowance				
Verified and Acknowledged	Examiner's Signature / Initials AGJ				

ADDRESS
20995

TITLE

Memory module decoder

FILING FEE RECEIVED		
1330	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11173175	BHAKTA ET AL.
	Examiner	Art Unit
	Sofocleous, Alexander	2824

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	01/09/2007	01/12/2007							
	1	+	✓							
	2	+	✓							
	3	+	✓							
	4	+	✓							
	5	+	✓							
	6	+	✓							
	7	+	✓							
	8	+	✓							
	9	+	✓							
	10	+	✓							
	11	+	✓							
	12	+	O							
	13	+	O							
	14	+	✓							
	15	+	✓							
	16	+	N							
	17	+	N							
	18	+	N							
	19	+	N							
	20	+	N							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11173175	BHAKTA ET AL.
	Examiner	Art Unit
	Sofocleous, Alexander	2824

SEARCHED			
Class	Subclass	Date	Examiner
326	105	01/09/2007	AGS
365	230.06	01/09/2007	AGS
711	5, 211	01/09/2007	AGS

SEARCH NOTES		
Search Notes	Date	Examiner
see EAST search history	01/09/2007	AGS

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	11/173175.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 13:40
S2	126	(rank with four) (memory adj module)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 13:35
S3	3	(rank near2 decoder) (memory adj module)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 11:52
S4	1	(10/037436).APP.	USPAT; USOCR	AND	ON	2007/01/09 12:55
S5	1	(10/100312).APP.	USPAT; USOCR	AND	ON	2007/01/09 12:56
S6	1	(09/023170).APP.	USPAT; USOCR	AND	ON	2007/01/09 13:30
S7	4039	(365/230.06).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/09 13:33
S8	1	S2 S7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 13:33
S9	776	(rank) (memory adj module)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 13:35

EAST Search History

S10	9	S7 S9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 13:40
S11	540234	CS$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 13:41
S12	546176	CS$2 or "CS.sub."$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 13:41
S13	203	S9 S12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 13:41
S14	201	S9 S11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 13:41
S15	8638	"CS.sub."$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 13:41
S16	6	S9 S15	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 13:41
S17	1	(10/453466).APP.	USPAT; USOCR	AND	ON	2007/01/09 14:05

EAST Search History

S18	5905	((326/105) or (365/230.06) or (711/5,211)).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/09 14:06
S19	18	S15 S18	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 14:21
S20	43	S9 S18	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/01/09 14:06
S21	56	((SOLOMON-JEFF SOLOMON-JEFFREY SOLOMON-JEFFREY-C) (BHAKTA-J BHAKTA-JAY BHAKTA-JAYESH-R BHAKTA-J-R)).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/09 14:24
S23	44	((SOLOMON-JEFF SOLOMON-JEFFREY SOLOMON-JEFFREY-C) (BHAKTA-J BHAKTA-JAY BHAKTA-JAYESH-R BHAKTA-J-R)).in. and (memory)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/09 14:24
S24	3	((SOLOMON-JEFF SOLOMON-JEFFREY SOLOMON-JEFFREY-C) and (BHAKTA-J BHAKTA-JAY BHAKTA-JAYESH-R BHAKTA-J-R)). in. and (memory)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/09 14:24
S25	1	(11/217056).APP.	USPAT; USOCR	AND	ON	2007/01/09 14:33
S26	1	(10/037436).APP.	USPAT; USOCR	AND	ON	2007/01/09 14:37
S27	1	(10/601104).APP.	USPAT; USOCR	AND	ON	2007/01/09 14:47

EAST Search History

S28	6	(11/010942 10/797941 10/850382). app. ("6683372" "5332922" "20020112119").pn.	US-PGPUB; USPAT; USOCR	OR	ON	2007/01/12 12:06
S29	16	("20010052057"|"20020088633"|"20030063514"|"20030191995"|"20030210275"|"20030210575"|"20040037158"|"20050036378"|"5247643"|"5703826"|"6154418"|"6453381"|"6518794"|"6785189"|"6807125"|"6813196").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/01/12 12:07

PATENT

Case Docket No. NETL.018CP1
Date: November 30, 2005

TRANSMITTAL LETTER
RESPONSE TO MISSING PARTS

Applicants	:	Jayesh R. Bhakta et al.
App. No	:	11/173,175
Filed	:	July 1, 2005
For	:	MEMORY MODULE DECODER
Art Unit	:	2818
Examiner	:	Unknown

CERTIFICATE OF MAILING

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Mail Stop Missing Parts, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

November 30, 2005
(Date)

Bruce S. Itchkawitz, Reg. No. 47,877

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Notice to File Missing Parts of Application Under 37 CFR 1.53(f), which was mailed by the Office on July 22, 2005, enclosed are:

(X) Executed Declaration by inventors in two (2) pages;

(X) Executed Power of Attorney and copy of Assignment in four (4) pages;

(X) Copy of Notice to File Missing Parts in two (2) pages;

(X) Information Disclosure Statement in one (1) page, with PTO Form SB/08 Equivalent in two (2) pages, citing twenty-five (25) references (no copies of references required); and

(X) Return prepaid postcard.

12/05/2005 FMETEKI1 00000044 11173175
06 FC:1253 1020.00 OP

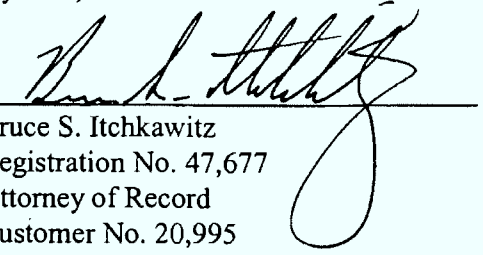
(X) Fees as calculated below:

FEE CALCULATION				
FEE TYPE		**FEE CODE**	**CALCULATION**	**TOTAL**
Basic Filing Fee	1.16(a)(1)	1011 ($300)		$300
Search Fee	1.16(k)	1111 ($500)		$500
Examination Fee	1.16(o)	1311 ($200)		$200
Total Claims	20 - 20 = 0	1202 ($50)		N/A
Independent Claims	4 - 3 = 1	1201 ($200)	1 x 200 =	$200
Multiple Claim		1203 ($360)		N/A
Application Size Fee	65 - 100 = 0	1081 ($250)		N/A
1 Month Extension	1.17(a)(1)	1251 ($120)		N/A
2 Month Extension	1.17(a)(2)	1252 ($450)		N/A
3 Month Extension	1.17(a)(3)	1253 ($1,020)		$1,020
4 Month Extension	1.17(a)(4)	1254 ($1,590)		N/A
5 Month Extension	1.17(a)(5)	1255 ($2,160)		N/A
Surcharge	1.16(e)	1051 ($130)		$130
			SUB TOTAL	$2,350
The present application qualifies for Small Entity status under 37 CFR § 1.27. **Fee reduced by ½.**				N/A
			TOTAL FEE DUE	**$2,350**

(X) An extension of time of three (3) months is hereby requested.

(X) A check in the amount of **$2,350.00** to cover the above fees is enclosed.

The Commissioner is hereby authorized to charge any additional fees which may be required, now or in the future, or credit any overpayment, to Account No. 11-1410.



Bruce S. Itchkawitz
Registration No. 47,677
Attorney of Record
Customer No. 20,995
(949) 760-0404

2124969
113005

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
11/173,175	07/01/2005		NETL.018CP1

CONFIRMATION NO. 6355

20995
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

FORMALITIES LETTER

OC000000016593636

Date Mailed: 07/22/2005

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

12/05/2005 FMETEKI1 00000044 11173175

01 FC:1011	300.00 OP	**FILED UNDER 37 CFR 1.53(b)**
02 FC:1111	500.00 OP	
03 FC:1311	200.00 OP	***Filing Date Granted***
04 FC:1201	200.00 OP	
05 FC:1051	130.00 OP	

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
  Applicant must submit $ **300** *to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).*
- The oath or declaration is missing. *A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.*
  Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(f) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Additional claim fees of $**200** as a non-small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is $**1330** for a Large Entity

- **$300** Statutory basic filing fee.
- **$130** Late oath or declaration Surcharge.

- The application search fee has not been paid. Applicant must submit **$500** to complete the search fee.
- The application examination fee has not been paid. Applicant must submit **$200** to complete the examination fee for a large entity

- Total additional claim fee(s) for this application is **$200**

  - **$200** for **1** independent claims over 3.

Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

A copy of this notice MUST be returned with the reply.

Office of Initial Patent Examination (703) 308-1202
PART 2 - COPY TO BE RETURNED WITH RESPONSE

Attorney's Docket No. NETL.018CP1

DECLARATION - USA PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, mailing address and citizenship are as stated below next to my name;

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled MEMORY MODULE DECODER; the specification of which was filed on July 1, 2005 as Application Serial No. 11/173,175.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims;

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56;

I hereby claim the benefit under Title 35, United States Codes § 119(e) of any United States provisional applications listed below.

Application No.: 60/550,668	Filing Date: March 5, 2004
Application No.: 60/575,595	Filing Date: May 28, 2004
Application No.: 60/588,244	Filing Date: July 15, 2004

I hereby claim the benefit under Title 35, United States Code, § 120 of the United States application listed below, and insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56, which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U.S.A. Application

Application No.: 11/075,395 Filing Date: March 7, 2005 Status: Pending

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first inventor: **Jayesh R. Bhakta**

Inventor's signature Jayesh R. Bhakta

Date Nov. 9. 2005

Residence: 12220 Rose Street, Cerritos, California 90703

Citizenship: United States

Mailing Address: Same

Full name of second inventor: **Jeffrey C. Solomon**

Inventor's signature Jeffrey C Solomon

Date Nov. 9, 2005

Residence: 16 Silver Fir, Irvine, California 92604

Citizenship: United States

Mailing Address: Same

Send Correspondence To:
KNOBBE, MARTENS, OLSON & BEAR, LLP
Customer No. 20,995

2004344
101905

ETL.018CP1 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jayesh R. Bhakta et al.
App. No.	:	11/173,175
Filed	:	July 1, 2005
For	:	MEMORY MODULE DECODER
Examiner	:	Unknown

ESTABLISHMENT OF RIGHT OF ASSIGNEE TO TAKE ACTION
AND
REVOCATION AND POWER OF ATTORNEY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The undersigned is empowered to act on behalf of the assignee below (the "Assignee"). A true copy of the original Assignment of the above-captioned application from the inventors to the Assignee is attached hereto. This Assignment represents the entire chain of title of this invention from the inventors to the Assignee.

I declare that all statements made herein are true, and that all statements made upon information and belief are believed to be true, and further, that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001, and that willful, false statements may jeopardize the validity of the application, or any patent issuing thereon.

The undersigned hereby revokes any previous powers of attorney in the subject application, and hereby appoints the registrants of Knobbe, Martens, Olson & Bear, LLP,

App. No. : 11/173,175
Filed : July 1, 2005

Customer No. 20,995, as its attorneys with full power of substitution and revocation to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected herewith. This appointment is to be to the exclusion of the inventors and their attorney(s) in accordance with the provisions of 37 C.F.R. § 3.71.

Please use **Customer No. 20,995** for all communications.

NETLIST, INC.

Dated: 11/28/05

By: _____
Christopher Lopes

Title: Vice President

Address: 475 Goddard, Suite 100
Irvine, California 92618

2004366
101905

ASSIGNMENT

WHEREAS, We, Jayesh R. Bhakta, a United States citizen, residing at 12220 Rose Street, Cerritos, California 90703, and Jeffrey C. Solomon, a United States citizen, residing at 16 Silver Fir, Irvine, California 92604, have invented certain new and useful improvements in a MEMORY MODULE DECODER for which we have filed an application for Letters Patent in the United States, Application No. 11/173,175, filed on July 1, 2005;

AND WHEREAS, Netlist, Inc. (hereinafter "ASSIGNEE"), a Delaware corporation, with its principal place of business at 475 Goddard, Suite 100, Irvine, California 92618, desires to acquire the entire right, title, and interest in and to the said improvements and the said Application:

NOW, THEREFORE, in consideration of good and valuable consideration, the receipt of which is hereby acknowledged, we, the said inventors, do hereby acknowledge that we have sold, assigned, transferred and set over, and by these presents do hereby sell, assign, transfer and set over, unto the said ASSIGNEE, its successors, legal representatives and assigns, the entire right, title, and interest throughout the world in, to and under the said improvements, and the said application and all provisional applications relating thereto, and all divisions, renewals and continuations thereof, and all Letters Patent of the United States which may be granted thereon and all reissues and extensions thereof, and all rights of priority under International Conventions and applications for Letters Patent which may hereafter be filed for said improvements in any country or countries foreign to the United States, and all Letters Patent which may be granted for said improvements in any country or countries foreign to the United States and all extensions, renewals and reissues thereof; and we hereby authorize and request the Commissioner of Patents of the United States, and any Official of any country or countries foreign to the United States, whose duty it is to issue patents on applications as aforesaid, to issue all Letters Patent for said improvements to the said ASSIGNEE, its successors, legal representatives and assigns, in accordance with the terms of this instrument.

AND WE DO HEREBY sell, assign, transfer, and convey to ASSIGNEE, his successors, legal representatives, and assigns all claims for damages and all remedies arising out of any violation of the rights assigned hereby that may have accrued prior to the date of assignment to ASSIGNEE, or may accrue hereafter, including, but not limited to, the right to sue for, collect, and retain damages for past infringements of the said Letters Patent before or after issuance.

AND WE HEREBY covenant and agree that we will communicate to the said ASSIGNEE, its successors, legal representatives and assigns, any facts known to us respecting said improvements, and testify in any legal proceeding, sign all lawful papers, execute all divisional, continuing and reissue applications, make all rightful oaths and generally do everything possible to aid the said ASSIGNEE, its successors, legal representatives and assigns, to obtain and enforce proper patent protection for said improvements in all countries.

IN TESTIMONY WHEREOF, I hereunto set my hand and seal this 23 day of NOV, 2005.

Jayesh R. Bhakta

Jayesh R. Bhakta

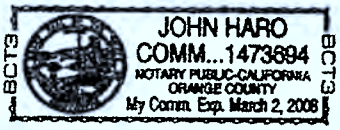
STATE OF CALIFORNIA)
} ss.
COUNTY OF ORANGE)

On 23RD NOV, 2005 before me, JOHN HARO NOTARY personally appeared Jayesh R. Bhakta, ~~personally known to me~~ (or proved to me on the basis of satisfactory evidence) to be the person whose name is subscribed to the within instrument, and acknowledged to me that he executed the same in his authorized capacity, and that by his signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

COPY

WITNESS my hand and official seal.

[SEAL]



Notary Signature

IN TESTIMONY WHEREOF, I hereunto set my hand and seal this 23rd day of November, 2005.

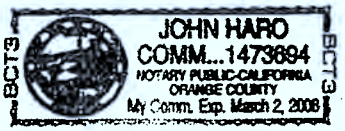
Jeffrey C. Solomon

STATE OF CALIFORNIA }
} ss.
COUNTY OF ORANGE }

On 23RD NOV, 2005, before me, JOHN HARO NOTARY, personally appeared Jeffrey C. Solomon, ~~personally known to me~~ (or proved to me on the basis of satisfactory evidence) to be the person whose name is subscribed to the within instrument, and acknowledged to me that he executed the same in his authorized capacity, and that by his signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

WITNESS my hand and official seal.

[SEAL]



Notary Signature

2004325
101905

Docket No.: NETL.018CP1 **Customer No. 20,995**

INFORMATION DISCLOSURE STATEMENT

Applicants	:	Jayesh R. Bhakta et al.
App. No	:	11/173,175
Filed	:	July 1, 2005
For	:	MEMORY MODULE DECODER
Examiner	:	Unknown
Art Unit	:	2818

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed is a PTO/SB/08 Equivalent listing twenty-five (25) references that are of record in U.S. patent application No. 11/075,395, filed March 7, 2005, which is the parent of this continuation-in-part application, and is relied upon for an earlier filing date under 35 U.S.C. § 120. Copies of the references are not submitted pursuant to 37 C.F.R. § 1.98(d).

This Information Disclosure Statement is being filed before the receipt of a first Office Action on the merits, and presumably no fee is required. If a first Office Action on the merits was mailed before the mailing date of this Statement, the Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: November 30, 2005

By: _____

Bruce S. Itchkawitz
Registration No. 47,677
Attorney of Record
Customer No. 20,995
(949) 760-0404

2074236
113005

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Multiple sheets used when necessary)

SHEET 1 OF 2

Application No.	11/173,175
Filing Date	July 1, 2005
First Named Inventor	Jayesh R. Bhakta
Art Unit	2818
Examiner	Unknown
Attorney Docket No.	NETL.018CP1

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Publication Date	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	1	5,247,643	09/21/1993	Shottan	
	2	5,703,826	12/30/1997	Hush et al.	
	3	6,154,418	11/28/2000	Li	
	4	6,453,381 B1	09/17/2002	Yuan et al.	
	5	6,518,794 B2	02/11/2003	Coteus et al.	
	6	6,681,301 B1	01/20/2004	Mehta et al.	
	7	6,785,189 B2	08/31/2004	Jacobs et al.	
	8	6,807,125 B2	10/19/2004	Coteus et al.	
	9	6,813,196 B2	11/02/2004	Park et al.	
	10	2001/0052057 A1	12/13/2001	Lai et al.	
	11	2002/0088633 A1	07/11/2002	Kong et al.	
	12	2003/0063514 A1	04/03/2003	Faue	
	13	2003/0191995 A1	10/09/2003	Abrosimov et al.	
	14	2003/0210575 A1	11/13/2003	Seo et al.	
	15	2004/0037158 A1	02/26/2004	Coteus et al.	
	16	2005/0036378 A1	02/17/2005	Kawaguchi et al.	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author, title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[1]
	17	CUPPU, Vinodh, et al., "A Performance Comparison of Contemporary DRAM Architectures," IEEE Proceedings of the 26th International Symposium on Computer Architecture, May 2-4, 1999, Atlanta, Georgia, pp. 1-12.	
	18	JEDEC Standard No. 21-C, 4.20-2 – 168 Pin, PC133 SDRAM Registered Design Specification, Revision 1.4, Release 11a, February 2002.	
	19	JEDEC Standard No. 21-C, 4.20-3 – 144 Pin, PC133 SDRAM Unbuffered SO-DIMM, Reference Design Specification, Revision 1.02, Release 11.	
	20	JEDEC Standard No. 21-C, DDR SDRAM PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification, Revision 1.3, Release 11b, January 2002.	
	21	JEDEC Standard No. 21-C, 4.20.5 – 184 Pin, PC1600/2100 DDR SDRAM Unbuffered DIMM Design Specification, Revision 1.1, Release 11b.	
	22	JEDEC Standard No. 21-C, 4.20.6 – 200 Pin, PC2700/PC2100/PC1600 DDR SDRAM Unbuffered SO-DIMM Reference Design Specification, Revision 1.1, Release 11b, April 26, 2002.	

Examiner Signature	Date Considered

***Examiner**: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

T[1] - Place a check mark in this area when an English language Translation is attached.

PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	11/173,175
	Filing Date	July 1, 2005
	First Named Inventor	Jayesh R. Bhakta
	Art Unit	2818
(Multiple sheets used when necessary)	Examiner	Unknown
SHEET 2 OF 2	Attorney Docket No.	NETL.018CP1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author, title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[1]
	23	JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification," published February 2004.	
	24	INTEL CORPORATION, PC SDRAM Registered DIMM Design Support Document, Revision 1.2, October 1998.	
	25	INTEL CORPORATION, 66/100 MHz PC SDRAM 64-Bit Non-ECC/Parity 144 Pin Unbuffered SO-DIMM Specification, Revision 1.0, February 1999.	

2074187
113005

Examiner Signature	Date Considered

***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

T[1] - Place a check mark in this area when an English language Translation is attached.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
11/173,175	07/01/2005		NETL.018CP1

CONFIRMATION NO. 6355

20995
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

FORMALITIES LETTER

OC000000016593636

Date Mailed: 07/22/2005

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
  Applicant must submit $ **300** *to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).*
- The oath or declaration is missing. *A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.*
  Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(f) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Additional claim fees of $**200** as a non-small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is $**1330** for a Large Entity

- **$300** Statutory basic filing fee.
- **$130** Late oath or declaration Surcharge.

- The application search fee has not been paid. Applicant must submit **$500** to complete the search fee.
- The application examination fee has not been paid. Applicant must submit **$200** to complete the examination fee for a large entity

- Total additional claim fee(s) for this application is **$200**

  - **$200** for **1** independent claims over 3.

Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

A copy of this notice MUST be returned with the reply.

Office of Initial Patent Examination (703) 308-1202

PART 3 - OFFICE COPY

UTILITY APPLICATION

Attorney Docket No.: NETL.018CP1
First Named Inventor: Not yet named
Title: MEMORY MODULE DECODER
Express Mail Label No.: EV 309179335 US

Direct all correspondence to Customer No.: 20995

Date: July 1, 2005

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

The following enclosures are transmitted herewith to be filed in the patent application of:

Inventor(s): Not yet named

APPLICATION:

(X) Specification in forty-seven (47) pages;

(X) Drawings in eighteen (18) sheets; and

(X) Return prepaid postcard

CONTINUITY INFORMATION:

Application	Relationship	Parent App. No.	Filing Date	Status
This Application	Continuation-in-Part of	11/075,395	03/07/05	Pending
11/075,395	Claims Benefit of	60/550,668	03/05/04	N/A
11/075,395	Claims Benefit of	60/575,595	05/28/04	N/A
This Application	Claims Benefit of	60/588,244	07/15/04	N/A

Reference to prior domestic applications is made in the:

(X) Reference to prior domestic applications is made in the specification.

FILING FEES:

FEE CALCULATION				
FEE TYPE		**FEE CODE**	**CALCULATION**	**TOTAL**
Basic Utility	*1.16(a)(1)*	1011 ($300)		$300
Search Fee	*1.16(k)*	1111 ($500)		$500
Examination Fee	*1.16(o)*	1311 ($200)		$200
Excess Claims > 20	20 - 20 = 0	1202 ($50)	0 x 50 =	0
Independent > 3	4 - 3 = 1	1201 ($200)	1 x 200 =	$200
Multiple Claim	*1.16(j)*	1203 ($360)		0
Application Size Fee	65 - 100 = 0	1081 ($250)±	0 x 250 =	N/A
Recordation Fee	*1.21(h)*	8021 ($40)	0 x 40 =	N/A
Non-English Spec.	*1.17(i)*	1053 ($130)		N/A
			TOTAL FEE DUE	$1,200

(X) The total fees calculated above will be paid at a later date.

Bruce S. Itchkawitz
Registration No. 47,677
Attorney of Record
Customer No. 20,995
(949) 760-0404

1799064
070105

Knobbe Martens Olson & Bear LLP
Intellectual Property Law

2040 Main Street
Fourteenth Floor
Irvine, CA 92614
Tel 949-760-0404
Fax 949-760-9502
www.kmob.com

Bruce S. Itchkawitz, Ph.D.
bsi@kmob.com

EV309179335US

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATE OF MAILING BY "EXPRESS MAIL"

Attorney Docket No.	:	NETL.018CP1
Applicant(s)	:	Not yet named
For	:	MEMORY MODULE DECODER
Attorney	:	Bruce S. Itchkawitz
"Express Mail" Label No.:		EV 309179335 US
Date of Deposit	:	July 1, 2005

I hereby certify that the accompanying

Transmittal Letter; Specification in 47 Pages; 18 Sheets of Drawings; Return Prepaid Postcard

are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and are addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Nelson Merida

1799091
070105

MEMORY MODULE DECODER

Cross-Reference to Related Applications

[0001] The present application is a continuation-in-part of U.S. Patent Application No. 11/075,395, filed March 7, 2005, which claims the benefit of U.S. Provisional Application No. 60/550,668, filed March 5, 2004 and U.S. Provisional Application No. 60/575,595, filed May 28, 2004. The present application also claims the benefit of U.S. Provisional Application No. 60/588,244, filed July 15, 2004, which is incorporated in its entirety by reference herein.

Background of the Invention

Field of the Invention

[0002] The present invention relates generally to memory modules of a computer system, and more specifically to devices and methods for improving the performance, the memory capacity, or both, of memory modules.

Description of the Related Art

[0003] Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the processor of the computer system. Memory modules typically have a memory configuration with a unique combination of rows, columns, and banks which result in a total memory capacity for the memory module.

[0004] For example, a 512-Megabyte memory module (termed a "512-MB" memory module, which actually has 2^{29} or 536,870,912 bytes of capacity) will typically utilize eight 512-Megabit DRAM devices (each identified as a "512-Mb" DRAM device, each actually having 2^{29} or 536,870,912 bits of capacity). The memory cells (or memory locations) of each 512-Mb DRAM device can be arranged in four banks, with each bank having an array of 2^{24} (or 16,777,216) memory locations arranged as 2^{13} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 64M 8-bit-wide memory locations (actually with four banks of 2^{27} or 134,217,728 one-bit

memory cells arranged to provide a total of 2^{26} or 67,108,864 memory locations with 8 bits each) are identified as having a "64Mb x 8" or "64M x 8-bit" configuration, or as having a depth of 64M and a bit width of 8. Furthermore, certain commercially-available 512-MB memory modules are termed to have a "64M x 8-byte" configuration or a "64M x 64-bit" configuration with a depth of 64M and a width of 8 bytes or 64 bits.

[0005] Similarly, a 1-Gigabyte memory module (termed a "1-GB" memory module, which actually has 2^{30} or 1,073,741,824 bytes of capacity) can utilize eight 1-Gigabit DRAM devices (each identified as a "1-Gb" DRAM device, each actually having 2^{30} or 1,073,741,824 bits of capacity). The memory locations of each 1-Gb DRAM device can be arranged in four banks, with each bank having an array of memory locations with 2^{14} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 128M 8-bit-wide memory locations (actually with a total of 2^{27} or 134,217,728 memory locations with 8 bits each) are identified as having a "128Mb x 8" or "128M x 8-bit" configuration, or as having a depth of 128M and a bit width of 8. Furthermore, certain commercially-available 1-GB memory modules are identified as having a "128M x 8-byte" configuration or a "128M x 64-bit" configuration with a depth of 128M and a width of 8 bytes or 64 bits.

[0006] The commercially-available 512-MB (64M x 8-byte) memory modules and the 1-GB (128M x 8-byte) memory modules described above are typically used in computer systems (e.g., personal computers) which perform graphics applications since such "x 8" configurations are compatible with data mask capabilities often used in such graphics applications. Conversely, memory modules with "x 4" configurations are typically used in computer systems such as servers which are not as graphics-intensive. Examples of such commercially available "x 4" memory modules include, but are not limited to, 512-MB (128M x 4-byte) memory modules comprising eight 512-Mb (128Mb x 4) memory devices.

[0007] The DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width. For example, a memory module in which each rank of the memory module is 64 bits wide is described as having an "x 64" organization. Similarly, a memory module having 72-bit-wide ranks is described as having an "x 72" organization.

[0008] The memory capacity of a memory module increases with the number of memory devices. The number of memory devices of a memory module can be increased by increasing the number of memory devices per rank or by increasing the number of ranks. For example, a memory module with four ranks has double the memory capacity of a memory module with two ranks and four times the memory capacity of a memory module with one rank. Rather than referring to the memory capacity of the memory module, in certain circumstances, the memory density of the memory module is referred to instead.

[0009] During operation, the ranks of a memory module are selected or activated by control signals that are received from the processor. Examples of such control signals include, but are not limited to, rank-select signals, also called chip-select signals. Most computer and server systems support one-rank and two-rank memory modules. By only supporting one-rank and two-rank memory modules, the memory density that can be incorporated in each memory slot is limited.

Summary of the Invention

[0010] In certain embodiments, a memory module is connectable to a computer system. The memory module comprises a printed circuit board, a plurality of memory devices coupled to the printed circuit board, and a logic element coupled to the printed circuit board. The plurality of memory devices has a first number of memory devices. The logic element receives a set of input control signals from the computer system. The set of input control signals corresponds to a second number of memory devices smaller than the first number of memory devices. The logic element generates a set of output control signals in response to the set of input control signals. The set of output control signals corresponds to the first number of memory devices.

[0011] In certain embodiments, a method utilizes a memory module in a computer system. The method comprises coupling the memory module to the computer system. The memory module comprises a plurality of memory devices arranged in a first number of ranks. The method further comprises inputting a first set of control signals to the memory module. The first set of control signals corresponds to a second number of ranks smaller than the first number of ranks. The method further comprises generating a second set of control signals in

response to the first set of control signals. The second set of control signals corresponds to the first number of ranks.

[0012] In certain embodiments, a memory module is connectable to a computer system. The memory module comprises a plurality of memory devices arranged in a first number of ranks. The memory module comprises means for coupling the memory module to the computer system. The memory module further comprises means for inputting a first set of control signals to the memory module. The first set of control signals corresponds to a second number of ranks smaller than the first number of ranks. The memory module further comprises means for generating a second set of control signals in response to the first set of control signals. The second set of control signals corresponds to the first number of ranks.

[0013] In certain embodiments, a memory module is connectable to a computer system. The memory module comprises a first memory device having a first data signal line and a first data strobe signal line. The memory module further comprises a second memory device having a second data signal line and a second data strobe signal line. The memory module further comprises a common data signal line connectable to the computer system. The memory module further comprises an isolation device electrically coupled to the first data signal line, to the second data signal line, and to the common data signal line. The isolation device selectively alternates between electrically coupling the first data signal line to the common data signal line and electrically coupling the second data signal line to the common data signal line.

Brief Description of the Drawings

[0014] Figure 1A schematically illustrates an exemplary memory module with four ranks of memory devices compatible with certain embodiments described herein.

[0015] Figure 1B schematically illustrates an exemplary memory module with two ranks of memory devices compatible with certain embodiments described herein.

[0016] Figure 1C schematically illustrates another exemplary memory module in accordance with certain embodiments described herein.

[0017] Figure 2A schematically illustrates an exemplary memory module which doubles the rank density in accordance with certain embodiments described herein.

[0018] Figure 2B schematically illustrates an exemplary logic element compatible with embodiments described herein.

[0019] Figure 3A schematically illustrates an exemplary memory module which doubles number of ranks in accordance with certain embodiments described herein.

[0020] Figure 3B schematically illustrates an exemplary logic element compatible with embodiments described herein.

[0021] Figure 4A shows an exemplary timing diagram of a gapless read burst for a back-to-back adjacent read condition from one memory device.

[0022] Figure 4B shows an exemplary timing diagram with an extra clock cycle between successive read commands issued to different memory devices for successive read accesses from different memory devices.

[0023] Figure 5 shows an exemplary timing diagram in which the last data strobe of memory device "a" collides with the pre-amble time interval of the data strobe of memory device "b."

[0024] Figure 6A schematically illustrates a circuit diagram of a conventional memory module showing the interconnections between the DQ data signal lines of two memory devices and their DQS data strobe signal lines.

[0025] Figure 6B schematically illustrates a circuit diagram of an exemplary memory module comprising an isolation device in accordance with certain embodiments described herein.

[0026] Figure 6C schematically illustrates an isolation device comprising a logic element which multiplexes the DQS data strobe signal lines from one another.

[0027] Figure 6D schematically illustrates an isolation device which multiplexes the DQS data strobe signal lines from one another and which multiplexes the DQ data signal lines from one another.

[0028] Figure 6E schematically illustrates an isolation device which comprises the logic element on the DQ data signal lines but not a corresponding logic element on the DQS data strobe signal lines.

[0029] Figure 7 schematically illustrates an exemplary memory module in which a data strobe (DQS) pin of a first memory device is electrically connected to a DQS pin of a second memory device while both DQS pins are active.

[0030] Figure 8 is an exemplary timing diagram of the voltages applied to the two DQS pins due to non-simultaneous switching.

[0031] Figure 9 schematically illustrates another exemplary memory module in which a DQS pin of a first memory device is connected to a DQS pin of a second memory device.

[0032] Figure 10 schematically illustrates an exemplary memory module in accordance with certain embodiments described herein.

[0033] Figures 11A and 11B schematically illustrate a first side and a second side, respectively, of a memory module with eighteen 64M x 4 bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board.

[0034] Figures 12A and 12B schematically illustrate an exemplary embodiment of a memory module in which a first resistor and a second resistor are used to reduce the current flow between the first DQS pin and the second DQS pin.

[0035] Figure 13 schematically illustrates another exemplary memory module compatible with certain embodiments described herein.

[0036] Figure 14 schematically illustrates a particular embodiment of the memory module schematically illustrated by Figure 13.

Detailed Description of Exemplary Embodiments

[0037] Most high-density memory modules are currently built with 512-Megabit ("512-Mb") memory devices wherein each memory device has a 64M x 8-bit configuration. For example, a 1-Gigabyte ("1-GB") memory module with error checking capabilities can be fabricated using eighteen such 512-Mb memory devices. Alternatively, it can be economically advantageous to fabricate a 1-GB memory module using lower-density memory devices and doubling the number of memory devices used to produce the desired word width. For example, by fabricating a 1-GB memory module using thirty-six 256-Mb memory devices with 64M x 4-bit configuration, the cost of the resulting 1-GB memory module can be reduced since the unit cost of each 256-Mb memory device is typically lower than one-half

the unit cost of each 512-Mb memory device. The cost savings can be significant, even though twice as many 256-Mb memory devices are used in place of the 512-Mb memory devices.

[0038] Market pricing factors for DRAM devices are such that higher-density DRAM devices (e.g., 1-Gb DRAM devices) are much more than twice the price of lower-density DRAM devices (e.g., 512-Mb DRAM devices). In other words, the price per bit ratio of the higher-density DRAM devices is greater than that of the lower-density DRAM devices. This pricing difference often lasts for months or even years after the introduction of the higher-density DRAM devices, until volume production factors reduce the costs of the newer higher-density DRAM devices. Thus, when the cost of a higher-density DRAM device is more than the cost of two lower-density DRAM devices, there is an economic incentive for utilizing pairs of the lower-density DRAM devices to replace individual higher-density DRAM devices.

[0039] Figure 1A schematically illustrates an exemplary memory module 10 compatible with certain embodiments described herein. The memory module 10 is connectable to a computer system (not shown). The memory module 10 comprises a printed circuit board 20 and a plurality of memory devices 30 coupled to the printed circuit board 20. The plurality of memory devices 30 has a first number of memory devices. The memory module 10 further comprises a logic element 40 coupled to the printed circuit board 20. The logic element 40 receives a set of input control signals from the computer system. The set of input control signals correspond to a second number of memory devices smaller than the first number of memory devices. The logic element 40 generates a set of output control signals in response to the set of input control signals. The set of output control signals corresponds to the first number of memory devices.

[0040] In certain embodiments, as schematically illustrated in Figure 1A, the memory module 10 further comprises a phase-lock loop device 50 coupled to the printed circuit board 20 and a register 60 coupled to the printed circuit board 20. In certain embodiments, the phase-lock loop device 50 and the register 60 are each mounted on the printed circuit board 20. In response to signals received from the computer system, the phase-lock loop device 50 transmits clock signals to the plurality of memory devices 30, the

logic element 40, and the register 60. The register 60 receives and buffers a plurality of control signals, including address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals), and transmits corresponding signals to the appropriate memory devices 30. In certain embodiments, the register 60 comprises a plurality of register devices. While the phase-lock loop device 50, the register 60, and the logic element 40 are described herein in certain embodiments as being separate components, in certain other embodiments, two or more of the phase-lock loop device 50, the register 60, and the logic element 40 are portions of a single component. Persons skilled in the art are able to select a phase-lock loop device 50 and a register 60 compatible with embodiments described herein.

[0041] In certain embodiments, the memory module 10 further comprises electrical components which are electrically coupled to one another and are surface-mounted or embedded on the printed circuit board 20. These electrical components can include, but are not limited to, electrical conduits, resistors, capacitors, inductors, and transistors. In certain embodiments, at least some of these electrical components are discrete, while in other certain embodiments, at least some of these electrical components are constituents of one or more integrated circuits.

[0042] Various types of memory modules 10 are compatible with embodiments described herein. For example, memory modules 10 having memory capacities of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, as well as other capacities, are compatible with embodiments described herein. In addition, memory modules 10 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. Furthermore, memory modules 10 compatible with embodiments described herein include, but are not limited to, single in-line memory modules (SIMMs), dual in-line memory modules (DIMMs), small-outline DIMMs (SO-DIMMs), unbuffered DIMMs (UDIMMs), registered DIMMs (RDIMMs), fully-buffered DIMM (FBDIMM), mini-DIMMs, and micro-DIMMs.

[0043] In certain embodiments, the printed circuit board 20 is mountable in a module slot of the computer system. The printed circuit board 20 of certain such embodiments has a plurality of edge connections electrically coupled to corresponding

contacts of the module slot and to the various components of the memory module 10, thereby providing electrical connections between the computer system and the components of the memory module 10.

[0044] Memory devices 30 compatible with embodiments described herein include, but are not limited to, random-access memory (RAM), dynamic random-access memory (DRAM), synchronous DRAM (SDRAM), and double-data-rate DRAM (e.g., DDR-1, DDR-2, DDR-3). In addition, memory devices 30 having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with embodiments described herein. Memory devices 30 compatible with embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μBGA), mini-BGA (mBGA), and chip-scale packaging (CSP). Memory devices 30 compatible with embodiments described herein are available from a number of sources, including but not limited to, Samsung Semiconductor, Inc. of San Jose, California, Infineon Technologies AG of San Jose, California, and Micron Technology, Inc. of Boise, Idaho. Persons skilled in the art can select appropriate memory devices 30 in accordance with certain embodiments described herein.

[0045] In certain embodiments, the plurality of memory devices 30 are arranged in a first number of ranks. For example, in certain embodiments, the memory devices 30 are arranged in four ranks, as schematically illustrated by Figure 1A. In other embodiments, the memory devices 30 are arranged in two ranks, as schematically illustrated by Figure 1B. Other numbers of ranks of the memory devices 30 are also compatible with embodiments described herein.

[0046] In certain embodiments, the logic element 40 comprises a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, or a complex programmable-logic device (CPLD). In certain embodiments, the logic element 40 is a custom device. Sources of logic elements 40 compatible with embodiments described herein include, but are not limited to, Lattice Semiconductor Corporation of Hillsboro, Oregon, Altera Corporation of San Jose, California, and Xilinx Incorporated of San Jose, California. In certain embodiments, the logic element 40 comprises various discrete electrical elements, while in

certain other embodiments, the logic element 40 comprises one or more integrated circuits. Persons skilled in the art can select an appropriate logic element 40 in accordance with certain embodiments described herein.

[0047] As schematically illustrated by Figures 1A and 1B, in certain embodiments, the logic element 40 receives a set of input control signals, which includes address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) and command signals (e.g., refresh, precharge) from the computer system. In response to the set of input control signals, the logic element 40 generates a set of output control signals which includes address signals and command signals.

[0048] In certain embodiments, the set of output control signals corresponds to a first number of ranks in which the plurality of memory devices 30 of the memory module 10 are arranged, and the set of input control signals corresponds to a second number of ranks per memory module for which the computer system is configured. The second number of ranks in certain embodiments is smaller than the first number of ranks. For example, in the exemplary embodiment as schematically illustrated by Figure 1A, the first number of ranks is four while the second number of ranks is two. In the exemplary embodiment of Figure 1B, the first number of ranks is two while the second number of ranks is one. Thus, in certain embodiments, even though the memory module 10 actually has the first number of ranks of memory devices 30, the memory module 10 simulates a virtual memory module by operating as having the second number of ranks of memory devices 30. In certain embodiments, the memory module 10 simulates a virtual memory module when the number of memory devices 30 of the memory module 10 is larger than the number of memory devices 30 per memory module for which the computer system is configured to utilize.

[0049] In certain embodiments, the computer system is configured for a number of ranks per memory module which is smaller than the number of ranks in which the memory devices 30 of the memory module 10 are arranged. In certain such embodiments, the computer system is configured for two ranks of memory per memory module (providing two chip-select signals CS_0, CS_1) and the plurality of memory modules 30 of the memory module 10 are arranged in four ranks, as schematically illustrated by Figure 1A. In certain other such

embodiments, the computer system is configured for one rank of memory per memory module (providing one chip-select signal CS_0) and the plurality of memory modules 30 of the memory module 10 are arranged in two ranks, as schematically illustrated by Figure 1B.

[0050] In the exemplary embodiment schematically illustrated by Figure 1A, the memory module 10 has four ranks of memory devices 30 and the computer system is configured for two ranks of memory devices per memory module. The memory module 10 receives row/column address signals or signal bits (A_0-A_{n+1}), bank address signals (BA_0-BA_m), chip-select signals (CS_0 and CS_1), and command signals (e.g., refresh, precharge, etc.) from the computer system. The A_0-A_n row/column address signals are received by the register 60, which buffers these address signals and sends these address signals to the appropriate ranks of memory devices 30. The logic element 40 receives the two chip-select signals (CS_0, CS_1) and one row/column address signal (A_{n+1}) from the computer system. Both the logic element 40 and the register 60 receive the bank address signals (BA_0-BA_m) and at least one command signal (e.g., refresh, precharge, etc.) from the computer system.

Logic Tables

[0051] Table 1 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices 30 using chip-select signals.

Table 1:

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

Note:

1. CS_0, CS_1, CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are active low signals.
2. A_{n+1} is an active high signal.
3. 'x' is a Don't Care condition.
4. Command involves a number of command signals that define operations such as refresh, precharge, and other operations.

[0052] In Logic State 1: CS_0 is active low, A_{n+1} is non-active, and Command is active. CS_{0A} is pulled low, thereby selecting Rank 0.

[0053] In Logic State 2: CS_0 is active low, A_{n+1} is active, and Command is active. CS_{0B} is pulled low, thereby selecting Rank 1.

[0054] In Logic State 3: CS_0 is active low, A_{n+1} is Don't Care, and Command is active high. CS_{0A} and CS_{0B} are pulled low, thereby selecting Ranks 0 and 1.

[0055] In Logic State 4: CS_1 is active low, A_{n+1} is non-active, and Command is active. CS_{1A} is pulled low, thereby selecting Rank 2.

[0056] In Logic State 5: CS_1 is active low, A_{n+1} is active, and Command is active. CS_{1B} is pulled low, thereby selecting Rank 3.

[0057] In Logic State 6: CS_1 is active low, A_{n+1} is Don't Care, and Command is active. CS_{1A} and CS_{1B} are pulled low, thereby selecting Ranks 2 and 3.

[0058] In Logic State 7: CS_0 and CS_1 are pulled non-active high, which deselects all ranks, i.e., CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are pulled high.

[0059] The "Command" column of Table 1 represents the various commands that a memory device (e.g., a DRAM device) can execute, examples of which include, but are not limited to, activation, read, write, precharge, and refresh. In certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of Table 1). In such embodiments, the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both associated ranks (e.g., state 6 of Table 1). In such embodiments, the command signal (e.g., refresh) is sent to both memory devices to ensure that the memory content of the memory devices remains valid over time. Certain embodiments utilize a logic table such as that of Table 1 to simulate a single memory device from two memory devices by selecting two ranks concurrently.

[0060] Table 2 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices 30 using gated CAS signals.

Table 2:

CS*	RAS*	CAS*	WE*	Density Bit	A_{10}	Command	CAS0*	CAS1*
1	x	x	x	x	x	NOP	x	x
0	1	1	1	x	x	NOP	1	1
0	0	1	1	0	x	ACTIVATE	1	1
0	0	1	1	1	x	ACTIVATE	1	1
0	1	0	1	0	x	READ	0	1
0	1	0	1	1	x	READ	1	0
0	1	0	0	0	x	WRITE	0	1
0	1	0	0	1	x	WRITE	1	0
0	0	1	0	0	0	PRECHARGE	1	1
0	0	1	0	1	0	PRECHARGE	1	1
0	0	1	0	x	1	PRECHARGE	1	1
0	0	0	0	x	x	MODE REG SET	0	0
0	0	0	1	x	x	REFRESH	0	0

[0061] In certain embodiments in which the density bit is a row address bit, for read/write commands, the density bit is the value latched during the activate command for the selected bank.

Serial-Presence-Detect Device

[0062] Memory modules typically include a serial-presence detect (SPD) device 70 (e.g., an electrically-erasable-programmable read-only memory or EEPROM device) comprising data which characterize various attributes of the memory module, including but not limited to, the number of row addresses the number of column addresses, the data width of the memory devices, the number of ranks, the memory density per rank, the number of memory devices, and the memory density per memory device. The SPD device 70 communicates this data to the basic input/output system (BIOS) of the computer system so that the computer system is informed of the memory capacity and the memory configuration available for use and can configure the memory controller properly for maximum reliability and performance.

[0063] For example, for a commercially-available 512-MB (64M x 8-byte) memory module utilizing eight 512-Mb memory devices each with a 64M x 8-bit

configuration, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3: Defines the number of row address bits in the DRAM device in the memory module [13 for the 512-Mb memory device].

Byte 4: Defines the number of column address bits in the DRAM device in the memory module [11 for the 512-Mb memory device].

Byte 13: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 512-Mb (64M x 8-bit) memory device].

Byte 14: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 512-Mb (64M x 8-bit) memory device].

Byte 17: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 512-Mb memory device].

[0064] In a further example, for a commercially-available 1-GB (128M x 8-byte) memory module utilizing eight 1-Gb memory devices each with a 128M x 8-bit configuration, as described above, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3: Defines the number of row address bits in the DRAM device in the memory module [14 for the 1-Gb memory device].

Byte 4: Defines the number of column address bits in the DRAM device in the memory module [11 for the 1-Gb memory device].

Byte 13: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 1-Gb (128M x 8-bit) memory device].

Byte 14: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 1-Gb (128M x 8-bit) memory device].

Byte 17: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 1-Gb memory device].

[0065] In certain embodiments, the SPD device 70 comprises data which characterize the memory module 10 as having fewer ranks of memory devices than the memory module 10 actually has, with each of these ranks having more memory density. For example, for a memory module 10 compatible with certain embodiments described herein having two ranks of memory devices 30, the SPD device 70 comprises data which characterizes the memory module 10 as having one rank of memory devices with twice the memory density per rank. Similarly, for a memory module 10 compatible with certain embodiments described herein having four ranks of memory devices 30, the SPD device 70

comprises data which characterizes the memory module 10 as having two ranks of memory devices with twice the memory density per rank. In addition, in certain embodiments, the SPD device 70 comprises data which characterize the memory module 10 as having fewer memory devices than the memory module 10 actually has, with each of these memory devices having more memory density per memory device. For example, for a memory module 10 compatible with certain embodiments described herein, the SPD device 70 comprises data which characterizes the memory module 10 as having one-half the number of memory devices that the memory module 10 actually has, with each of these memory devices having twice the memory density per memory device.

[0066] Figure 1C schematically illustrates an exemplary memory module 10 in accordance with certain embodiments described herein. The memory module 10 comprises a pair of substantially identical memory devices 31, 33. Each memory device 31, 33 has a first bit width, a first number of banks of memory locations, a first number of rows of memory locations, and a first number of columns of memory locations. The memory module 10 further comprises an SPD device 70 comprising data that characterizes the pair of memory devices 31, 33. The data characterize the pair of memory devices 31, 33 as a virtual memory device having a second bit width equal to twice the first bit width, a second number of banks of memory locations equal to the first number of banks, a second number of rows of memory locations equal to the first number of rows, and a second number of columns of memory locations equal to the first number of columns.

[0067] In certain such embodiments, the SPD device 70 of the memory module 10 is programmed to describe the combined pair of lower-density memory devices 31, 33 as one virtual or pseudo-higher-density memory device. In an exemplary embodiment, two 512-Mb memory devices, each with a 128M x 4-bit configuration, are used to simulate one 1-Gb memory device having a 128M x 8-bit configuration. The SPD device 70 of the memory module 10 is programmed to describe the pair of 512-Mb memory devices as one virtual or pseudo-1-Gb memory device.

[0068] For example, to fabricate a 1-GB (128M x 8-byte) memory module, sixteen 512-Mb (128M x 4-bit) memory devices can be used. The sixteen 512-Mb (128M x 4-bit) memory devices are combined in eight pairs, with each pair serving as a

virtual or pseudo-1-Gb (128M x 8-bit) memory device. In certain such embodiments, the SPD device 70 contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3: 13 row address bits.
Byte 4: 12 column address bits.
Byte 13: 8 bits wide for the primary virtual 1-Gb (128M x 8-bit) memory device.
Byte 14: 8 bits wide for the error checking virtual 1-Gb (128M x 8-bit) memory device.
Byte 17: 4 banks.

[0069] In this exemplary embodiment, bytes 3, 4, and 17 are programmed to have the same values as they would have for a 512-MB (128M x 4-byte) memory module utilizing 512-Mb (128M x 4-bit) memory devices. However, bytes 13 and 14 of the SPD data are programmed to be equal to 8, corresponding to the bit width of the virtual or pseudo-higher-density 1-Gb (128M x 8-bit) memory device, for a total capacity of 1-GB. Thus, the SPD data does not describe the actual-lower-density memory devices, but instead describes the virtual or pseudo-higher-density memory devices. The BIOS accesses the SPD data and recognizes the memory module as having 4 banks of memory locations arranged in 2^{13} rows and 2^{12} columns, with each memory location having a width of 8 bits rather than 4 bits.

[0070] In certain embodiments, when such a memory module 10 is inserted in a computer system, the computer system's memory controller then provides to the memory module 10 a set of input control signals which correspond to the number of ranks or the number of memory devices reported by the SPD device 70. For example, placing a two-rank memory module 10 compatible with certain embodiments described herein in a computer system compatible with one-rank memory modules, the SPD device 70 reports to the computer system that the memory module 10 only has one rank. The logic element 40 then receives a set of input control signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output control signals corresponding to two ranks to the appropriate memory devices 30 of the memory module 10. Similarly, when a two-rank memory module 10 compatible with certain embodiments described herein is placed in a computer system compatible with either one- or two-rank memory modules, the SPD device 70 reports to the computer system that the memory module 10 only has one rank. The logic element 40 then receives a set of input control signals

corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output control signals corresponding to two ranks to the appropriate memory devices 30 of the memory module 10. Furthermore, a four-rank memory module 10 compatible with certain embodiments described herein simulates a two-rank memory module whether the memory module 10 is inserted in a computer system compatible with two-rank memory modules or with two- or four-rank memory modules. Thus, by placing a four-rank memory module 10 compatible with certain embodiments described herein in a module slot that is four-rank-ready, the computer system provides four chip-select signals, but the memory module 10 only uses two of the chip-select signals.

Memory Density Multiplication

[0071] In certain embodiments, two memory devices having a memory density are used to simulate a single memory device having twice the memory density, and an additional address signal bit is used to access the additional memory. Similarly, in certain embodiments, two ranks of memory devices having a memory density are used to simulate a single rank of memory devices having twice the memory density, and an additional address signal bit is used to access the additional memory. As used herein, such simulations of memory devices or ranks of memory devices are termed as "memory density multiplication," and the term "density transition bit" is used to refer to the additional address signal bit which is used to access the additional memory.

[0072] In certain embodiments utilizing memory density multiplication embodiments, the memory module 10 can have various types of memory devices 30 (e.g., DDR1, DDR2, DDR3, and beyond). The logic element 40 of certain such embodiments utilizes implied translation logic equations having variations depending on whether the density transition bit is a row, column, or internal bank address bit. In addition, the translation logic equations of certain embodiments vary depending on the type of memory module 10 (e.g., UDIMM, RDIMM, FBDIMM, etc.). Furthermore, in certain embodiments, the translation logic equations vary depending on whether the implementation multiplies memory devices per rank or multiplies the number of ranks per memory module.

[0073] Table 3A provides the numbers of rows and columns for DDR-1 memory devices, as specified by JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification," published February 2004, and incorporated in its entirety by reference herein.

Table 3A:

	128-Mb	256-Mb	512-Mb	1-Gb
Number of banks	4	4	4	4
Number of row address bits	12	13	13	14
Number of column address bits for "x 4" configuration	11	11	12	12
Number of column address bits for "x 8" configuration	10	10	11	11
Number of column address bits for "x 16" configuration	9	9	10	10

[0074] As described by Table 3A, 512-Mb (128M x 4-bit) DRAM devices have 2^{13} rows and 2^{12} columns of memory locations, while 1-Gb (128M x 8-bit) DRAM devices have 2^{14} rows and 2^{11} columns of memory locations. Because of the differences in the number of rows and the number of columns for the two types of memory devices, complex address translation procedures and structures would typically be needed to fabricate a 1-GB (128M x 8-byte) memory module using sixteen 512-Mb (128M x 4-bit) DRAM devices.

[0075] Table 3B shows the device configurations as a function of memory density for DDR2 memory devices.

Table 3B:

	Number of Rows	Number of Columns	Number of Internal Banks	Page Size (x4s or x8s)
256 Mb	13	10	4	1 KB
512 Mb	14	10	4	1 KB
1 Gb	14	10	8	1 KB
2 Gb	15	10	8	1 KB
4 Gb	to be determined	to be determined	8	1 KB

Table 4 lists the corresponding density transition bit for the density transitions between the DDR2 memory densities of Table 3B.

Table 4:

Density Transition	Density Transition Bit
256 Mb to 512 Mb	A_{13}
512 Mb to 1 Gb	BA_2

1 Gb to 2 Gb	A_{14}
2 Gb to 4 Gb	to be determined

Because the standard memory configuration of 4-Gb DDR2 SDRAM modules is not yet determined by the appropriate standards-setting organization, Tables 3B and 4 have "to be determined" in the appropriate table entries.

[0076] In certain embodiments, the logic translation equations are programmed in the logic element 40 by hardware, while in certain other embodiments, the logic translation equations are programmed in the logic element 40 by software. Examples 1 and 2 provide exemplary sections of Verilog code compatible with certain embodiments described herein. As described more fully below, the code of Examples 1 and 2 includes logic to reduce potential problems due to "back-to-back adjacent read commands which cross memory device boundaries or "BBARX." Persons skilled in the art are able to provide additional logic translation equations compatible with embodiments described herein.

[0077] An exemplary section of Verilog code compatible with memory density multiplication from 512 Mb to 1 Gb using DDR2 memory devices with the BA_2 density transition bit is listed below in Example 1. The exemplary code of Example 1 corresponds to a logic element 40 which receives one chip-select signal from the computer system and which generates two chip-select signals.

[0078] Example 1:

```
always @(posedge clk_in)
  begin
            rs0N_R <= rs0_in_N;     // cs0
            rasN_R <= ras_in_N;
            casN_R <= cas_in_N;
            weN_R <= we_in_N;
  end

// Gated Chip Selects
assign              pcs0a_1 = (~rs0_in_N & ~ras_in_N & ~cas_in_N)                          // ref,md reg set
                    |(~rs0_in_N & ras_in_N & cas_in_N)                                     // ref exit, pwr dn
                    |(~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in)                // pchg all
                    |(~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ~ba2_in)// pchg single bnk
                    |(~rs0_in_N & ~ras_in_N & cas_in_N & we_in_N       & ~ba2_in)          // activate
                    |(~rs0_in_N & ras_in_N & ~cas_in_N              & ~ba2_in)             // xfr
                    ;
assign              pcs0b_1 = (~rs0_in_N & ~ras_in_N & ~cas_in_N)                          // ref,md reg set
                    |(~rs0_in_N & ras_in_N & cas_in_N)                                     // ref exit, pwr dn
                    |(~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in)                // pchg all
                    |(~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ba2_in)// pchg single bnk
                    |(~rs0_in_N & ~ras_in_N & cas_in_N & we_in_N       & ba2_in)           // activate
                    |(~rs0_in_N & ras_in_N & ~cas_in_N              & ba2_in) // xfr
                    ;
//-------------------------------------
  always @(posedge clk_in)
   begin
```

```
            a4_r <= a4_in ;
            a5_r <= a5_in ;
            a6_r <= a6_in ;
            a10_r <= a10_in ;
            ba0_r <= ba0_in ;
            ba1_r <= ba1_in ;
            ba2_r <= ba2_in ;
            q_mrs_cmd_cyc1 <= q_mrs_cmd ;
  end
////////////////////////////////////////////////////////////////
// determine the cas latency
////////////////////////////////////////////////////////////////
assign q_mrs_cmd_r = (!rasN_R & !casN_R & !weN_R)
            & !rs0N_R
          & (!ba0_r & !ba1_r)
            ;       // md reg set cmd

 always @(posedge clk_in)
  if (~reset_N)         // lmr
            cl3 <= 1'b1 ;
  else if (q_mrs_cmd_cyc1)      // load mode reg cmd
  begin
            cl3 <= (~a6_r & a5_r & a4_r ) ;
  end

 always @(posedge clk_in)
  if (~reset_N)             // reset
            cl2 <= 1'b0 ;
  else if (q_mrs_cmd_cyc1)      // load mode reg cmd
  begin
            cl2 <= (~a6_r & a5_r & ~a4_r ) ;
  end

 always @(posedge clk_in)
  if (~reset_N)             // reset
            cl4 <= 1'b0 ;
  else if (q_mrs_cmd_cyc1)      // load mode reg cmd
  begin
            cl4 <= (a6_r & ~a5_r & ~a4_r ) ;
  end

always @(posedge clk_in)
  if (~reset_N)             cl5 <= 1'b0 ;
  else if (q_mrs_cmd_cyc1)      // load mode reg cmd
  begin
            cl5 <= (a6_r & ~a5_r & a4_r ) ;
  end

assign          pre_cyc2_enfet = (wr_cmd_cyc1 & acs_cyc1 & cl3)   // wr brst cl3 preamble
                        ;
assign          pre_cyc3_enfet = (rd_cmd_cyc2 & cl3)              // rd brst cl3 preamble
                        |(wr_cmd_cyc2 & cl3)                      // wr brst cl3 1st pair
                        |(wr_cmd_cyc2 & cl4)                      // wr brst cl4 preamble

                        ;

assign          pre_cyc4_enfet = (wr_cmd_cyc3 & cl3)              // wr brst cl3 2nd pair
                        |(wr_cmd_cyc3 & cl4)                      // wr brst cl4 1st pair

                        |(rd_cmd_cyc3 & cl3)                      // rd brst cl3 1st pair
                        |(rd_cmd_cyc3 & cl4)                      // rd brst cl4 preamble
                        ;

assign          pre_cyc5_enfet = (rd_cmd_cyc4  & cl3)             // rd brst cl3 2nd pair
                        |(wr_cmd_cyc4  & cl4)                     // wr brst cl4 2nd pair

                        |(rd_cmd_cyc4  & cl4)                     // rd brst cl4 1st pair
                        ;
```

```
// dq
assign                  pre_dq_cyc = pre_cyc2_enfet
                          | pre_cyc3_enfet
                          | pre_cyc4_enfet
                          | pre_cyc5_enfet
                          ;

assign                  pre_dq_ncyc = enfet_cyc2
                          | enfet_cyc3
                          | enfet_cyc4
                          | enfet_cyc5
                          ;

// dqs
assign                  pre_dqsa_cyc = (pre_cyc2_enfet & ~ba2_r)
                          | (pre_cyc3_enfet & ~ba2_cyc2)
                          | (pre_cyc4_enfet & ~ba2_cyc3)
                          | (pre_cyc5_enfet & ~ba2_cyc4)
                          ;
assign                  pre_dqsb_cyc = (pre_cyc2_enfet & ba2_r)
                          | (pre_cyc3_enfet & ba2_cyc2)
                          | (pre_cyc4_enfet & ba2_cyc3)
                          | (pre_cyc5_enfet & ba2_cyc4)
                          ;

assign                  pre_dqsa_ncyc = (enfet_cyc2 & ~ba2_cyc2)
                          | (enfet_cyc3 & ~ba2_cyc3)
                          | (enfet_cyc4 & ~ba2_cyc4)
                          | (enfet_cyc5 & ~ba2_cyc5)
                          ;
assign                  pre_dqsb_ncyc = (enfet_cyc2 & ba2_cyc2)
                          | (enfet_cyc3 & ba2_cyc3)
                          | (enfet_cyc4 & ba2_cyc4)
                          | (enfet_cyc5 & ba2_cyc5)
                          ;

always @(posedge clk_in)
  begin
            acs_cyc2 <= acs_cyc1 ;          // cs active
            ba2_cyc2 <= ba2_r ;
            ba2_cyc3 <= ba2_cyc2 ;
            ba2_cyc4 <= ba2_cyc3 ;
            ba2_cyc5 <= ba2_cyc4 ;

            rd_cmd_cyc2 <= rd_cmd_cyc1 & acs_cyc1;
            rd_cmd_cyc3 <= rd_cmd_cyc2 ;
            rd_cmd_cyc4 <= rd_cmd_cyc3 ;
            rd_cmd_cyc5 <= rd_cmd_cyc4 ;
            rd_cmd_cyc6 <= rd_cmd_cyc5 ;
            rd_cmd_cyc7 <= rd_cmd_cyc6 ;

            wr_cmd_cyc2 <= wr_cmd_cyc1 & acs_cyc1;
            wr_cmd_cyc3 <= wr_cmd_cyc2 ;
            wr_cmd_cyc4 <= wr_cmd_cyc3 ;
            wr_cmd_cyc5 <= wr_cmd_cyc4 ;
  end

  always @(negedge clk_in)
   begin
            dq_ncyc <= dq_cyc;
            dqs_ncyc_a <= dqs_cyc_a;
            dqs_ncyc_b <= dqs_cyc_b;
   end

// DQ FET enables
assign          enq_fet1  = dq_cyc  | dq_ncyc          ;
assign          enq_fet2  = dq_cyc  | dq_ncyc  ;
```

```
assign          enq_fet3 = dq_cyc | dq_ncyc          ;
assign            enq_fet4 = dq_cyc | dq_ncyc ;
assign            enq_fet5 = dq_cyc | dq_ncyc ;
// DQS FET enables
assign            ens_fet1a = dqs_cyc_a | dqs_ncyc_a   ;
assign            ens_fet2a = dqs_cyc_a | dqs_ncyc_a   ;
assign            ens_fet3a = dqs_cyc_a | dqs_ncyc_a   ;
assign            ens_fet1b = dqs_cyc_b | dqs_ncyc_b   ;
assign            ens_fet2b = dqs_cyc_b | dqs_ncyc_b   ;
assign            ens_fet3b = dqs_cyc_b | dqs_ncyc_b   ;
```

[0079] Another exemplary section of Verilog code compatible with memory density multiplication from 256 Mb to 512 Mb using DDR2 memory devices and gated CAS signals with the row A_{13} density transition bit is listed below in Example 2. The exemplary code of Example 2 corresponds to a logic element 40 which receives one gated CAS signal from the computer system and which generates two gated CAS signals.

[0080] Example 2:

```
// latched a13 flags cs0, banks 0-3
  always @(posedge clk_in)
   if (actv_cmd_R & ~rs0N_R & ~bnk1_R & ~bnk0_R ) // activate
   begin
            l_a13_00 <= a13_r;
   end
  always @(posedge clk_in)
   if (actv_cmd_R & ~rs0N_R & ~bnk1_R &  bnk0_R)    // activate
   begin
            l_a13_01 <= a13_r;
   end
  always @(posedge clk_in)
   if (actv_cmd_R & ~rs0N_R & bnk1_R & ~bnk0_R)     // activate
   begin
            l_a13_10 <= a13_r;
   end
  always @(posedge clk_in)
   if (actv_cmd_R & ~rs0N_R & bnk1_R & bnk0_R)      // activate
   begin
            l_a13_11 <= a13_r;
   end
// gated cas
assign cas_i = ~(casN_R);
assign  cas0_o = ( ~rasN_R & cas_i)
            |( rasN_R & ~l_a13_00 & ~bnk1_R & ~bnk0_R & cas_i)
            |( rasN_R & ~l_a13_01 & ~bnk1_R &  bnk0_R & cas_i)
            |( rasN_R & ~l_a13_10 &  bnk1_R & ~bnk0_R & cas_i)
            |( rasN_R & ~l_a13_11 &  bnk1_R &  bnk0_R & cas_i)
            ;
assign  cas1_o = ( ~rasN_R  & cas_i)
            |( rasN_R & l_a13_00          & ~bnk1_R & ~bnk0_R & cas_i)
            |( rasN_R & l_a13_01          & ~bnk1_R &  bnk0_R & cas_i)
            |( rasN_R & l_a13_10          &  bnk1_R & ~bnk0_R & cas_i)
            |( rasN_R & l_a13_11          &  bnk1_R &  bnk0_R & cas_i)
            ;
assign      pcas_0_N = ~cas0_o;
assign      pcas_1_N = ~cas1_o;

assign      rd0_o_R1 = rasN_R & cas0_o & weN_R & ~rs0N_R;  // rnk0 rd cmd cyc

assign      rd1_o_R1 = rasN_R & cas1_o & weN_R & ~rs0N_R;  // rnk1 rd cmd cyc

assign      wr0_o_R1 = rasN_R & cas0_o & ~weN_R & ~rs0N_R; // rnk0 wr cmd cyc
```

```
assign      wr1_o_R1 = rasN_R & cas1_o & ~weN_R & ~rs0N_R ; // rnk1 wr cmd cyc

 always @(posedge clk_in)
  begin
            rd0_o_R2 <= rd0_o_R1 ;
            rd0_o_R3 <= rd0_o_R2;
            rd0_o_R4 <= rd0_o_R3;
            rd0_o_R5 <= rd0_o_R4;

            rd1_o_R2 <= rd1_o_R1 ;
            rd1_o_R3 <= rd1_o_R2;
            rd1_o_R4 <= rd1_o_R3;
            rd1_o_R5 <= rd1_o_R4;

            wr0_o_R2 <= wr0_o_R1 ;
            wr0_o_R3 <= wr0_o_R2;
            wr0_o_R4 <= wr0_o_R3;

            wr1_o_R2 <= wr1_o_R1 ;
            wr1_o_R3 <= wr1_o_R2;
            wr1_o_R4 <= wr1_o_R3;
 end

 always @(posedge clk_in)
  begin
  if (
     (rd0_o_R2 & ~rd1_o_R4)                                  // pre-am rd if no ped on rnk 1
   | rd0_o_R3                                                // 1st cyc of rd brst
   | rd0_o_R4                                                // 2nd cyc of rd brst
   | (rd0_o_R5 & ~rd1_o_R2 & ~rd1_o_R3)                      // post-rd cyc if no ped on rnk 1
   | (wr0_o_R1)                                              // pre-am wr
   | wr0_o_R2 | wr0_o_R3                                     // wr brst 1st & 2nd cyc
   | (wr0_o_R4)                                              // post-wr cyc  (chgef9)
   | wr1_o_R1 | wr1_o_R2 | wr1_o_R3 | wr1_o_R4 // rank 1  (chgef9)
    )
                    en_fet_a <= 1'b1;                        // enable fet
 else
                    en_fet_a <= 1'b0;                        // disable fet
 end

 always @(posedge clk_in)
            begin
             if (
                  (rd1_o_R2 & ~rd0_o_R4)
                | rd1_o_R3
                | rd1_o_R4
                | (rd1_o_R5 & ~rd0_o_R2 & ~rd0_o_R3)
               | (wr1_o_R1)                                  // (chgef8)
               | wr1_o_R2 | wr1_o_R3
      | (wr1_o_R4)                                           // post-wr cyc          (chgef9)
      | wr0_o_R1 | wr0_o_R2 | wr0_o_R3 | wr0_o_R4           // rank 0  (chgef9)
                )
                    en_fet_b <= 1'b1;                        //
            else
                    en_fet_b <= 1'b0;
            end
```

[0081] Figure 2A schematically illustrates an exemplary memory module 10 which doubles the rank density in accordance with certain embodiments described herein. The memory module 10 has a first memory capacity. The memory module 10 comprises a plurality of substantially identical memory devices 30 configured as a first rank 32 and a second rank 34. In certain embodiments, the memory devices 30 of the first rank 32 are

configured in pairs, and the memory devices 30 of the second rank 34 are also configured in pairs. In certain embodiments, the memory devices 30 of the first rank 32 are configured with their respective DQS pins tied together and the memory devices 30 of the second rank 34 are configured with their respective DQS pins tied together, as described more fully below. The memory module 10 further comprises a logic element 40 which receives a first set of address and control signals from a memory controller (not shown) of the computer system. The first set of address and control signals is compatible with a second memory capacity substantially equal to one-half of the first memory capacity. The logic element 40 translates the first set of address and control signals into a second set of address and control signals which is compatible with the first memory capacity of the memory module 10 and which is transmitted to the first rank 32 and the second rank 34.

[0082] The first rank 32 of Figure 2A has 18 memory devices 30 and the second rank 34 of Figure 2A has 18 memory devices 30. Other numbers of memory devices 30 in each of the ranks 32, 34 are also compatible with embodiments described herein.

[0083] In the embodiment schematically illustrated by Figure 2A, the memory module 10 has a width of 8 bytes (or 64 bits) and each of the memory devices 30 of Figure 2A has a bit width of 4 bits. The 4-bit-wide ("x 4") memory devices 30 of Figure 2A have one-half the width, but twice the depth of 8-bit-wide ("x 8") memory devices. Thus, each pair of "x 4" memory devices 30 has the same density as a single "x 8" memory device, and pairs of "x 4" memory devices 30 can be used instead of individual "x 8" memory devices to provide the memory density of the memory module 10. For example, a pair of 512-Mb 128M x 4-bit memory devices has the same memory density as a 1-Gb 128M x 8-bit memory device.

[0084] For two "x 4" memory devices 30 to work in tandem to mimic a "x 8" memory device, the relative DQS pins of the two memory devices 30 in certain embodiments are advantageously tied together, as described more fully below. In addition, to access the memory density of a high-density memory module 10 comprising pairs of "x 4" memory devices 30, an additional address line is used. While a high-density memory module comprising individual "x 8" memory devices with the next-higher density would also utilize

an additional address line, the additional address lines are different in the two memory module configurations.

[0085] For example, a 1-Gb 128M x 8-bit DDR-1 DRAM memory device uses row addresses A_{13}-A_0 and column addresses A_{11} and A_9-A_0. A pair of 512-Mb 128M x 4-bit DDR-1 DRAM memory devices uses row addresses A_{12}-A_0 and column addresses A_{12}, A_{11}, and A_9-A_0. In certain embodiments, a memory controller of a computer system utilizing a 1-GB 128M x 8 memory module 10 comprising pairs of the 512-Mb 128M x 4 memory devices 30 supplies the address and control signals including the extra row address (A_{13}) to the memory module 10. The logic element 40 receives the address and control signals from the memory controller and converts the extra row address (A_{13}) into an extra column address (A_{12}).

[0086] Figure 2B schematically illustrates an exemplary logic element 40 compatible with embodiments described herein. The logic element 40 is used for a memory module 10 comprising pairs of "x 4" memory devices 30 which mimic individual "x 8" memory devices. In certain embodiments, each pair has the respective DQS pins of the memory devices 30 tied together. In certain embodiments, as schematically illustrated by Figure 2B, the logic element 40 comprises a programmable-logic device (PLD) 42, a first multiplexer 44 electrically coupled to the first rank 32 of memory devices 30, and a second multiplexer 46 electrically coupled to the second rank 34 of memory devices 30. In certain embodiments, the PLD 42 and the first and second multiplexers 44, 46 are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD 42, first multiplexer 44, and second multiplexer 46 in accordance with embodiments described herein.

[0087] In the exemplary logic element 40 of Figure 2B, during a row access procedure (CAS is high), the first multiplexer 44 passes the A_{12} address through to the first rank 32, the second multiplexer 46 passes the A_{12} address through to the second rank 34, and the PLD 42 saves or latches the A_{13} address from the memory controller. In certain embodiments, a copy of the A_{13} address is saved by the PLD 42 for each of the internal banks (e.g., 4 internal banks) per memory device 30. During a subsequent column access procedure (CAS is low), the first multiplexer 44 passes the previously-saved A_{13} address through to the

first rank 32 as the A_{12} address and the second multiplexer 46 passes the previously-saved A_{13} address through to the second rank 34 as the A_{12} address. The first rank 32 and the second rank 34 thus interpret the previously-saved A_{13} row address as the current A_{12} column address. In this way, in certain embodiments, the logic element 40 translates the extra row address into an extra column address in accordance with certain embodiments described herein.

[0088] Thus, by allowing two lower-density memory devices to be used rather than one higher-density memory device, certain embodiments described herein provide the advantage of using lower-cost, lower-density memory devices to build "next-generation" higher-density memory modules. Certain embodiments advantageously allow the use of lower-cost readily-available 512-Mb DDR-2 SDRAM devices to replace more expensive 1-Gb DDR-2 SDRAM devices. Certain embodiments advantageously reduce the total cost of the resultant memory module.

[0089] Figure 3A schematically illustrates an exemplary memory module 10 which doubles number of ranks in accordance with certain embodiments described herein. The memory module 10 has a first plurality of memory locations with a first memory density. The memory module 10 comprises a plurality of substantially identical memory devices 30 configured as a first rank 32, a second rank 34, a third rank 36, and a fourth rank 38. The memory module 10 further comprises a logic element 40 which receives a first set of address and control signals from a memory controller (not shown). The first set of address and control signals is compatible with a second plurality of memory locations having a second memory density. The second memory density is substantially equal to one-half of the first memory density. The logic element 40 translates the first set of address and control signals into a second set of address and control signals which is compatible with the first plurality of memory locations of the memory module 10 and which is transmitted to the first rank 32, the second rank 34, the third rank 36, and the fourth rank 38.

[0090] Each rank 32, 34, 36, 38 of Figure 3A has 9 memory devices 30. Other numbers of memory devices 30 in each of the ranks 32, 34, 36, 38 are also compatible with embodiments described herein.

[0091] In the embodiment schematically illustrated by Figure 3A, the memory module 10 has a width of 8 bytes (or 64 bits) and each of the memory devices 30 of Figure 3A has a bit width of 8 bits. Because the memory module 10 has twice the number of 8-bit-wide ("x 8") memory devices 30 as does a standard 8-byte-wide memory module, the memory module 10 has twice the density as does a standard 8-byte-wide memory module. For example, a 1-GB 128M x 8-byte memory module with 36 512-Mb 128M x 8-bit memory devices (arranged in four ranks) has twice the memory density as a 512-Mb 128M x 8-byte memory module with 18 512-Mb 128M x 8-bit memory devices (arranged in two ranks).

[0092] To access the additional memory density of the high-density memory module 10, the two chip-select signals (CS_0, CS_1) are used with other address and control signals to gate a set of four gated CAS signals. For example, to access the additional ranks of four-rank 1-GB 128M x 8-byte DDR-1 DRAM memory module, the CS_0 and CS_1 signals along with the other address and control signals are used to gate the CAS signal appropriately, as schematically illustrated by Figure 3A. Figure 3B schematically illustrates an exemplary logic element 40 compatible with embodiments described herein. In certain embodiments, the logic element 40 comprises a programmable-logic device (PLD) 42 and four "OR" logic elements 52, 54, 56, 58 electrically coupled to corresponding ranks 32, 34, 36, 38 of memory devices 30.

[0093] In certain embodiments, the PLD 42 comprises an ASIC, an FPGA, a custom-designed semiconductor device, or a CPLD. In certain embodiments, the PLD 42 and the four "OR" logic elements 52, 54, 56, 58 are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD 42 and appropriate "OR" logic elements 52, 54, 56, 58 in accordance with embodiments described herein.

[0094] In the embodiment schematically illustrated by Figure 3B, the PLD 42 transmits each of the four "enabled CAS" ($ENCAS_0a$, $ENCAS_0b$, $ENCAS_1a$, $ENCAS_1b$) signals to a corresponding one of the "OR" logic elements 52, 54, 56, 58. The CAS signal is also transmitted to each of the four "OR" logic elements 52, 54, 56, 58. The CAS signal and the "enabled CAS" signals are "low" true signals. By selectively activating each of the four

"enabled CAS" signals which are inputted into the four "OR" logic elements 52, 54, 56, 58, the PLD 42 is able to select which of the four ranks 32, 34, 36, 38 is active.

[0095] In certain embodiments, the PLD 42 uses sequential and combinatorial logic procedures to produce the gated CAS signals which are each transmitted to a corresponding one of the four ranks 32, 34, 36, 38. In certain other embodiments, the PLD 42 instead uses sequential and combinatorial logic procedures to produce four gated chip-select signals (e.g., CS_0a, CS_0b, CS_1a, and CS_1b) which are each transmitted to a corresponding one of the four ranks 32, 34, 36, 38.

Back-to-Back Adjacent Read Commands

[0096] Due to their source synchronous nature, DDR SDRAM (e.g., DDR1, DDR2, DDR3) memory devices operate with a data transfer protocol which surrounds each burst of data strobes with a pre-amble time interval and a post-amble time interval. The pre-amble time interval provides a timing window for the receiving memory device to enable its data capture circuitry when a known valid level is present on the strobe signal to avoid false triggers of the memory device's capture circuit. The post-amble time interval provides extra time after the last strobe for this data capture to facilitate good signal integrity. In certain embodiments, when the computer system accesses two consecutive bursts of data from the same memory device, termed herein as a "back-to-back adjacent read," the post-amble time interval of the first read command and the pre-amble time interval of the second read command are skipped by design protocol to increase read efficiency. Figure 4A shows an exemplary timing diagram of this "gapless" read burst for a back-to-back adjacent read condition from one memory device.

[0097] In certain embodiments, when the second read command accesses data from a different memory device than does the first read command, there is at least one time interval (e.g., clock cycle) inserted between the data strobes of the two memory devices. This inserted time interval allows both read data bursts to occur without the post-amble time interval of the first read data burst colliding or otherwise interfering with the pre-amble time interval of the second read data burst. In certain embodiments, the memory controller of the computer system inserts an extra clock cycle between successive read commands issued to

different memory devices, as shown in the exemplary timing diagram of Figure 4B for successive read accesses from different memory devices.

[0098] In typical computer systems, the memory controller is informed of the memory boundaries between the ranks of memory of the memory module prior to issuing read commands to the memory module. Such memory controllers can insert wait time intervals or clock cycles to avoid collisions or interference between back-to-back adjacent read commands which cross memory device boundaries, which are referred to herein as "BBARX."

[0099] In certain embodiments described herein in which the number of ranks of the memory module is doubled or quadrupled, the logic element 40 generates a set of output control signals so that the selection decoding is transparent to the computer system. However, in certain such embodiments, there are memory device boundaries of which the computer system is unaware, so there are occasions in which BBARX occurs without the cognizance of the memory controller of the computer system. As shown in Figure 5, the last data strobe of memory device "a" collides with the pre-amble time interval of the data strobe of memory device "b," resulting in a "collision window."

[0100] Figure 6A schematically illustrates a circuit diagram of a conventional memory module 100 showing the interconnections between the DQ data signal lines 102 of the memory devices "a" and "b" (not shown) and their DQS data strobe signal lines 104. In certain embodiments, the electrical signal lines are etched on the printed circuit board. As shown in Figure 6A, each of the memory devices has their DQ data signal lines 102 electrically coupled to a common DQ line 112 and the DQS data strobe signal lines 104 electrically coupled to a common DQS line 114.

[0101] In certain embodiments, BBARX collisions are avoided by a mechanism which electrically isolates the DQS data strobe signal lines 104 of the memory devices from one another during the transition from the first read data burst of one rank of memory devices to the second read data burst of another rank of memory devices. Figure 6B schematically illustrates a circuit diagram of an exemplary memory module 10 comprising an isolation device 120 in accordance with certain embodiments described herein. As shown in Figure 6B, each of the memory devices 30 otherwise involved in a BBARX collision have

their DQS data strobe signal lines 104 electrically coupled to the common DQS line 114 through the isolation element 120. The isolation device 120 of certain embodiments multiplexes the DQS data strobe signal lines 104 of the two ranks of memory devices 30 from one another to avoid a BBARX collision.

[0102] In certain embodiments, as schematically illustrated by Figure 6B, the isolation device 120 comprises a first switch 122 electrically coupled to a first data strobe signal line (e.g., DQSa) of a first memory device (not shown) and a second switch 124 electrically coupled to a second data strobe signal line (e.g., DQSb) of a second memory device (not shown). Exemplary switches compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Texas. In certain embodiments, the time for switching the first switch 122 and the second switch 124 is between the two read data bursts (e.g., after the last DQS data strobe of the read data burst of the first memory device and before the first DQS data strobe of the read data burst of the second memory device). During the read data burst for a first memory device, the first switch 122 is enabled. After the last DQS data strobe of the first memory device and before the first DQS data strobe of the second memory device, the first switch 122 is disabled and the second switch 124 is enabled.

[0103] In certain embodiments, as schematically illustrated by Figure 6C, the isolation device 120 comprises a logic element 140 which multiplexes the DQS data strobe signal lines 104 from one another. Exemplary logic elements compatible with embodiments described herein include, but are not limited to multiplexers, such as the SN74AUC2G53 2:1 analog multiplexer/demultiplexer available from Texas Instruments, Inc. of Dallas, Texas. The logic element 140 receives a first DQS data strobe signal from the first memory device and a second DQS data strobe signal from a second memory device and selectively switches one of the first and second DQS data strobe signals to the common DQS data strobe signal line 114. Persons skilled in the art can select other types of isolation devices 120 compatible with embodiments described herein.

[0104] In certain embodiments, as schematically illustrated by Figure 6D, the isolation device 120 also multiplexes the DQ data signal lines 102 of the two memory

devices from one another. For example, in certain embodiments, the isolation device 120 comprises a pair of switches on the DQ data signal lines 102, similar to the switches 122, 124 on the DQS data strobe signal lines 104 schematically illustrated by Figure 6B. In certain other embodiments, the isolation device 120 comprises a logic element 150, as schematically illustrated by Figure 6D. In certain embodiments, the same types of switches and/or logic elements are used for the DQ data signal lines 102 as for the DQS data strobe signal lines 104. The logic element 150 receives a first DQ data signal from the first memory device and a second DQ data signal from the second memory device and selectively switches one of the first and second DQ data signals to the common DQ data signal line 112. Persons skilled in the art can select other types of isolation devices 120 compatible with embodiments described herein.

[0105] In certain embodiments, the isolation device 120 advantageously adds propagation delays to the DQ data signals which match the DQS strobe signals being multiplexed by the isolation device 120. In certain embodiments, the isolation device 120 advantageously presents a reduced impedance load to the computer system by selectively switching between the two ranks of memory devices to which it is coupled. This feature of the isolation device 120 is used in certain embodiments in which there is no memory density multiplication of the memory module (e.g., for a computer system with four chip-select signals), but where the impedance load of the memory module may otherwise limit the number of ranks or the number of memory devices per memory module. As schematically illustrated by Figure 6E, the isolation device 120 of certain such embodiments comprises the logic element 150 on the DQ data signal lines but not a corresponding logic element on the DQS data strobe signal lines.

[0106] In certain embodiments, the control and timing of the isolation device 120 is performed by an isolation-control logic element (e.g., application-specific integrated circuit, custom programmable logic device, field-programmable gate array, etc.) which is resident on the memory module 10. In certain embodiments, the isolation-control logic element is the same logic element 40 as schematically illustrated in Figures 1A and 1B, is part of the isolation device 120 (e.g., logic element 140 or logic element 150 as schematically illustrated by Figure 6D), or is a separate component. The isolation-control logic element of

certain embodiments controls the isolation device 120 by monitoring commands received by the memory module 10 from the computer system and producing "windows" of operation whereby the appropriate components of the isolation device 120 are switched to enable and disable the DQS data strobe signal lines 104 to mitigate BBARX collisions. In certain other embodiments, the isolation-control logic element monitors the commands received by the memory module from the computer system and selectively enables and disables the DQ data signal lines 102 to reduce the load impedance of the memory module 10 on the computer system. In still other embodiments, this logic element performs both of these functions together.

Tied Data Strobe Signal Pins

[0107] For proper operation, the computer system advantageously recognizes a 1-GB memory module comprising 256-Mb memory devices with 64M x 4-bit configuration as a 1-GB memory module having 512-Mb memory devices with 64M x 8-bit configuration (e.g., as a 1-GB memory module with 128M x 8-byte configuration). This advantageous result is desirably achieved in certain embodiments by electrically connecting together two output signal pins (e.g., DQS or data strobe pins) of the two 256-Mb memory devices such that both output signal pins are concurrently active when the two memory devices are concurrently enabled. The DQS or data strobe is a bi-directional signal that is used during both read cycles and write cycles to validate or latch data. As used herein, the terms "tying together" or "tied together" refer to a configuration in which corresponding pins (e.g., DQS pins) of two memory devices are electrically connected together and are concurrently active when the two memory devices are concurrently enabled (e.g., by a common chip-select or CS signal). Such a configuration is different from standard memory module configurations in which the output signal pins (e.g., DQS pins) of two memory devices are electrically coupled to the same source, but these pins are not concurrently active since the memory devices are not concurrently enabled. However, a general guideline of memory module design warns against tying together two output signal pins in this way.

[0108] Figures 7 and 8 schematically illustrate a problem which may arise from tying together two output signal pins. Figure 7 schematically illustrates an exemplary memory module 205 in which a first DQS pin 212 of a first memory device 210 is electrically

connected to a second DQS pin 222 of a second memory device 220. The two DQS pins 212, 222 are both electrically connected to a memory controller 230.

[0109] Figure 8 is an exemplary timing diagram of the voltages applied to the two DQS pins 212, 222 due to non-simultaneous switching. As illustrated by Figure 8, at time t_1, both the first DQS pin 212 and the second DQS pin 222 are high, so no current flows between them. Similarly, at time t_4, both the first DQS pin 212 and the second DQS pin 222 are low, so no current flows between them. However, for times between approximately t_2 and approximately t_3, the first DQS pin 212 is low while the second DQS pin 222 is high. Under such conditions, a current will flow between the two DQS pins 212, 222. This condition in which one DQS pin is low while the other DQS pin is high can occur for fractions of a second (e.g., 0.8 nanoseconds) during the dynamic random-access memory (DRAM) read cycle. During such conditions, the current flowing between the two DQS pins 212, 222 can be substantial, resulting in heating of the memory devices 210, 220, and contributing to the degradation of reliability and eventual failure of these memory devices.

[0110] A second problem may also arise from tying together two output signal pins. Figure 9 schematically illustrates another exemplary memory module 205 in which a first DQS pin 212 of a first memory device 210 is electrically connected to a second DQS pin 214 of a second memory device 220. The two DQS pins 212, 214 of Figure 9 are both electrically connected to a memory controller (not shown). The DQ (data input/output) pin 222 of the first memory device 210 and the corresponding DQ pin 224 of the second memory device 220 are each electrically connected to the memory controller by the DQ bus (not shown). Typically, each memory device 210, 220 will have a plurality of DQ pins (e.g., eight DQ pins per memory device), but for simplicity, Figure 9 only shows one DQ pin for each memory device 210, 220.

[0111] Each of the memory devices 210, 220 of Figure 9 utilizes a respective on-die termination or "ODT" circuit 232, 234 which has termination resistors (e.g., 75 ohms) internal to the memory devices 210, 220 to provide signal termination. Each memory device 210, 220 has a corresponding ODT signal pin 262, 264 which is electrically connected to the memory controller via an ODT bus 240. The ODT signal pin 262 of the first memory device 210 receives a signal from the ODT bus 240 and provides the signal to the ODT circuit 232

of the first memory device 210. The ODT circuit 232 responds to the signal by selectively enabling or disabling the internal termination resistors 252, 256 of the first memory device 210. This behavior is shown schematically in Figure 9 by the switches 242, 244 which are either closed (dash-dot line) or opened (solid line). The ODT signal pin 264 of the second memory device 220 receives a signal from the ODT bus 240 and provides the signal to the ODT circuit 234 of the second memory device 220. The ODT circuit 234 responds to the signal by selectively enabling or disabling the internal termination resistors 254, 258 of the second memory device 220. This behavior is shown schematically in Figure 9 by the switches 246, 248 which are either closed (dash-dot line) or opened (solid line). The switches 242, 244, 246, 248 of Figure 9 are schematic representations of the operation of the ODT circuits 232, 234, and do not signify that the ODT circuits 232, 234 necessarily include mechanical switches.

[0112] Examples of memory devices 210, 220 which include such ODT circuits 232, 234 include, but are not limited to, DDR2 memory devices. Such memory devices are configured to selectively enable or disable the termination of the memory device in this way in response to signals applied to the ODT signal pin of the memory device. For example, when the ODT signal pin 262 of the first memory device 210 is pulled high, the termination resistors 252, 256 of the first memory device 210 are enabled. When the ODT signal pin 262 of the first memory device 210 is pulled low (e.g., grounded), the termination resistors 252, 256 of the first memory device 210 are disabled. By selectively disabling the termination resistors of an active memory device, while leaving the termination resistors of inactive memory devices enabled, such configurations advantageously preserve signal strength on the active memory device while continuing to eliminate signal reflections at the bus-die interface of the inactive memory devices.

[0113] In certain configurations, as schematically illustrated by Figure 9, the DQS pins 212, 214 of each memory device 210, 220 are selectively connected to a voltage VTT through a corresponding termination resistor 252, 254 internal to the corresponding memory device 210, 220. Similarly, in certain configurations, as schematically illustrated by Figure 9, the DQ pins 222, 224 are selectively connected to a voltage VTT through a corresponding termination resistor 256, 258 internal to the corresponding memory device 210, 220. In

certain configurations, rather than being connected to a voltage VTT, the DQ pins 212, 214 and/or the DQS pins 222, 224 are selectively connected to ground through the corresponding termination resistors 252, 254, 256, 258. The resistances of the internal termination resistors 252, 254, 256, 258 are selected to clamp the voltages so as to reduce the signal reflections from the corresponding pins. In the configuration schematically illustrated by Figure 9, each internal termination resistor 252, 254, 256, 258 has a resistance of approximately 75 ohms.

[0114] When connecting the first memory device 210 and the second memory device 220 together to form a double word width, both the first memory device 210 and the second memory device 220 are enabled at the same time (e.g., by a common CS signal). Connecting the first memory device 210 and the second memory device 220 by tying the DQS pins 212, 214 together, as shown in Figure 9, results in a reduced effective termination resistance for the DQS pins 212, 214. For example, for the exemplary configuration of Figure 9, the effective termination resistance for the DQS pins 212, 214 is approximately 37.5 ohms, which is one-half the desired ODT resistance (for 75-ohm internal termination resistors) to reduce signal reflections since the internal termination resistors 252, 254 of the two memory devices 210, 220 are connected in parallel. This reduction in the termination resistance can result in signal reflections causing the memory device to malfunction.

[0115] Figure 10 schematically illustrates an exemplary memory module 300 in accordance with certain embodiments described herein. The memory module 300 comprises a first memory device 310 having a first data strobe (DQS) pin 312 and a second memory device 320 having a second data strobe (DQS) pin 322. The memory module 300 further comprises a first resistor 330 electrically coupled to the first DQS pin 312. The memory module 300 further comprises a second resistor 340 electrically coupled to the second DQS pin 322 and to the first resistor 330. The first DQS pin 312 is electrically coupled to the second DQS pin 322 through the first resistor 330 and through the second resistor 340.

[0116] In certain embodiments, the memory module 300 is a 1-GB unbuffered Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) high-density dual in-line memory module (DIMM). Figures 11A and 11B schematically illustrate a first side 362 and a second side 364, respectively, of such a memory module 300 with eighteen 64M x 4-bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed

circuit board (PCB) 360. In certain embodiments, the memory module 300 further comprises a phase-lock-loop (PLL) clock driver 370, an EEPROM for serial-presence detect (SPD) data 380, and decoupling capacitors (not shown) mounted on the PCB in parallel to suppress switching noise on VDD and VDDQ power supply for DDR-1 SDRAM. By using synchronous design, such memory modules 300 allow precise control of data transfer between the memory module 300 and the system controller. Data transfer can take place on both edges of the DQS signal at various operating frequencies and programming latencies. Therefore, certain such memory modules 300 are suitable for a variety of high-performance system applications.

[0117] In certain embodiments, the memory module 300 comprises a plurality of memory devices configured in pairs, each pair having a first memory device 310 and a second memory device 320. For example, in certain embodiments, a 128M x 72-bit DDR SDRAM high-density memory module 300 comprises thirty-six 64M x 4-bit DDR-1 SDRAM integrated circuits in FBGA packages configured in eighteen pairs. The first memory device 310 of each pair has the first DQS pin 312 electrically coupled to the second DQS pin 322 of the second memory device 320 of the pair. In addition, the first DQS pin 312 and the second DQS pin 322 are concurrently active when the first memory device 310 and the second memory device 320 are concurrently enabled.

[0118] In certain embodiments, the first resistor 330 and the second resistor 340 each has a resistance advantageously selected to reduce the current flow between the first DQS pin 312 and the second DQS pin 322 while allowing signals to propagate between the memory controller and the DQS pins 312, 322. In certain embodiments, each of the first resistor 330 and the second resistor 340 has a resistance in a range between approximately 5 ohms and approximately 50 ohms. For example, in certain embodiments, each of the first resistor 330 and the second resistor 340 has a resistance of approximately 22 ohms. Other resistance values for the first resistor 330 and the second resistor 340 are also compatible with embodiments described herein. In certain embodiments, the first resistor 330 comprises a single resistor, while in other embodiments, the first resistor 330 comprises a plurality of resistors electrically coupled together in series and/or in parallel. Similarly, in certain embodiments, the second resistor 340 comprises a single resistor, while in other

embodiments, the second resistor 340 comprises a plurality of resistors electrically coupled together in series and/or in parallel.

[0119] Figures 12A and 12B schematically illustrate an exemplary embodiment of a memory module 300 in which the first resistor 330 and the second resistor 340 are used to reduce the current flow between the first DQS pin 312 and the second DQS pin 322. As schematically illustrated by Figure 12A, the memory module 300 is part of a computer system 400 having a memory controller 410. The first resistor 330 has a resistance of approximately 22 ohms and the second resistor 340 has a resistance of approximately 22 ohms. The first resistor 330 and the second resistor 340 are electrically coupled in parallel to the memory controller 410 through a signal line 420 having a resistance of approximately 25 ohms. The first resistor 330 and the second resistor 340 are also electrically coupled in parallel to a source of a fixed termination voltage (identified by VTT in Figures 12A and 12B) by a signal line 440 having a resistance of approximately 47 ohms. Such an embodiment can advantageously be used to allow two memory devices having lower bit widths (e.g., 4-bit) to behave as a single virtual memory device having a higher bit width (e.g., 8-bit).

[0120] Figure 12B schematically illustrates exemplary current-limiting resistors 330, 340 in conjunction with the impedances of the memory devices 310, 320. During an exemplary portion of a data read operation, the memory controller 410 is in a high-impedance condition, the first memory device 310 drives the first DQS pin 312 high (e.g., 2.7 volts), and the second memory device 320 drives the second DQS pin 322 low (e.g., 0 volts). The amount of time for which this condition occurs is approximated by the time between t_2 and t_3 of Figure 8, which in certain embodiments is approximately twice the tDQSQ (data strobe edge to output data edge skew time, e.g., approximately 0.8 nanoseconds). At least a portion of this time in certain embodiments is caused by simultaneous switching output (SSO) effects.

[0121] In certain embodiments, as schematically illustrated by Figure 12B, the DQS driver of the first memory device 310 has a driver impedance R_1 of approximately 17 ohms, and the DQS driver of the second memory device 320 has a driver impedance R_4 of approximately 17 ohms. Because the upper network of the first memory device 310 and the

first resistor 330 (with a resistance R_2 of approximately 22 ohms) is approximately equal to the lower network of the second memory device 320 and the second resistor 340 (with a resistance R_3 of approximately 22 ohms), the voltage at the midpoint is approximately 0.5 * (2.7 - 0) = 1.35 volts, which equals VTT, such that the current flow across the 47-ohm resistor of Figure 12B is approximately zero.

[0122] The voltage at the second DQS pin 322 in Figure 12B is given by V_{DQS2} = 2.7 * $R_4/(R_1+R_2+R_3+R_4)$ = 0.59 volts and the current flowing through the second DQS pin 322 is given by I_{DQS2} = 0.59 / R_4 = 34 milliamps. The power dissipation in the DQS driver of the second memory device 320 is thus P_{DQS2} = 34 mA * 0.59 V = 20 milliwatts. In contrast, without the first resistor 330 and the second resistor 340, only the 17-ohm impedances of the two memory devices 310, 320 would limit the current flow between the two DQS pins 312, 322, and the power dissipation in the DQS driver of the second memory device 320 would be approximately 107 milliwatts. Therefore, the first resistor 330 and the second resistor 340 of Figures 12A and 12B advantageously limit the current flowing between the two memory devices during the time that the DQS pin of one memory device is driven high and the DQS pin of the other memory device is driven low.

[0123] In certain embodiments in which there is overshoot or undershoot of the voltages, the amount of current flow can be higher than those expected for nominal voltage values. Therefore, in certain embodiments, the resistances of the first resistor 330 and the second resistor 340 are advantageously selected to account for such overshoot/undershoot of voltages.

[0124] For certain such embodiments in which the voltage at the second DQS pin 322 is V_{DQS2} = 0.59 volts and the duration of the overdrive condition is approximately 0.8 nanoseconds at maximum, the total surge is approximately 0.59 V * 1.2 ns = 0.3 V-ns. For comparison, the JEDEC standard for overshoot/undershoot is 2.4 V-ns, so certain embodiments described herein advantageously keep the total surge within predetermined standards (e.g., JEDEC standards).

[0125] Figure 13 schematically illustrates another exemplary memory module 500 compatible with certain embodiments described herein. The memory module 500 comprises a termination bus 505. The memory module 500 further comprises a first memory device 510

having a first data strobe pin 512, a first termination signal pin 514 electrically coupled to the termination bus 505, a first termination circuit 516, and at least one data pin 518. The first termination circuit 516 selectively electrically terminating the first data strobe pin 512 and the first data pin 518 in response to a first signal received by the first termination signal pin 514 from the termination bus 505. The memory module 500 further comprises a second memory device 520 having a second data strobe pin 522 electrically coupled to the first data strobe pin 512, a second termination signal pin 524, a second termination circuit 526, and at least one data pin 528. The second termination signal pin 524 is electrically coupled to a voltage, wherein the second termination circuit 526 is responsive to the voltage by not terminating the second data strobe pin 522 or the second data pin 528. The memory module 500 further comprises at least one termination assembly 530 having a third termination signal pin 534, a third termination circuit 536, and at least one termination pin 538 electrically coupled to the data pin 528 of the second memory device 520. The third termination signal pin 534 is electrically coupled to the termination bus 505. The third termination circuit 536 selectively electrically terminates the data pin 528 of the second memory device 520 through the termination pin 538 in response to a second signal received by the third termination signal pin 534 from the termination bus 505.

[0126] Figure 14 schematically illustrates a particular embodiment of the memory module 500 schematically illustrated by Figure 13. The memory module 500 comprises an on-die termination (ODT) bus 505. The memory module 500 comprises a first memory device 510 having a first data strobe (DQS) pin 512, a first ODT signal pin 514 electrically coupled to the ODT bus 505, a first ODT circuit 516, and at least one data (DQ) pin 518. The first ODT circuit 516 selectively electrically terminates the first DQS pin 512 and the DQ pin 518 of the first memory device 510 in response to an ODT signal received by the first ODT signal pin 514 from the ODT bus 505. This behavior of the first ODT circuit 516 is schematically illustrated in Figure 14 by the switches 572, 576 which are selectively closed (dash-dot line) or opened (solid line).

[0127] The memory module 500 further comprises a second memory device 520 having a second DQS pin 522 electrically coupled to the first DQS pin 512, a second ODT signal pin 524, a second ODT circuit 526, and at least one DQ pin 528. The first DQS pin

512 and the second DQS pin 522 are concurrently active when the first memory device 510 and the second memory device 520 are concurrently enabled. The second ODT signal pin 524 is electrically coupled to a voltage (e.g., ground), wherein the second ODT circuit 526 is responsive to the voltage by not terminating the second DQS pin 522 or the second DQ pin 524. This behavior of the second ODT circuit 526 is schematically illustrated in Figure 14 by the switches 574, 578 which are opened.

[0128] The memory module 500 further comprises at least one termination assembly 530 having a third ODT signal pin 534 electrically coupled to the ODT bus 505, a third ODT circuit 536, and at least one termination pin 538 electrically coupled to the DQ pin 528 of the second memory device 520. The third ODT circuit 536 selectively electrically terminates the DQ pin 528 of the second memory device 520 through the termination pin 538 in response to an ODT signal received by the third ODT signal pin 534 from the ODT bus 505. This behavior of the third ODT circuit 536 is schematically illustrated in Figure 14 by the switch 580 which is either closed (dash-dot line) or opened (solid line).

[0129] In certain embodiments, the termination assembly 530 comprises discrete electrical components which are surface-mounted or embedded on the printed-circuit board of the memory module 500. In certain other embodiments, the termination assembly 530 comprises an integrated circuit mounted on the printed-circuit board of the memory module 500. Persons skilled in the art can provide a termination assembly 530 in accordance with embodiments described herein.

[0130] Certain embodiments of the memory module 500 schematically illustrated by Figure 14 advantageously avoid the problem schematically illustrated by Figure 7 of electrically connecting the internal termination resistances of the DQS pins of the two memory devices in parallel. As described above in relation to Figure 9, Figures 13 and 14 only show one DQ pin for each memory device for simplicity. Other embodiments have a plurality of DQ pins for each memory device. In certain embodiments, each of the first ODT circuit 516, the second ODT circuit 526, and the third ODT circuit 536 are responsive to a high voltage or signal level by enabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by disabling the corresponding termination resistors. In other embodiments, each of the first ODT circuit 516, the second

ODT circuit 526, and the third ODT circuit 536 are responsive to a high voltage or signal level by disabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by enabling the corresponding termination resistors. Furthermore, the switches 572, 574, 576, 578, 580 of Figure 14 are schematic representations of the enabling and disabling operation of the ODT circuits 516, 526, 536 and do not signify that the ODT circuits 516, 526, 536 necessarily include mechanical switches.

[0131] The first ODT signal pin 514 of the first memory device 510 receives an ODT signal from the ODT bus 505. In response to this ODT signal, the first ODT circuit 516 selectively enables or disables the termination resistance for both the first DQS pin 512 and the DQ pin 518 of the first memory device 510. The second ODT signal pin 524 of the second memory device 520 is tied (e.g., directly hard-wired) to the voltage (e.g., ground), thereby disabling the internal termination resistors 554, 558 on the second DQS pin 522 and the second DQ pin 528, respectively, of the second memory device 520 (schematically shown by open switches 574, 578 in Figure 14). The second DQS pin 522 is electrically coupled to the first DQS pin 512, so the termination resistance for both the first DQS pin 512 and the second DQS pin 522 is provided by the termination resistor 552 internal to the first memory device 510.

[0132] The termination resistor 556 of the DQ pin 518 of the first memory device 510 is enabled or disabled by the ODT signal received by the first ODT signal pin 514 of the first memory device 510 from the ODT bus 505. The termination resistance of the DQ pin 528 of the second memory device 520 is enabled or disabled by the ODT signal received by the third ODT signal pin 534 of the termination assembly 530 which is external to the second memory device 520. Thus, in certain embodiments, the first ODT signal pin 514 and the third ODT signal pin 534 receive the same ODT signal from the ODT bus 505, and the termination resistances for both the first memory device 510 and the second memory device 520 are selectively enabled or disabled in response thereto when these memory devices are concurrently enabled. In this way, certain embodiments of the memory module 500 schematically illustrated by Figure 14 provides external or off-chip termination of the second memory device 520.

[0133] Certain embodiments of the memory module 500 schematically illustrated by Figure 14 advantageously allow the use of two lower-cost readily-available 512-Mb DDR-2 SDRAM devices to provide the capabilities of a more expensive 1-GB DDR-2 SDRAM device. Certain such embodiments advantageously reduce the total cost of the resultant memory module 500.

[0134] Certain embodiments described herein advantageously increase the memory capacity or memory density per memory slot or socket on the system board of the computer system. Certain embodiments advantageously allow for higher memory capacity in systems with limited memory slots. Certain embodiments advantageously allow for flexibility in system board design by allowing the memory module 10 to be used with computer systems designed for different numbers of ranks (e.g., either with computer systems designed for two-rank memory modules or with computer systems designed for four-rank memory modules). Certain embodiments advantageously provide lower costs of board designs.

[0135] In certain embodiments, the memory density of a memory module is advantageously doubled by providing twice as many memory devices as would otherwise be provided. For example, pairs of lower-density memory devices can be substituted for individual higher-density memory devices to reduce costs or to increase performance. As another example, twice the number of memory devices can be used to produce a higher-density memory configuration of the memory module. Each of these examples can be limited by the number of chip select signals which are available from the memory controller or by the size of the memory devices. Certain embodiments described herein advantageously provide a logic mechanism to overcome such limitations.

[0136] Various embodiments of the present invention have been described above. Although this invention has been described with reference to these specific embodiments, the descriptions are intended to be illustrative of the invention and are not intended to be limiting. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention.

WHAT IS CLAIMED IS:

1. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of memory devices coupled to the printed circuit board, the plurality of memory devices having a first number of memory devices; and

a logic element coupled to the printed circuit board, the logic element receiving a set of input control signals from the computer system, the set of input control signals corresponding to a second number of memory devices smaller than the first number of memory devices, the logic element generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of memory devices.

2. The memory module of Claim 1, wherein the memory devices comprise dynamic random-access memory (DRAM) devices.

3. The memory module of Claim 1, wherein the set of input control signals comprises a first number of chip-select signals and wherein the set of output control signals comprises a second number of chip-select signals, wherein the first number of chip-select signals is less than the second number of chip-select signals, the memory module simulating a virtual memory module having the second number of memory devices.

4. The memory module of Claim 1, wherein the logic element comprises an application-specific integrated circuit.

5. The memory module of Claim 1, wherein the logic element comprises a field-programmable gate array.

6. The memory module of Claim 1, wherein the logic element comprises a custom-designed semiconductor device.

7. The memory module of Claim 1, wherein the logic element comprises a complex programmable-logic device.

8. The memory module of Claim 1, wherein the plurality of memory devices are arranged in a first number of ranks, and the set of input control signals corresponds to a

second number of ranks of memory modules, the second number of ranks less than the first number of ranks.

9. The memory module of Claim 8, wherein the first number of ranks is four, and the second number of ranks is two.

10. The memory module of Claim 8, wherein the first number of ranks is two, and the second number of ranks is one.

11. The memory module of Claim 8, wherein the set of input control signals comprises two chip-select signals and an address signal and the set of output control signals comprises four chip-select signals.

12. The memory module of Claim 8, wherein the logic element further responds to a first command signal from the computer system by generating a second command signal transmitted to the plurality of memory devices, the first command signal corresponding to the second number of ranks and the second command signal corresponding to the first number of ranks.

13. The memory module of Claim 12, wherein the first command signal is a refresh signal or a precharge signal.

14. The memory module of Claim 1, wherein the printed circuit board is mountable in a module slot of the computer system, the printed circuit board having a plurality of edge connections electrically coupled to corresponding contacts of the module slot.

15. The memory module of Claim 1, wherein the plurality of memory devices are arranged to provide a first memory density per rank, and the set of output control signals corresponds to a second memory density per rank, the second memory density greater than the first memory density per rank.

16. A method of utilizing a memory module in a computer system, the method comprising:

coupling the memory module to the computer system, the memory module comprising a plurality of memory devices arranged in a first number of ranks;

inputting a first set of control signals to the memory module, the first set of control signals corresponding to a second number of ranks smaller than the first number of ranks; and

generating a second set of control signals in response to the first set of control signals, the second set of control signals corresponding to the first number of ranks.

17. A memory module connectable to a computer system, the memory module comprising a plurality of memory devices arranged in a first number of ranks, the memory module comprising:

means for coupling the memory module to the computer system;

means for inputting a first set of control signals to the memory module, the first set of control signals corresponding to a second number of ranks smaller than the first number of ranks; and

means for generating a second set of control signals in response to the first set of control signals, the second set of control signals corresponding to the first number of ranks.

18. A memory module connectable to a computer system, the memory module comprising:

a first memory device having a first data signal line and a first data strobe signal line;

a second memory device having a second data signal line and a second data strobe signal line;

a common data signal line connectable to the computer system; and

an isolation device electrically coupled to the first data signal line, to the second data signal line, and to the common data signal line, the isolation device selectively alternating between electrically coupling the first data signal line to the common data signal line and electrically coupling the second data signal line to the common data signal line.

19. The memory module of Claim 18, wherein the isolation device comprises a logic element selected from the group consisting of: an application-specific integrated circuit, a custom-programmable logic device, and a field-programmable gate array.

20. The memory module of Claim 18, wherein the memory module further comprises a common data strobe signal line connectable to the computer system, the isolation device electrically coupled to the first data strobe signal line, to the second data strobe signal line, and to the common data strobe signal line, the isolation device selectively alternating between electrically coupling the first data strobe signal line to the common data strobe signal line and electrically coupling the second data strobe signal line to the common data strobe signal line.

MEMORY MODULE DECODER

Abstract

A memory module connectable to a computer system includes a printed circuit board, a plurality of memory devices coupled to the printed circuit board, and a logic element coupled to the printed circuit board. The plurality of memory devices has a first number of memory devices. The logic element receives a set of input control signals from the computer system. The set of input control signals corresponds to a second number of memory devices smaller than the first number of memory devices. The logic element generates a set of output control signals in response to the set of input control signals. The set of output control signals corresponds to the first number of memory devices.

1777728
062005

Figure 1A:

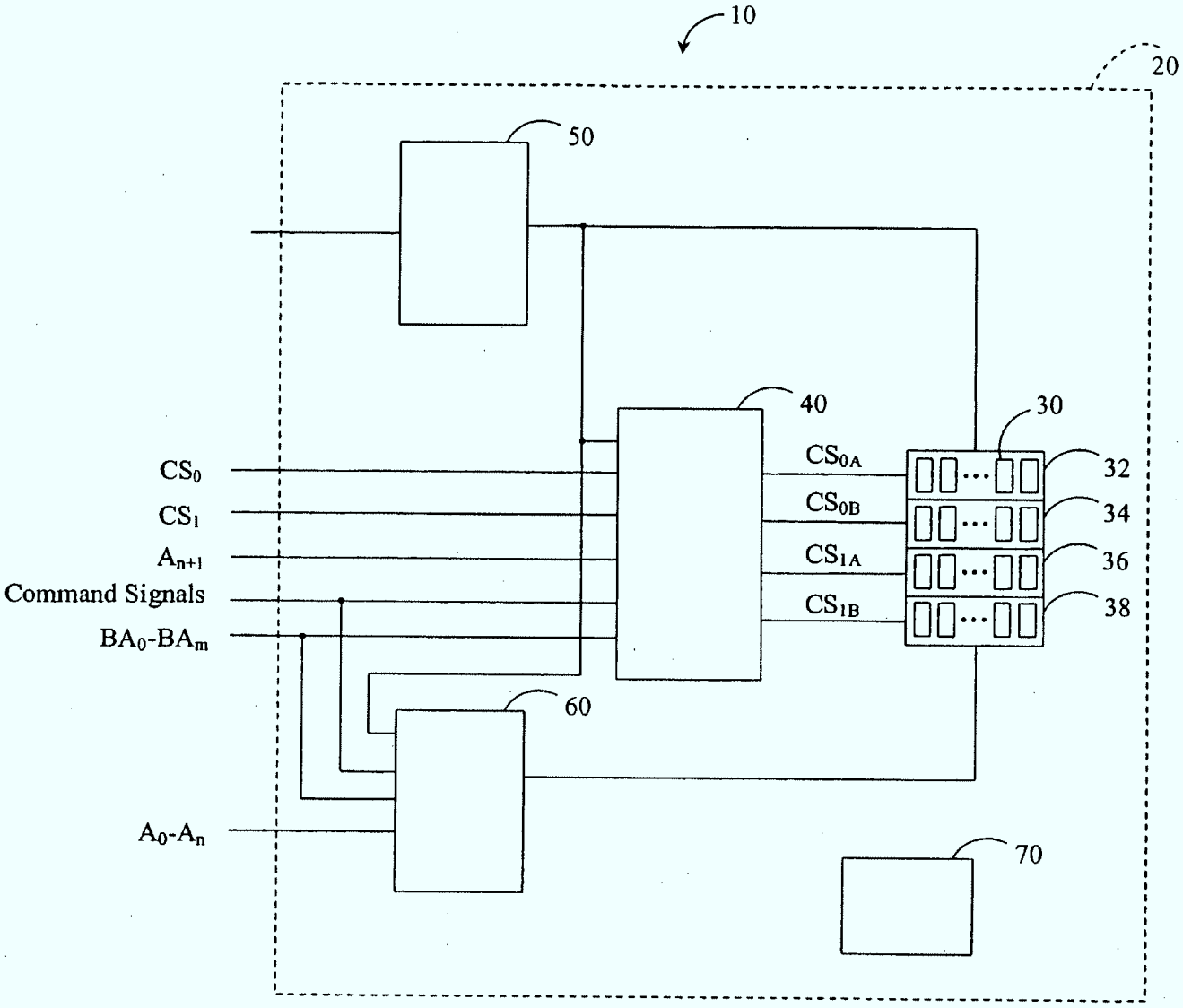

10
20
50
40
30
CS_0
CS_1
A_{n+1}
Command Signals
BA_0-BA_m
CS_{0A}
CS_{0B}
CS_{1A}
CS_{1B}
32
34
36
38
60
A_0-A_n
70

Figure 1B:

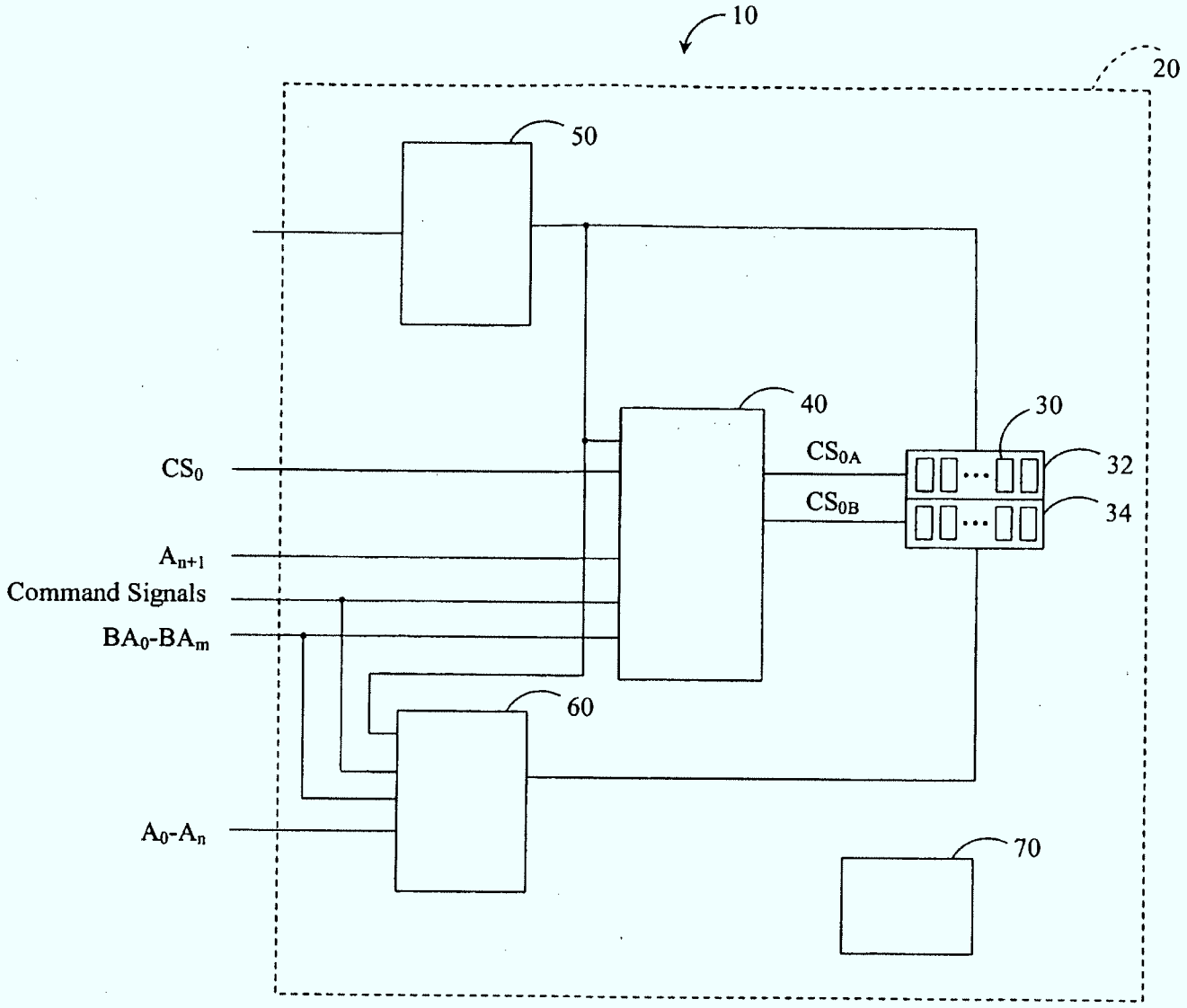

10
20
50
40
30
CS_0
CS_{0A}
CS_{0B}
32
34
A_{n+1}
Command Signals
BA_0-BA_m
60
A_0-A_n
70

Figure 1C: