Exhibit 3

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AUG 0 9 2010

CENTRAL REEXAMINATION UNIT

Transmittal of Communication to Third Party Requester
Inter Partes Reexamination

REEXAMINATION CONTROL NO. : 95000546
PATENT NO. : 7289386
TECHNOLOGY CENTER : 3999
ART UNIT : 3992

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified Reexamination proceeding. 37 CFR 1.903.

Prior to the filing of a Notice of Appeal, each time the patent owner responds to this communication, the third party requester of the inter partes reexamination may once file written comments within a period of 30 days from the date of service of the patent owner's response. This 30-day time period is statutory (35 U.S.C. 314(b)(2)), and, as such, it cannot be extended. See also 37 CFR 1.947.

If an ex parte reexamination has been merged with the inter partes reexamination, no responsive submission by any ex parte third party requester is permitted.

All correspondence relating to this inter partes reexamination proceeding should be directed to the Central Reexamination Unit at the mail, FAX, or hand-carry addresses given at the end of the communication enclosed with this transmittal.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
95/000,546	05/11/2010	7289386	19473-0052RX1	8688

20995 7590 08/09/2010

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EXAMINER
PEIKARI, BEHZAD

ART UNIT	PAPER NUMBER
3992	

MAIL DATE	DELIVERY MODE
08/09/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

ORDER GRANTING/DENYING REQUEST FOR* INTER PARTES *REEXAMINATION	**Control No.**	**Patent Under Reexamination**	
	95/000,546	7289386	
	Examiner	**Art Unit**	
	B. James Peikari	3992	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address. --

The request for *inter partes* reexamination has been considered. Identification of the claims, the references relied on, and the rationale supporting the determination are attached.

Attachment(s): ☐ PTO-892 ☒ PTO/SB/08 ☐ Other: _____

1. ☒ The request for *inter partes* reexamination is GRANTED.

   ☐ An Office action is attached with this order.

   ☒ An Office action will follow in due course.

2. ☐ The request for *inter partes* reexamination is DENIED.

This decision is not appealable. 35 U.S.C. 312(c). Requester may seek review of a denial by petition to the Director of the USPTO within ONE MONTH from the mailing date hereof. 37 CFR 1.927. EXTENSIONS OF TIME ONLY UNDER 37 CFR 1.183. In due course, a refund under 37 CFR 1.26(c) will be made to requester.

All correspondence relating to this *inter partes* reexamination proceeding should be directed to the **Central Reexamination Unit** at the mail, FAX, or hand-carry addresses given at the end of this Order.

Transmittal of Communication to Third Party Requester Inter Partes Reexamination	Control No.	Patent Under Reexamination	
	95/000,546	7289386	
	Examiner	Art Unit	
	B. James Peikari	3992	

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If an *ex parte* reexamination has been merged with the *inter partes* reexamination, no responsive submission by any *ex parte* third party requester is permitted.

All correspondence relating to this inter partes reexamination proceeding should be directed to the **Central Reexamination Unit** at the mail, FAX, or hand-carry addresses given at the end of the communication enclosed with this transmittal.

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	
Filing Date	5/11/2010
First Named Inventor	Jayesh R. Bhakta
Art Unit	
Examiner Name	Peikari
Attorney Docket Number	19473-0052RX1

95000546

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 7,289,386	10/30/2007	Bhakta et al.	
		US- 6,209,074	03/27/2001	Dell et al.	
		US- 6,414,868	07/02/2002	Wong et al.	
		US- 4,368,515	01/11/1983	Nielsen	
		US- 2006/0117152	06/01/2006	Amidi et al.	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature	/B. James Peikari/	Date Considered	08/05/2010

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /BJP/

PTO/SB/08b (07-09)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 2 of 2

Complete if Known	
Application Number	
Filing Date	5/11/2010
First Named Inventor	Jayesh R. Bhakta
Art Unit	
Examiner Name	Peikari
Attorney Docket Number	19473-0052RX1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Barr, Michael, "Programmable Logic: What's it to Ya?," Embedded Systems Programming, June 1999, pp. 75-84.	

Examiner Signature	/B. James Peikari/	Date Considered	08/05/2010

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /BJP/

RESPONSE TO REQUEST FOR *INTER PARTES* REEXAMINATION

1. The Request filed May 11, 2010 alleges that there are substantial new questions of patentability (SNQ) affecting claims 1-12 of U.S. Patent Number 7,289,386 (the '386 patent) based on the following prior art references:

- U.S. Patent No. 6,209,074 to Dell ("Dell").
- U.S. Patent No. 6,414,868 to Wong ("Wong").
- U.S. Patent No. 4,368,515 to Nielsen ("Nielsen").
- U.S. Patent Publication No. 2006/0117152 to Amidi ("Amidi").
- Barr, Michael, "Programmable Logic: What's it to Ya?" Embedded Systems Programming, June 1999, pp. 75-84 ("Barr").

Brief Overview of the Patent

2. The '386 patent is directed to a memory module decoder wherein a memory module is connectable to a computer system and includes a printed circuit board, a plurality of memory devices coupled to the printed circuit board, and a logic element coupled to the printed circuit board. The plurality of memory devices has a first number of memory devices. The logic element receives a set of input control signals from the computer system. The set of input control signals corresponds to a second number of memory devices smaller than the first number of memory devices. The logic element generates a set of output control signals in response to the set of input control signals. The set of output control signals corresponds to the first number of memory devices.

Prosecution History

3. The '386 patent matured from patent application number 11/173,175, whose relevant prosecution history may be summarized as follows:

- Application 11/173,175 is a continuation of 11/075,395 (which issued as U.S. Patent No. 7,286,436).
- Application 11/173,175 was filed on July 1, 2005 with claims 1-20.
- In a telephone interview on January 10, 2007, an election was made to prosecute claims 1-15 due to a restriction requirement.
- In the Office Action mailed January 26, 2007, claims 1, 2, 8-10, 14 and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee (U.S. No. 7,120,727); claims 4-7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of Barr; claims 1-3, 8, 11 and 14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Miyasaka (U.S. No. 4,392,212); claims 4-7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Miyasaka in view of Barr; and claims 12 and 13 were indicated as having allowable subject matter.
- On June 19, 2007, an amendment was filed which cancelled claims 1-11 and 14-20, amended claim 12, and added new claims 21-31.

- On July 30, 2007, a Notice of Allowance was mailed, in which the examiner allowed claims 12, 13 and 21-31 and provided the following reasons for allowance:

"With respect to **independent claim** 12, there is no teaching, suggestion, or motivation for combination in the prior art to the logic element generating a second command signal, corresponding to a first number of ranks, based on the first command signal, corresponding to a second number of ranks, wherein the second number of ranks is less than the first number of ranks (i.e., the logic element generates more rank select signals from a number of rank select signals)."

- On July 19, 2007, comments on the statement of reasons for allowance were filed.
- On October 30, 2007, the application issued as U.S. Patent No. 7,289,386.
- On May 13, 2008 a Certificate of Correction was issued.

SNQs Raised in the Request

4. The Requester identified the following SNQs (see Request, pages 5-6):

- **Issue 1:** A substantial new question of patentability as to claims 1-5, 7 and 9-12 is raised by Dell.
- **Issue 2:** A substantial new question of patentability as to claims 6 and 8 is raised by Dell in view of Barr.
- **Issue 3:** A substantial new question of patentability as to claims 1-4, 10 and 12 is raised by Wong.
- **Issue 4:** A substantial new question of patentability as to claims 5-8 is raised by Wong in view of Barr.

- **Issue 5:** A substantial new question of patentability as to claims 1, 3, 10 and 12 is raised by Nielsen.
- **Issue 6:** A substantial new question of patentability as to claims 5-8 is raised by Nielsen in view of Barr.
- **Issue 7:** A substantial new question of patentability as to claims 1-12 is raised by Amidi.

Discussion of SNQs

5. A prior art patent or printed publication raises a substantial new question of patentability where there is:

> (A) a substantial likelihood that a reasonable Examiner would consider the prior art patent or printed publication important in deciding whether or not the claim is patentable, MPEP §2242 (I) and,
>
> (B) the same question of patentability as to the claim has not been decided in a previous or pending proceeding or in a final holding of invalidity by a federal court. See MPEP §2242 (III).

For any reexamination ordered on or after November 2, 2002, reliance on previously cited/considered art, i.e., "old art," does not necessarily preclude the existence of a substantial new question of patentability that is based exclusively on that old art. Rather, determinations on whether a substantial new question of patentability exists in such an instance shall be based upon a fact-specific inquiry done on a case-by-case basis. See MPEP 2242.

Issue 1

A substantial new question of patentability as to claims 1-5, 7 and 9-12 is raised by Dell.

6. Dell is directed to a memory module that has a logic circuit and multiple memory devices that are each configured in M banks. The logic circuit receives from a memory controller a number of address inputs and a number of bank address signals. The received address inputs and bank address input signals correspond to N-bank memory devices. The logic circuit re-maps at least one of the address inputs as an additional bank address signal to the memory device having M banks (*note the Abstract*). This remapping allows a system that expects a module with N banks to use a module that actually has 2N banks (*note column 8, lines 15-28, 52-61*). Dell further notes an application in which a "system may need a two bank memory chip, but the memory module may include a memory device that is a four bank device" (*see column 2, lines 29-31*).

Thus, Dell appears to teach or suggest a logic element generating a second command signal, corresponding to a first number of ranks, based on the first command signal, corresponding to a second number of ranks, wherein the second number of ranks is less than the first number of ranks, which it appears that the examiner considered as allowable features of claims 1-5, 7 and 9-12.

7. There is a substantial likelihood that a reasonable examiner would consider the teachings of Dell important in deciding the patentability of claims 1-5, 7 and 9-12 of the '386 patent. Dell is not of record in the file of the '386 patent and is not cumulative to the art of record in the

original file. The teachings of Dell were not subject to a final holding of invalidity by a federal court.

Accordingly, Dell raises a substantial new question of patentability with regard to claims 1-5, 7 and 9-12.

Issue 2

A substantial new question of patentability as to claims 6 and 8 is raised by Dell in view of Barr.

8. In addition to the teachings of Dell described above, Barr discloses that field-programmable gate array (FPGAs) and complex programmable-logic devices (CPLDs) are commonly used in memory circuitry as address decoders (*see Barr, pages 2-4*).

Thus, Barr appears compatible with Dell in teaching the use of FPGAs or CPLDs for use with a logic element generating a second command signal, corresponding to a first number of ranks, based on the first command signal, corresponding to a second number of ranks, wherein the second number of ranks is less than the first number of ranks, which it appears that the examiner considered as allowable features of claims 6 and 8.

9. There is a substantial likelihood that a reasonable examiner would consider the combination of Dell and Barr important in deciding the patentability of the claims of the '386 patent. Barr was of record in the file of the '386 patent and was used in rejections during the original prosecution. However, the request describes the applicability of the logic elements of

Barr to prior art systems that were never cited during the original prosecution. Therefore, the teachings of Barr have been presented in a new light.

The teachings of Barr were not subject to a final holding of invalidity by a federal court.

Accordingly, the combination of Dell and Barr raises a substantial new question of patentability as to claims 6 and 8.

Issue 3

A substantial new question of patentability as to claims 1-4, 10 and 12 is raised by Wong.

10. Wong is directed to a memory module that has a logic circuit, including a buffer and a bank control circuit, and multiple memory devices that are organized into banks (i.e., "ranks") on the module. The logic circuit receives from a memory controller a number of address inputs and a number of bank select signals. The received address input signals and bank select input signals correspond to that number of banks. The logic circuit re-maps at least one of the address input signals and the bank address signals into more bank address signals than were received from the memory controller. This remapping allows a system that expects a module with one bank, for example, to use a module that actually has two banks. (*note, e.g., Figs. 4A and 4B, showing the mapping of one bank select input signal PASO and one address input signal A 13 into two bank select output signals RASUX and RASLX, which select two different banks*).

Thus, Wong appears to teach or suggest a logic element generating a second command signal, corresponding to a first number of ranks, based on the first command signal, corresponding to a second number of ranks, wherein the second number of ranks is less than the

first number of ranks, which it appears that the examiner considered as allowable features of claims 1-4, 10 and 12.

11. There is a substantial likelihood that a reasonable examiner would consider the teachings of Wong important in deciding the patentability of claims 1-4, 10 and 12 of the '386 patent. Wong is not of record in the file of the '386 patent and is not cumulative to the art of record in the original file. The teachings of Wong were not subject to a final holding of invalidity by a federal court.

Accordingly, Wong raises a substantial new question of patentability with regard to claims 1-4, 10 and 12.

Issue 4

A substantial new question of patentability as to claims 5-8 is raised by Wong in view of Barr.

12. The teachings of Wong and Barr have been described above.

Barr appears compatible with Wong in teaching the use of FPGAs or CPLDs for use with a logic element generating a second command signal, corresponding to a first number of ranks, based on the first command signal, corresponding to a second number of ranks, wherein the second number of ranks is less than the first number of ranks, which it appears that the examiner considered as allowable features of claims 5-8.

13. There is a substantial likelihood that a reasonable examiner would consider the combination of Wong and Barr important in deciding the patentability of the claims of the '386 patent.

Accordingly, the combination of Wong and Barr raises a substantial new question of patentability as to claims 5-8.

Issue 5

A substantial new question of patentability as to claims 1, 3, 10 and 12 is raised by Nielsen.

14. Nielsen is directed to a memory module that has a logic circuit, which includes address decode logic, and multiple memory devices. The multiple memory devices are each activated by a separate chip select (CS) signal and thus each memory device is a "rank" on the module. A chip select is not a necessary input into the module; however, a single rank can be addressed from the computer side without necessarily using a chip select signal.

The address lines for the module provide signal lines for only a single memory. The logic circuit generates more chip select signals than it receives (which could be zero) in order to address more ranks and increase the number of addressable memory locations (*see column 2, lines 3-5, and Fig. 4*).

The logic circuit detects certain preprogrammed addresses appearing on the address signal lines from the computer (the game console) and switches the active rank that responds to general addresses accordingly (*see column 5, lines 54-66*).

Absent the use of and response to the preprogrammed switching addresses, the memory module would provide in effect a single rank of memory. The logic circuit converts a sequence of address signals for one rank into signals that address multiple ranks (*see, e.g., Figs. 3 and 4, showing the generation of multiple chip select (CS) signals*).

Thus, Nielsen appears to teach or suggest a logic element generating a second command signal, corresponding to a first number of ranks, based on the first command signal, corresponding to a second number of ranks, wherein the second number of ranks is less than the first number of ranks, which it appears that the examiner considered as allowable features of claims 1, 3, 10 and 12.

15. There is a substantial likelihood that a reasonable examiner would consider the teachings of Nielsen important in deciding the patentability of claims 1, 3, 10 and 12 of the '386 patent. Nielsen is not of record in the file of the '386 patent and is not cumulative to the art of record in the original file. The teachings of Nielsen were not subject to a final holding of invalidity by a federal court.

Accordingly, Nielsen raises a substantial new question of patentability with regard to claims 1, 3, 10 and 12.

Issue 6

A substantial new question of patentability as to claims 5-8 is raised by Nielsen in view of Barr.

16. The teachings of Nielsen and Barr have been described above.

Barr appears compatible with Nielsen in teaching the use of FPGAs or CPLDs for use with a logic element generating a second command signal, corresponding to a first number of ranks, based on the first command signal, corresponding to a second number of ranks, wherein the second number of ranks is less than the first number of ranks, which it appears that the examiner considered as allowable features of claims 5-8.

17. There is a substantial likelihood that a reasonable examiner would consider the combination of Nielsen and Barr important in deciding the patentability of the claims of the '386 patent.

Accordingly, the combination of Nielsen and Barr raises a substantial new question of patentability as to claims 5-8.

Issue 7

A substantial new question of patentability as to claims 1-12 is raised by Amidi.

18. Amidi is directed to a memory module that has a logic circuit, which includes a CPLD (complex programmable logic device) and register circuitry, and multiple DRAM memory devices organized into "ranks". The ranks of memory devices are each activated by one of a larger number of output chip select (CS) signals, e.g., one of four signals rcs0, rcs1, rcs2 or rcs3, that are generated from a smaller number of input chip select signals, e.g., one of two signals cs0 or csl, and an address signal (*see, e.g., Fig. 6A, or paragraphs 8-11*).

Thus, Amidi appears to teach or suggest a logic element generating a second command signal, corresponding to a first number of ranks, based on the first command signal, corresponding to a second number of ranks, wherein the second number of ranks is less than the first number of ranks, which it appears that the examiner considered as allowable features of claims 1-12.

19. There is a substantial likelihood that a reasonable examiner would consider the teachings of Amidi important in deciding the patentability of claims 1-12 of the '386 patent. Amidi is not of record in the file of the '386 patent and is not cumulative to the art of record in the original file. The teachings of Amidi were not subject to a final holding of invalidity by a federal court.

Accordingly, Amidi raises a substantial new question of patentability with regard to claims 1-12.

Conclusion

20. Claims 1-12 are subject to reexamination.

21. On page 21 of the request, the conclusion states:

"For the foregoing reasons, substantial and new questions of patentability exist with respect to claims 1-12 of the ' 386 patent. The references cited above render claims 1 - 13 of the '386 patent unpatentable as set forth above. Reexamination of these claims is therefore requested."

From this passage, it is not clear to which set of claims the requestor was referring when requesting reexamination.

Also, there is some confusion as to whether requester meant to assert the existence of a substantial new question of patentability (SNQ) for claim 13. For example, in contrast to the statement from page 21 recited above, claim 13 was listed among the substantial new questions of patentability (SNQ) on pages 3 and 4 of the request. On the other hand, the proposed rejections in the table of contents (pages i and ii) mention claims 1-12, but not claim 13.

All things considered, it appears that the request did *not* assert the existence of a substantial new question of patentability (SNQ) for claim 13, inasmuch as claim 13 is missing from the claim charts submitted with the request (see 35 U.S.C. § 311 (b)(2); see also 37 CFR 1.915b and 1.923). Consequently, claim 13 will not be reexamined.

Note *Sony Computer Entertainment America Inc., et al. v. Jon W. Dudas*, Civil Action No. 1:05CV1447 (E.D.Va. May 22, 2006), Slip Copy, 2006 WL 1472462, in which the District Court upheld the Office's discretion to not reexamine claims in an *inter partes* reexamination proceeding other than those claims for which reexamination had specifically been requested. The Court stated:

> "To be sure, a party may seek, and the PTO may grant, ... review of each and every claim of a patent. Moreover, while the PTO in its discretion may review claims for which ... review was not requested, nothing in the statute compels it to do so. To ensure that the PTO considers a claim for ... review, § 311 (b)(2) requires that the party seeking reexamination demonstrate why the PTO should reexamine each and every claim for which it seeks review. Here, it is undisputed that Sony did not seek review of every claim under the '213 and '333 patents. Accordingly, Sony cannot now claim that the PTO wrongly failed to reexamine claims for which Sony never requested review, and its argument that AIPA compels a contrary result is unpersuasive."

Service of Papers

22. Any paper filed with the USPTO, i.e., any submission made, by either the Patent Owner or the Third Party Requester must be served on every other party in the reexamination proceeding, including any other third party requester that is part of the proceeding due to merger of the reexamination proceedings. As proof of service, the party submitting the paper to the Office must attach a Certificate of Service to the paper, which sets forth the name and address of the party served and the method of service. Papers filed without the required Certificate of Service may be denied consideration. 37 CFR 1.903; MPEP 2666.06.

Amendments in Reexamination Proceedings

23. Any proposed amendment to the specification and/or claims in this reexamination proceeding must comply with 37 CFR 1.530(d)-(j), must be formally presented pursuant to 37 CFR 1.52(a) and (b), and must contain any fees required by 37 CFR 1.20(c). Amendments in an *inter partes* reexamination proceeding are made in the same manner that amendments in an *ex parte* reexamination are made. MPEP 2666.01. See MPEP 2250 for guidance as to the manner of making amendments in a reexamination proceeding.

Extensions of Time

24. Extensions of time under 37 CFR 1.136(a) will not be permitted in *inter partes* reexamination proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant" and not to the patent owner in a reexamination proceeding. Additionally, 35 U.S.C. 314(c) requires that *inter partes* reexamination proceedings "will be conducted with special dispatch"

(37 CFR 1.937). Patent owner extensions of time in *inter partes* reexamination proceedings are provided for in 37 CFR 1.956. Extensions of time are not available for third party requester comments, because a comment period of 30 days from service of patent owner's response is set by statute. 35 U.S.C. 314(b)(3).

Notification of Concurrent Proceedings

25. The patent owner is reminded of the continuing responsibility under 37 CFR 1.985(a), to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving the patent undergoing reexamination or any related patent throughout the course of this reexamination proceeding. The third party requester is also reminded of the ability to similarly inform the Office of any such activity or proceeding throughout the course of this reexamination proceeding. See MPEP § 2686 and 2686.04.

All correspondence relating to this *inter partes* reexamination proceeding should be directed:

By Mail to: Mail Stop *Inter Partes* Reexam
Central Reexamination Unit
Commissioner for Patents
United States Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

By FAX to: (571) 273-9900
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Any inquiry concerning this communication should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

/B. James Peikari/

B. James Peikari
Primary Examiner
Central Reexamination Unit 3992

JESSICA HARRISON
SUPERVISORY PATENT EXAMINER