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GOOGLE INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

(OAKLAND DIVISION)

GOOGLE INC.,

Plaintiff,

v.

NETLIST, INC.,

Defendant.

AND RELATED COUNTERCLAIMS.

Case No. C 08-04144 SBA

[REDACTED] GOOGLE INC.'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

Date: November 12, 2009
Time: 9:00 a.m.
Place: Courtroom 3, 3rd Floor
Judge: Hon. Saundra Brown Armstrong

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I. INTRODUCTION

U.S. Patent No. 7,289,386 (the '386 patent) discloses memory modules for a computer system that allow the computer system to operate more memory devices per module than the computer system is configured to handle. The parties' disagreement as to the meaning of claim terms boils down to a dispute over the specification's role in claim construction. Google submits that terms must be interpreted in the context of the specification of which they are a part, as required by *Phillips v. AWH Corp.*, 415 F.3d. 1303, 1315 (Fed. Cir. 2005) (*en banc*). Netlist, by contrast, defines terms in a vacuum using dictionary definitions instead of the specification or any other portion of the intrinsic record.

The disclosure of the '386 patent is limited in scope. Every embodiment and every claim describes a memory module that reports to the computer system that it contains a smaller number of memory devices or ranks of memory devices than it actually has, thus "tricking" the computer system into generating input signals for the smaller number reported, instead of the actual number of memory devices or ranks of memory devices[1]. Claim 1 requires this process with its "corresponding to" limitations, which recite that the computer system generates a "set of input control signals *corresponding to* a second number of memory devices smaller than the first number of memory devices" and a "first command signal *corresponding to* the second number of ranks." Since the specification makes clear that the computer system generates signals corresponding to a smaller number of devices than the module actually has, Google construes claim 1 and any other claims that recite the "corresponding to" limitation to include this requirement. Netlist's definitions, on the other hand, read "corresponding to" out of the claims entirely in an effort to broaden claim scope beyond the patent's disclosure. But claims may have

[1] The '386 patent calls the smaller number the "second number" of ranks. 33:42-44 (claim 1). For clarity, Google refers to this "second number" as the "apparent number" of ranks, representing the number of ranks of memory devices the computer system understands the memory module to contain. The patent calls the actual number the "first number" of ranks. 33:39-41 (claim 1). Google refers to this "first number" as the "actual number" of ranks, representing the actual number of ranks of memory devices on the memory module.

no broader scope than their supporting disclosure. *Id.* at 1323. Accordingly, only Google's constructions are proper.

The '386 patent's disclosure as to the remaining disputed terms is also limited. The claims require that input signals come "from the computer system." The drawings also make clear that the memory module's logic element receives input signals directly from the computer system, none of them showing intervening circuitry between the logic element and the computer system. The drawings also illustrate that signals sent to and from the logic element are transmitted on dedicated pins, and the memory module embodying the alleged invention transmits signals on dedicated signal lines and pins.

No alternative mechanism for transmitting signals is disclosed or suggested by the patent. Despite this limited disclosure, Netlist offers broad, generic dictionary definitions for "logic element" and "signal," improperly ignoring the specification and the context in which these terms appear. Since only Google's constructions conform to the intrinsic record, they should be adopted in full.

II. THE TECHNOLOGY OF THE '386 PATENT

A. The '386 Patent Specification

1. Purpose of the Alleged Invention

The '386 patent describes memory modules that allow a computer system to use more memory devices per module than the computer system is configured to operate. 7:6-44, 10:31-55.[2] In normal operation, a computer system activates individual ranks of memory devices on a memory module using control signals generated by the computer system. 2:34-36. Because most computer systems are configured to operate memory modules arranged in only one or two ranks of memory devices, total memory capacity is limited. 2:38-42. The '386 patent attempts to overcome this memory capacity limitation by "tricking" the computer system into seeing its memory modules as having no more than the maximum number of memory devices or ranks of devices the computer system is configured to operate, when in fact the module has more than that

[2] Unless otherwise noted, all citations herein are citations to columns and lines, respectively, of the '386 patent.

maximum number of devices or ranks. 7:6-44, 10:31-55;

Because "the computer system [] see[s] a smaller number of devices than is actually there," it is "tricked" into generating a set of input control signals corresponding to the apparent number of devices it sees on the module.

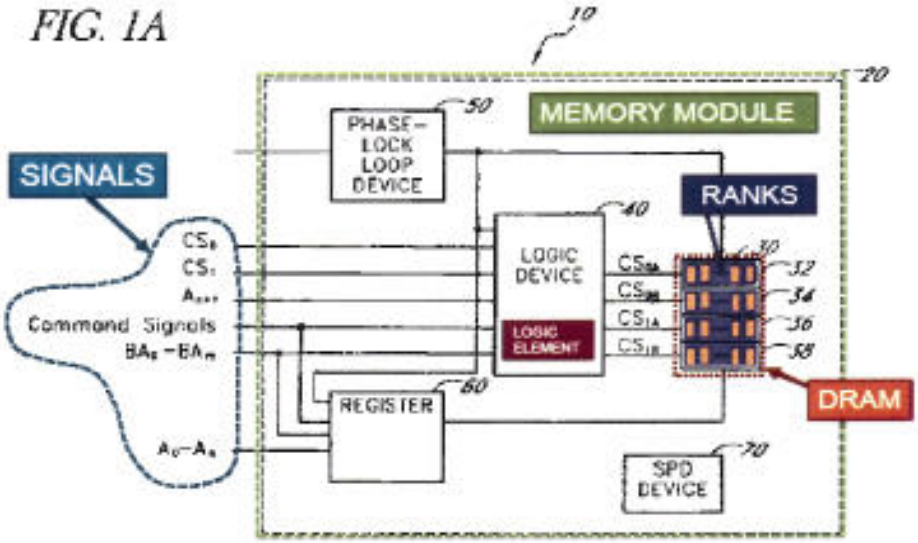
The logic element receives those input control signals from the computer system, and responds by generating a set of output control signals corresponding to the actual number of devices. 6:64-7:14; 10:35-55.

The patent describes this as a "virtual memory system" (7:20, 10:66), and Netlist elsewhere described it as "fool[ing] the computer" to understand the module to have a smaller number of devices than it actually has. Ex. 3 at 2 (5/19/09 Ltr. Br. to J. Spero) (infringing products "fool[] the computer into thinking that it is accessing two sets of memory chips, when in fact its access requests are split among four less-expensive sets of memory chips"). By "tricking" the computer system, the claimed module can use more memory devices and ranks of devices than the computer system is configured to handle, so manufacturers can save money by using larger numbers of cheaper, lower-density (lower capacity) memory devices instead of a smaller number of more expensive higher-density (higher capacity) devices. 4:52-5:10, 22:20-29, 32:51-33:16.

2. Elements of The '386 Patent's Memory Module Are A Printed Circuit Board, Logic Element, And Memory Devices

The claimed module consists of a printed circuit board ("PCB"), multiple memory devices connected (or "coupled") to the PCB, and a logic element coupled to the PCB. 5:14-19. Memory devices (e.g., DRAM chips) are arranged on the PCB in "ranks," or rows. 2:16-18.

FIG. 1A



The annotated copy above of Figure 1A of the patent shows different types of signals sent from the computer system to the logic element on dedicated signal lines, and output signals sent from the logic element to sixteen DRAM memory devices arranged in four ranks. Figure 1A shows the memory module of claim 1 of the '386 patent.

Total memory capacity of the module depends on the number and type of memory devices it contains. 1:29-2:2, 2:23-33. Total memory capacity can be increased by adding more ranks to the module or by increasing the number of devices in a rank. 2:23-27.

3. Operation of the '386 Patent's Memory Module

The '386 patent describes a way to "trick" the computer system to operate more memory devices or ranks of devices per module than the computer system is configured to operate. *Id.* at 57:5-23. The patent states that prior art memory modules send data to the computer system reporting the memory density (the memory capacity, i.e., the amount of memory on the module) and number of devices and ranks, "so that the computer system is informed of the memory capacity and the memory configuration available for use." 9:24-38;

. Instead of informing the computer system of its actual number of memory devices and ranks, the claimed memory module informs the computer system that it has a smaller number of devices or ranks. 10:31-49 ("In certain embodiments, the SPD device 70 comprises data which characterize the memory module 10 as having fewer ranks of memory devices than the memory module 10 actually has, with each of these ranks having more memory density."), 10:59-11:15 ("In certain such embodiments, the SPD device 70 of the memory module 10 is programmed to describe the combined pair of lower-density memory devices 31, 33 as one virtual or pseudo-higher-density memory device."); . For example, the computer system using a patented module could see an apparent two-rank module when the actual number of ranks on the module is four.

After receiving density and configuration data from the memory module, the computer system generates a set of input control signals corresponding to the apparent number of memory devices, and sends those signals to the module's logic element. 7:30-67, 12:2-11;

. In response, the logic element generates

additional output control signals to operate the actual number of devices. 2:50-58, 5:16-26, 11:44-12:11. Neither the claims nor any disclosed embodiment includes a memory module that sends correct information to the computer system about the number of its memory devices and ranks.

To increase memory capacity, each embodiment "tricks" the computer system into seeing a memory configuration that is not really there.[3]

B. Claim 1 of the 386 Patent

Claim 1 of the 386 patent, the only independent claim at issue, reads as follows:

> A memory module connectable to a computer system, the memory module comprising:
> a printed circuit board;
> a plurality of memory devices coupled to the printed circuit board, the plurality of memory devices having a first number of memory devices; and
> a logic element coupled to the printed circuit board, **[1a]** the ***logic element receiving a set of input control signals from the computer system, the set of input control signals corresponding to a second number of memory devices smaller than the first number of memory devices***, **[2]** the logic element generating a set of output ***control signals*** in response to the set of input control signals, the set of output control signals corresponding to the first number of memory devices, **[1b]** wherein the plurality of memory devices are arranged in a first number of ***ranks***, and the set of input control signals corresponds to a second ***number of ranks of memory modules***, the second number of ranks less than the first number of ranks, **[3a]** wherein the logic element further responds to a first ***command signal*** from the computer system by **[4a]** generating a second command signal transmitted to the plurality of memory devices, **[3b]** ***the first command signal corresponding to the second number of ranks*** and **[4b]** the second command signal corresponding to the first number of ranks.

33:25-34:2 (emphasis and annotations added). The final paragraph requires that the logic element:

1. receive a set of input control signals from the computer system corresponding to the smaller apparent number of devices on the memory module (clause 1a);
2. in response to the input control signals, generate a set of output control signals corresponding to the actual number of memory devices on the memory module (clause 2);
3. receive from the computer system a command signal corresponding to the smaller apparent

[3] Netlist erroneously claims the patent discloses embodiments in which the SPD communicates "the [actual] number of memory devices and the memory density per memory device" to the computer system. (Op. Br. at 14, 16.) The specification section Netlist cites describes normal SPD operation in prior art memory modules, not the patented module. 9:24-37. Every allegedly inventive embodiment and the claims require a memory module to "trick" the computer system to see fewer devices or ranks on the memory module than are actually present.

number of ranks of devices (clauses 3a and 3b); and

4. in response, generate a command signal corresponding to the larger actual number of ranks of devices on the memory module (clauses 1b, 4a and 4b).

III. LEGAL STANDARDS GOVERNING CLAIM CONSTRUCTION

A. Plain and Ordinary Meaning In The Context of The Intrinsic Record Generally Controls

During claim construction, "words of a claim 'are generally given their ordinary and customary meaning.'" *Phillips*, 415 F.3d at 1312 (citation omitted). A term's plain meaning is not determined in a vacuum, but is its "meaning to the ordinary artisan after reading the entire patent." *Id.* at 1321, 1313. Extrinsic sources are less helpful than intrinsic sources, and "unlikely to result in a reliable interpretation of patent claim scope unless considered in the context of the intrinsic evidence." *Id.* at 1319. "[H]eavy reliance on the dictionary divorced from the intrinsic evidence risks transforming the meaning of the claim term to the artisan into the meaning of the term in the abstract, out of its particular context, which is the specification." *Id.* at 1321.

B. The Specification Is Always Highly Relevant and Typically Dispositive

The specification is always highly relevant to claim construction; it is the single best guide to the meaning of disputed terms, and is usually dispositive. *Id.* at 1315. The specification may reveal that claim scope is limited by a narrow enabling disclosure. *Id.* at 1323; *Gentry Gallery*, 134 F.3d 1473, 1479-80 (Fed. Cir. 1998). Claim language is also important, and "the context in which a term is used in the asserted claim can be highly instructive." *Phillips*, 415 F.3d at 1314.

C. The Disclosed Embodiments Restrict the Scope of the Claims

When the only disclosed embodiment is the invention itself, it is not just a "certain" or "preferred" embodiment – it sets the scope and outer boundary of the claims. *Curtiss-Wright Flow Control Corp. v. Velan, Inc.*, 438 F.3d 1374, 1379-80 (Fed. Cir. 2006); *Toro Co. v. White Consol. Indus., Inc.*, 199 F.3d 1295, 1301-1302 (Fed. Cir. 1999). When it is "clear from the specification that there is 'nothing in the context to indicate that the patentee contemplated any alternative embodiment,'" the scope of the claims is limited accordingly. *Phillips*, 415 F.3d at 1323 (quoting *Snow v. Lake Shore & M.S. Ry. Co.*, 121 U.S. 617, 630 (1887)).

D. Each Claim Element Must Be Given Meaning

It is fundamental that "[e]ach element contained in a patent claim is deemed material to defining the scope of the patented invention." *Warner-Jenkinson Co. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 29 (1997). Claims must be interpreted to "give[] effect to all terms in the claim." *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 950 (Fed. Cir. 2006).

IV. GOOGLE'S PROPOSED CONSTRUCTIONS SHOULD BE ADOPTED IN FULL

A. "logic element receiving a set of input control signals from the computer system"

Google's Proposed Construction	Netlist's Proposed Construction
"electronic circuitry operable to perform one or more particular functions and that receives input signals directly from the computer system"	"logic element" means "a hardware circuit that performs a predefined function on input signals and presents the resulting signals as its output"

The parties' dispute over construction of this phrase results from Netlist's attempt to divorce its terms from their intrinsic context, which makes clear that the input control signals are received by the logic element from the computer system, and that there is no intervening circuitry between the computer system and the logic element. The phrase should be construed in full to resolve the lurking claim construction dispute over how the logic element receives signals from the computer system – a dispute Netlist sidesteps by entirely ignoring "...from the computer system" in its unreasonably broad construction.

1. The Intrinsic Evidence Supports Google's Proposed Construction

Google's construction of this phrase conforms to the specification and the claim language. Because Google's construction clearly states the structural relationship between the computer system and logic element, it will aid the jury more than Netlist's definition. *02 Micro Int'l Ltd. v. Beyond Innovation Tech. Co., Ltd.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008) (purpose of construction is "to clarify and when necessary to explain what the patentee covered by the claims").

The plain language of claim 1 requires that input control signals be received by the logic element "*from the computer system*," not from some intervening piece of circuitry. Without exception, the specification also consistently discloses that the logic element receives input control

signals directly from the computer system without intervening circuitry, stating that:

- "The logic element 40 receives a set of input control signals *from the computer system*." 5:19-21 (emphasis added); *see also* 11:63-66.
- "As schematically illustrated by Figs. 1A and 1B, in certain embodiments, the logic element 40 receives a set of input control signals . . . from the computer system" 6:63-7:2.
- "The memory module 10 receives row/column address signals or signal bits (A_0-A_{n+1}), bank address signals (BA_0-BA_m), chip-select signals (CS_0 and CS_1), and command signals (e.g., refresh, precharge, etc.) *from the computer system*." 7:48-52 (emphasis added); *see also* 7:56-62, 14:25-26, 17:37-39.
- "The memory module 10 further comprises a logic element 40 which receives a first set of address and control signals *from* a memory controller (not shown) of *the computer system*." 20:63-66 (emphasis added); *see also* 21:45-49.

No disclosed embodiment contains intervening circuitry between the computer system and logic element to change the signals. All embodiments require the logic element to receive signals *from the computer system directly*, not from intervening circuitry.

The patent's figures also show signals are received by the logic element directly from the computer system, not from any intervening circuitry. Figures 1A, 1B, 2A, 2B, 3A and 3B all depict signal lines connecting the computer system directly to the logic element – none of them routed through interim circuitry. Fig. 1A (signal lines CS_0, CS_1, A_{n+1}, Command, and BA_0-BA_m connected directly to logic device 40), Fig. 1B (signal lines CS_0, A_{n+1}, Command, and BA_0-BA_m connected directly to logic device 40), Fig. 2A (signal lines BA_0, BA_1, A_0-A_{11}, RAS/CAS/WE, CS_0, CS_1, A_{12} and A_{13} connected directly to logic element 40), Fig. 2B (signal lines A_{12}, BA_0, BA_1, RAS/CAS/WE, CS_0, CS_1 and A_{13} connected directly to PLD (logic element) 40), Fig. 3A (signal lines BA_0, BA_1, A_0-A_{12}, RAS/CAS/WE, CS_0, CS_1 and A_{13} connected directly to logic element 40), Fig. 3B (signal lines BA_0, BA_1, RAS/CAS/WE, CS_0, CS_1 and A_{13} connected directly to logic element 40). It is simply not true (as Netlist claims) that the patent never describes the logic element as "directly" receiving signals from the computer system – all six of these drawings show precisely this arrangement, and none of them show any circuitry to change the signals

between the logic element and computer system. Op. Br. at 8. In no disclosed embodiment does the logic element receive signals from intervening circuitry instead of the computer system.

2. Netlist's Proposed Construction Conflicts with the Intrinsic Record

Netlist's construction of "logic element" attempts to expand claim 1 so that input control signals need not be received "from the computer system," but from any source. By construing "logic element" more broadly than the claim language permits, Netlist hopes to characterize a much broader range of memory modules as infringing. Because it conflicts with the language of claim 1 and the specification, Netlist's construction of "logic element" is improper.

Netlist's construction of "logic element" is contradicted by the intrinsic record. Its "predefined function" language, for instance, does not appear in the specification. *Id.* at 7. This language covers a much broader range of computer operations than claim 1, which describes only the logic element's generation of output signals from a set of input signals. Moreover, while Netlist's definition limits the logic element to a "hardware circuit," the specification states that it may be comprised of a variety of integrated circuits as well as discrete elements, 6:47-60, and that the logic element may be programmed using either hardware *or* software, 14:6-10.

Netlist's construction strays so far from the context of claim 1 because it is based on an extrinsic dictionary definition and not the specification. Op. Br. at 7. This extrinsic evidence, even from a technical dictionary, is not helpful and ignores the patent's language. *Phillips*, 415 F.3d at 1321. As Netlist's construction conflicts with the intrinsic record, it must be rejected.

B. "rank"

Google's Proposed Construction	Netlist's Proposed Construction
"row"	"row of memory devices"

The parties' dispute over construction of the term "rank" arises from Netlist's attempt to define it in a way that is redundant and nonsensical in the context of claim 1.

1. The Intrinsic Evidence Unambiguously Shows a "Rank" Is a Row

The specification's text and drawings equate a "rank" with a "row." Without exception, the specification consistently describes "ranks" as "rows," stating that the "DRAM devices of a memory module are generally *arranged as ranks or rows of memory*, each rank of memory

generally having a bit width." 2:16-22 (emphasis added); *see also* 6:38-43. Figures 1A, 1B, 2A and 3A also show each "rank" as a row of memory devices. Figure 1A shows four ranks of memory devices (32, 34, 36 and 38), and Figure 1B shows two ranks (32 and 34). *See also* 19:62-64; 22:34-37. Figure 3A includes four ranks depicted as rows (32, 34, 36, 38), each comprised of nine memory devices. Fig. 3A; 22:51-54.

2. Netlist's Construction Of "Rank" Leads To A Nonsensical Reading Of Claim 1

Netlist argues that "ranks" are "rows of memory devices." Inserting this construction into claim 1 results in a clause that would read, "the set of input control signals corresponds to a second number of **rows of memory devices** of memory modules." Because "rows of memory devices of memory modules" makes no sense, Netlist's construction should be rejected.

C. "signal"

Google's Proposed Construction	Netlist's Proposed Construction
"information presented on one or more pins of a device dedicated for that specific information"	no construction required, or, alternatively, "an event or phenomenon that conveys information"

The parties' dispute over "signal" stems from Netlist's improper attempt to construe it with a dictionary definition instead of in its intrinsic context. Google's description of a "particular mechanical structure" in its construction is proper in light of the intrinsic record

Op. Br. at p. 9. By contrast, Netlist's overbroad and ambiguous construction of "signal" out of its intrinsic context is improperly drawn to the term's generic function. Claim construction should focus on the structure embodying claim limitations, not merely on their function. *Halliburton Energy Servs. Inc. v. M-I LLC*, 514 F.3d 1244, 1255 (Fed. Cir. 2008). It is for this reason -- to clarify what the term "signal" means and structurally requires in its context -- that it requires construction.

1. The Intrinsic Evidence Affirms Google's Construction

(a) The Drawings Show Signals Presented On Dedicated Pins

The specification consistently shows signals presented on dedicated pins of the logic

element.[4] Google's construction is not based, as Netlist suggests, on simply a "narrow excerpt" of the patent relating to DQ and DQS data pins. The patent's figures consistently show different lines, each dedicated to a particular type of signal, on which signals are transmitted between devices. Because signals presented on signal lines are always presented on pins or equivalent metal connectors, each of these signal lines necessarily connects to the logic element on a dedicated pin.

Figures 1A, 1B, 2A, 2B, 3A and 3B all show signals as information presented to the logic element on dedicated signal lines and pins. Fig. 1A (CS_0, CS_1, A_{n+1}, Command Signals, BA_0-BA_m, CS_{0A}, CS_{0B}, CS_{1A}, CS_{1B}); Fig. 1B (CS_0, A_{n+1}, Command Signals, BA_0-BA_m, CS_{0A}, CS_{0B}); Fig. 2A (BA_0, BA_1, A_0-A_{11}, RAS/CAS/WE, CS_0, CS_1, A_{12}, A_{13}); Fig. 2B (A_{12}, BA_0, BA_1, RAS/CAS/WE, CS_0, CS_1, A_{13}); Fig. 3A (BA_0, BA_1, A_0-A_{12}, RAS/CAS/WE, CS_0, CS_1, A_{13}); Fig. 3B (BA_0, BA_1, RAS/CAS/WE, CS_0, CS_1, A_{13});

. Fig. 1A shows two chip-select signals CS_0 and CS_1 as inputs to two corresponding pins of logic element 40. Address signal A_{n+1}, command signals, and bank address signals BA_0-BA_m are shown as inputs to dedicated pins of the logic element, and four output chip-select signals CS_{0A} - CS_{1B} are presented on output pins of the logic element.

The module of Figure 1A and claim 1 distinguishes amongst types of signals based on which signal line carries them to the logic element.

(b) The Text Of The Specification Confirms Signals Are Transmitted On Dedicated Pins

The specification consistently explains that signals are transmitted by varying voltages on pins. The specification describes data signals as described transmitted on dedicated pins of the logic element and memory devices. 29:58-63; 31:65-32:11. Table 1 and the accompanying text also show logical states for logic element inputs and outputs during rank selection. To select Rank 0, the logic element "pulls"[5] the voltage to a low value on the pin assigned to receive rank select

[4] In the context of memory modules, a pin is a small metal part that physically and electrically connects the memory device to the PCB. The parties do not dispute the definition of "pin."

[5] "Pulling" high or low sends a signal by varying a voltage on a signal line connected to a device pin.

signals for that rank; here, CS_{0A} is assigned to signals that select Rank 0.[6] 8:15-24. To select Rank 1, the logic element pulls the voltage to a low value on the CS_{0B} pin. 8:21-28. Table 1 shows other pins being pulled to a high or low voltage to select other ranks. 8:15-45. Even the allegedly embodying devices built by Netlist all transmit data signals on dedicated signal lines and pins.

(c) Google Does Not Import Limitations Into Claim 1

Google's construction does not read limitations into claim 1, but only gives the claim its proper scope and meaning in the context of the specification. "Although the specification need not present every embodiment or permutation of the invention …neither do the claims enlarge what is patented beyond what the inventor has described as the invention." *Netword v. Centraal*, 242 F.3d 1347, 1352 (Fed. Cir. 2001). Netlist does not, and cannot, point to a single embodiment using the term "signal" to refer to information presented in any way other than on a dedicated pin of a device. Netlist simply has not described embodiments that do not use dedicated pins to transmit signals. *Nikon Corp v. ASM Lithography*, 308 F.Supp.2d 1039, 1100, (N.D. Cal. 2004) ("Where specification language identifies an essential claim feature, and where the embodiments uniformly disclose that feature, the feature proves a required limitation of all the relevant claims.").

2. Netlist's Overly Broad Construction Lacks Intrinsic Support

Netlist's construction of "signal" is overly broad, vague, unhelpful to a jury and divorced from the specification. "Events" and "phenomena" are broad generic terms that do not appear in the intrinsic record, do not relate to memory modules, and have no technical meaning. A "phenomenon," in particular, has no relevance in this context – even smoke signals, clearly outside the realm of computer memory technology, are "signals" under Netlist's construction.

Instead of relying on the specification, Netlist's construction derives from extrinsic evidence alone. Netlist arbitrarily chose one dictionary definition out of 16 possibilities for "signal," and picked one of the broadest, most general and least helpful in this context. Netlist

[6] While Table 1 does not use the term "pins," the varying voltages it describes applying to particular signal lines must be received by the logic element and memory devices on pins or equivalent metal connectors. Without such metal connectors, the electrical signal cannot travel from one device to another.

does not explain why this definition is preferable to one more closely tied to digital data devices. In this case, reference to extrinsic evidence is unnecessary and inappropriate, since the intrinsic evidence plainly shows that signals are presented on dedicated pins of the logic element.

D. "control signals"

Google's Proposed Construction	Netlist's Proposed Construction
"signals presented on control pins of the logic element"	"signals, including address and command signals, that regulate system operations"

As with "signal," the parties dispute whether "control signal" should be given the simple meaning it has in the specification, or a much broader, and more ambiguous, extrinsic definition that introduces further undefined terms and essentially leaves claim construction to the jury.

1. The Specification And Industry Standards Confirm Google's Construction of "Control Signal"

Google's construction affirms that since signals are transmitted on dedicated pins, control signals are received or transmitted on control pins. The specification refers to "control signals" to describe signals, received from the computer system on dedicated pins, which select or activate portions of the memory module. 2:34-36. Control signals include rank-select and chip-select signals, as well as certain address signals and commands. 2:36-38, 5:36-40. As shown in Figures 1A and 1B, these signals are always input on separate, dedicated signal lines and pins. Control signals CS_0, CS_1, BA_0-BA_m, and A_0-A_n are all shown as tied to control pins, each pin dedicated to its respective signal. Figures 2A and 2B also show control signals BA_0, BA_1, CS_0 and CS_1 transmitted on separate, dedicated signal lines and control pins. The same is true of control signals generated by the logic element, which are received by the memory devices on dedicated pins. None of the drawings depict control signals transmitted in any other way.

Extrinsic evidence also supports Google's construction. JEDEC specification JESD79F, concerning DRAM devices, is an industry standard that those skilled in the art would reference.[7] It refers to control signals as inputs on dedicated pins. Ex. 4 (JESD79F) at Table 2, p. 6 (showing

[7] JEDEC is a standard setting organization that develops specifications and standards for the computer memory module industry.

Bank Address and Address signal inputs in table of "Pin Descriptions"). JEDEC specifications are particularly relevant since Netlist claims that its patent covers Mode C of a related JEDEC standard for FBDIMM devices. Ex. 5 (Am. Infrg. Cont.); . The inventors' incorporation of a JEDEC standard into the patent demonstrates that JEDEC standards are relevant to the alleged invention. 12:41-45.

2. Netlist's Proposed Construction Lacks Intrinsic Support

Netlist's construction of "control signals" is overbroad and not supported by intrinsic *or* extrinsic evidence. Nothing in the intrinsic record describes control signals as "signals… *that regulate system operations*" – this language appears nowhere in the specification or prosecution history. Neither of the specification excerpts Netlist cites refers to "regulat[ing] system operations" or explain what it means to "regulate system operations." Op. Br. at 12; 6:64-7:2, 2:34-36. Furthermore, Netlist presents no extrinsic evidence to support this language. "Regulate system operations" is so broad as to be virtually limitless, and would do more to confuse than to enlighten the jury. In particular, Netlist's construction gives the jury no way to distinguish "control signals" from other signals (like "command signals") sent by the computer system.

E. "the set of input control signals corresponding to a second number of memory devices smaller than the first number of memory devices"

Google's Proposed Construction	Netlist's Proposed Construction
"the set of input control signals generated by the computer system to control a memory module having the second number of memory devices, based on the computer system understanding the memory module to have the second number of devices"[8]	no construction required, or, alternatively, "the set of input control signals received from the computer system, which is configured to utilize a memory module having a second number of memory devices"

The parties' dispute over this phrase stems from Netlist's effort to read the "corresponding to" limitation – the heart of the alleged invention -- out of the claim entirely.[9]

[8] *See* footnotes 1 and 2, *supra*, for clarification of the terms "first number" and "second number."

[9] Unless the two "corresponding to" limitations in the patent are construed to preclude a signal from "corresponding to" both the actual number and the apparent number of memory devices and ranks of devices, the asserted claims are indefinite. The claims implicitly require that the signal "corresponding to" the smaller, apparent number of devices or ranks does not also "correspond to"

1. The Intrinsic Evidence Supports Google's Proposed Construction

(a) The Patent's Purpose Is To Allow A Module To Use More Memory Devices Than The System Is Configured To Operate

The specification shows Google's construction is correct. It repeatedly indicates, including in the Summary of the Invention, that the patent's purpose is to allow a computer system to use a memory module with more memory devices or ranks than it was designed to operate, stating that:

- "In certain embodiments, the memory module 10 simulates a virtual memory module when the number of memory devices 30 of the memory module 10 is larger than the number of memory devices 30 per memory module for which the computer system is configured to utilize." 7:23-28.
- "In certain embodiments, the set of output control signals corresponds to a first number of ranks in which the plurality of memory devices 30 of the memory module 10 are arranged, and the set of input control signals corresponds to a second number of ranks per memory module for which the computer system is configured. The second number of ranks in certain embodiments is smaller than the first number of ranks." 7:6-14.
- "In certain embodiments, the computer system is configured for a number of ranks per memory module which is smaller than the number of ranks in which the memory devices 30 of the memory module 10 are arranged." 7:30-33; *see also* 7:33-43.
- "The logic element receives a set of input control signals from the computer system. The set of input control signals corresponds to a second number of memory devices smaller than the first number of memory devices. The logic element generates a set of output control signals in response to the set of input control signals. The set of output control signals corresponds to the first number of memory devices." 2:51-58; *see also* 2:63-3:3; 3:8-16.

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the actual number of devices or ranks, and this is necessarily so; otherwise, the claims would encompass modules in which the actual number of memory devices and ranks is the same as the apparent number of devices and ranks, and such modules are clearly prior art.

Netlist admitted as much when it told the Court that the patented modules "fool[] the computer into thinking that it is accessing two sets of memory chips, when in fact its access requests are split among four less-expensive sets of memory chips." Ex. 3 at 2 (5/19/09 Ltr. Br. to J. Spero). the essence of the alleged invention as the memory module's ability to "trick" the computer system into seeing only the apparent number of memory devices on the memory module instead of the actual number.

(b) The Memory Module Informs The Computer System That The Module Has Fewer Memory Devices Than It Actually Contains

To allow the computer system to operate a memory module with more memory devices or ranks than it was configured to operate, claim 1 and every disclosed embodiment require that the module inform the computer system that it has fewer devices or ranks than are actually present -- thus "tricking" the computer system to see the module as having the apparent number of devices. The specification consistently explains this process of "tricking" the computer system, stating that:

- "[I]n certain embodiments, the SPD[10] device 70 comprises data which characterizes the memory module 10 as having fewer memory devices than the memory module 10 actually has, with each of these memory devices having more memory density per memory device. 10:45-49; *see also* 10:49-55.
- "In certain embodiments, the SPD device 70 comprises data which characterize the memory module 10 as having fewer ranks of memory devices than the memory module 10 actually has, with each of these ranks having more memory density." 10:31-35; *see also* 10:35-45.
- "In certain such embodiments, the SPD device 70 of the memory module 10 is programmed to describe the combined pair of lower-density memory devices 31, 33 as one virtual or pseudo-higher-density memory device." 11:6-9; *see also* 10:63-11:5; 11:9-15.

[10] The serial-presence detect, or "SPD," device is the memory module component that reports information to the computer system about the memory module's configuration and number of memory devices. 9:24-38, 11:44-49;

- "In certain embodiments, when such a memory module 10 is inserted in a computer system, the computer system's memory controller than provides to the memory module 10 a set of input control signals which correspond to the number of ranks or the number of memory devices reported by the SPD device 70. For example, placing a two-rank memory module 10 compatible with certain embodiments described herein in a computer system compatible with one-rank memory modules, the SPD device 70 reports to the computer system that the memory module 10 only has one rank." 11:44-53; *see also* 11:37-43; 11:53-12:11.

Netlist does not, and cannot, identify a single embodiment using any alternative to this way of "tricking" the computer system. As one of the inventors confirmed, "tricking" the computer system to see a smaller number of memory devices than the memory module actually contains is the core of the alleged invention.

(c) The Computer System Generates A Set Of Input Signals For The Number Of Devices Reported By The Memory Module

Because the computer system sees only the apparent number of memory devices on the memory module, the computer system generates and sends input control signals corresponding to the apparent number of devices.[11] The specification repeatedly explains (including in the Summary of the Invention) that the computer system generates input control signals based on its understanding that the memory module contains the apparent number of devices, stating that:

- "The logic element receives a set of input control signals from the computer system. The set of input control signals corresponds to a second number of memory devices smaller than the first number of memory devices. The logic element generates a set of output control signals in response to the set of input control signals. The set of output control signals corresponds to the first number of memory devices." 2:51-58; *see also* 2:63-3:3, 3:8-16.

[11] As explained in footnotes 2 and 3, the "first number" in claim 1 is the actual number of devices, while the "second number" is the smaller, apparent number of devices.

- "[W]hen a two-rank memory module 10 compatible with certain embodiments described herein is placed in a computer system compatible with either one- or two-rank memory modules, the SPD device 70 reports to the computer system that the memory module 10 only has one rank. The logic element 40 then receives a set of input control signals corresponding to a single rank from the computer system's memory controller...." 11:59-66; *see also* 7:6-18, 11:44-59, 12:2-11.
- "The memory module 10 further comprises a logic element 40 which receives a first set of address and control signals from a memory controller (not shown) of the computer system. The first set of address and control signals is compatible with a second memory capacity substantially equal to one-half of the first memory capacity." 20:63-21:1.

The drawings also show the computer system understands the memory module to have the apparent number of devices, and generates a set of input control signals corresponding to that apparent number. Figures 1A and 1B show that in response to being informed by the module that it has the apparent number of devices, the computer system generates input control signals to operate the apparent number of devices. Figure 1A depicts a computer system configured to use two ranks of devices and to present a corresponding two chip-select signals to the logic element. Fig. 1A (CS_0, CS_1). Figure 1B shows a computer system configured for one rank of devices and to present one corresponding chip-select signal to the logic element. Fig. 1B (CS_0), 7:39-44.

(d) The Specification Does Not Disclose Any Embodiment Where The Memory Module Reports To The Computer System The Actual Number of Memory Devices It Contains

The specification does not disclose a single embodiment where the patented module informs the computer system of its actual configuration. Claim 1 requires the computer system to understand the memory module to have the *apparent number* of memory devices, not the actual number, since the claim recites that the logic element receives signals from the computer system corresponding to the apparent number of devices. 33:25-34:2 (claim 1); . While Netlist claims embodiments are disclosed where the computer system is aware of the actual number of devices, the only section Netlist cites is one describing prior art computer operations, not the claimed invention. Op. Br. at 14, 16; 9:31-

37. It is not dispositive that the specification refers to "certain embodiments" when describing how to "trick" the computer system. Op. Br. at 14-15. As every disclosed embodiment requires this limitation, it restricts the scope of the claims. *Curtiss-Wright*, 438 F.3d at 1379-80.

(e) Google's Construction Does Not Improperly Import A Limitation Into The Claim

Google's construction does not import a limitation into claim 1 by requiring that the "computer system understand[] the memory module to have the second [smaller] number of devices." Op. Br. at 13-14. Google simply explains the "corresponding to" limitation as it appears in the patent. Every time "corresponding to" appears in the specification referring to input signals, it is in the context of language explaining that the computer system sees the module as having the apparent number (not the actual number) of devices and generates signals according to that understanding. 2:50-55; 2:62-67; 3:5-12; 5:16-23; 7:7-14; 11:44-55; 11:59-65. Only Google's construction gives meaning to each word of the claim, as required by settled law. *Warner-Jenkinson*, 520 U.S. at 29.

2. Netlist's Proposed Construction Reads The "Corresponding To" Limitation Out Of Claim 1 And Ignores The Intrinsic Record

Netlist's suggestion that this phrase needs no construction at all, like its fallback definition, is untenable in light of the intrinsic record. Op. Br. at 13-15. Netlist's fallback construction is erroneous since it reads "corresponding to" out of the claim entirely. Netlist draws no connection at all between the input control signals and the devices to which they correspond. Netlist also reads "smaller than the first number" out of the claim, and does not even require that the "second number of memory devices" be "smaller than the first number of memory devices." Because Netlist's construction fails to give meaning to each element of claim 1, it must be rejected. *Warner-Jenkinson*, 520 U.S. at 29. The fact that the parties disagree as to the import of "corresponding to" shows why this term requires construction. *02 Micro*, 521 F.3d at 1361-62.

F. "command signal"

Google's Proposed Construction	Netlist's Proposed Construction
"a signal presented on command pins of the logic element"	"a signal, such as a read, write, refresh, or precharge signal, that initiates a predetermined type of computer operation"

1. The Intrinsic and Extrinsic Evidence Support Google's Construction

Google's construction of "command signal" is correct for the same reasons as its "signal" and "control signal" definitions. Google's construction affirms that since the patent shows signals are presented on separate, dedicated signal lines and pins, command signals are presented on command pins. Fig. 1A (Command Signals); Fig. 1B (same); 6:64-7:2; 7:60-62. JEDEC specification 79F, an industry standard referenced by those skilled in the art, also includes in its "Pin Descriptions" table entries for RAS, CAS, and WE, calling them "command inputs [that] define the command being entered." Ex. 4 (JEDEC79F) at Table 2, p. 6. In other words, the JEDEC standard defines command signals as signals input on command pins. The patent's deference to JEDEC standards makes this highly relevant extrinsic evidence. 12:41-45.

2. Netlist's Vague Construction Is Not Derived From the Specification

Netlist's construction is so overly broad and ambiguous that it adds more confusion than it dispels. For example, Netlist uses the term "computer operation" in a confusing and incorrect way in the context of claim 1. The computer initiates the operation in claim 1; the command signal does not "initiate" the computer to do anything. 33:45-46. Moreover, neither of the specification sections Netlist cites supports the "initiates a predetermined type of computer operation" part of its construction, as that phrase appears nowhere in the specification. Op. Br. at 11; Table 1, n.4 (command signals "define operations"), 8:48 (describing command column of Table 1).

Since the intrinsic record lends it no support, Netlist again resorts to an extrinsic dictionary. Op. Br. at 11. Dictionary definitions are less relevant than the specification. *Phillips*, 415 F.3d at 1321. The definition Netlist cherry-picks is overly broad in view of the specification, which shows pins as the only mechanism for conveying command signals between the computer system, the logic element, and the memory devices. Netlist also gives the jury no way to

distinguish "command signals" from other kinds of signals (like "control signals") sent by the computer system.

G. "number of ranks of memory modules"

Google's Proposed Construction	Netlist's Proposed Construction
no construction required	"the common number of ranks in which memory devices are arranged on particular memory modules"

1. This Term Requires No Construction

"Number of ranks of memory modules" requires no construction. It contains no ambiguous terms, as the parties essentially agree that "ranks" are arranged in "rows," and "number" and "memory module" have plain and ordinary meanings.

2. Netlist's Proposed Construction Is Contrary to the Specification

Netlist attempts to correct an apparent incongruity in claim 1 with a construction contrary to the intrinsic evidence. While the specification explains that memory devices may be arranged in "ranks" on a memory module, claim 1 claims a memory module which, in part, is comprised of a "number of ranks of memory modules." Netlist attempts to correct this incongruity by offering a construction of the claim language that simply masks the discrepancy in the claim language.

The specification, however, does not disclose any "common number of ranks" of memory devices on memory modules. Instead, it discusses various numbers of ranks of devices (one, two, and four) on a module, 2:27-30, and states the patented module is compatible with other numbers of ranks of devices not specifically disclosed, 6:44-46. Netlist fabricates a "characteristic" of memory modules that does not exist, and improperly imports it into claim 1.[12] Its "common number of ranks" language is also nonsensical. In a computer system using one two-rank module and one four-rank module, for instance, there is no "common number" of ranks of memory modules. Because Netlist's construction is erroneous and nonsensical, this term should be given its plain meaning.

[12] Claim 1, after all, is directed to a particular memory module, and does not purport to describe universal "characteristics" of all memory modules.

H. "the first command signal corresponding to the second number of ranks"

Google's Proposed Construction	Netlist's Proposed Construction
"the first command signal generated by the computer system to command a memory module having the second number of ranks, based on the computer system understanding the memory module to have the second number of ranks"	no construction required, or, alternatively, "the first command signal received from the computer system, which is configured to utilize a memory module having the second number of ranks"

The parties' dispute over this phrase again stems from Netlist's effort to read "corresponding to" out of claim 1. The phrase requires construction due to the parties' evident disagreement as to its scope. *O2 Micro*, 521 F.3d at 1361-62.

1. The Specification Shows That The System Generates A Command Signal To Operate The Number Of Ranks Reported By The Module

The intrinsic evidence supports Google's construction and makes clear that the computer system generates a command signal to operate the apparent number of ranks of devices. The specification describes this process consistently throughout, explaining that the module reports to the computer system that it contains the apparent number of ranks instead of the actual number:

> In certain embodiments, the SPD device 70 comprises data which characterize the memory module 10 as having fewer ranks of memory devices than the memory module actually has, with each of these ranks having more memory density. For example, for a memory module 10 compatible with certain embodiments described herein having two ranks of memory devices 30, the SPD device 70 comprises data which characterizes the memory module 10 as having one rank of memory devices with twice the memory density per rank.

10:31-40; *see also* 10:40-45; 8:60-64; . The specification repeatedly explains that the computer system thus understands the module to contain the apparent number of ranks of devices, not the actual number of ranks:

- "Thus, in certain embodiments, even though the memory module 10 actually has the first number of ranks of memory devices 30, the memory module 10 simulates a virtual memory module by operating as having the second number of ranks of memory devices 30." 7:18-24.

- "[A] four-rank memory module 10 compatible with certain embodiments described herein simulates a two-rank memory module…." 12:2-4.
- "[I]n certain embodiments, two ranks of memory devices having a memory density are used to simulate a single rank of memory devices having twice the memory density, and an additional address signal bit is used to access the additional memory." 12:18-22.

Based on this understanding, the computer system generates a command signal to operate the apparent number of ranks of devices. As the specification explains:

> In certain embodiments, the computer system is configured for a number of ranks per memory module which is smaller than the number of ranks in which the memory devices 30 of the memory module 10 are arranged. In certain such embodiments, the computer system is configured for two ranks of memory per memory module (providing two chip-select signals CS_0, CS_1) and the plurality of memory [devices] 30 of the memory module 10 are arranged in four ranks, as schematically illustrated by Fig. 1A. In certain other such embodiments, the computer system is configured for one rank of memory per memory module (providing one chip-select signal CS_0) and the plurality of memory modules 30 of the memory module 10 are arranged in two ranks, as schematically illustrated by Fig. 1B.

7:30-44; *see also* 7:45-62; 12:2-11;

2. The Patent Does Not Describe Any Embodiment Where The Computer System Generates A Command Signal Corresponding To The Actual Number Of Ranks Of Memory Devices On The Module

Netlist erroneously claims the patent describes embodiments where the module informs the computer system of the actual number of ranks . Op. Br. at 16;

. The only specification section Netlist cites describes how prior art modules transmit data to the computer system specifying their number of devices and ranks. 9:24-37. It does not describe any claimed embodiment. *Id.* It is not dispositive that the patent refers to "certain embodiments" when explaining how the module "tricks" the computer system into generating a command signal to operate the apparent number of ranks. As each embodiment requires this limitation, it restricts the scope of claim 1. *Curtiss-Wright*, 438 F.3d at 1379-80.

3. Google's Construction Does Not Import Limitations Into Claim 1

Google does not import limitations into claim 1 by requiring that the computer system understand the module to have the apparent number of ranks of devices. Op. Br. at 16. Google's construction simply accounts for the "corresponding to" limitation that Netlist ignores altogether.

Google's construction does not limit the scope of claim1 to only one of many embodiments. *Id.* at 16. In each disclosed embodiment using command signals, the computer system generates a command signal for the apparent number of ranks that the computer system sees. 7:39-44; 7:45-62; 12:2-11; 20:63-21:6; . Since every embodiment has this limitation, it restricts the scope of claim 1. *Phillips*, 415 F.3d at 1323.

4. Netlist's Construction Does Not Give Meaning to Each Claim Term

Netlist's construction again reads the "corresponding to" limitation out of claim 1. Netlist's construction is far broader than the claim, requiring only that (1) the first command signal be "received from the computer system," and (2) the computer system be configured for the apparent number of ranks. This construction ascribes no meaning at all to the "corresponding to" limitation. It identifies no relationship between the "first command signal" and the "second number of ranks," let alone a "corresponding" relationship. Because Netlist fails to give meaning to each claim term, its construction is incorrect. *Warner-Jenkinson*, 520 U.S. at 29.

I. "chip-select signal"

Google's Proposed Construction	Netlist's Proposed Construction
"signal presented on chip-select pins of the logic element"	"an address signal that enables the input and output of data to and/or from a memory device"

1. Google's Construction Accords With the Intrinsic Evidence and Industry Standards

Google's construction of "chip-select signal" is correct for the same reasons as its constructions of the other "signal" terms. Google's construction affirms that since the patent describes only signals presented on dedicated pins, "chip-select signals" are signals presented on chip-select pins.

The specification leaves no doubt that chip-select signals are transmitted on dedicated pins. Chip-select signals CS_0 and CS_1 in Figures 1A, 1B, 2A, 2B, 3A and 3B are transmitted on separate, dedicated signal lines and pins. *See also* 7:56-59. The logic table in Table 1 and accompanying text at 8:14-45 describing chip selection show chips or ranks are selected by

pulling voltages high or low on dedicated chip-select pins.[13] 8:26-27 ("CS_{0B} is pulled low, thereby selecting Rank 1"); *see also* 8:23-24; 8:29-30; 8:33-34; 8:36-37; 8:40-41; 8:43-45.

JEDEC standard 79F also supports Google's construction. The standard explicitly references chip-select pins: "The standard pinout includes one CS [chip-select] pin. Optional pinouts include CS_0 and CS_1 on different pins." Ex. 4 (JESD79F) at Table 2, p. 6. JEDEC Standard No. 100B.01 is in accord. Ex. 6 (JEDEC Standard No. 100B.01) at 3. By referring to signals as "active" and "prevent[ing] input or output to or from *the integrated circuit.*" the standard clearly describes signals transmitted by varying voltages on pins.

2. Netlist's Construction Conflicts With the Specification and Is Technically Inaccurate

Netlist's construction conflicts with the specification and is technically inaccurate. The specification distinguishes between chip-select signals and address signals, stating that "[t]he logic element 40 receives the two chip-select signals (CS_0 and CS_1) ***and*** one row/column address signal (A_{n+1}) from the computer system." 7:56-59 (emphasis added). It would be odd to list chip-select signals and address signals if one were a subset of the other. Moreover, chip-select signals as described in the patent, do not control input and output to and from a particular device, but instead enable or disable (activate or deactivate) entire ranks of devices. 2:34-38.

V. CONCLUSION

For the foregoing reasons, Google requests that the Court adopt its proposed constructions.

Dated: August 25, 2009

FISH & RICHARDSON P.C.

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[13] As previously noted, a signal created by "pulling" high or low to vary voltage on a signal line necessarily travels on a metal connector called a pin in order to reach its destination. Without a metal pin connecting the signal line to the device receiving the signal, the signal could not be received by the destination device.