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GOOGLE INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

OAKLAND DIVISION

GOOGLE INC.,

Plaintiff,

v.

NETLIST, INC.,

Defendant.

AND RELATED COUNTERCLAIMS.

Case No. 08-04144 SBA

APPENDIX 1 TO GOOGLE'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

Date: November 12, 2009
Time: 9:00 a.m.
Place: Courtroom 3, 3rd Floor
Judge: Hon. Saundra Brown Armstrong

Claim 1 of U.S. Patent No. 7,289,386 ("the '386 patent) recites:

> 1. A memory module connectable to a computer system, the memory module comprising:
> a printed circuit board;
> a plurality of memory devices coupled to the printed circuit board, the plurality of memory devices having a first number of memory devices; and
> a logic element coupled to the printed circuit board, the **[1]** ***logic element receiving a set of input control signals from the computer system***, **[5]** ***the set of input control signals corresponding to a second number of memory devices smaller than the first number of memory devices***, the logic element generating a set of output **[4]** ***control signals*** in response to the set of input control signals, the set of output control signals corresponding to the first number of memory devices, wherein the plurality of memory devices are arranged in a first number of **[2]** ***ranks***, and the set of input control signals corresponds to a second **[7]** ***number of ranks of memory modules***, the second number of ranks less than the first number of ranks, wherein the logic element further responds to a first command **[3]** ***signal*** from the computer system by generating a second **[6]** ***command signal*** transmitted to the plurality of memory devices, **[8]** ***the first command signal corresponding to the second number of ranks*** and the second command signal corresponding to the first number of ranks.

'386 Patent, at 33:24-34:2 (emphasis and annotations added).

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No.	Google's Proposed Construction	Netlist's Proposed Construction
1.	**"logic element receiving a set of input control signals from the computer system"**	
	electronic circuitry operable to perform one or more particular functions and that receives input signals directly from the computer system	"logic element" means a hardware circuit that performs a predefined function on input signals and presents the resulting signals as its output
2.	**"rank"**	
	row	rows of memory devices
3.	**"signal"**	
	information presented on one or more pins of a device dedicated for that specific information	[1] no construction required, or, alternatively, [2] an event or phenomenon that conveys information
4.	**"control signals"**	
	signals presented on control pins of the logic element	signals, including address and command signals, that regulate system operations
5.	**"the set of input control signals corresponding to a second number of memory devices smaller than the first number of memory devices"**	
	the set of input control signals generated by the computer system to control a memory module having the second number of memory devices, based on the computer system understanding the memory module to have the second number of devices	[1] no construction required, or, alternatively, [2] the set of input control signals received from the computer system, which is configured to utilize a memory module having a second number of memory devices
6.	**"command signal"**	
	a signal presented on command pins of the logic element	a signal, such as a read, write, refresh, or precharge signal, that initiates a predetermined type of computer operation
7.	**"number of ranks of memory modules"**	
	no construction required	the common number of ranks in which memory devices are arranged on particular memory modules
8.	**"the first command signal corresponding to the second number of ranks"**	
	the first command signal generated by the computer system to command a memory module having the second number of ranks, based on the computer system understanding the memory module to have the second number of ranks	[1] no construction required, or, alternatively, [2] the first command signal received from the computer system, which is configured to utilize a memory module having the second number of ranks

Claim 11 of the '386 patent recites:

> 11. The memory module of claim 1, wherein the set of input control signals comprises two **[9]** ***chip-select signals*** and an address signal and the set of output control signals comprises four chip-select signals.

'386 Patent, at 34:32-35 (emphasis and annotation added).

No.	Google's Proposed Construction	Netlist's Proposed Construction
9.	**"chip-select signal"**	
	signal presented on chip-select pins of the logic element	an address signal that enables the input and output of data to and/or from a memory device

Dated: August 25, 2009

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