EXHIBIT B

JEDEC STANDARD

JEDEC Dictionary of Terms for Solid State Technology — 5th Edition

JESD88D

(Revision of JESD88C, July 2007)

DECEMBER 2009

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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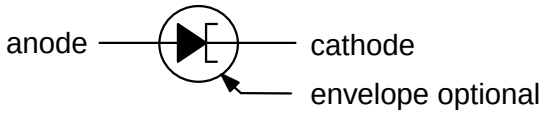
Terms, abbreviations, letter symbols, and definitions **References**

backward diode: A semiconductor diode in which quantum-mechanical tunneling leads to a current-voltage characteristic with a reverse current greater than the forward current, for equal and opposite applied voltages, in some voltage range centered about the origin. JESD77C, 10/09

Graphic symbol (ref. IEEE Std 315):



balanced amplifier: An amplifier in which the quiescent dc output voltage (or, if the output is a differential output, the difference between the two quiescent dc output voltages) has been reduced to zero or other specified level. JESD99B, 5/07

ball bond: See "bond, ball".

ball grid array (BGA): A package in which the external connections to the package are made via a rectangular array of ball-type connections, all on a common plane. JESD21-C, 1/97 JESD22-B112, 5/05

NOTE See also "grid array package".

bandwidth (*B* or BW): The range of frequencies within which the gain of the amplifier is not more than 3 dB below the value of the midband gain. JESD99B, 5/07

NOTE Midband gain is the gain at a specified frequency or the average gain over a specified frequency range.

bandwidth, maximum output swing (B_{OM}): The range of frequencies within which the maximum output voltage swing is above the specified value at a specified load impedance. JESD99B, 5/07

bandwidth, unity gain: The range of frequencies within which the open-loop amplification is greater than unity. JESD99B, 5/07

bank address (BA): In a RAM that has multiple banks in its architecture, the address used to select any one of the available banks. JESD21-C, 1/97

bar code label: A label that includes information in a code consisting of parallel bars and spaces or a 2-D matrix format. J-STD-033B.1, 1/07

NOTE 1 See also "linear bar code label".

NOTE 2 For the purpose of J-STD-033, the bar code label is on the lowest level shipping container and includes information that describes the product, e.g., part number, quantity, lot information, supplier identification, and moisture-sensitivity level.

bar code symbol: A symbol that gives information in a code consisting of parallel bars and spaces of various specific widths. JESD22-B114, 3/08

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

EXHIBIT C

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

OAKLAND DIVISION

GOOGLE INC.,)
)Case No. C-08-04144SBA
Plaintiff,)
)
vs.)
)
NETLIST, INC.,)
)
Defendant.)
_____)

*** HIGHLY CONFIDENTIAL ***

DEPOSITION OF: WILLIAM HOFFMAN

DATE: Tuesday, May 18, 2010

LOCATION: 1185 Avenue of the Americas
34th floor
New York, New York 10036

REPORTED BY: AYLETTE GONZALEZ

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

OAKLAND DIVISION

GOOGLE INC.,)
)Case No. C-08-04144SBA
Plaintiff,)
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vs.)
)
NETLIST, INC.,)
)
Defendant.)
_____)

*** HIGHLY CONFIDENTIAL ***

Videotaped Deposition of WILLIAM HOFFMAN, taken on behalf of Plaintiff, held at the offices of KING & SPALDING, LLP., 1185 Avenue of the Americas, New York, New York 10036, beginning at 8:35 a.m. and ending at 5:33 p.m., on Tuesday, May 18, 2010, before AYLETTE GONZALEZ, a Notary Public of the State of New York.

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ALSO PRESENT:

LISA LIVOTE, VIDEOGRAPHER

24-bit command field?

A. I believe so.

Q. The yellow portions in the table identify row-column address bits, right?

A. Yes.

Q. We say row-column because address signals for D-RAMs are multiplexed, correct?

A. That's correct.

Q. And the green boxes in Table 4-40 describe bank addresses, right?

A. That's correct.

Q. Those refer to internal sub-arrays within a DRAM chip, right?

A. Yes.

Q. So, for example, in Table 4-40 we see a one-gigabit row, correct?

A. Yes.

Q. And that has three bank address signals identified, or three bank address bits identified, right?

A. Yes.

Q. And those are identified as B-0, B-1, B-2?

A. Yes.

Q. And a one-gigabit DRAM has eight banks in it, right?
A. Yes.
Q. So, those three bank address bits allow you to uniquely identify one of eight banks?
A. Yes.
Q. Because each bank address bit has two logical states, right?
A. Correct.
Q. Then Column 17 says RS. Do you see that?
A. Yes.
Q. That's a rank select bit?
A. Yes.
Q. It has two logical states?
A. Yes, it does.
Q. So it identifies one of two possible ranks?
A. Yes.
Q. Now, if you look again in the one-gigabit row, there is a sub-row that says COL for column. Do you see that?
A. Yes.

I'm sorry. You asked me an either/or, didn't you?

Q. Let me ask it a different way.

This is a module that in your view transmits commands to those boxes marked RAM 22, right?

A. Yes.

Q. It transmits -- when those commands are transmitted, are they transmitted to one of those RAM chips at a time?

MS. ALTERSOHN: Objection to form, vague.

A. I believe it goes to all of them at the same time.

Q. So, all the RAMS respond to whatever command is supplied at the same time?

A. That's my understanding.

Q. There's no signal that disconnects any of those RAMS from the data bus, is there?

A. I believe that is true.

Q. This Dell 074 patent uses the term bank select signal, right?

A. Yes.

Q. And in that -- in the context of this particular reference, bank refers to an internal sub-array within the individual RAM chips, right?

A. That's correct.

Q. Now, figure 1 of the Dell 074 has a line that says, SPD read/write. Do you see that?

A. Yes, I do.

Q. Is the box identified as non-volatile memory with the number 30 and SPD?

A. Yes -- no, I'm not sure. It's a presence detect, and I'm not sure if it's serial or not.

Q. If you turn to column 5, if you would look at line 23, start there. I'll read this into the record.

In the embodiment of figure 1, the system controller 12 accesses SPD data stored in a non-volatile memory 30. The non-volatile memory 30 may be a separate memory device, such as an EEPROM or may be a

charts and combine them in Exhibit E?

A. I'm not positive that that's exactly what I did, but I certainly used a significant portion of it. Whether it's identically every piece or not, I don't know.

Q. What specific changes, if any, did you determine that one skilled in the art would have had to make -- let me ask it differently.

How, if at all, did you determine that one skilled in the art would have combined the modules of Dell 074 with those of Dell 827 to come up with the 836 patent?

MS. ALTERSOHN: Objection to form; vague, incomplete hypothetical.

A. What I'd like to do is go back to -- I believe it's the 074. Do you remember which exhibit that was? I'll look at it very quickly.

The most significant thing that I would see is that in my analysis of the 074, I observed that they aren't in fact translating -- they aren't dealing with ranks. They're dealing with banks. And it's

not just a name difference. They're actually banks that are on the chip.

But the technique that they use to deal with the notion that they have more elements, whether in this case it's banks, than the computer is prepared to send them, could be addressed by simply emulating it through logic, and so I say it's inherent that any engineer that would look at this would say, oh, if I had the same problem with ranks, I could do that. And that's why I feel it anticipates it.

But if one were to say, well, that's not a valid concern, you know, inherency doesn't stand here, if one were to make that judgment, then one certainly would be able to read this patent and understand that whatever was taught here could be applied to distinguish between the different numbers of chips as well.

Q. Just to be clear, though, in your report, you didn't identify particular features of Dell 074 which you contend would have been obvious to combine with particular

EXHIBIT D

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The Authoritative Dictionary of IEEE Standards Terms

Seventh Edition

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ccitation control system with the
circuited.
fference between the upper and
ne response is 0.707 (−3 dB) of
e frequency. Usually both upper
are specified rather than the dif-
n only one number appears, it is
ites: 1. The reference frequency
ıter for the lower bandwidth limit
r the upper bandwidth limit than
ɔer and lower reference frequen-
: same. In cases where exceptions
noted. 2. This definition assumes
ɔe essentially free of departures
acteristic. 3. If the lower band-
frequency, the response at zero
he response at the reference fre-
(IM/HFIM) [40]
persive delay lines) A specified
the amplitude response does not
ount. *Note:* Typically, amplitude
dB bandwidth. (UFFC) [22]
) Of a signal, the difference be-
cies encountered in the signal.
device, the range of frequencies
n respect to some characteristic
(C) 165-1977
he range of frequencies within
pect to some characteristic, falls
/idth is commonly defined at the
three decibels less than the ref-
(PE) 599-1985w
networks) The frequency range
system passes or uses. For ex-
telephone requires a bandwidth
A television channel occupies a
(6 MHz). Cable systems occupy
: electromagnetic spectrum.
(LM/C) 802.7-1989r
es, expressed in hertz, that can
ee also: pass band.
(C) 610.7-1995
ange over which the amplitude
: than a defined amount. *Note:*
ns to specify bandwidth are 1 dB
lispersive delay lines).
(UFFC) 1037-1992w
fiber bandwidth. 812-1984w
ls The protocols used to allocate
involves inhibiting send-packet
ore nodes when another node is
opportunity to transmit its send
(C/MM) 1596-1992
ism A procedure to facilitate ef-
idth, whereby a node occasion-
lueued Arbitrated (QA) slots.
(LM/C) 8802-6-1994
ersive bandwidth.
persive bandwidth.
:tive bandwidth.
ive *See:* frequency selective

fiber optics) The condition pre-
width, rather than the amplitude
s performance. The condition is
orts the shape of the waveform
linear systems, bandwidth-lim-
to distortion-limited operation.
ɔperation; distortion-limited op-
(Std100) 812-1984w
entation feature that multiplies
ıpacity of the spaceborne fiber-
work by allowing independent

ring segments to use the same dedicated data bandwidth.
(C/BA) 1393-1999

bang snuffer (nonlinear, active, and nonreciprocal waveguide components). A switch used in radar receivers to suppress carrier leakage during the transmit period. *See also:* gate.
(MTT) 457-1982w

bank (A) (navigation) Lateral inclination of an aircraft in flight. *See also:* list. **(B)** An aggregation of similar devices (for example, transformers, lamps, etc.) connected together and used in cooperation. *Note:* In automatic switching, a bank is an assemblage of fixed contacts over which one or more wipers or brushes move in order to establish electric connections. *See also:* relay level.
(AES/EEC/PE/GCS) 172-1983, [119]

(2) (A) One or more disk drives lined up in a row. **(B)** Any group of similar devices that are connected together for use as a single device. For example, a row of light-emitting diodes connected to form a display. **(C)** A contiguous section of addressable memory. For example, eight memory devices, each of which is 64 kB by 1; forming a 64 kB × 8 memory bank. (C) 610.10-1994

bank-and-wiper switch (telephone switching systems) A switch in which an electromagnetic ratchet or other mechanisms are used, first, to move the wipers to a desired group of terminals, and second, to move the wipers over the terminals of this group to the desired bank contacts.
(EEC/PE) [119]

banked winding *See:* bank winding.

bank winding (banked winding) A compact multilayer form of coil winding, for the purpose of reducing distributed capacitance, in which single turns are wound successively in each of two or more layers, the entire winding proceeding from one end of the coil to the other, without return.
(IM) [120]

bar (1) (illuminating engineering) (of lights) A group of three or more aeronautical ground lights placed in a line transverse to the axis, or extended axis, of the runway.
(EEC/IE) [126]

(2) The darker element of a bar code.
(PE/TR) C57.12.35-1996

bar code (1) An identification code consisting of a pattern of vertical bars whose width and spacing identifies the item marked. *Note:* The code is meant to be read by an optical input device, such as a bar code scanner. Applications include retail product pricing labels, identification of library documents, and railroad box car identification. *Synonym:* optical bar code. *See also:* universal product code.
(C) 610.2-1987, 610.10-1994w

(2) An array of rectangular marks and spaces in a predetermined pattern. (PE/TR) C57.12.35-1996

bar code reader *See:* bar code scanner.

bar code symbol An array of rectangular bars and spaces which are arranged in a predetermined pattern following specific rules to represent elements of data that are referred to as characters. A bar code symbol typically contains a leading quiet zone, start character, data character(s) including a check character (if any), stop character, and a trailing quiet zone.
(PE/TR) C57.12.35-1996

bar code scanner An optical scanner used to read a bar-code using reflected light. *Synonym:* bar code reader. *See also:* light pen. (C) 610.10-1994w

bare conductor A conductor having no covering or electrical insulation whatsoever. *See also:* covered conductor.
(NESC/NEC) [86]

barehand work A technique of performing live maintenance on energized wires and equipment whereby one or more line workers work directly on an energized part after having been raised and bonded to the same potential as the energized wire or equipment. These line workers are normally supported by an insulating ladder, nonconductive rope, insulating aerial device, helicopter, or the energized wires or equipment being worked on. Most barehand work includes the use of insulating live tools. (T&D/PE) 516-1995

bare lamp (illuminating engineering) A light source with no shielding. *Synonym:* exposed lamp. (EEC/IE) [126]

barette (illuminating engineering) A short bar in which the lights are closely spaced so that from a distance they appear to be a linear light. *Note:* Barettes are usually less than 4.6 m (15 ft) in length. (EEC/IE) [126]

bar generator (television) A generator of pulses that are uniformly spaced in time and are synchronized to produce a stationary bar pattern on a television screen. *See also:* television. 188-1952w

Barker code A binary phase code used for pulse compression, in which a long pulse is divided into n subpulses with the phase of each subpulse being 0 or π radians. Barker coded pulses have the property that after matched filter processing there are $(n-1)/2$ sidelobes, or $n/2$ for n even, on each side of the main response, each at a voltage level $1/n$ relative to the main response. Barker codes exist with $n = 2, 3, 4, 5, 7, 9$, and 13. *See also:* coded pulse. (AES) 686-1997

Barkhausen-Kurz oscillator An oscillator of the retarding-field type in which the frequency of oscillation depends solely upon the electron transit-time within the tube. *See also:* oscillatory circuit. (AP/ANT) 145-1983s

Barkhausen tube *See:* positive-grid oscillator tube.

barometric altimeter (navigation aid terms) Essentially an aneroid barometer, an instrument which determines atmospheric pressure and is graduated in feet above sea level.
(AES/GCS) 172-1983w

barothermograph (navigation aid terms) An instrument which automatically records pressure and temperature.
(AES/GCS) 172-1983w

bar pattern (television) A pattern of repeating lines or bars on a television screen. When such a pattern is produced by pulses that are equally separated in time, the spacing between the bars on the television screen can be used to measure the linearity of the horizontal or vertical scanning systems. *See also:* television. (EEC/PE) [119]

bar printer An element printer in which the members of the character set are carried on a type bar. (C) 610.10-1994w

barrel connector A double-sided male coupling that interconnects two coaxial cables. *Contrast:* end connector.
(C) 610.7-1995

barrel distortion (1) A defect in a display surface that causes parallel lines to bow away from each other, causing a distorted image. *See also:* pin-cushion distortion.
(C) 610.6-1991w

(2) A distortion that results in a progressive decrease in radial magnification in the reproduced image away from the axis of symmetry of the electron optical system. *Note:* For a camera tube, the reproducer is assumed to have no geometric distortion. (ED) 161-1971w

barrel plating Mechanical plating in which the cathodes are kept loosely in a container that rotates. *See also:* electroplating. (EEC/PE) [119]

barrel shifter A circuit which will shift a word a certain number of bits in either direction within a single clock cycle.
(C) 610.10-1994w

barretter (waveguide components) A form of bolometer element having a positive temperature coefficient of resistivity which typically employs a power-absorbing wire or thin metal film. (MTT) 147-1979w

barrier (1) A partition for the insulation or isolation of electric circuits or electric arcs.
(SWG/PE) C37.40-1993, C37.100-1992

(2) (Class 1E equipment and circuits) A device or structure interposed between redundant Class 1E equipment or circuits, or between Class 1E equipment or circuits and a potential source of damage to limit damage to Class 1E systems to an acceptable level. (PE/NP) 384-1992r

for transmission, or the effect of such departure on a transmitted signal. (PE) 599-1985w

(3) Instantaneous phase departure from a nominal phase. (SCC27) 1139-1999

phase difference (general) The difference in phase between two sinusoidal functions having the same periods. (Std100) 270-1966w

(2) (A) (automatic control) Between sinusoidal input and output of the same frequency, phase angle of the output minus phase angle of the input: it is called "phase lead" if the input angle is the smaller, "phase lag" if the larger. **(B) (automatic control)** Of two periodic phenomena (for example, in nonlinear systems) the difference between the phase angles of their two fundamental waveforms. *Note:* Regarded as part of the transfer function which relates output to input at a specified frequency, phase difference is simply the phase angle $\theta(j\omega)$ in $A(j\omega)\exp j\theta(j\omega)$. Measurement of phase difference in the complex case is sometimes made in terms of the angular interval between respective crossings of a mean reference line, but values so measured will generally differ from those made in terms of the fundamental waveforms. *See also:* phase shift. (PE/EDPG) [3]

phase distance relay A distance relay designed to detect phase-to-phase and three-phase faults. (PE/PSR) C37.113-1999

phase distortion (1) (data transmission) Either the lack of direct proportionality of phase shift to frequency over the frequency range required for transmission, or the effect of such departure on a transmitted signal. (PE) 599-1985w

(2) (facsimile) *See also:* delay distortion; phase-frequency distortion. (C) 610.7-1995

phased satellite (communication satellite) A satellite, the center of mass of which is maintained in a desired relation relative to other satellites, to a point on earth or to some other point of reference such as the sub-solar point. *Note:* If it is necessary to identify those satellites that are not phased satellites, the term "unphased satellites" may be used. (COM) [19]

phase-failure protection *See:* open-phase protection; phase-undervoltage protection.

phase-frequency distortion (facsimile) Distortion due to lack of direct proportionality of phase shift to frequency over the frequency range required for transmission. *Notes:* 1. Delay distortion is a special case. 2. This definition includes the case of a linear phase-frequency relation with the zero frequency intercept differing from an integral multiple of p. *See also:* phase delay distortion; phase distortion; facsimile transmission; distortion. (COM) 168-1956w

phase function matrix The matrix that results when the elements of the Mueller matrix are averaged over all scatterer orientations. The phase function matrix relates the average scattered Stokes vector to the incident Stokes vector. (AP/PROP) 211-1997

phase grouping The same phase of a number of circuit breaker' poles is grouped in an adjacent configuration along the line of the same row. (SWG/SUB/PE) C37.122-1983s, C37.100-1992

phase hit or change A sudden change in the received signal phase (or frequency) lasting longer than 4 ms. Since two common modulation techniques for high-speed data transmission are phase and frequency modulation, phase hits cause errors by looking like data. *See also:* gain hit or change; dropouts. (PE/IC) 1143-1994r

phase instability ($S_\phi(f)$) One-sided spectral density of the phase deviation. (SCC27) 1139-1999

phase-insulated terminal box (rotating machinery) A terminal box so designed that the protection of phase conductors against electric failure within the terminal box is by insulation only. (PE) [9]

phase jitter An instability in the phase of a transmission signal. *See also:* amplitude jitter. (C) 610.7-1995

phase lag (phase delay) (2-port network) The phase angle of the input wave relative to the output wave ($\phi_{in} - \phi_{out}$), or the initial phase angle of the output wave relative to the final phase angle of the output wave ($\phi_i - \phi_f$). *Note:* Under matched conditions, phase lag is the negative of the angle of the transmission coefficient of the scattering matrix for a 2-port network. *See also:* phase difference. (IM) 285-1968w, [38]

phase localizer (navigation aid terms) A localizer in which the on-course line is defined by the phase reversal of energy radiated by the sideband antenna system, a reference carrier signal being radiated and used for the detection of phase. (AES/GCS) 172-1983w

phase lock The state of synchronization between two ac signals in which they remain at the same frequency and with constant phase difference. This term is typically applied to a circuit that synchronizes a variable oscillator with an independent signal. (PE/PSR) 1344-1995

phase-locked Pertaining to two signals whose phases relative to each other are kept constant by a controlling device. (C) 610.10-1994w

phase lock loop (communication satellite) A circuit for synchronizing a variable local oscillator with the phase of a transmitted signal. Widely used in space communication for coherent carrier tracking, and threshold extension, bit synchronization and symbol synchronization. (COM) [24]

phase locus (for a loop transfer function, say G(s) H(s) A plot in the *s* plane of those points for which the phase angle, ang *GH*, has some specified constant value. *Note:* The phase loci for 180 degrees plus or minus *n* 360 degrees are also root loci. *See also:* feedback control system. (PE/EDPG) [3]

phase margin (1) (loop transfer function for a stable feedback control system) (excitation systems) 180 degrees minus the absolute value of the loop phase angle at a frequency where the loop gain is unity. *Note:* Phase margin is a convenient way of expressing relative stability of a linear system under parameter changes, in Nyquist, Bode, or Nichols diagrams. In a conditionally stable feedback control system where the loop gain becomes unity at several frequencies, the term is understood to apply to the value of phase margin at the highest of these frequencies. *See also:* feedback control system. (PE/EDPG) 421A-1978s

(2) (speed governing of hydraulic turbines) 180 degrees minus the absolute value of the open-loop phase angle at a frequency where the open-loop gain is unity. (PE/EDPG) 125-1977s

(3) The absolute value of loop phase angle subtracted from 180 degrees found in a feedback system at the frequency for which its gain reaches unity. The margin from 180 degrees represents a measure of dynamic stability. (PEL) 1515-2000

phase meter (phase-angle meter) An instrument for measuring the difference in phase between two alternating quantities of the same frequency. *See also:* instrument. (EEC/PE) [119]

phase modifier (rotating machinery) An electric machine, the chief purpose of which is to supply leading or lagging reactive power to the system to which it is connected. Phase modifiers may be either synchronous or asynchronous. *See also:* converter. (IA/PE/MT) 45-1983s, [9]

phase-modulated transmitter A transmitter that transmits a phase-modulated wave. (AP/BT/ANT) 145-1983s, 182-1961w

phase modulation (1) (data transmission) Angle modulation in which the angle of a carrier is caused to depart from its reference value by an amount proportional to the instantaneous value of the modulating function. *Notes:* 1. A wave phase modulated by a given function can be regarded as a wave frequency modulated by the time derivative of that function. 2. Combinations of phase and frequency modulation are commonly referred to as frequency modulation. *See also:* reactance modulator; angle or phase; pulse duration; phase deviation. (IT/AP/PE/ANT) 145-1983s, 599-1985w, [123]

(2) (overhead-power-line corona and radio noise) Modulation in which the angle of a carrier is caused to depart from

region, Geiger-Mueller *See:* Geiger-Mueller region.

region growing (image processing and pattern recognition) An image segmentation technique in which regions are formed by repeatedly taking the union of subregions that are similar in gray levels or textures. *See also:* region partitioning. (C) 610.4-1990w

region of limited proportionality (radiation counter tubes) The range of applied voltage below the Geiger-Mueller threshold, in which the gas amplification depends upon the charge liberated by the initial ionizing event. (ED) 161-1971w

region partitioning (image processing and pattern recognition) An image segmentation technique in which regions are formed by repeatedly taking the union of sub-regions that are similar in gray levels or textures and by repeatedly splitting apart subregions that are dissimilar. *See also:* region growing. (C) 610.4-1990w

region, proportional *See:* proportional region.

regions of electromagnetic spectrum (1) (illuminating engineering) For convenience of reference, the electromagnetic spectrum is arbitrarily divided as follows:

Vacuum ultraviolet
Extreme ultraviolet 10–100 nm
Far ultraviolet 100–200 nm
Middle ultraviolet 200–300 nm
Near ultraviolet 300–380 nm
Visible 380–770 nm
Near (short wavelength) 770–1400 nm infrared
Intermediate infrared 1400–5000 nm
Far (long wavelength) 5000–1 000 000 nm infrared

Note: The spectral limits indicated above have been chosen as a matter of practical convenience. There is a gradual transition from region to region without sharp delineation. Also, the division of the spectrum is not unique. In various fields of science, the classifications may differ due to the phenomena of interest. Another division of the ultraviolet spectrum often used by photobiologists is given by the International Commission on Illumination (CIE):

- UV-A 315 to 400 nm
- UV-B 280 to 315 nm
- UV-C 100 to 280 nm

(EEC/IE) [126]

(2) (light-emitting diodes) For convenience of reference the electromagnetic spectrum near the visible spectrum is divided as follows.

Spectrum	Wavelength in Nanometers
far ultraviolet	10–280
middle ultraviolet	280–315
near ultraviolet	315–380
visible	380–780
infrared	790–10^5

Note: The spectral limits indicated above should not be construed to represent sharp delineations between the various regions. There is a gradual transition from region to region. The above ranges have been established for practical purposes. *See also:* radiant energy. (EEC/IE) [126]

register (1) (electronic computation) A device capable of retaining information, often that contained in a small subset (for example, one word), of the aggregate information in a digital computer. *See also:* address register; index register; circulating register; shift register. (C) 162-1963w

(2) (telephone switching systems) A part of an automatic switching system that receives and stores signals from a calling device or other source for interpretation and action. (COM) 312-1977w

(3) A term used to describe quadlet addresses that can be read or written by software. In the context of this document, a register does not imply a specific hardware implementation. If a bus standard allows transactions to be split, and sufficient time is allowed between the request and response subactions, the functionality of the register can be emulated by a processor on the module. (C/MM) 1212-1991

(4) A storage device or storage location having a specified storage capacity. *See also:* strobe. (C) 610.10-1994w

(5) A set of records (paper, electronic, or a combination) maintained by a Registration Authority containing assigned names and the associated information. (C/LM) 802.10g-1995

register architecture A computer architecture whose design is based on the maintenance of data items in registers. *Contrast:* stack architecture. (C) 610.10-1994w

register-arithmetic and logic unit An arithmetic and logic unit which also contains a register array. (C) 610.10-1994w

register array *See:* register file.

register-based device A servant-only device that supports VXIbus configuration registers. Register-based devices are typically controlled by message-based devices via device-dependent register reads and writes. (C/MM) 1155-1992

register constant (meter) The factor by which the register reading must be multiplied in order to provide proper consideration of the register, or gear, ratio and of the instrument transformer ratios to obtain the registration in the desired unit. *Note:* It is commonly denoted by the symbol *Kr*. *See also:* electricity meter; moving element. (ELM) C12.1-1982s

registered images Two or more images of the same scene that have been positioned with respect to one another so that corresponding points in the images represent the same point in the scene. (C) 610.4-1990w

register file A set of registers which may be addressed by their number in the set. *Synonym:* register array. (C) 610.10-1994w

register length (1) (electronic computation) The number of characters that a register can store. (Std100) 270-1966w

(2) The storage capacity of a register. (C) 610.10-1994w

register marks Any mark or line printed or otherwise impressed on a web of material and which is used as a reference to maintain register. *See also:* photoelectric control. (IA/ICTL/IAC) [60]

register, mechanical *See:* mechanical register.

register memory (A) Use of high-speed general purpose registers as one would use memory, as in using registers to hold frequently-used data items. **(B)** Registers specifically included in the machine design for use as high-speed storage. (C) 610.10-1994

register ratio (watthour meter) The number of revolutions of the first gear of the register, for one revolution of the first dial pointer. *Note:* This is commonly denoted by the symbol R_r. (ELM) C12.1-1982s

register reading The numerical value indicated by the register. Neither the register constant nor the test dial (or dials), if any exist, is considered. *See also:* electricity meter. (EEC/PE) [119]

register set A subset of the full array of registers in a machine which the processing unit is currently allowed to use. *Note:* Machines may have N registers of which the processor may be able to address only M at a time; this divides the register array into N/M register sets. (C) 610.10-1994w

register transfer language (RTL) A computer language used to represent the flow of information on a system level; for example, to show data at the level of computer devices such as registers, gates, and ALUs. (C) 610.10-1994w

register-transfer level (RTL) (1) A description of computer operations where data transfers from register to register, latch to latch and through logic gates are described. *Note:* This may be an abstract description or microcoding. (C) 610.10-1994w

(2) A level of description of a digital design in which the clocked behavior of the design is expressly described in terms of data transfers between storage elements, which may be implied, and combinational logic, which may represent any computing or arithmetic-logic-unit logic. RTL modeling al-

EXHIBIT E

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o·pe·ra cloak ▸*n.* a cloak of rich material worn over evening clothes, esp. by women.

o·pé·ra co·mique /ˈäp(ə)rə kəˈmēk; ˌôpärä kôˈmēk/ ▸*n.* an opera on a lighthearted theme, typically in French and with spoken dialogue. ■ such works as a genre.

op·er·a glass·es (or **op·er·a glass**) ▸*plural n.* small binoculars for use at the opera or theater.

op·er·a·go·er /ˈäp(ə)rəˌgōər/ ▸*n.* one who attends opera performances.

op·er·a hat ▸*n.* a collapsible top hat.

op·er·a house ▸*n.* a theater designed for the performance of opera.

op·er·and /ˈäpəˌrand/ ▸*n. Mathematics* the quantity on which an operation is to be done. ▷late 19th cent.: from Latin *operandum*, neuter gerundive of *operari* 'expend labor on' (see **OPERATE**).

op·er·ant /ˈäpərənt/ *Psychology* ▸*adj.* involving the modification of behavior by the reinforcing or inhibiting effect of its own consequences (instrumental conditioning).

▸*n.* an item of behavior that is initially spontaneous, rather than a response to a prior stimulus, but whose consequences may reinforce or inhibit recurrence of that behavior. ▷late Middle English: from Latin *operant-* 'being at work,' from the verb *operari*.

op·er·a queen ▸*n. informal* a male homosexual who is fanatical about opera, esp. one characterized as being affectedly haughty and overrefined.

o·pe·ra se·ri·a /ˈäp(ə)rə ˈsi(ə)rēə; ˈōpeˌrä ˈserēˌä/ ▸*n.* an opera, typically one of the 18th century in Italian, on a serious, usually classical or mythological theme. ■ such works as a genre. ▷Italian, literally 'serious opera.'

op·er·ate /ˈäpəˌrāt/ ▸*v.* **1** [*trans.*] (of a person) control the functioning of (a machine, process, or system): *a shortage of workers to operate new machines.* ■ [*intrans.*] (of a machine, process, or system) function in a specified manner: *market forces were allowed to operate freely.* ■ [*intrans.*] be in effect: *there is a powerful law that operates in politics.* ■ (of a person or organization) manage and run (a business): *many foreign companies operate factories in the U.S.* ■ [*intrans.*] (of an organization) be managed and run in a specified way: *neither company had operated within the terms of its charter.* ■ [*intrans.*] (of an armed force) conduct military activities in a specified area or from a specified base: *the mountain bases from which the guerrillas were operating.* **2** [*intrans.*] perform a surgical operation: *the surgeons refused to operate | my brother had to be* ***operated on*** *last week.* **3** [*intrans.*] function; work: *we have as yet no conclusive evidence on how these cells operate.* ▷early 17th cent.: from Latin *operat-* 'done by labor,' from the verb *operari*, from *opus*, *oper-* 'work.'

op·er·at·ic /ˌäpəˈratik/ ▸*adj.* of, relating to, or characteristic of opera: *operatic arias.* ■ extravagantly theatrical; overly dramatic: *she wrung her hands in operatic despair.* ▷mid 18th cent.: formed irregularly from **OPERA**[1], on the pattern of words such as *dramatic*. **—op·er·at·i·cal·ly** /-ik(ə)lē/ *adv.*

op·er·at·ics /ˌäpəˈratiks/ ▸*plural n.* [often treated as *sing.*] the production or performance of operas. ■ theatrically exaggerated or overemotional behavior.

op·er·at·ing prof·it ▸*n.* profit from business operations (gross profit less operating expenses) before deduction of fixed costs.

op·er·at·ing room (abbr.: **OR**) (*Brit.* **operating theatre**) ▸*n.* a room in a hospital specially equipped for surgical operations.

op·er·at·ing sys·tem ▸*n.* the software that supports a computer's basic functions, such as scheduling tasks, executing applications, and controlling peripherals.

op·er·a·tion /ˌäpəˈrāSHən/ ▸*n.* **1** the fact or condition of functioning or being active: *the construction and operation of power stations | some of these ideas could be put into operation.* ■ an active process; a discharge of a function: *the operations of the mind.* ■ a business organization; a company: *he reopened his operation under a different name.* ■ an activity in which such an organization is involved: *the company is selling most of its commercial banking operations.* **2** an act of surgery performed on a patient. **3** [often with *adj.*] a piece of organized and concerted activity involving a number of people, esp. members of the armed forces or the police: *a rescue operation | military operations.* ■ (**Operation**) preceding a code name for such an activity: *Operation Desert Storm.* **4** *Mathematics* a process in which a number, quantity, expression, etc., is altered or manipulated according to formal rules, such as those of addition, multiplication, and differentiation. ▷late Middle English: via Old French from Latin *operatio(n-)*, from the verb *operari* 'expend labor on' (see **OPERATE**).

op·er·a·tion·al /ˌäpəˈrāSHənl/ ▸*adj.* in or ready for use: *the new laboratory is fully operational.* ■ of or relating to the routine functioning and activities of a business or organization: *the coffee bar's initial operational costs.* ■ engaged in or relating to active operations of the armed forces, police, or emergency services: *an operational fighter squadron.* **—op·er·a·tion·al·ly** *adv.*

op·er·a·tion·al am·pli·fi·er (abbr.: **op-amp**) ▸*n. Electronics* an amplifier with high gain and high input impedance (usually with external feedback), used esp. in circuits for performing mathematical operations on an input voltage.

op·er·a·tion·al·ism /äpəˈrāSHənlˌizəm/ ▸*n.* (also **op·er·a·tion·ism**) *Philosophy* a form of positivism that defines scientific concepts in terms of the operations used to determine or prove them. **—op·er·a·tion·al·ist** *n.* & *adj.*

op·er·a·tion·al·ize /ˌäpəˈrāSHənlˌīz/ ▸*v.* [*trans.*] **1** put into operation or use. **2** *Philosophy* express or define (something) in terms of the operations used to determine or prove it.

op·er·a·tions re·search ▸*n.* the application of scientific principles to business management, providing a quantitative basis for complex decisions.

op·er·a·tive /ˈäp(ə)ritiv; ˈäpəˌrātiv/ ▸*adj.* **1** functioning; having effect: *the transmitter is operative | the mining ban would remain operative.* ■ [*attrib.*] (of a word) having the most relevance or significance in a phrase or sentence: *a young man, and the operative word is young, should go into the armed services at around seventeen.* **2** [*attrib.*] of or relating to surgery: *they had wounds needing operative treatment.*

▸*n.* a worker, esp. a skilled one in a manufacturing industry. ■ a private detective or secret agent. ▷late Middle English: from late Latin *operativus*, from Latin *operat-* 'done by labor,' from the verb *operari* (see **OPERATE**). **—op·er·a·tive·ly** *adv.* **—op·er·a·tive·ness** *n.*

op·er·a·tor /ˈäpəˌrātər/ ▸*n.* **1** [often with *adj.*] a person who operates equipment or a machine: *a radio operator.* ■ (usu. **the operator**) a person who works for a telephone company assisting users, or who works at a telephone switchboard. **2** [usu. with *adj.*] a person or company that engages in or runs a business or enterprise: *a tour operator.* **3** [with *adj.*] *informal* a person who acts in a specified, esp. a manipulative, way: *her reputation as a cool, clever operator.* **4** *Mathematics* a symbol or function denoting an operation (e.g., ×, +).

op·er·a win·dow ▸*n.* a small fixed window usually behind the rear side window of an automobile.

o·per·cu·lum /ōˈpərkyələm/ ▸*n.* (*pl.* **-la** /-lə/) *Zoology* & *Botany* a structure that closes or covers an aperture, in particular: ■ technical term for **GILL COVER.** ■ a secreted plate that serves to close the aperture of a gastropod mollusk's shell when the animal is retracted. ■ a lidlike structure of the spore-containing capsule of a moss. ▷early 18th cent.: from Latin, literally 'lid, covering,' from *operire* 'to cover.' **—o·per·cu·lar** /-lər/ *adj.* **—o·per·cu·late** /-lāt/ *adj.* **—o·per·cu·li-** *comb. form.*

op·er·et·ta /ˌäpəˈretə/ ▸*n.* a short opera, usually on a light or humorous theme and typically having spoken dialogue. Notable composers of operettas include Offenbach, Johann Strauss, Lehár, and Gilbert and Sullivan. ▷late 18th cent.: from Italian, diminutive of *opera* (see **OPERA**[1]).

op·er·on /ˈäpəˌrän/ ▸*n. Biology* a unit made up of linked genes that is thought to regulate other genes responsible for protein synthesis. ▷1960s: from French *opérer* 'to effect, work' + **-ON.**

op·er·ose /ˈäpəˌrōs/ ▸*adj. rare* involving or displaying much industry or effort. ▷late 17th cent.: from Latin *operosus*, from *opus* 'work.'

oph·i·cleide /ˈäfiˌklīd/ ▸*n.* an obsolete bass brass instrument with keys, used in bands in the 19th century but superseded by the tuba. ▷mid 19th cent.: from French *ophicléide*, from Greek *ophis* 'serpent' + *kleis*, *kleid-* 'key.'

O·phid·i·a /ōˈfidēə/ *Zoology* a group of reptiles that comprises the snakes. Also called **SERPENTES.** • Suborder Ophidia, order Squamata. ▷modern Latin (plural), from Greek *ophis*, *ophid-* 'snake.' **—o·phid·i·an** *n.* & *adj.*

oph·i·o·lite /ˈäfēəˌlīt; ˈōfē-/ ▸*n. Geology* an igneous rock consisting largely of serpentine, believed to have been formed from the submarine eruption of oceanic crustal and upper mantle material. ▷mid 19th cent.: from Greek *ophis* 'snake' + **-LITE.** **—oph·i·o·lit·ic** /ˌäfēəˈlitik; ˌōfē-/ *adj.*

oph·i·ol·o·gy /ˌäfēˈäləjē; ˌōfē-/ ▸*n.* the branch of zoology that deals with snakes. ▷early 19th cent.: from Greek *ophis* 'snake' + **-LOGY.** **—oph·i·ol·o·gist** /-jist/ *n.*

O·phir /ˈōfər/ (in the Bible) an unidentified region, perhaps in southeastern Arabia, famous for its fine gold and precious stones.

oph·ite /ˈäfit; ˈōfit/ ▸*n. Geology* a green rock with spots or markings like a snake that can be either eruptive or metamorphic; serpentine. ▷mid 17th cent.: via Latin from Greek *ophitēs* 'serpentine stone,' from *ophis* 'snake,' + **-ITE**[1].

o·phit·ic /ōˈfitik/ ▸*adj. Geology* relating to or denoting a poikilitic rock texture in which crystals of feldspar are interposed between plates of augite. ▷late 19th cent.: via Latin from Greek *ophitēs* 'serpentine stone' (from *ophis* 'snake') + **-IC.**

Oph·i·u·chus /ˌäfēˈyōōkəs; ˌōfē-/ *Astronomy* a large constellation (the Serpent Bearer or Holder), said to represent a man in the coils of a snake. Both the celestial equator and the ecliptic pass through it, but it is not counted among the signs of the zodiac. ■ [*as genitive*] (**Ophiuchi**) used with a preceding letter or numeral to designate a star in this constellation: *the star Eta Ophiuchi.* ▷via Latin from Greek *Ophioukos*.

Oph·i·u·roi·de·a /ˌäfēyōōroidēə; ˌōfē-/ *Zoology* a class of echinoderms that comprises the brittle stars. ▷modern Latin (plural), based on the genus name *Ophiura*, from Greek *ophis* 'snake' + *oura* 'tail.' **—oph·i·ur·oid** /-ˈyōōroid/ *n.* & *adj.*

oph·thal·mi·a /äfˈTHalmēə; äp-/ ▸*n. Medicine* inflammation of the eye, esp. conjunctivitis. ▷late Middle English: via late Latin from Greek, from *ophthalmos* 'eye.'

oph·thal·mic /äfˈTHalmik; äp-/ ▸*adj.* [*attrib.*] of or relating to the eye and its diseases. ▷early 17th cent.: via Latin from Greek *ophthalmikos*, from *ophthalmos* 'eye.'

oph·thal·mi·tis /ˌäfTHəlˈmīdis; ˌäp-/ ▸*n. Medicine* inflammation of the eye.

ophthalmo- ▸*comb. form Medicine* relating to the eyes: *ophthalmoscope.* ▷from Greek *ophthalmos* 'eye.'

oph·thal·mol·o·gy /ˌäfTHə(l)ˈmäləjē; ˌäp-/ ▸*n.* the branch of medicine concerned with the study and treatment of disorders and diseases of the eye. **—oph·thal·mo·log·i·cal** /-məˈläjikəl/ *adj.* **—oph·thal·mol·o·gist** /-jist/ *n.*

oph·thal·mo·ple·gia /äfˌTHalmə ˈplējē(ə)ə/ ▸*n. Medicine* paralysis of the muscles within or surrounding the eye. **—oph·thal·mo·ple·gic** /-ˈplējik/ *adj.*

oph·thal·mo·scope /äfˈTHalməˌskōp; äp-/ ▸*n.* an instrument for inspecting the retina and other parts of the eye. **—oph·thal·mo·scop·ic** /ˌäfTHəlməˈskäpik; ˌäp-/ *adj.* **—oph·thal·mos·co·py** /ˌäfTHəlˈmäskəpē; ˌäp-/ *n.*

-opia ▸*comb. form* denoting a visual disorder: *myopia.* ▷from Greek *ōps*, *ōp-* 'eye, face.'

o·pi·ate ▸*adj.* /ˈōpē-it; -ˌāt/ relating to, resembling, or containing opium: *the use of opiate drugs.* ■ *figurative, dated* causing drowsiness or a dulling of the senses.

▸*n.* /ˈōpē-it; -ˌāt/ a drug with morphinelike effects, derived from opium. ■ *figurative* a thing that soothes or stupefies.

▸*v.* /-ˌāt/ [*trans.*] [often as *adj.*] (**opiated**) impregnate with opium. ▷late Middle English (as a noun): from medieval Latin *opiatus* (adjective), *opiatus* (noun), based on Latin *opium* (see **OPIUM**).

▸*PHRASE* □ **the opiate of the masses** (or **people**) something regarded as inducing a false and unrealistic sense of contentment among people. [translating the German phrase *Opium des Volks*, used by Karl Marx in reference to religion (1844).]

o·pine /ōˈpīn/ ▸*v.* [*reporting verb*] *formal* hold and state as one's opinion: [with *direct speech*] *"The man is a genius," he opined* | [with *clause*] *the critic opined that the most exciting musical moment occurred when the orchestra struck up the national anthem.* ▷late Middle English: from Latin *opinari* 'think, believe.'

o·pin·ion /əˈpinyən/ ▸*n.* a view or judgment formed about something, not necessarily based on fact or knowledge: *I'm writing to voice my opinion on an issue of great importance | that,* ***in my opinion****, is dead right.* ■ the beliefs or views of a large number or majority of people about a particular thing: *the changing climate of opinion.* ■ (**opinion of**) an estimation of the quality or worth of someone or something: *I had a higher opinion of myself than I deserved.* ■ a formal

EXHIBIT F

Manual of PATENT EXAMINING PROCEDURE

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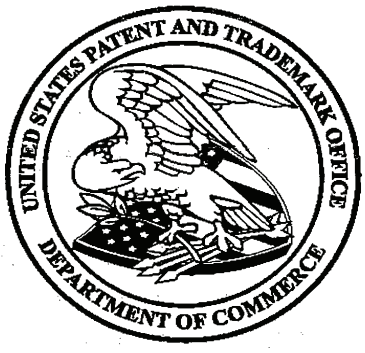

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preamble does not render the claim indefinite under 35 U.S.C. 112, second paragraph. See *In re Larsen*, No. 01-1092 (Fed. Cir. May 9, 2001) (unpublished) (The preamble of the *Larsen* claim recited only a hanger and a loop but the body of the claim positively recited a linear member. The examiner rejected the claim under 35 U.S.C. 112, second paragraph, because the omission from the claim's preamble of a critical element (i.e., a linear member) renders that claim indefinite. The court reversed the examiner's rejection and stated that the totality of all the limitations of the claim and their interaction with each other must be considered to ascertain the inventor's contribution to the art. Upon review of the claim in its entirety, the court concluded that the claim at issue apprises one of ordinary skill in the art of its scope and, therefore, serves the notice function required by 35 U.S.C. 112, paragraph 2.).

2173.05(f) Reference to Limitations in Another Claim

A claim which makes reference to a preceding claim to define a limitation is an acceptable claim construction which should not necessarily be rejected as improper or confusing under 35 U.S.C. 112, second paragraph. For example, claims which read: "The product produced by the method of claim 1." or "A method of producing ethanol comprising contacting amylose with the culture of claim 1 under the following conditions ....." are not indefinite under 35 U.S.C. 112, second paragraph, merely because of the reference to another claim. See also *Ex parte Porter*, 25 USPQ2d 1144 (Bd. Pat. App. & Inter. 1992) where reference to "the nozzle of claim 7" in a method claim was held to comply with 35 U.S.C. 112, second paragraph. However, where the format of making reference to limitations recited in another claim results in confusion, then a rejection would be proper under 35 U.S.C. 112, second paragraph.

2173.05(g) Functional Limitations [R-3]

A functional limitation is an attempt to define something by what it does, rather than by what it is (e.g., as evidenced by its specific structure or specific ingredients). There is nothing inherently wrong with defining some part of an invention in functional terms. Functional language does not, in and of itself, render a claim improper. *In re Swinehart*, 439 F.2d 210, 169 USPQ 226 (CCPA 1971).

A functional limitation must be evaluated and considered, just like any other limitation of the claim, for what it fairly conveys to a person of ordinary skill in the pertinent art in the context in which it is used. A functional limitation is often used in association with an element, ingredient, or step of a process to define a particular capability or purpose that is served by the recited element, ingredient or step. >In *Innova/Pure Water Inc. v. Safari Water Filtration Sys. Inc.*, 381 F.3d 1111, 1117-20, 72 USPQ2d 1001, 1006-08 (Fed. Cir. 2004), the court noted that the claim term "operatively connected" is "a general descriptive claim term frequently used in patent drafting to reflect a functional relationship between claimed components," that is, the term "means the claimed components must be connected in a way to perform a designated function." "In the absence of modifiers, general descriptive terms are typically construed as having their full meaning." *Id.* at 1118, 72 USPQ2d at 1006. In the patent claim at issue, "subject to any clear and unmistakable disavowal of claim scope, the term 'operatively connected' takes the full breath of its ordinary meaning, i.e., 'said tube [is] operatively connected to said cap' when the tube and cap are arranged in a manner capable of performing the function of filtering." *Id.* at 1120, 72 USPQ2d at 1008.<

Whether or not the functional limitation complies with 35 U.S.C. 112, second paragraph, is a different issue from whether the limitation is properly supported under 35 U.S.C. 112, first paragraph, or is distinguished over the prior art. A few examples are set forth below to illustrate situations where the issue of whether a functional limitation complies with 35 U.S.C. 112, second paragraph, was considered.

It was held that the limitation used to define a radical on a chemical compound as "incapable of forming a dye with said oxidizing developing agent" although functional, was perfectly acceptable because it set definite boundaries on the patent protection sought. *In re Barr*, 444 F.2d 588, 170 USPQ 33 (CCPA 1971).

In a claim that was directed to a kit of component parts capable of being assembled, the Court held that limitations such as "members adapted to be positioned" and "portions . . . being resiliently dilatable whereby said housing may be slidably positioned" serve to precisely define present structural attributes

of interrelated component parts of the claimed assembly. *In re Venezia*, 530 F.2d 956, 189 USPQ 149 (CCPA 1976).

2173.05(h) Alternative Limitations

I. MARKUSH GROUPS

Alternative expressions are permitted if they present no uncertainty or ambiguity with respect to the question of scope or clarity of the claims. One acceptable form of alternative expression, which is commonly referred to as a Markush group, recites members as being "selected from the group consisting of A, B and C." See *Ex parte Markush*, 1925 C.D. 126 (Comm'r Pat. 1925).

Ex parte Markush sanctions claiming a genus expressed as a group consisting of certain specified materials. Inventions in metallurgy, refractories, ceramics, pharmacy, pharmacology and biology are most frequently claimed under the Markush formula but purely mechanical features or process steps may also be claimed by using the Markush style of claiming. See *Ex parte Head*, 214 USPQ 551 (Bd. App. 1981); *In re Gaubert*, 524 F.2d 1222, 187 USPQ 664 (CCPA 1975); and *In re Harnisch*, 631 F.2d 716, 206 USPQ 300 (CCPA 1980). It is improper to use the term "comprising" instead of "consisting of." *Ex parte Dotter*, 12 USPQ 382 (Bd. App. 1931).

The use of Markush claims of diminishing scope should not, in itself, be considered a sufficient basis for objection to or rejection of claims. However, if such a practice renders the claims indefinite or if it results in undue multiplicity, an appropriate rejection should be made.

Similarly, the double inclusion of an element by members of a Markush group is not, in itself, sufficient basis for objection to or rejection of claims. Rather, the facts in each case must be evaluated to determine whether or not the multiple inclusion of one or more elements in a claim renders that claim indefinite. The mere fact that a compound may be embraced by more than one member of a Markush group recited in the claim does not necessarily render the scope of the claim unclear. For example, the Markush group, "selected from the group consisting of amino, halogen, nitro, chloro and alkyl" should be acceptable even though "halogen" is generic to "chloro."

The materials set forth in the Markush group ordinarily must belong to a recognized physical or chemical class or to an art-recognized class. However, when the Markush group occurs in a claim reciting a process or a combination (not a single compound), it is sufficient if the members of the group are disclosed in the specification to possess at least one property in common which is mainly responsible for their function in the claimed relationship, and it is clear from their very nature or from the prior art that all of them possess this property. While in the past the test for Markush-type claims was applied as liberally as possible, present practice which holds that claims reciting Markush groups are not generic claims (MPEP § 803) may subject the groups to a more stringent test for propriety of the recited members. Where a Markush expression is applied only to a portion of a chemical compound, the propriety of the grouping is determined by a consideration of the compound as a whole, and does not depend on there being a community of properties in the members of the Markush expression.

When materials recited in a claim are so related as to constitute a proper Markush group, they may be recited in the conventional manner, or alternatively. For example, if "wherein R is a material selected from the group consisting of A, B, C and D" is a proper limitation, then "wherein R is A, B, C or D" shall also be considered proper.

Subgenus Claim

Genus, subgenus, and Markush-type claims, if properly supported by the disclosure, are all acceptable ways for applicants to claim their inventions. They provide different ways to present claims of different scope. Examiners should therefore not reject Markush-type claims merely because there are genus claims that encompass the Markush-type claims.

See also MPEP § 608.01(p) and § 715.03.

See MPEP § 803.02 for restriction practice re Markush-type claims.

II. "OR" TERMINOLOGY

Alternative expressions using "or" are acceptable, such as "wherein R is A, B, C, or D." The following phrases were each held to be acceptable and not in violation of 35 U.S.C. 112, second paragraph in *In re Gaubert*, 524 F.2d 1222, 187 USPQ 664 (CCPA 1975): "made entirely or in part of"; "at least one

EXHIBIT G

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UNITED STATES DISTRICT COURT FOR THE

NORTHERN DISTRICT OF CALIFORNIA

OAKLAND DIVISION

NETLIST, INC., Plaintiff, v. GOOGLE INC., Defendant.	Case No. CV09-05718 SBA [Related to Case No: CV08-04144 SBA] **DEFENDANT GOOGLE INC.'S INVALIDITY CONTENTIONS PURSUANT TO PATENT L.R. 3-3 AND 3-4**

Pursuant to Patent L.R. 3-3, Google Inc. ("Google") hereby serves its Invalidity Contentions on Plaintiff Netlist, Inc. ("Netlist"). In the absence of a claim construction order from the Court, Google has based its Invalidity Contentions in part upon the disclosure of the specification of U.S. Patent No. 7,619, 912 B2 ("the '912 Patent") and, to the extent any apparent construction of the asserted claims of the '912 Patent were advanced by Netlist in its Infringement Contentions served on April 8, 2010, on any such asserted construction. Nothing herein should be construed as an admission that Google agrees with Netlist's apparent claim constructions. Google expressly reserves the right to propose alternative constructions to those advocated by Netlist and to request Netlist's actual claim construction position during the claim construction portion of this case. Google expressly reserves the right to challenge the sufficiency of Netlist's Infringement Contentions and any claims or claim terms that Netlist purports to have explicitly or implicitly construed therein.

Prior art not included in this disclosure, whether or not now known to Google, may become relevant depending on the claim constructions that Netlist asserts and the constructions that this Court may adopt. Google's own ongoing investigations may also uncover additional prior art. The obviousness combinations of references under 35 U.S.C. § 103 that are provided below and in the accompanying exhibits are merely exemplary and are not intended to be exhaustive. Additional obviousness combinations of the references identified below are possible, and Google reserves the right to use any such combinations in this litigation. In particular, Google is currently unaware of the extent, if any, to which Netlist will contend that the art identified by Google does not disclose limitations of the asserted claims. Should such an issue arise, Google reserves the right to identify other references that would have made the addition of the allegedly missing limitation to the disclosed device obvious.

Accordingly, Google reserves the right to supplement or modify these Invalidity Contentions based on claim construction and further discovery and in a manner consistent with the Federal Rules of Civil Procedure and this Court's rules, including the Patent Local Rules. In addition to these Invalidity Contentions and prior art identified herein, Google expressly

incorporates by reference in their entirety and reserves the right to rely upon any and all invalidity contentions and prior art served in any other action involving the '912 Patent.

I. IDENTIFICATION OF PRIOR ART

Pursuant to Patent L.R. 3-3(a), and in light of Netlist's allegations set forth in its Infringement Contentions and accompanying claim charts served on April 8, 2010, Google lists below the prior art now known to Google which it contends anticipates or renders obvious Claims 1, 3, 4, 6-11, 15, 18-22, 24-25, 27-29, 31-34, 36-39, 41-45, and 50 (collectively, "the Asserted Claims") of the '912 Patent.

Pursuant to Patent L.R. 3-3(a), Google identifies the following United States patents and publications as prior art that anticipate or render obvious the Asserted Claims of the '912 Patent. Google reserves the right to modify and/or supplement this list of prior art.

Patents and Published Applications

Number	Country of Origin	Date of Issue/Publication
U.S. Pat. Appl. No. 2006/0117152 A1 (GNET 000552-000568)	United States	June 1, 2006
U.S. Pat. No. 6,209,074 (GNET 001088-001097)	United States	March 27, 2001
U.S. Pat. No. 5,926,827 (GNET 000894-000901)	United States	July 20, 1999
U.S. Pat. No. 5,745,914 (GNET 000845-000858)	United States	April 28, 1999
U.S. Pat No. 4,368,515 (GNET 000616-000625)	United States	January 11, 1983
U.S. Pat. No. 6,414,868 (GNET 001109-001120)	United States	July 2, 2002
U.S. Pat. No. 5,581,498 (GNET 000772-000790)	United States	December 3, 1996
U.S. Pat. No. 6,961,281 (GNET 001298-001309)	United States	November 1, 2005
U.S. Pub. No. 2006/0044860 A1 (GNET 002302-002313)	United States	March 2, 2006

Number	Country of Origin	Date of Issue/Publication
U.S. Pat. No. 7,356,639 (GNET 001519-001571)	United States	April 8, 2008
U.S. Pat. No. 7,120,727 (GNET 001405-001418)	United States	October 10, 2006
U.S. Pat. No. 4,392,212 (GNET 000626-000635)	United States	July 5, 1983

Google further identifies those products and systems that practice the subject matter of the cited prior art and prior art that may be found in the future. Discovery relating to prior art products, systems, and inventions is ongoing, and Google reserves the ability to supplement these contentions with any additional prior art products, systems, and inventions it becomes aware of through this discovery.

II. STATUTORY BASIS FOR INVALIDITY

A. Anticipation (35 U.S.C. § 102) and Obviousness (35 U.S.C. § 103)

Pursuant to Patent L.R. 3-3(b) and 3-3(c), and in light of Netlist's Infringement Contentions and accompanying claim chart served on April 8, 2010, Google attaches hereto as Exhibits 1-13 claim charts identifying prior art references that anticipate the Asserted Claims as well as combinations of prior art references which render the Asserted Claims obvious. The attached charts identify specifically where, in each alleged item of prior art, each element of each asserted claim is found.

Patent L.R. 3-3(b) requires Google to identify any combinations of prior art showing obviousness and "an explanation of why the prior art renders the asserted claim obvious." Pursuant to the Supreme Court's decision in *KSR Int'l Co. v. Teleflex, Inc.*, to the extent an express motivation to combine references is required under current law at all this requirement is minimal. For example, "any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the element." *KSR Int'l*, 550 U.S. 398, 402 (2007). In addition, "common sense" teaches that "a person of ordinary skill often will be able to fit the teachings of multiple patents together like pieces of a puzzle." *Id.*

Moreover, the rationale for combining any of these references with others exists within the references themselves, as well as within the knowledge of those of ordinary skill in the art. These references identify and address the same technical issues and suggest very similar solutions to those issues. If and to the extent Netlist challenges the correspondence of any of these references with respect to particular elements of the asserted claims, Google reserves the right to supplement these Invalidity Contentions to identify a reason to combine particular references with one another with additional particularity. An index identifying the prior art discussed in each of the attached exhibits is provided below.

Invalidity Charts for the '912 Patent	
U.S. Pat. Appl. No. 2006/0117152 A1	Exhibit 1
U.S. Pat. No. 6,209,074	Exhibit 2
U.S. Pat. No. 5,926,827	Exhibit 3
U.S. Pat. No. 5,745,914	Exhibit 4
U.S. Pat No. 4,368,515	Exhibit 5
U.S. Pat. No. 6,414,868	Exhibit 6
U.S. Pat. No. 5,581,498	Exhibit 7
U.S. Pat. Appl. No. 2006/0117152 A1 in combination with U.S. Pat. No. 6,209,074	Exhibit 8
U.S. Pat. No. 6,209,074 in combination with U.S. Pat. No. 5,926,827	Exhibit 9
U.S. Pat. No. 6,209,074 in combination with U.S. Pat. No. 5,745,914	Exhibit 10
U.S. Pat. No. 6,209,074 in combination with U.S. Pat. No. 5,581,498	Exhibit 11
U.S. Pat. No. 6,209,074 in combination with U.S. Pat No. 4,368,515	Exhibit 12
U.S. Pat. No. 6,209,074 in combination with U.S. Pat. No. 6,414,868	Exhibit 13

In charts where Google identifies a combination of references, Google may rely upon a subset of the references or all of the references depending upon the Court's claim construction and

Google's own further investigation. Further, Google's identification of multiple references in any given chart and contention that various combinations thereof render an asserted claim obvious under 35 U.S.C. § 103 is in no way an admission or suggestion that each reference does not independently anticipate the asserted claims under 35 U.S.C. § 102. The obviousness combinations stated in the attached charts are merely exemplary and are not intended to be exhaustive. Any of the references listed above in Section I for the '912 Patent may be combined to render obvious, and therefore invalid, the asserted claims of the '912 Patent.

B. Indefiniteness and Lack of Enablement (35 U.S.C. § 112 ¶¶ 1-2)

Pursuant to Patent L.R. 3-3(d), Google attaches hereto as Exhibit 14 a claim chart that identifies exemplary grounds of invalidity for the asserted claims based on indefiniteness and lack of enablement and/or written description, under 35 U.S.C. § 112 ¶¶ 1-2.

III. DOCUMENT PRODUCTION ACCOMPANYING PRELIMINARY INFRINGEMENT CONTENTIONS (PATENT L.R. 3-4)

Pursuant to Patent L.R. 3-4, Google has served, either concurrently with these Invalidity Contentions or previously produced in related Case No. 08-04144-SBA, documentation required by Pat. L.R. 3-4 (a) and (b). If Google subsequently acquires or locates any further documents falling into the categories set forth in Patent L.R. 3-4, Google will produce such documents to Netlist. Google reserves the right to rely on any such subsequently acquired and produced documents.

IV. ADDITIONAL PRIOR ART

In addition to the prior art references identified above, Google lists below the following patents, patent applications, printed publications, and products which are pertinent to the invalidity of the '912 Patent. Google has not provided claim charts for each of these references either because at this time Google does not intent to rely on them, because they have substantially similar disclosures to other prior art for which invalidity charts have been provided, or because they are used as supporting references in an obviousness combination. However, Google reserves the right to revise its invalidity contentions to rely on these references to prove the invalidity of the

asserted claims of the '912 Patent in a manner consistent with the Federal Rules of Civil Procedure and this Court's Local Rules.

Patent or Published Application Number / Title	Date of Issue/Publication
Dell 827 Information Disclosure Statement (NETLG00005198)	September 4, 2007
U.S. Patent No. 4,392,212 (GNET 000626 - 000635))	July 5, 1983
U.S. Patent No. 5,247,643 (GNET 000697 - 000735)	September 21, 1993
U.S. Patent No. 5,426,753 (GNET 000747 - 000753)	June 20, 1995
U.S. Patent No. 5,703,826 (GNET 000835 - 000844)	December 30, 1997
U.S. Patent No. 5,805,520 (GNET 000859 - 000869)	September 8, 1998
U.S. Patent No. 5,959,930 (GNET 000902 - 000949)	September 28, 1998
U.S. Patent No. 6,154,418 (GNET 001043 - 001055)	November 28, 2000
U.S. Patent No. 6,453,381 (GNET 001121 - 001129)	September 17, 2002
U.S. Patent No. 6,518,794 (GNET 001162 - 001180)	February 11, 2003
U.S. Patent No. 6,681,301 (GNET 001199 - 001212)	January 20, 2004
U.S. Patent No. 6,785,189 (GNET 001241 - 001245)	August 31, 2004
U.S. Patent No. 6,807,125 (GNET 002254 - 002265)	October 19, 2004
U.S. Patent No. 6,813,196 (GNET 001246 - 001251)	November 2, 2004
U.S. Patent No. 6,944,694 (GNET 001275 - 001297)	September 13, 2005
U.S. Patent No. 6,981,089 (GNET 001310 - 001323)	December 27, 2005
U.S. Patent No. 6,982,893 (GNET 001342 - 001347)	January 3, 2006
U.S. Patent No. 6,996,686 (GNET 001348 - 001356)	February 14, 2006
U.S. Patent No. 7,046,538 (GNET 001393 - 001404)	May 16, 2006
U.S. Patent No. 7,120,727 (GNET 001405 - 001418)	October 10, 2006
U.S. Patent No. 7,200,021 (GNET 001467 - 001476)	April 3, 2007
U.S. Patent Application Publication: US 2001/0052057 A1 (GNET 000369 - 000386)	December 31, 2001

Patent or Published Application Number / Title	Date of Issue/Publication
U.S. Patent Application Publication: US 2002/0088633 A1 (GNET 000387 - 000405)	July 11, 2002
U.S. Patent Application Publication: US 2003/0063514 A1 (GNET 000406 - 000417)	April 3, 2003
U.S. Patent Application Publication: US 2003/0191995 A1 (GNET 002266 - 002276)	October 9, 2003
U.S. Patent Application Publication: US 2003/0210575 A1 (GNET 002277 - 002301)	November 11, 2003
U.S. Patent Application Publication: US 2004/0037158 A1 (GNET 000461 - 000472)	February 26, 2004
U.S. Patent Application Publication: US 2005/0036378 A1 (GNET 000484 - 000528)	February 17, 2005
U.S. Patent Application Publication: US 2005/0281096 A1 (GNET 000529 - 000551)	December 22, 2005
U.S. Patent Application Publication: US 2006/0126369 A1 (GNET 000569 - 000578)	June 15, 2006
U.S. Patent Application Publication: US 2006/0129755 A1 (GNET 000579 - 000589)	June 15, 2006
U.S. Patent No. 6,961,281 (GNET 001298-1309)	March 17, 2005
U.S. Patent No. 7,356,639 (GNET 001519-1571)	April 8, 2008
U.S. Patent Application Publication: 2006-0044860 (GNET 002302 - 2313)	March 2, 2006
U.S. Patent No. 4,633,429 (GNET000636-642)	December 30, 1986
U.S. Patent No. 4,958,322 (GNET000643-653)	September 18, 1990
U.S. Patent No. 4,961,172 (GNET000654-671)	October 2, 1990
U.S. Patent No. 4,980,850 (GNET000672-696)	December 25, 1990
U.S. Patent No. 5,345,412 (GNET000736-746)	September 6, 1994
U.S. Patent No. 5,483,497 (GNET000754-771)	January 9, 1996
U.S. Patent No. 5,699,542 (GNET000805-818)	December 16, 1997
U.S. Patent No. 5,822,251 (GNET000870-888)	October 13, 1998
U.S. Patent No. 5,966,736 (GNET000958-982)	October 12, 1999

Patent or Published Application Number / Title	Date of Issue/Publication
U.S. Patent No. 6,108,745 (GNET001019-1042)	August 22, 2000
U.S. Patent No. 6,185,654 (GNET001056-1087)	February 6, 2001
U.S. Patent No. 6,487,102	November 26, 2002
U.S. Patent No. 6,646,949 (GNET001181-1189)	November 11, 2003
U.S. Patent No. 6,674,684 (GNET001190-1198)	January 6, 2004
U.S. Patent No. 6,697,888 (GNET001213-1222)	February 24, 2004
U.S. Patent No. 6,742,098 (GNET001223-1240)	May 25, 2004
U.S. Patent No. 6,834,014 (GNET001252-1274)	December 21, 2004
U.S. Patent No. 6,982,892 (GNET001324-1341)	January 3, 2006
U.S. Patent No. 7,007,130 (GNET001357-1392)	February 28, 2006
U.S. Patent No. 7,124,260 (GNET001419-1436)	October 17, 2006
U.S. Patent No. 7,133,960 (GNET001437-1444)	November 7, 2006
U.S. Patent No. 7,181,591 (GNET001445-1466)	February 20, 2007
U.S. Patent No. 7,266,639 (GNET001477-1487)	September 4, 2007
U.S. Patent No. 7,281,079 (GNET001488-1504)	October 9, 2007
U.S. Patent No. 7,346,750 (GNET001505-1518)	March 18, 2008
U.S. Patent Application Publication: US 2003-0090879 (GNET000418-0460)	May 15, 2003
U.S. Patent Application Publication: US 2004-0201968 (GNET000473-0483)	October 14, 2004
U.S. Patent Application Publication: US 2006-0179206 (GNET000590-0599)	August 10, 2006
U.S. Patent Application Publication: US 2006-0267172 (GNET000600-0615)	November 30, 2006
WO 1992/002879	February 20, 1992
WO 1994/007242	March 31, 1994
WO 1995/034030	December 14, 2005
WO 2002/058069	July 25, 2002

Patent or Published Application Number / Title	Date of Issue/Publication
WO 2003/017283	February 27, 2003
WO 2003/069484	August 21, 2003
WO 2006/055497	May 26, 2006
U.S. Patent No. 6,502,161 (GNET001141-1161)	December 31, 2002
U.S. Patent No. 6,553,450	April 22, 2003
U.S. Patent No. 6,639,820	October 28, 2003
U.S. Patent No. 6,683,372	January 27, 2004
U.S. Patent No. 6,968,440	November 22, 2005
U.S. Patent No. 6,970,968	November 29, 2005
U.S. Patent No. 7,078,793	July 18, 2006
U.S. Patent No. 7,266,634	September 4, 2007
U.S. Patent No. 7,363,422	April 22, 2008
U.S. Patent No. 7,155,627	December 26, 2006

Publication Title	Date of Publication
DM74LS138 • DM74LS139, Decoder/Demultiplexer, Fairchild Semiconductor Corp., August 1986, Revised March 2000 (GNET001928-1935)	August 1986
Extended abstract: Dynamically reconfigurable heterogeneous multi-processor systems with transputer-controlled communication, Tudruj, M., Journal of Systems Architecture, Vol. 43, pp. 27-32 (1997) (GNET002248-2253)	March, 1997
A 32-Bit SoPC Implementation of a P5, Toal, C., Proceedings of the Eighth IEEE International Symposium on Computers and Communication (ISCC'03), IEEE, 1530-1346/03, 2003 (GNET001936-1939)	July 2003
A banked-promotion translation lookaside buffer system, Lee, J., Journal of Systems Architecture, Vol. 47, pp. 1065-1078, (2002) (GNET001940-1952)	August 2002

Publication Title	Date of Publication
A Fully-Programmable Memory Management System Optimizing Queue Handling at Multi Gigabit Rates, Kornaros, G., 5.1, pp. 54 - 59 (GNET001953-1958)	June 2003
Accelerating system integration by enhancing hardware, firmware, and co-simulation, Schubert, K., et al. , IBM J. Res. & Dev. Vol. 48, No. 3/4, May/July 2004 (GNET001959-1971)	May/July 2004
Access Rate/Availability Improvement Logic for Dynamic Memories, Grimes, WD, IBM Techn. Discl. Bulletin, pp. 2678-2681, Oct. 1982, (GNET001972-1974)	October 1982
MPC8260 SDRAM Support, Freescale Semiconductor, Appl. Note, Doc. Number: AN2165/D, Rev. 1, 10/2006	October 2006
An 88-Way Multiprocessor Within An FPGA With Customizable Instructions, Hoare, R., Proceedings of the 18th International Parallel and Distributed Processing Symposium (IPDPS'04), 2004 (GNET001974-1982)	April 2004
An Enable Signal Circuit for Multiple Small Banks, IBM Techn. Discl. Bulletin, IP.com number: IPCOM000015887D, June 1, 2002, IP.com Electronic Publication: June 21, 2003 (GNET001983-1987)	June 1, 2002
An on-chip cache compression technique to reduce decompression overhead and design complexity, Lee, J., Journal of Systems Architecture Vol. 46, pp. 1365-1382, (2000) (GNET001988-2005)	December 2000
Bank Striping Of Data Across Internal Sdram Banks, IBM Technical Disclosure Bulletin, IP.com number: IPCOM000013697D, August 1, 2000, IP.com Electronic Publication: June 18, 2003 (GNET002006-2008)	August 1, 2000
Chip Select Circuit for Multi-Chip RAM Modules, Fitzgerald, B.F., et al., IBM Technical Disclosure Bulletin, pp. 3932-3934, Dec. 1, 1984, IP.com number: IPCOM000044404D, IP.com Electronic Publication: February 5, 2005 (GNET002028-2030)	December 1, 1984
Chip Select Decoder Circuit, Smith, B.A., IBM Technical Disclosure Bulletin, pp. 5826-5827, March 1, 1985, IP.com Number: IPCOM000063400D, IP.com Electronic Publication: February 18, 2005 (GNET002031-2033)	March 1, 1985

Publication Title	Date of Publication
Chip Select Technique for Multi Chip Decoding, Hession, J., IBM Technical Disclosure Bulletin, pp. 1563-1564, Sept. 1, 1978, IPCOM000070404D, IP.com Electronic Publication: February 21, 2005 (GNET002034-2036)	September 1, 1978
Concurrency, Latency, or System Overhead: Which Has the Largest Impact on Uniprocessor DRAM-System Performance?, Cuppu, V., et al., IEEE, pp. 62-71, 2001,.Proceedings of the 28th International Symposium on Computer Architecture, June 30–July 4, 2001 (GNET002037-2046)	July 2001
Continuous RAS Access Method in Multiple-bank DRAM Chip, Sunaga, T, et al., IBM Technical Disclosure Bulletin, Vol. 41, No. 414, pp. 10-48, Article 41473, October 1, 1998, IP.com No: IPCOM0001233750, IP.com Electronic Publication: April 4, 2005 (GNET002047-2049)	October 1, 1998
Designing a Modern Memory Hierarchy with Hardware Prefetching, Lin, W., IEEE Transactions On Computers, Vol. 50, No. 11, pp. 1202-1217, Nov. 2001 (GNET002050-2065)	November 2001
Designing And Implementing A Fast Crossbar Scheduler, Gyupta, P., IEEE Micro, pp. 20-28, 1999 (GNET002066-2074)	January-February 1999
Distributed Memory Mapping, IBM Technical Disclosure Bulletin, October 1, 2000, IP.com No: IPCOM0000147880, IP.com Electronic Publication: June 20, 2003 (GNET002075-2077)	October 1, 2000
Dual Addressable Memory, Pellinger, R.D., et al., IBM Technical Disclosure Bulletin, January 1, 1978, pp. 3259-3260, IP.com No: IPCOM000068610D, IP.com Electronic Publication: February 20, 2005 (GNET002080-2082)	January 1, 1978
Embedded Memory in System-on-Chip Design: Architecture and Prototype Implementation, Jin, H., et al., IEEE, pp. 141- 146, 2003 (GNET002083-2088)	May 2003
Enhancement of Memory Card Redundant Bit Usage Via Simplified Fault Alignment Exclusion, Implementation, Arlington, DL, IBM Technical Disclosure Bulletin, pp. 507-509, July 1987 (GNET002089-2090)	July 1987

Publication Title	Date of Publication
Fast Multichip Memory System With Power Select Signal, Blum, A, IBM Technical Disclosure Bulletin, pp. 1057-1058, Aug. 1979 (GNET002091-2092)	August 1979
Fet Ram Chip Double Density Scheme, Gray, K., IBM Technical Disclosure Bulletin, p. 2927, Oct. 1, 1984, IP.com No: IPCOM000043942D, IP.com Electronic Publication: Feb. 5, 2005 (GNET002093-2095)	October 1, 1984
FPGA: take Five, www.electronicsnews.com, Aug. 26, 2002, p. 24 (GNET002096)	August 26, 2002
High Density Memory Selection Circuit, Yao, YL, IBM Technical Disclosure Bulletin, pp. 2042-2044, Dec. 1, 1972, IP.com No: IPCOM000078218D, IP.com Electronic Publication: Feb. 25, 2005 (GNET002097-2100)	December 1, 1972
High-Performance DRAMs in Workstation Environments, Cuppu, V., IEEE Transactions On Computers, Vol. 50, No. 11, pp. 1133-1153, Nov. 2001 (GNET002101-2120)	November 2001
IBM's *S/390* G5 Microprocessor Design, Siegel, T., (IBM Corp.), IEEE - March-April 1999, pp. 12-23 (GNET002121-2132)	March-April 1999
Input/Output Chip Select Doubler, Bennayoun, A, IBM Technical Disclosure Bulletin, April 1, 1995, Vol. 38, No. 4, p. 237-240, IP.com No: IPCOM000115289D, IP.com Electronic Publication: March 30, 2005 (GNET002133-2137)	April 1, 1995
Interface Synthesis using Memory Mapping for an FPGA Platform, Luthra, M., Proceedings of the 21st International Conference on Computer Design (ICCD'03), IEEE 2003 (GNET002138-2143)	October 2003
WSI Aims Programmable MCU Peripherals At DSPs - Integrated Solution Can Stand In For Two Chips, Electronic Buyer's News, n. 927 , p. 39, 1994	1994
Logic and Decoder Arrangement for Controlling Spill/Wrap Boundaries of a Bit-Addressable Memory Decoder, Matick, R., IBM Technical Disclosure Bulletin, pp 3699-3702, Dec. 1984 (GNET002156-2158)	December 1984
Logic Processor for Logic Simulation Machine, Denneau, M., IBM Technical Disclosure Bulletin, Vol. 25, No. 1, pp. 91-94, June 1982 (GNET002158)	June 1982

Publication Title	Date of Publication
Memory Expansion Technology (MXT): Software Support and Performance, Abali, B., IBM J. Res. & Dev. Vol. 45, No. 2, pp. 287-300, March 2001 (GNET002160-2173)	March 2001
Method for a high-performance DRAM address mapping mechanism, IP.com No: IPCOM000008164D, IP.com Electronic Publication: May 22, 2002 (GNET002174-2178)	May 22, 2002
Method For Memory Probing On A Multiple-DIMM Bus, IP.com No: IPCOM000019063D, IP.com Electronic Publication: August 27, 2003 (GNET002179-2181)	August 27, 2003
Method for Multiple Device Interface Testing Using A Single Device, IP.com Electronic Publication: October 16, 2002, IP.com number: IPCOM000010054D (GNET002182-2185)	October 16, 2002
Method of Executing Manufacturing ROM Code Without Removing System Roms, Arroyo, RX, IBM Technical Disclosure Bulletin, Nov. 1, 1989, pp. 479-480, IP.com Electronic Publication: January 29, 2005, IP.com No: IPCOM000037214D (GNET002186-2188)	November 1, 1989
Partial Two Way Mapping Technique, Ofek, H., IBM Technical Disclosure Bulletin, pp. 429-430, Aug. 1969 (GNET002189-2190)	August 1969
Planar Memory Boundary Registers with Remap Feature, Stelzer, K., IBM Technical Disclosure Bulletin, pp. 627-628, Nov. 1993 (GNET002191-2192)	November 1993
Program Controlled Paging Scheme for Memory Expansion, IBM Technical Disclosure Bulletin, Dec. 1, 1982, p. 3865, IP.com number: IPCOM000050954D , IP.com Electronic Publication: February 10, 2005 (GNET002193-2195)	December 1, 1982
Programmable Memory Address Decoding For Microprocessor Memory Devices, Paldan, D., Motorola Technical Disclosure Bulletin, March 1, 1983, IP.com number: IPCOM000005486D, IP.com Electronic Publication: October 9, 2001 (GNET002196-2198)	March 1, 1983
"Programmable Logic: What's it to Ya?," How Programmable Logic Works, Barr, Michael, Embedded Systems Programming, June 1999, pp. 75-84. (GNET002122-2206)	June 1999

Publication Title	Date of Publication
Prototype Implementation and Evaluation of a Multibank Embedded Memory Architecture in Programmable Logic, Jin, H., IEEE, 2003, pp. 13-16 (GNET002207-2210)	August 2003
Read-Select Capability for Static Random-Access Memory, Matick, R., IBM Technical Disclosure Bulletin, pp. 6640-6642, April 1985 (GNET002214-2216)	April 1985
Shuffle Your Chips For Better Performance, Plotnick, N., PC Week - Netweek, p. 90, Aug. 17, 1998 (GNET002217)	August 17, 1998
Use Of Partially Good Memory Chips, Meyers, R., IBM Technical Disclosure Bulletin, Feb. 1, 1979, pp. 3582-3583, IP.com number: IPCOM000066246D, IP.com Electronic Publication: February 19, 2005 (GNET002233-2235)	February 1, 1979
Read Only Store Memory Extension, Kane, M., et al., IBM Technical Disclosure Bulletin, Feb. 1, 1975, pp. 2695-2696, IP.com No: IPCOM000082845D, IP.com Electronic Publication: Feb. 28, 2005 (GNET002211-2213)	February 1, 1975
QBM Alliance, "Quad Band Memory: DDR 200/266/333 devices producing DDR 400/533/667," January 23-24, 2002.	January 23-24, 2002
Miles J. Murdocca and Vincent P. Heuring, Principles of Computer Architecture, 2000.	2000
U.S. Patent Application Publication: US 2005/0138267 A1	June 23, 2005
A Performance Comparison of Contemporary DRAM Architectures, Cuppu, V., Proceedings of the 26th International Symposium on Computer Architecture, May 2-4, 1999 (GNET 002236 - 002247)	May, 1999
Micron DDR SDRAM RDIMM MT36VDDF12872 – 1GB MT36VDDF25672 – 2GB	2002

Products	Company	Date of First Sale/Public Use
ProLiant 7000 Server	Compaq	June 1998

DATED: May 14, 2010

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CERTIFICATE OF SERVICE

I hereby certify that a true and correct copy of *DEFENDANT GOOGLE INC.'S INVALIDITY CONTENTIONS PURSUANT TO PATENT L.R. 3-3 AND 3-4* is being served by electronic mail upon the following counsel of record on this 14th day of May, 2010:

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Exhibit 6

U.S. Patent No. 6,414,868 alone or in combination with other prior art invalidates U.S. Patent No. 7,619,912 under 35 U.S.C. § 102(b) and 35 U.S.C. § 103(a)

All cited text is taken from the following documents:

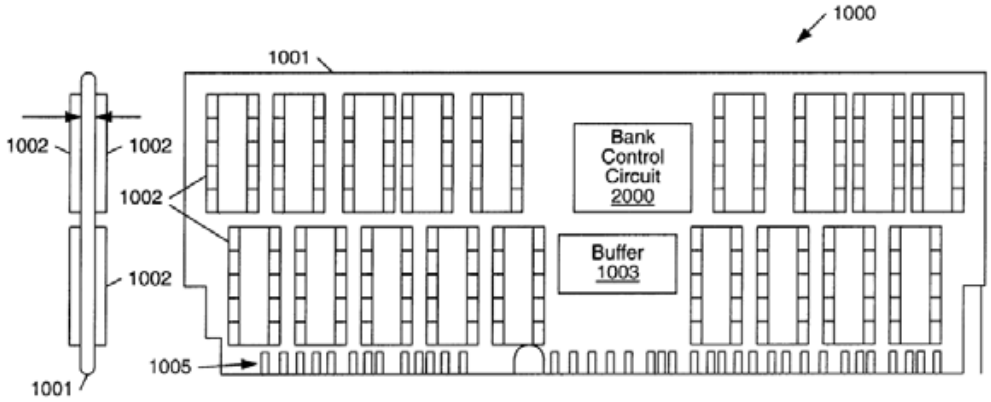
U.S. Patent No. 6,414,868 (the "'868 Patent") to Wong et al. entitled "Memory Expansion Module Including Multiple Memory Banks and a Bank Control Circuit," filed June 7, 1999 and issued July 2, 2002 (prior art to the '912 Patent under 35 U.S.C. § 102(b))

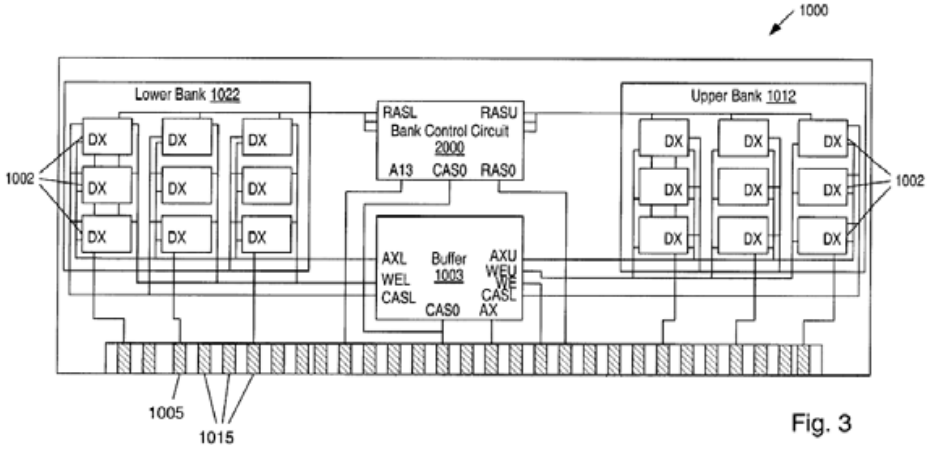
Summary:

Claims 1, 3, 4, 6, 8-11, 15, 18-21, 24, 25, 27-29, 31-34, 36-39, 41-45 and 50 are invalid under 35 U.S.C. § 102 as anticipated by the '868 Patent or under 35 U.S.C. § 103 as obvious over the '868 Patent alone or in view of other prior art

Claim Chart of U.S. Patent No. 7,619,912

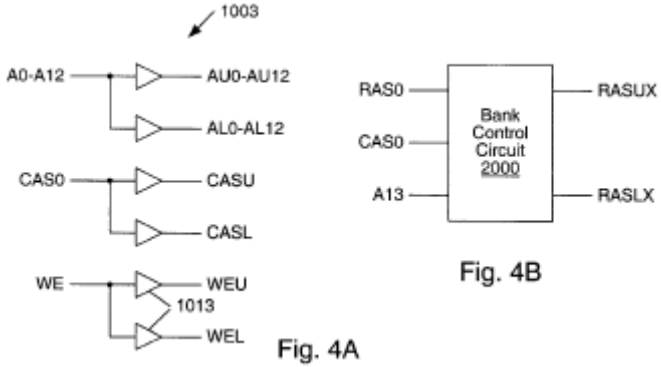
Based on U.S. Patent No. 6,414,868

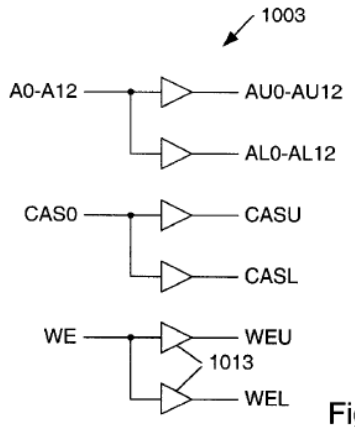
Claim Element	Disclosure of U.S. Patent No. 6,414,868
Claim 1. A memory module connectable to a computer system, the memory module comprising:	The '868 Patent discloses a memory module connectable to a computer system at 1:8-10: "This invention generally relates to memory hardware for computer systems, and more specifically to memory expansion modules for expanding memory in computer systems."
a printed circuit board;	The '868 Patent discloses a printed circuit board. "Turning now to FIG. 2, a diagram illustrating components associated with a memory module 1000 is shown. In this particular embodiment, a plurality of memory elements 1002, typically DRAM (Dynamic Random Access Memory) chips, are surface mounted upon a printed circuit board (PCB) 1001." (3:58-63)  Fig. 2
a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR	The '868 Patent discloses a plurality of memory devices mounted to the printed circuit board. "Turning now to FIG. 2, a diagram illustrating components associated with a memory module 1000 is shown. In this particular embodiment, a plurality of memory elements 1002, typically DRAM (Dynamic Random Access Memory)

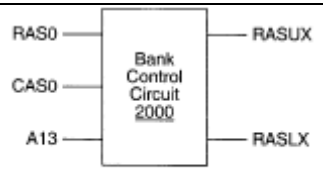
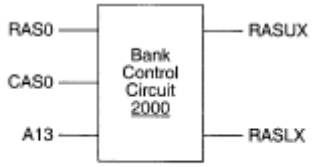
Claim Element	Disclosure of U.S. Patent No. 6,414,868
memory devices having a first number of DDR memory devices arranged in a first number of ranks;	chips, are surface mounted upon a printed circuit board (PCB) 1001." (3:58-63) "Memory module 1000 includes an edge connector 1005, a lower memory bank 1022, and upper memory bank 1012, a bank control circuit 2000 and a buffer 1003. Each memory bank includes of a plurality of memory chips 1002." (4:15-19) FIG. 3 shows the memory module 1000 with 18 memory devices 1002.  Fig. 3 One of ordinary skill in the art at the time the application that matured into the '912 Patent was filed would understand that DRAM memory chips could comprise double-data-rate (DDR) memory devices. For example, JEDEC Standard JESD-82 entitled "Definition of CDCV857 PLL Clock Driver for Registered **DDR** DIMM Applications" was published in July 2000. (emphasis added) FIG. 3, reproduced above, shows the memory devices arranged in two ranks, the lower 1022, and the upper 1012. The term "rank" in the claim has the same meaning as the term "bank" in Wong.
a circuit mounted to the printed circuit board, the circuit comprising a	The '868 Patent discloses a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register. The logic element includes the buffer 1003 and the bank control circuit 2000. (The

Claim Element	Disclosure of U.S. Patent No. 6,414,868
logic element and a register,	buffer 1003 is also referred to as the buffer chip 1003 and the buffer circuit 1003.) The buffer can be considered a register because one of ordinary skill in the art would understand that buffering is what a register does. "Also mounted on PCB 1001 are a buffer chip 1003 . . . and a bank control circuit 2000." (4:7-9) "Turning now to FIG. 5, a schematic of one embodiment of the bank control circuit 2000 is shown. This particular embodiment of bank control circuit 2000 is a programmable logic device (PLD. (sic) In this embodiment, bank control circuit 2000 comprises a plurality of AND gates 2001, NAND gates 2002, inverters 2003, and flip-flops 2004 (D-type flip-flops in this embodiment). Bank control circuit 2000 drives multiple RAS signals for each memory bank in order to provide sufficient signal drive strength to each of the memory chips. The operation of the bank control circuit will be further illustrated in FIG. 6 and FIG. 7. It should be noted that alternative embodiments of the bank control circuit are possible using other types of electronic circuitry." (5:10-23)
the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal,	The '868 Patent discloses the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal. The buffer chip 1003 receives input control signals A0-A12, CAS0, and WE and the bank control circuit 2000 receives input control signals RAS0, CAS0, and A13 from a computer system to which the memory module is connected. The RAS signal in the '868 Patent is used as a chip-select signal. "[A] memory module includes a printed circuit board with a connector edge adapted for insertion in an expansion socket of a computer system." (Abstract) "Signals passing through the edge connector include data signals, address signals, and control signals." (3:58 –4:2) "In the embodiment shown, buffer chip 1003 receives a plurality of address

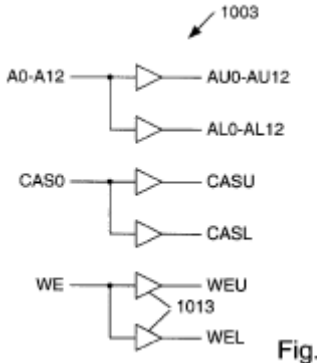
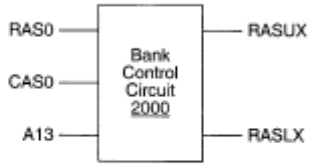
Claim Element	Disclosure of U.S. Patent No. 6,414,868
	signals, A0-A12, a CAS0 signal, and a WE signal." (4:44-46) "In this embodiment, bank control circuit 2000 receives input signals RAS0, CAS0, and address signal A13." (4:56-57) FIG. 3, reproduced above, shows the signals as being received from the computer system through electrical contact pads 1015. (4:19-21)
the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks,	The '868 Patent discloses the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks. The input control signals, which are received from the computer system, include 14 address signals (A0-A13) and one row access strobe (RAS) signal. The input control signals include only one row access strobe (RAS) signal, and therefore correspond to one rank (the second number) of memory devices. The second number of ranks, one, is less than the first number of ranks, which is two. "[The] presence of only one RAS and one CAS signal also limits the ability to expand system memory, as a separate bank of memory typically requires at minimum either a unique RAS or unique CAS signal for each bank." (2:3-7) "By using the bank control circuit to enable the addition of a second memory bank, a memory expansion can be realized without the need for higher capacity memory chips, which may result in an advantageous cost savings." (2:33-37) "The use of memory chips with a greater number of address inputs, and hence higher capacity, may disproportionately increase the cost of the desired memory expansion." (1:62-65) "Buffer 1003 receives . . . a plurality of address signals, shown as AX. Buffer circuit 1003 drives a plurality of address signals AXL and AXU, which are

Claim Element	Disclosure of U.S. Patent No. 6,414,868
	conveyed to the lower memory bank 1022 and upper memory bank 1012, respectively. . . . The bank control circuit 2000 is configured to receive an address signal A13 for selecting the upper and lower bank. Address signal A13, in this embodiment, is the most significant address bit of an address bus that is 14 bits wide." (4:23-37) "Address signal A13, in this embodiment [of FIG. 3], is the most significant address bit of an address bus that is 14 bits wide." (4:35- 37) The remaining address bits, A0 – A12, are designated "AX" in FIG. 3. As illustrated in FIGS. 3, 4A and 4B, address bits A0-A12 go through the buffer 1003 and are used to address the memory devices within a rank, unlike A13, which is used by bank control circuit 2000 to select the upper or lower rank of the memory module 1000.  Fig. 4A Fig. 4B
the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first	The '868 Patent discloses the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks. The buffer chip 1003 (which constitutes the logic element together with the bank control circuit) generates output control signals AU0-AU12, AL0-AL12, CASU,

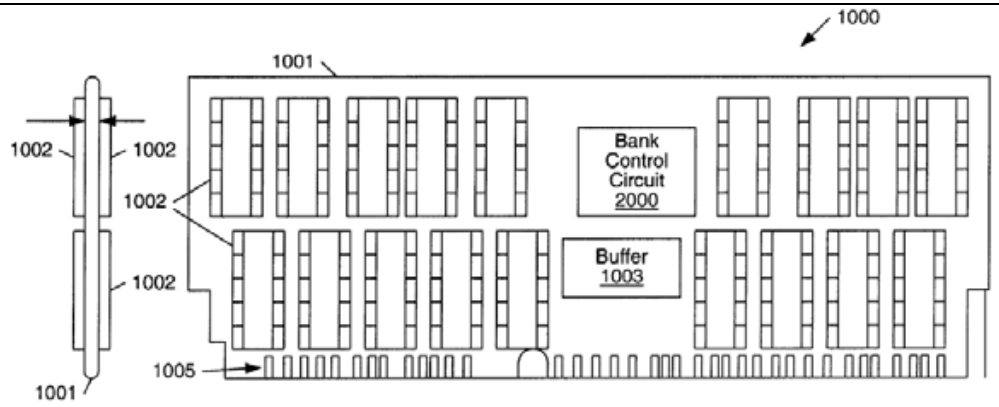
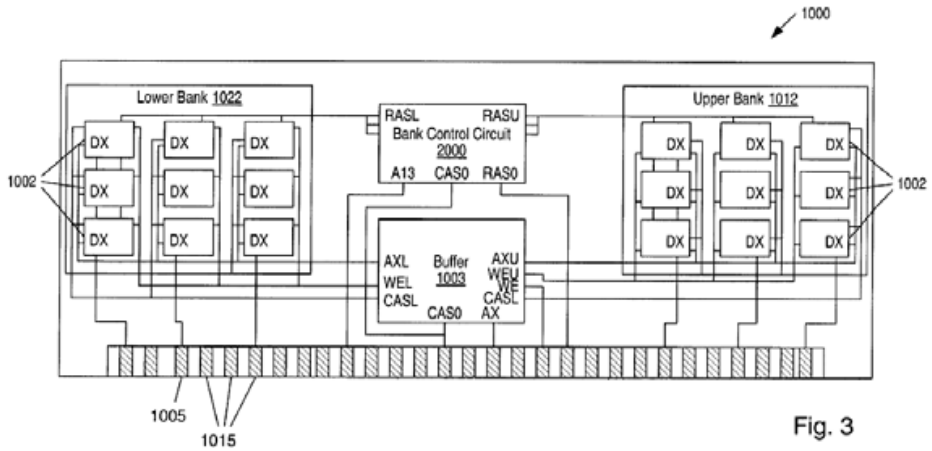
Claim Element	Disclosure of U.S. Patent No. 6,414,868
number of DDR memory devices arranged in the first number of ranks,	CASL, WEU, and WEL and the bank control circuit 2000 generates output control signals RASLX, and RASUX in response to the input control signals A0-A13, CAS0, RAS0, and WE. These signals control and therefore correspond to all the memory devices (the "first number of DDR memory devices arranged in the first number of ranks") on the module. "FIG. 4A further illustrates an internal configuration of an embodiment of a buffer chip 1003. In the embodiment shown, buffer chip 1003 receives a plurality of address signals, A0-A12, a CAS0 signal, and a WE signal. The signals are passed through buffers 1013, generating corresponding signals that will be provided to an upper bank and a lower bank of memory chips." (4:43-49)  Fig. 4A "One embodiment of bank control circuit 2000 is shown in FIG. 4B. In this embodiment, bank control circuit 2000 receives input signals RAS0, CAS0, and address signal A13. Bank control circuit 2000 drives a plurality of RASLX and RASUX signals to the lower and upper memory banks, respectively." (4:55-60)

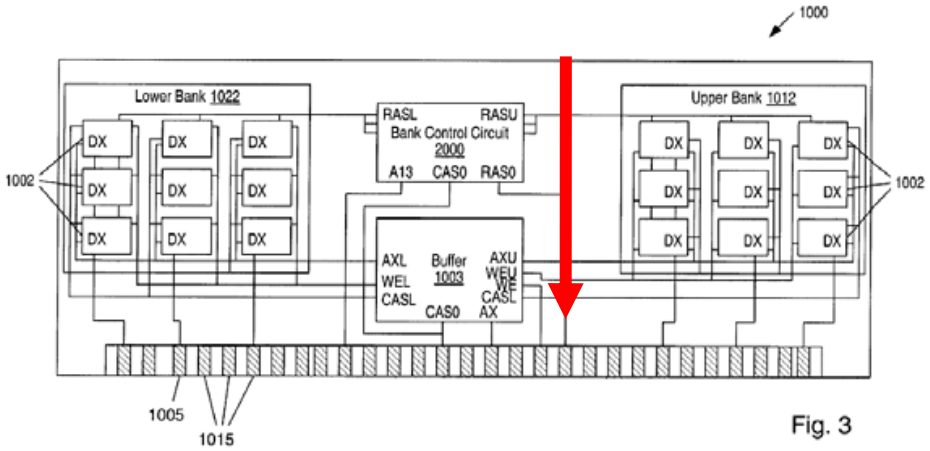
Claim Element	Disclosure of U.S. Patent No. 6,414,868
	 Fig. 4B
wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks;	The '868 Patent discloses the circuit further responding to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks. The signals received by the memory module 1000 from the computer system include a WE (write) signal. (The '912 patent identifies write and refresh signals, among others, as command signals. See, e.g., '912 patent, 8:45-60) As shown in FIG. 4B, below, the Bank Control Circuit 2000 (which is part of the logic element) receives one RAS0 signal (corresponding to one, the second number of ranks) and generates two or more RAS signals (corresponding to two, the first number of ranks).  Fig. 4B In addition, the bank control circuit 2000 receives "receive a row address strobe (RAS) signal and a column address strobe signal, and at least one address signal, wherein said bank control circuit is configured to selectively provide at least one

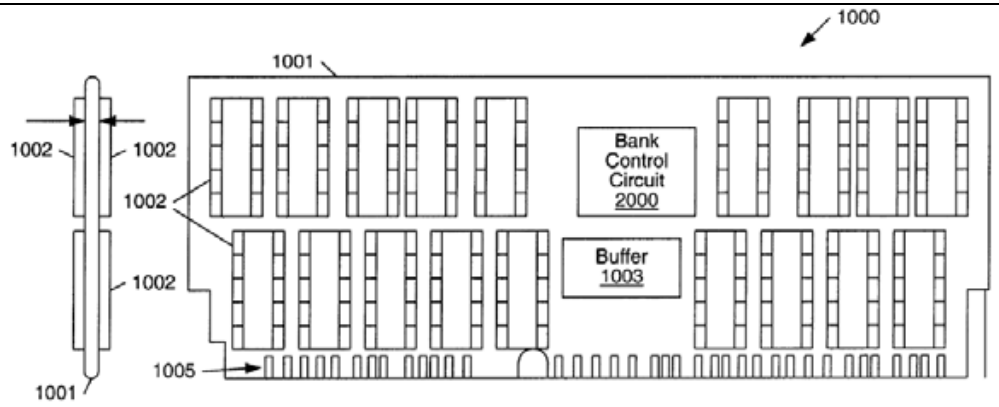
Claim Element	Disclosure of U.S. Patent No. 6,414,868
	corresponding RAS output signal to either said upper bank of memory chips or said lower bank of memory chips depending upon said address signal to thereby allow either said lower bank of memory chips or said upper bank of memory chips to be selectively accessed during a given memory operation" (Claim 1 of the '868 Patent)
and a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register.	The use of a phase-lock loop device in memory modules was known to those of ordinary skill in the art at the time of the filing of the application that matured into the '912 Patent. For example, JEDEC Standard JESD-82 entitled "Definition of CDCV857 PLL Clock Driver for Registered DDR DIMM Applications" was published in July 2000. Furthermore, the inventor of the '912 Patent admitted that "Persons skilled in the art are able to select a phase-lock loop device 50 and a register 60 compatible with embodiments described herein." '912 Patent at 5:42-45.
Claim 3. The memory module of claim 1, wherein the set of input control signals comprises a first number of chip-select signals and wherein the set of output control signals comprises a second number of chip-select signals greater than the first number of chip-select signals.	The '868 Patent discloses the set of input control signals comprising a first number of chip-select signals and wherein the set of output control signals comprises a second number of chip-select signals greater than the first number of chip-select signals. The input control signals, which are received from the computer system, include 14 address signals (A0-A13) and one row access strobe (RAS) signal. The RAS signal is used as the chip-select signal. "The use of memory chips with a greater number of address inputs, and hence higher capacity, may disproportionately increase the cost of the desired memory expansion." (*1:62-65*) "Buffer 1003 receives . . . a plurality of address signals, shown as AX. Buffer circuit 1003 drives a plurality of address signals AXL and AXU, which are conveyed to the lower memory bank 1022 and upper memory bank 1012, respectively. . . . The bank control circuit 2000 is configured to receive an address

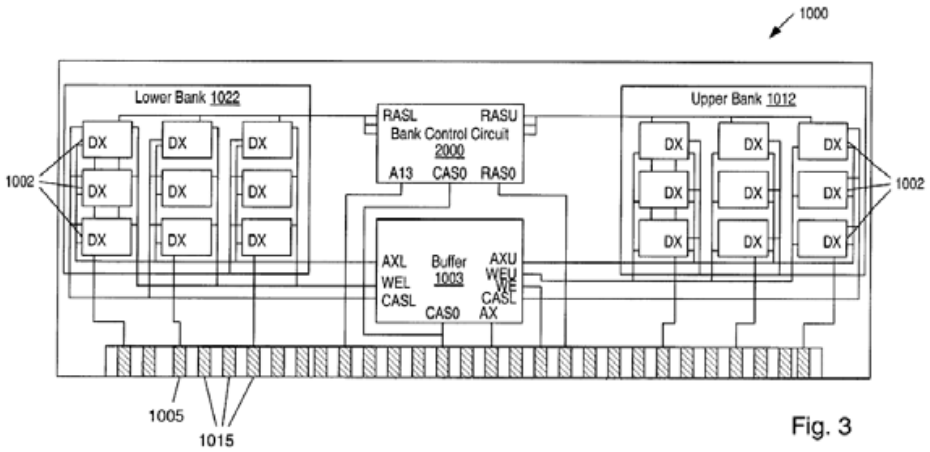
Claim Element	Disclosure of U.S. Patent No. 6,414,868
	signal A13 for selecting the upper and lower bank. Address signal A13, in this embodiment, is the most significant address bit of an address bus that is 14 bits wide." (4:23- 37) The remaining address bits, A0 – A12, are designated "AX" in FIG. 3. As illustrated in FIGS. 3, 4A and 4B, address bits A0-A12 go through the buffer 1003 and are used to address the memory devices within a rank, unlike A13, which is used by bank control circuit 2000 to select the upper or lower rank of the memory module 1000.  Fig. 4A  Fig. 4B
Claim 4. The memory module of claim 3, wherein the first number of chip-select signals is two and the second number of chip-select signals is four.	As discussed above in connection claim 1, the '868 Patent discloses an embodiment where the first number of chip-select signals is one and the second number of chip-select signals is two. One of ordinary skill in the art would understand that the first number of chip-select signals being two and the second number of chip-select signals being four was within the scope of the '868 invention. "While the present invention has been described with reference to particular embodiments, it will be understood that the embodiments are illustrative and that the invention scope is not so limited. Any variations, modifications, additions, and improvements to the embodiments described are possible. These variations, modifications, additions, and improvements may fall within the scope of the

Claim Element	Disclosure of U.S. Patent No. 6,414,868
	inventions as detailed within the following claims." (6:4-11)
6. The memory module of claim 1, wherein the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device.	The '868 Patent discloses the logic element comprising an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device. "In this embodiment, the bank control circuit is a programmable logic device (PLD), although this circuit may be implemented in other forms for different embodiments." 2:41-44.
9. The memory module of claim 1, wherein the register comprises a plurality of register devices.	The inventor of the '912 Patent admitted that one of ordinary skill in the art would know how to select a register that comprised a plurality of register devices at 5:42-45: "Persons skilled in the art are able to select a phase-lock loop device 50 and a register 60 compatible with embodiments described herein."
10. The memory module of claim 1, wherein the plurality of DDR memory devices is arranged as a first set of DDR memory devices on a first side of the printed circuit board, a second set of DDR memory devices on the first side of the printed circuit board, a third set of DDR memory devices	The '868 Patent discloses the plurality of DDR memory devices being arranged as a first set of DDR memory devices on a first side of the printed circuit board, a second set of DDR memory devices on the first side of the printed circuit board, a third set of DDR memory devices on a second side of the printed circuit board, and a fourth set of DDR memory devices on the second side of the printed circuit board, the DDR memory devices of the second set spaced from the DDR memory devices of the first set, the DDR memory devices of the fourth set spaced from the DDR memory devices of the third set. Figure 2 shows memory chips 1002 arranged on the first and second sides of a printed circuit board.

Claim Element	Disclosure of U.S. Patent No. 6,414,868
on a second side of the printed circuit board, and a fourth set of DDR memory devices on the second side of the printed circuit board, the DDR memory devices of the second set spaced from the DDR memory devices of the first set, the DDR memory devices of the fourth set spaced from the DDR memory devices of the third set.	 Fig. 2 Figure 3 of the '868 Patent reproduced below shows one side of a printed circuit board with the second set of memory devices (upper bank 1012) spaced from the first set of memory devices (lower bank 1022). One of ordinary skill in the art would understand that the memory devices on the second side of the printed circuit board shown in Figure 2 could be arranged in the same way as the memory devices on the first side of the printed circuit board.  Fig. 3

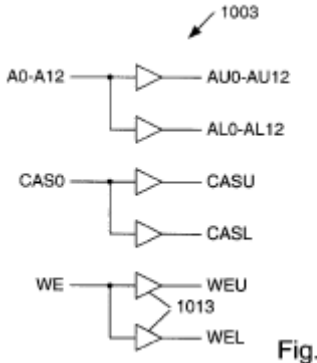
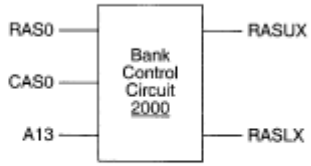
Claim Element	Disclosure of U.S. Patent No. 6,414,868
11. The memory module of claim 10, wherein the DDR memory devices of the second set are spaced from the DDR memory devices of the first set in a direction along the first side and the memory devices of the fourth set are spaced from the memory devices of the third set in a direction along the second side.	The ‘868 Patent discloses the DDR memory devices of the second set being spaced from the DDR memory devices of the first set in a direction along the first side and the memory devices of the fourth set are spaced from the memory devices of the third set in a direction along the second side. See figure 3 reproduced below with the direction shown by the red arrow (added)  Fig. 3
15. A memory module connectable to a computer system, the memory module comprising:	The ‘868 Patent discloses a memory module connectable to a computer system at 1:8-10: “This invention generally relates to memory hardware for computer systems, and more specifically to memory expansion modules for expanding memory in computer systems.”
a printed circuit board;	The ‘868 Patent discloses a printed circuit board. “Turning now to FIG. 2, a diagram illustrating components associated with a memory module 1000 is shown. In this particular embodiment, a plurality of memory elements 1002, typically DRAM (Dynamic Random Access Memory) chips, are surface mounted upon a printed circuit board (PCB) 1001.” (3:58-63)

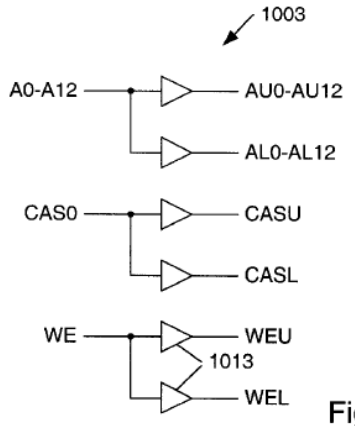
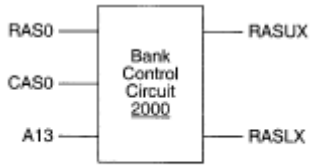
Claim Element	Disclosure of U.S. Patent No. 6,414,868
	 Fig. 2
a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;	The '868 Patent discloses a plurality of memory devices mounted to the printed circuit board. "Turning now to FIG. 2, a diagram illustrating components associated with a memory module 1000 is shown. In this particular embodiment, a plurality of memory elements 1002, typically DRAM (Dynamic Random Access Memory) chips, are surface mounted upon a printed circuit board (PCB) 1001." (3:58-63) "Memory module 1000 includes an edge connector 1005, a lower memory bank 1022, and upper memory bank 1012, a bank control circuit 2000 and a buffer 1003. Each memory bank includes of a plurality of memory chips 1002." (4:15-19) FIG. 3 shows the memory module 1000 with 18 memory devices 1002.

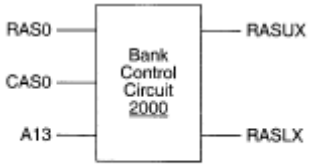
Claim Element	Disclosure of U.S. Patent No. 6,414,868
	 Fig. 3 One of ordinary skill in the art at the time the application that matured into the '912 Patent was filed would understand that DRAM memory chips could comprise double-data-rate (DDR) memory devices. For example, JEDEC Standard JESD-82 entitled "Definition of CDCV857 PLL Clock Driver for Registered **DDR** DIMM Applications" was published in July 2000. (emphasis added) FIG. 3, reproduced above, shows the memory devices arranged in two ranks, the lower 1022, and the upper 1012. The term "rank" in the claim has the same meaning as the term "bank" in Wong.
a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register,	The '868 Patent discloses a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register. The logic element includes the buffer 1003 and the bank control circuit 2000. (The buffer 1003 is also referred to as the buffer chip 1003 and the buffer circuit 1003.) The buffer can be considered a register because one of ordinary skill in the art would understand that buffering is what a register does. "Also mounted on PCB 1001 are a buffer chip 1003 . . . and a bank control circuit 2000." (4:7-9)

Claim Element	Disclosure of U.S. Patent No. 6,414,868
	"Turning now to FIG. 5, a schematic of one embodiment of the bank control circuit 2000 is shown. This particular embodiment of bank control circuit 2000 is a programmable logic device (PLD. (sic) In this embodiment, bank control circuit 2000 comprises a plurality of AND gates 2001, NAND gates 2002, inverters 2003, and flip-flops 2004 (D-type flip-flops in this embodiment). Bank control circuit 2000 drives multiple RAS signals for each memory bank in order to provide sufficient signal drive strength to each of the memory chips. The operation of the bank control circuit will be further illustrated in FIG. 6 and FIG. 7. It should be noted that alternative embodiments of the bank control circuit are possible using other types of electronic circuitry." (5:10-23)
the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal,	The '868 Patent discloses the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal. The buffer chip 1003 receives input control signals A0-A12, CAS0, and WE and the bank control circuit 2000 receives input control signals RAS0, CAS0, and A13 from a computer system to which the memory module is connected. The RAS signal in the '868 Patent is used as a chip-select signal. "[A] memory module includes a printed circuit board with a connector edge adapted for insertion in an expansion socket of a computer system." (Abstract) "Signals passing through the edge connector include data signals, address signals, and control signals." (3:58 –4:2) "In the embodiment shown, buffer chip 1003 receives a plurality of address signals, A0-A12, a CAS0 signal, and a WE signal." (4:44-46) "In this embodiment, bank control circuit 2000 receives input signals RAS0, CAS0, and address signal A13." (4:56-57) FIG. 3, reproduced above, shows the signals as being received from the computer

Claim Element	Disclosure of U.S. Patent No. 6,414,868
	system through electrical contact pads 1015. (4:19-21)
the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks,	The '868 Patent discloses the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks. The input control signals, which are received from the computer system, include 14 address signals (A0-A13) and one row access strobe (RAS) signal. The input control signals include only one row access strobe (RAS) signal, and therefore correspond to one rank (the second number) of memory devices. The second number of ranks, one, is less than the first number of ranks, which is two. "[The] presence of only one RAS and one CAS signal also limits the ability to expand system memory, as a separate bank of memory typically requires at minimum either a unique RAS or unique CAS signal for each bank." (2:3-7) "By using the bank control circuit to enable the addition of a second memory bank, a memory expansion can be realized without the need for higher capacity memory chips, which may result in an advantageous cost savings." (2:33-37) "The use of memory chips with a greater number of address inputs, and hence higher capacity, may disproportionately increase the cost of the desired memory expansion." (1:62-65) "Buffer 1003 receives . . . a plurality of address signals, shown as AX. Buffer circuit 1003 drives a plurality of address signals AXL and AXU, which are conveyed to the lower memory bank 1022 and upper memory bank 1012, respectively. . . . The bank control circuit 2000 is configured to receive an address signal A13 for selecting the upper and lower bank. Address signal A13, in this embodiment, is the most significant address bit of an address bus that is 14 bits wide." (4:23-37)

Claim Element	Disclosure of U.S. Patent No. 6,414,868
	"Address signal A13, in this embodiment [of FIG. 3], is the most significant address bit of an address bus that is 14 bits wide." (4:35- 37) The remaining address bits, A0 – A12, are designated "AX" in FIG. 3. As illustrated in FIGS. 3, 4A and 4B, address bits A0-A12 go through the buffer 1003 and are used to address the memory devices within a rank, unlike A13, which is used by bank control circuit 2000 to select the upper or lower rank of the memory module 1000.  Fig. 4A  Fig. 4B
the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks,	The '868 Patent discloses the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks. The buffer chip 1003 (which constitutes the logic element together with the bank control circuit) generates output control signals AU0-AU12, AL0-AL12, CASU, CASL, WEU, and WEL and the bank control circuit 2000 generates output control signals RASLX, and RASUX in response to the input control signals A0-A13, CAS0, RAS0, and WE. These signals control and therefore correspond to all the memory devices (the "first number of DDR memory devices arranged in the first number of ranks") on the module.

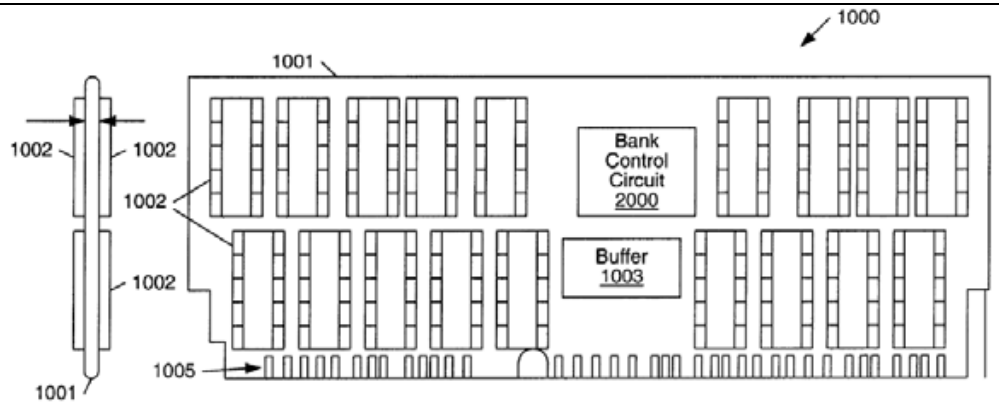
Claim Element	Disclosure of U.S. Patent No. 6,414,868
	"FIG. 4A further illustrates an internal configuration of an embodiment of a buffer chip 1003. In the embodiment shown, buffer chip 1003 receives a plurality of address signals, A0-A12, a CAS0 signal, and a WE signal. The signals are passed through buffers 1013, generating corresponding signals that will be provided to an upper bank and a lower bank of memory chips." (4:43-49)  Fig. 4A "One embodiment of bank control circuit 2000 is shown in FIG. 4B. In this embodiment, bank control circuit 2000 receives input signals RAS0, CAS0, and address signal A13. Bank control circuit 2000 drives a plurality of RASLX and RASUX signals to the lower and upper memory banks, respectively." (4:55-60)  Fig. 4B
wherein the circuit further responds to a	The '868 Patent discloses the circuit further responding to a command signal and the set of input signals from the computer system by selecting one or two ranks of

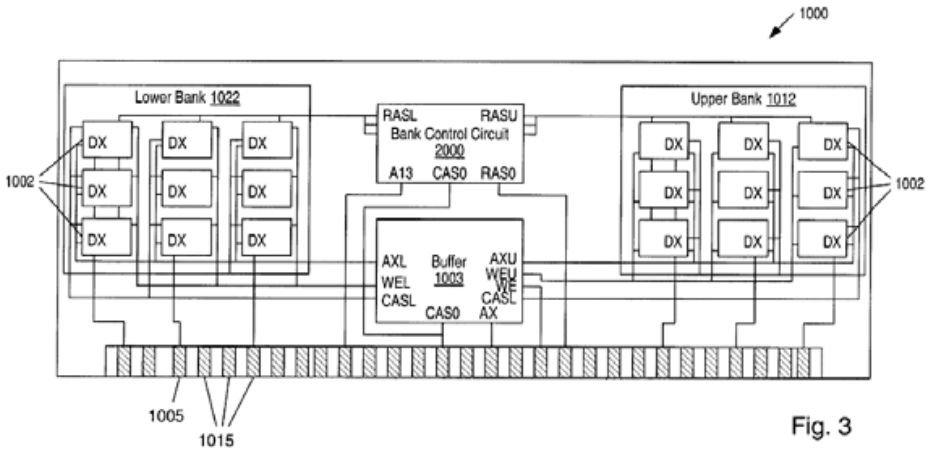
Claim Element	Disclosure of U.S. Patent No. 6,414,868
command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks;	the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks. The signals received by the memory module 1000 from the computer system include a WE (write) signal. (The '912 patent identifies write and refresh signals, among others, as command signals. See, e.g., '912 patent, 8:45-60) As shown in FIG. 4B, below, the Bank Control Circuit 2000 (which is part of the logic element) receives one RAS0 signal (corresponding to one, the second number of ranks) and generates two or more RAS signals (corresponding to two, the first number of ranks).  Fig. 4B In addition, the bank control circuit 2000 receives "receive a row address strobe (RAS) signal and a column address strobe signal, and at least one address signal, wherein said bank control circuit is configured to selectively provide at least one corresponding RAS output signal to either said upper bank of memory chips or said lower bank of memory chips depending upon said address signal to thereby allow either said lower bank of memory chips or said upper bank of memory chips to be selectively accessed during a given memory operation" (Claim 1 of the '868 Patent)
and a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR	The use of a phase-lock loop device in memory modules was known to those of ordinary skill in the art at the time of the filing of the application that matured into the '912 Patent. For example, JEDEC Standard JESD-82 entitled "Definition of CDCV857 PLL Clock Driver for Registered DDR DIMM Applications" was published in July 2000. Furthermore, the inventor of the '912 Patent admitted that "Persons skilled in the art are able to select a phase-lock loop device 50 and a

Claim Element	Disclosure of U.S. Patent No. 6,414,868
memory devices, the logic element, and the register.	register 60 compatible with embodiments described herein." '912 Patent at 5:42-45.
18. The memory module of claim 15, wherein the command signal is transmitted to two ranks of the first number of ranks at a time.	The '868 Patent discloses the command signal being transmitted to two ranks of the first number of ranks at a time. "WEL and WEU are write enable signals driven by buffer 1003 to a lower memory bank 1022 and an upper memory bank 1012, respectively. CASL and CASU are CAS signals driven by buffer 1003 to the lower memory bank 1022 and upper memory bank 1012, respectively." (4:28-33)
19. The memory module of claim 18, wherein the command signal comprises a refresh command signal.	The '868 patent discloses the command signal comprising a refresh command signal. "The bank control circuit is further configured to drive RAS signals to both banks simultaneously during **CBR (CAS before RAS) refresh operations**, which occur when a CAS signal is asserted before a RAS signal." (Abstract) (emphasis added)
20. The memory module of claim 18, wherein the command signal is transmitted to the two ranks of the first number of ranks concurrently.	The '868 Patent discloses the command signal being transmitted to the two ranks of the first number of ranks concurrently. "The bank control circuit is further configured **to drive RAS signals to both banks simultaneously** during CBR (CAS before RAS) refresh operations, which occur when a CAS signal is asserted before a RAS signal." (Abstract) (emphasis added)
22. The memory module of claim 15, wherein the command signal comprises a read command signal or a write command signal, the set of input signals comprises a density bit which is a row address	The '868 Patent discloses the command signal comprising a read command signal or a write command signal, the set of input signals comprising a density bit which is a row address bit, and the circuit being configured to store the row address bit during an activate command for a selected bank. "3. The memory module as recited in claim 2, wherein said connector edge includes contact pads for receiving control signals, said control signals comprising at least one column address strobe (CAS) signal, at least one row address strobe (RAS) signal, and at least one write enable (WE) signal.

Claim Element	Disclosure of U.S. Patent No. 6,414,868
bit, and the circuit is configured to store the row address bit during an activate command for a selected bank.	4. The memory module as recited in claim 3, wherein said electrical signals include address signals, and, wherein said address signals form an address bus, and, wherein said address bus is at least 14 bits wide." (Claims 3 and 4) "When the bank control circuit is in an idle state, receiving a RAS signal will cause a memory access operation to begin. The bank of memory to be selected will depend on the logic level of the address input to the bank control circuit. The bank control circuit will then drive RAS signals to the selected memory bank, allowing a row address to be selected. When the memory chips of the selected bank receive a CAS signal, the column address is selected, and the requested memory address is accessed." (2:47-55)
24. The memory module of claim 15, wherein the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device.	The '868 Patent discloses the logic element comprising an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device. "In this embodiment, the bank control circuit is a programmable logic device (PLD), although this circuit may be implemented in other forms for different embodiments." 2:41-44.
25. The memory module of claim 15, wherein the set of input signals comprises a plurality of row/column address signals received and buffered by the register and sent from the	The '868 Patent discloses the set of input signals comprising a plurality of row/column address signals received and buffered by the register and sent from the register to the plurality of DDR memory devices. "When the bank control circuit is in an idle state, receiving a RAS signal will cause a memory access operation to begin. The bank of memory to be selected will depend on the logic level of the address input to the bank control circuit. The bank control circuit will then drive RAS signals to the selected memory bank, allowing a row address to be selected. When the memory chips of the selected bank receive a

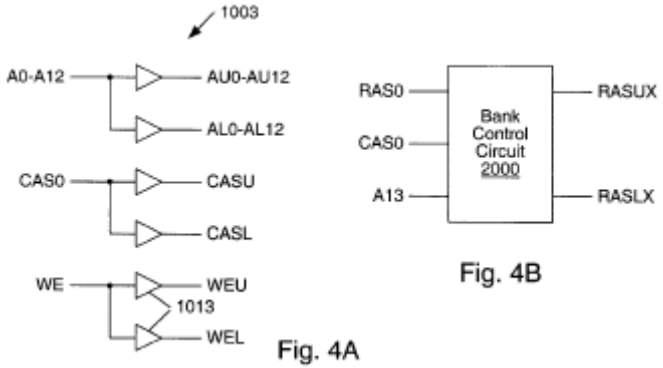
Claim Element	Disclosure of U.S. Patent No. 6,414,868
register to the plurality of DDR memory devices.	CAS signal, the column address is selected, and the requested memory address is accessed." (2:47-55) "Buffer 1003 receives signals WE (write enable), CAS0 (Column Address Strobe 0), and a plurality of address signals, shown as AX. Buffer circuit 1003 drives a plurality of address signals AXL and AXU, which are conveyed to the lower memory bank 1022 and upper memory bank 1012, respectively. WEL and WEU are write enable signals driven by buffer 1003 to a lower memory bank 1022 and an upper memory bank 1012, respectively. CASL and CASU are CAS signals driven by buffer 1003 to the lower memory bank 1022 and upper memory bank 1012, respectively." (4:23-30)
28. A memory module connectable to a computer system, the memory module comprising:	The '868 Patent discloses a memory module connectable to a computer system at 1:8-10: "This invention generally relates to memory hardware for computer systems, and more specifically to memory expansion modules for expanding memory in computer systems."
a printed circuit board;	The '868 Patent discloses a printed circuit board. "Turning now to FIG. 2, a diagram illustrating components associated with a memory module 1000 is shown. In this particular embodiment, a plurality of memory elements 1002, typically DRAM (Dynamic Random Access Memory) chips, are surface mounted upon a printed circuit board (PCB) 1001." (3:58-63)

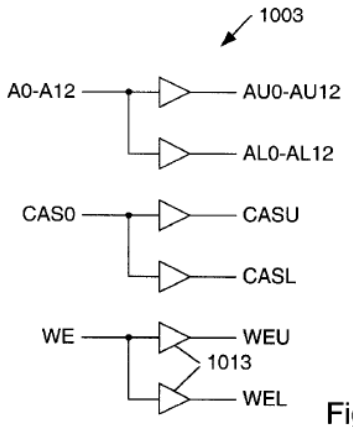
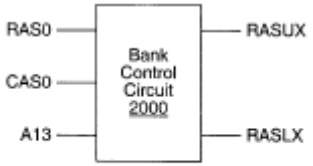
Claim Element	Disclosure of U.S. Patent No. 6,414,868
	 Fig. 2
a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices coupled to the printed circuit board, the plurality of DDR DRAM devices having a first number of DDR DRAM devices arranged in a first number of ranks;	The '868 Patent discloses a plurality of memory devices mounted to the printed circuit board. "Turning now to FIG. 2, a diagram illustrating components associated with a memory module 1000 is shown. In this particular embodiment, a plurality of memory elements 1002, typically DRAM (Dynamic Random Access Memory) chips, are surface mounted upon a printed circuit board (PCB) 1001." (3:58-63) "Memory module 1000 includes an edge connector 1005, a lower memory bank 1022, and upper memory bank 1012, a bank control circuit 2000 and a buffer 1003. Each memory bank includes of a plurality of memory chips 1002." (4:15-19) FIG. 3 shows the memory module 1000 with 18 memory devices 1002.

Claim Element	Disclosure of U.S. Patent No. 6,414,868
	 Fig. 3 One of ordinary skill in the art at the time the application that matured into the '912 Patent was filed would understand that DRAM memory chips could comprise double-data-rate (DDR) memory devices. For example, JEDEC Standard JESD-82 entitled "Definition of CDCV857 PLL Clock Driver for Registered **DDR** DIMM Applications" was published in July 2000. (emphasis added) FIG. 3, reproduced above, shows the memory devices arranged in two ranks, the lower 1022, and the upper 1012. The term "rank" in the claim has the same meaning as the term "bank" in Wong.
a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register,	The '868 Patent discloses a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register. The logic element includes the buffer 1003 and the bank control circuit 2000. (The buffer 1003 is also referred to as the buffer chip 1003 and the buffer circuit 1003.) The buffer can be considered a register because one of ordinary skill in the art would understand that buffering is what a register does. "Also mounted on PCB 1001 are a buffer chip 1003 . . . and a bank control circuit 2000." (4:7-9)

Claim Element	Disclosure of U.S. Patent No. 6,414,868
	"Turning now to FIG. 5, a schematic of one embodiment of the bank control circuit 2000 is shown. This particular embodiment of bank control circuit 2000 is a programmable logic device (PLD. (sic) In this embodiment, bank control circuit 2000 comprises a plurality of AND gates 2001, NAND gates 2002, inverters 2003, and flip-flops 2004 (D-type flip-flops in this embodiment). Bank control circuit 2000 drives multiple RAS signals for each memory bank in order to provide sufficient signal drive strength to each of the memory chips. The operation of the bank control circuit will be further illustrated in FIG. 6 and FIG. 7. It should be noted that alternative embodiments of the bank control circuit are possible using other types of electronic circuitry." (5:10-23)
the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising a row/column address signal, bank address signals, a chip-select signal, and an input command signal,	The '868 Patent discloses the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, a chip-select signal, and an input command signal. The buffer chip 1003 receives input control signals A0-A12, CAS0, and WE and the bank control circuit 2000 receives input control signals RAS0, CAS0, and A13 from a computer system to which the memory module is connected. The RAS signal in the '868 Patent is used as a chip-select signal. "[A] memory module includes a printed circuit board with a connector edge adapted for insertion in an expansion socket of a computer system." (Abstract) "Signals passing through the edge connector include data signals, address signals, and control signals." (3:58 –4:2) "In the embodiment shown, buffer chip 1003 receives a plurality of address signals, A0-A12, a CAS0 signal, and a WE signal." (4:44-46) "In this embodiment, bank control circuit 2000 receives input signals RAS0, CAS0, and address signal A13." (4:56-57) FIG. 3, reproduced above, shows the signals as being received from the computer

Claim Element	Disclosure of U.S. Patent No. 6,414,868
	system through electrical contact pads 1015. (4:19-21)
the set of input control signals configured to control a second number of DDR DRAM devices arranged in a second number of ranks, the second number of DDR DRAM devices smaller than the first number of DDR DRAM devices, the second number of ranks smaller than the first number of ranks,	The '868 Patent discloses the set of input control signals configured to control a second number of DDR DRAM devices arranged in a second number of ranks, the second number of DDR DRAM devices smaller than the first number of DDR DRAM devices, the second number of ranks smaller than the first number of ranks. The input control signals, which are received from the computer system, include 14 address signals (A0-A13) and one row access strobe (RAS) signal. The input control signals include only one row access strobe (RAS) signal, and therefore correspond to one rank (the second number) of memory devices. The second number of ranks, one, is less than the first number of ranks, which is two. "[The] presence of only one RAS and one CAS signal also limits the ability to expand system memory, as a separate bank of memory typically requires at minimum either a unique RAS or unique CAS signal for each bank." (2:3-7) "By using the bank control circuit to enable the addition of a second memory bank, a memory expansion can be realized without the need for higher capacity memory chips, which may result in an advantageous cost savings." (2:33-37) "The use of memory chips with a greater number of address inputs, and hence higher capacity, may disproportionately increase the cost of the desired memory expansion." (1:62-65) "Buffer 1003 receives . . . a plurality of address signals, shown as AX. Buffer circuit 1003 drives a plurality of address signals AXL and AXU, which are conveyed to the lower memory bank 1022 and upper memory bank 1012, respectively. . . . The bank control circuit 2000 is configured to receive an address signal A13 for selecting the upper and lower bank. Address signal A13, in this embodiment, is the most significant address bit of an address bus that is 14 bits wide." (4:23-37)

Claim Element	Disclosure of U.S. Patent No. 6,414,868
	"Address signal A13, in this embodiment [of FIG. 3], is the most significant address bit of an address bus that is 14 bits wide." (4:35- 37) The remaining address bits, A0 – A12, are designated "AX" in FIG. 3. As illustrated in FIGS. 3, 4A and 4B, address bits A0-A12 go through the buffer 1003 and are used to address the memory devices within a rank, unlike A13, which is used by bank control circuit 2000 to select the upper or lower rank of the memory module 1000.  Fig. 4A Fig. 4B
the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals comprising an output command signal, the set of output control signals configured to control the first number of DDR DRAM devices arranged	The '868 Patent discloses the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals comprising an output command signal, the set of output control signals configured to control the first number of DDR DRAM devices arranged in the first number of ranks. The buffer chip 1003 (which constitutes the logic element together with the bank control circuit) generates output control signals AU0-AU12, AL0-AL12, CASU, CASL, WEU, and WEL and the bank control circuit 2000 generates output control signals RASLX, and RASUX in response to the input control signals A0-A13, CAS0, RAS0, and WE. These signals control and therefore correspond to all the memory devices (the "first number of DDR memory devices arranged in the first

Claim Element	Disclosure of U.S. Patent No. 6,414,868
in the first number of ranks,	number of ranks") on the module. "FIG. 4A further illustrates an internal configuration of an embodiment of a buffer chip 1003. In the embodiment shown, buffer chip 1003 receives a plurality of address signals, A0-A12, a CAS0 signal, and a WE signal. The signals are passed through buffers 1013, generating corresponding signals that will be provided to an upper bank and a lower bank of memory chips." (4:43-49)  Fig. 4A "One embodiment of bank control circuit 2000 is shown in FIG. 4B. In this embodiment, bank control circuit 2000 receives input signals RAS0, CAS0, and address signal A13. Bank control circuit 2000 drives a plurality of RASLX and RASUX signals to the lower and upper memory banks, respectively." (4:55-60)  Fig. 4B
wherein the circuit	The '868 Patent discloses the circuit further responding to the set of input control

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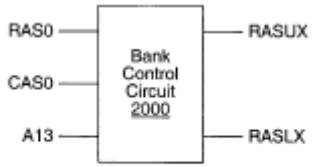
further responds to the set of input control signals from the computer system by selecting at least one rank of the first number of ranks and transmitting the set of output control signals to at least one DDR DRAM device of the selected at least one rank;	signals from the computer system by selecting at least one rank of the first number of ranks and transmitting the set of output control signals to at least one DDR DRAM device of the selected at least one rank. The signals received by the memory module 1000 from the computer system include a WE (write) signal. (The ’912 patent identifies write and refresh signals, among others, as command signals. See, e.g., ’912 patent, 8:44-60) As shown in FIG. 4B, below, the Bank Control Circuit 2000 (which is part of the logic element) receives one RAS0 signal (corresponding to one, the second number of ranks) and generates two or more RAS signals (corresponding to two, the first number of ranks).  Fig. 4B In addition, the bank control circuit 2000 receives “receive a row address strobe (RAS) signal and a column address strobe signal, and at least one address signal, wherein said bank control circuit is configured to selectively provide at least one corresponding RAS output signal to either said upper bank of memory chips or said lower bank of memory chips depending upon said address signal to thereby allow either said lower bank of memory chips or said upper bank of memory chips to be selectively accessed during a given memory operation” (Claim 1 of the ‘868 Patent)
and a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to	The use of a phase-lock loop device in memory modules was known to those of ordinary skill in the art at the time of the filing of the application that matured into the ‘912 Patent. For example, JEDEC Standard JESD-82 entitled “Definition of CDCV857 PLL Clock Driver for Registered DDR DIMM Applications” was published in July 2000. Furthermore, the inventor of the ‘912 Patent admitted that

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the plurality of DDR DRAM devices, the logic element, and the register.	"Persons skilled in the art are able to select a phase-lock loop device 50 and a register 60 compatible with embodiments described herein." '912 Patent at 5:42-45.
29. The memory module of claim 28, wherein the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device.	The '868 Patent discloses the logic element comprising an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device. "In this embodiment, the bank control circuit is a programmable logic device (PLD), although this circuit may be implemented in other forms for different embodiments." 2:41-44.
31. The memory module of claim 28, wherein the set of input control signals comprises fewer chip-select signals than does the set of output control signals.	The '868 Patent discloses the set of input control signals comprising fewer chip-select signals than does the set of output control signals. The RAS signal is an input control chip-select signal that comes into the bank control circuit. The RASU signal is an output control chip-select signal from the bank control circuit. As shown in the emphasized areas below, one RAS signal generates multiple RASU signals. "Operation of one embodiment of the bank control circuit is further illustrated with a state diagram in FIG. 7. When no memory access operations or refresh cycles are occurring, the bank control circuit is in an idle state 3001. **When the bank control circuit receives an active low RAS signal**, a memory access operation is initiated. Selection of the particular bank is dependent upon the state of address signal A13. For example, if A13 is a logic 0, the upper bank will be selected. **The bank control circuit will transition to state 3021 and drive RASU signals to DRAM chips in the upper bank.** When the DRAM chips of the upper bank receive the RAS signals, a row address is selected based on the address signals driven to them.

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	When the active low CAS signal is asserted, the system will transition to state 3022, where a column address is selected. The data from the upper bank is then active. At the end of the memory cycle, both the CAS and RAS signals are deasserted, and the system returns to idle state 3001. The sequence is identical, with the exception of the state A13, for lower bank access."
32. The memory module of claim 31, wherein the set of input control signals comprises two chip-select signals and the set of output control signals comprises four chip-select signals.	One of ordinary skill in the art would understand that in the invention of the '868 Patent, the set of input control signals could comprise two chip-select signals at the same time the set of output control signals comprised four chip-select signals. "While the present invention has been described with reference to particular embodiments, it will be understood that the embodiments are illustrative and that the invention scope is not so limited. Any variations, modifications, additions, and improvements to the embodiments described are possible. These variations, modifications, additions, and improvements may fall within the scope of the inventions as detailed within the following claims." (6:4-11)
34. The memory module of claim 28, wherein the first number of ranks is four and the second number of ranks is two.	One of ordinary skill in the art would understand that in the invention of the '868 Patent, the first number of ranks could be four and the second number of ranks could be two. "While the present invention has been described with reference to particular embodiments, it will be understood that the embodiments are illustrative and that the invention scope is not so limited. Any variations, modifications, additions, and improvements to the embodiments described are possible. These variations, modifications, additions, and improvements may fall within the scope of the inventions as detailed within the following claims." (6:4-11)
36. The memory module of claim 28, wherein the input command signal is a refresh signal and the output command signal is a refresh signal.	The '868 Patent discloses the input command signal being a refresh signal and the output command signal being a refresh signal. "The bank control circuit is further configured to drive RAS signals to both banks simultaneously during CBR (CAS before RAS) refresh operations, which occur when a CAS signal is asserted before a RAS signal." (Abstract)

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37. The memory module of claim 28, wherein the input command signal is a precharge signal and the output command signal is a precharge signal.	One of ordinary skill in the art at the time of filing of the application that matured into the '912 Patent would understand that the input command signal could be a precharge signal and the output command signal could be a precharge signal.
38. The memory module of claim 28, wherein the input command signal is a read signal or a write signal and the output command signal is a read signal or a write signal.	The '868 Patent discloses the input command signal being a read signal or a write signal and the output command signal being a read signal or a write signal. "**Buffer 1003 receives signals WE (write enable),** CAS0 (Column Address Strobe 0), and a plurality of address signals, shown as AX. Buffer circuit 1003 drives a plurality of address signals AXL and AXU, which are conveyed to the lower memory bank 1022 and upper memory bank 1012, respectively. **WEL and WEU are write enable signals driven by buffer 1003 to a lower memory bank 1022 and an upper memory bank 1012, respectively.**" (4:23-30)
39. A memory module connectable to a computer system, the memory module comprising:	The '868 Patent discloses a memory module connectable to a computer system at 1:8-10: "This invention generally relates to memory hardware for computer systems, and more specifically to memory expansion modules for expanding memory in computer systems."
a printed circuit board having a first side and a second side;	The '868 Patent discloses a printed circuit board having a first side and a second side. "Turning now to FIG. 2, a diagram illustrating components associated with a memory module 1000 is shown. In this particular embodiment, a plurality of memory elements 1002, typically DRAM (Dynamic Random Access Memory) chips, are surface mounted upon a printed circuit board (PCB) 1001." (3:58-63)

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	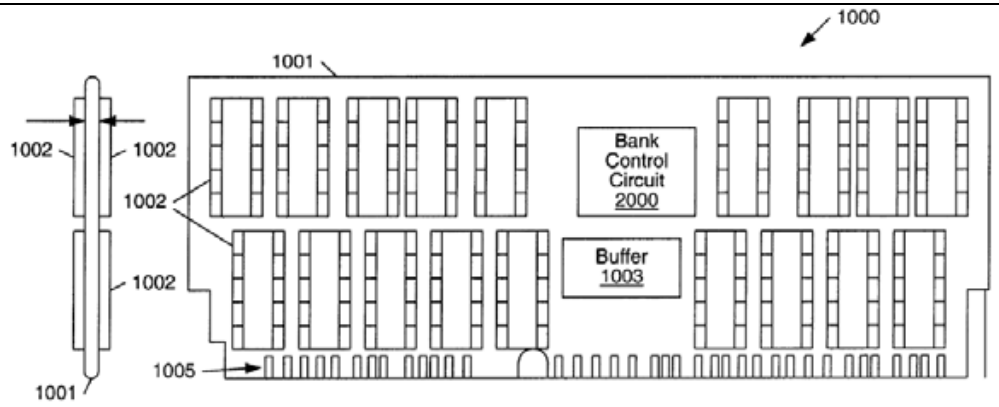 Fig. 2 "The circuit boards used to implement SIMMs and DIMMs include an edge connector comprising a plurality of contact pads, with contact pads typically being present on **both sides** of the circuit board." (1:18-21) (emphasis added)
a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, each DDR memory device comprising one or more banks, the plurality of DDR memory devices arranged in two or more ranks which are selectable by a first number of chip-select signals;	The '868 Patent discloses a plurality of memory devices mounted to the printed circuit board. "Turning now to FIG. 2, a diagram illustrating components associated with a memory module 1000 is shown. In this particular embodiment, a plurality of memory elements 1002, typically DRAM (Dynamic Random Access Memory) chips, are surface mounted upon a printed circuit board (PCB) 1001." (3:58-63) "Memory module 1000 includes an edge connector 1005, a lower memory bank 1022, and upper memory bank 1012, a bank control circuit 2000 and a buffer 1003. Each memory bank includes of a plurality of memory chips 1002." (4:15-19) The RAS signal in the '868 Patent is used as a chip-select signal. "One embodiment of bank control circuit 2000 is shown in FIG. 4B. In this embodiment, bank control circuit 2000 receives input signals RAS0, CAS0, and address signal A13. Bank control circuit 2000 drives a plurality of RASLX and RASUX signals to the lower and upper memory banks, respectively. Depending on

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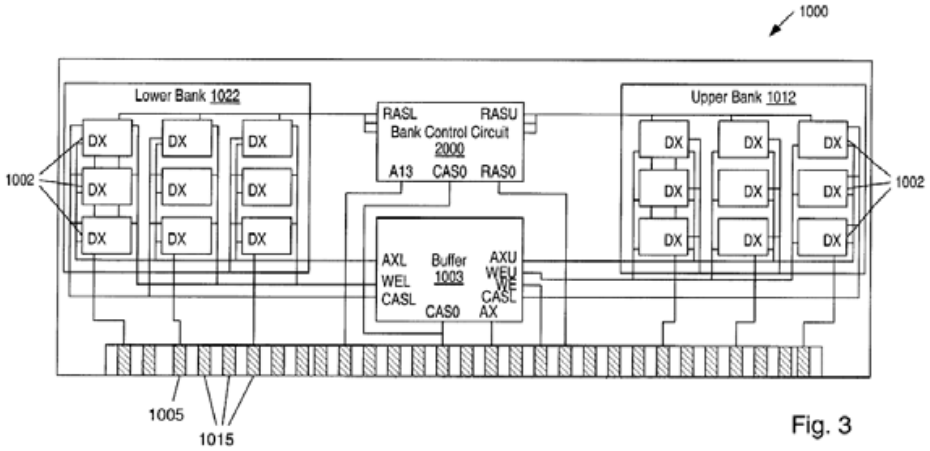
	the combination of inputs received by bank control circuit 2000, either the RASUX or RASLX signal groups can be asserted exclusively for memory access operations." (4:55-63) FIG. 3 shows the memory module 1000 with 18 memory devices 1002.  Fig. 3 One of ordinary skill in the art at the time the application that matured into the '912 Patent was filed would understand that DRAM memory chips could comprise double-data-rate (DDR) memory devices. For example, JEDEC Standard JESD-82 entitled "Definition of CDCV857 PLL Clock Driver for Registered **DDR** DIMM Applications" was published in July 2000. (emphasis added) FIG. 3, reproduced above, shows the memory devices arranged in two ranks, the lower 1022, and the upper 1012. The term "rank" in the claim has the same meaning as the term "bank" in Wong.
and at least one integrated circuit element mounted to the printed circuit board, the at least one integrated	The '868 Patent discloses at least one integrated circuit element mounted to the printed circuit board, the at least one integrated circuit element comprising a logic element, a register, and a phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register.

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circuit element comprising a logic element, a register, and a phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register,	The logic element includes the buffer 1003 and the bank control circuit 2000. (The buffer 1003 is also referred to as the buffer chip 1003 and the buffer circuit 1003.) The buffer can be considered a register because one of ordinary skill in the art would understand that buffering is what a register does. "Also mounted on PCB 1001 are a buffer chip 1003 . . . and a bank control circuit 2000." (4:7-9) "Turning now to FIG. 5, a schematic of one embodiment of the bank control circuit 2000 is shown. This particular embodiment of bank control circuit 2000 is a programmable logic device (PLD. (sic) In this embodiment, bank control circuit 2000 comprises a plurality of AND gates 2001, NAND gates 2002, inverters 2003, and flip-flops 2004 (D-type flip-flops in this embodiment). Bank control circuit 2000 drives multiple RAS signals for each memory bank in order to provide sufficient signal drive strength to each of the memory chips. The operation of the bank control circuit will be further illustrated in FIG. 6 and FIG. 7. It should be noted that alternative embodiments of the bank control circuit are possible using other types of electronic circuitry." (5:10-23) One of ordinary skill in the art would understand that these alternative embodiments could include an integrated circuit comprising the logic element, a register, and a phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register. The use of a phase-lock loop device in memory modules was known to those of ordinary skill in the art at the time of the filing of the application that matured into the '912 Patent. For example, JEDEC Standard JESD-82 entitled "Definition of CDCV857 PLL Clock Driver for Registered DDR DIMM Applications" was published in July 2000. Furthermore, the inventor of the '912 Patent admitted that "Persons skilled in the art are able to select a phase-lock loop device 50 and a register 60 compatible with embodiments described herein." '912 Patent at 5:42-45.
the at least one	The '868 Patent discloses the at least one integrated circuit element receiving a

Claim Element	Disclosure of U.S. Patent No. 6,414,868
integrated circuit element receiving a plurality of input signals from the computer system, the plurality of input signals comprising row address signals, column address signals, bank address signals, command signals, and a second number of chip-select signals less than the first number of chip-select signals, wherein the logic element receives the bank address signals and at least one command signal of the plurality of input signals,	plurality of input signals from the computer system, the plurality of input signals comprising row address signals, column address signals, bank address signals, command signals, and a second number of chip-select signals less than the first number of chip-select signals, wherein the logic element receives the bank address signals and at least one command signal of the plurality of input signals. The buffer chip 1003 receives input control signals A0-A12, CAS0, and WE and the bank control circuit 2000 receives input control signals RAS0, CAS0, and A13 from a computer system to which the memory module is connected. "[A] memory module includes a printed circuit board with a connector edge adapted for insertion in an expansion socket of a computer system." (Abstract) "Signals passing through the edge connector include data signals, address signals, and control signals." (3:58 –4:2) "In the embodiment shown, buffer chip 1003 receives a plurality of address signals, A0-A12, a CAS0 signal, and a WE signal." (4:44-46) "In this embodiment, bank control circuit 2000 receives input signals RAS0, CAS0, and address signal A13." (4:56-57) FIG. 3, reproduced above, shows the signals as being received from the computer system through electrical contact pads 1015. (4:19-21)
the at least one integrated circuit element generating a plurality of output signals in response to the plurality of input signals, the plurality of output signals comprising row address signals, column address signals, bank address signals,	The '868 Patent discloses the at least one integrated circuit element generating a plurality of output signals in response to the plurality of input signals, the plurality of output signals comprising row address signals, column address signals, bank address signals, command signals, and the first number of chip-select signals. The buffer chip 1003 (which constitutes the logic element together with the bank control circuit) generates output control signals AU0-AU12, AL0-AL12, CASU, CASL, WEU, and WEL and the bank control circuit 2000 generates output control signals RASLX, and RASUX in response to the input control signals A0-A13, CAS0, RAS0, and WE. These signals control and therefore correspond to all the memory devices (the "first number of DDR memory devices arranged in the first

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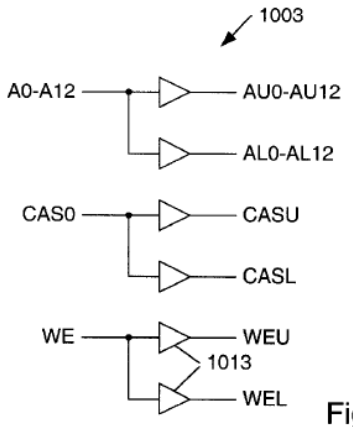
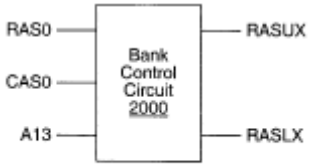
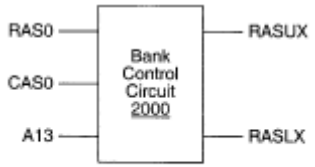
command signals, and the first number of chip-select signals,	number of ranks") on the module. "FIG. 4A further illustrates an internal configuration of an embodiment of a buffer chip 1003. In the embodiment shown, buffer chip 1003 receives a plurality of address signals, A0-A12, a CAS0 signal, and a WE signal. The signals are passed through buffers 1013, generating corresponding signals that will be provided to an upper bank and a lower bank of memory chips." (4:43-49)  Fig. 4A "One embodiment of bank control circuit 2000 is shown in FIG. 4B. In this embodiment, bank control circuit 2000 receives input signals RAS0, CAS0, and address signal A13. Bank control circuit 2000 drives a plurality of RASLX and RASUX signals to the lower and upper memory banks, respectively." (4:55-60)  Fig. 4B
the at least one	The '868 Patent discloses the at least one integrated circuit element further

Claim Element	Disclosure of U.S. Patent No. 6,414,868
integrated circuit element further responsive to the plurality of input signals by selecting at least one rank of the two or more ranks and transmitting the plurality of output signals to at least one DDR memory device of the selected at least one rank.	responsive to the plurality of input signals by selecting at least one rank of the two or more ranks and transmitting the plurality of output signals to at least one DDR memory device of the selected at least one rank. The signals received by the memory module 1000 from the computer system include a WE (write) signal. (The ’912 patent identifies write and refresh signals, among others, as command signals. See, e.g., ’912 patent, 8:45-60) As shown in FIG. 4B, below, the Bank Control Circuit 2000 (which is part of the logic element) receives one RAS0 signal (corresponding to one, the second number of ranks) and generates two or more RAS signals (corresponding to two, the first number of ranks).  Fig. 4B In addition, the bank control circuit 2000 receives “receive a row address strobe (RAS) signal and a column address strobe signal, and at least one address signal, wherein said bank control circuit is configured to selectively provide at least one corresponding RAS output signal to either said upper bank of memory chips or said lower bank of memory chips depending upon said address signal to thereby allow either said lower bank of memory chips or said upper bank of memory chips to be selectively accessed during a given memory operation” (Claim 1 of the ‘868 Patent)
41. The memory module of claim 39, wherein the at least one integrated circuit element comprises one or more	The ‘868 Patent discloses the at least one integrated circuit element comprising one or more integrated circuit elements selected from the group consisting of: an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, and a complex programmable-logic device. “In this embodiment, the bank control circuit is a programmable logic device

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integrated circuit elements selected from the group consisting of: an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, and a complex programmable-logic device.	(PLD), although this circuit may be implemented in other forms for different embodiments." 2:41-44.
50. The memory module of claim 39, wherein the at least one integrated circuit element is configured to respond to the plurality of input signals by selecting at least one rank of the two or more ranks and transmitting a command signal to at least one DDR memory device of the selected at least one rank.	The '868 Patent discloses the at least one integrated circuit element being configured to respond to the plurality of input signals by selecting at least one rank of the two or more ranks and transmitting a command signal to at least one DDR memory device of the selected at least one rank. "A block diagram illustrating the electrical connections associated with one embodiment of the memory module is shown in FIG. 3. Memory module 1000 includes an edge connector 1005, a lower memory bank 1022, and upper memory bank 1012, a bank control circuit 2000 and a buffer 1003. Each memory bank includes of a plurality of memory chips 1002. The edge connector 1005 includes a plurality of electrical contact pads 1015 which convey signals between the memory module and the system memory bus. Edge connector 1005 is adapted for mounting in a socket within a computer system. Buffer 1003 receives signals WE (write enable), CAS0 (Column Address Strobe 0), and a plurality of address signals, shown as AX. Buffer circuit 1003 drives a plurality of address signals AXL and AXU, which are conveyed to the lower memory bank 1022 and upper memory bank 1012, respectively. WEL and WEU are write enable signals driven by buffer 1003 to a lower memory bank 1022 and an upper memory bank 1012, respectively. CASL and CASU are CAS signals driven by buffer 1003 to the lower memory bank 1022 and upper memory bank 1012, respectively. The bank control circuit

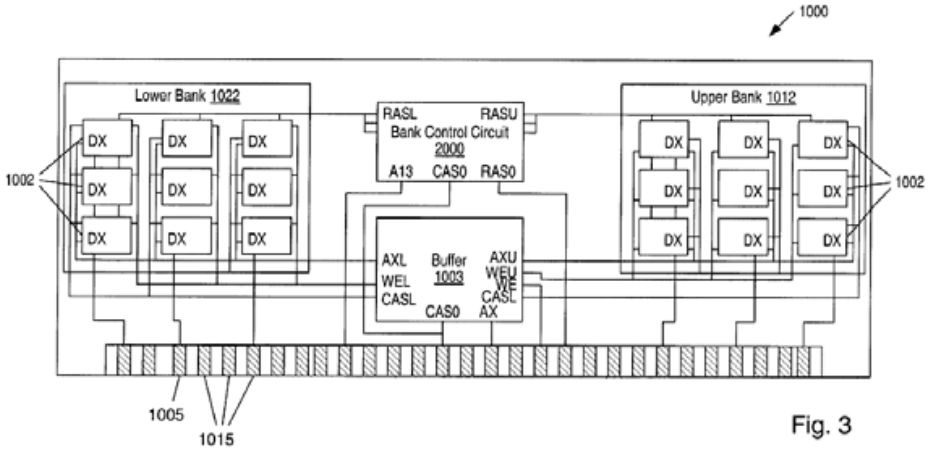
Claim Element	Disclosure of U.S. Patent No. 6,414,868
	2000 is configured to receive an address signal A13 for selecting the upper and lower bank." 4:13-35  Fig. 3

Exhibit 14: Invalidity under 35 U.S.C. § 112

Claim 1 of the ‘912 Patent recites in relevant part “the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks.” The ’912 patent does not contain any disclosure relating to generation of a set of output control signals that corresponds to the first number of ranks (which is the number of ranks on the printed circuit board). Instead, the ’912 patent discloses only that the circuit generates a command signal that is sent to an individual rank or ranks selected by the circuit, and does not “correspond to” any number of ranks at all, under any interpretation of the word “correspond.”

Not only is there a lack of support in the ‘912 specification for the claimed element, but also the claimed invention is not supported in the Figures presented as required under 37 CFR § 1.83 and MPEP § 608.02(d). The testimony of Dr. Turley in the '386 litigation has confirmed that there is no illustration that shows the claimed element of a second control signal that corresponds to the first number of ranks. Dr. Turley stated that command signals are not shown at all in Figure 1A and B and to the extent that they are shown as Column address strobe (CAS) signals in Figure 3, they do not correspond to the first number of ranks since they address only one rank each. Turley Rough Dep. Trans. at 121:13-123:3. The ’912 patent does not show that the inventors of the ’912 patent were in possession of the claimed invention at the time the patent was issued, nor does it enable a person of skill in the art to make and use the claimed invention without undue experimentation. Therefore, at least claim 1 is invalid for lack of written description and/or enablement under 35 U.S.C. § 112 ¶ 1 as interpreted by MPEP §§ 2161, 2162, 2163.01, 2163.02, 2163.03, 2164 and 2164.08.