

Exhibit A

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Page 2

1 Videotaped deposition of RICHARD TURLEY, Ph.D.,
2 held at the offices of:

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4
5 King & Spalding, LLP
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14 Pursuant to notice, before Dianna C. Kilgalen,
15 Registered Professional Reporter and Notary Public
16 for the District of Columbia.

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A P P E A R A N C E S

ON BEHALF OF THE PLAINTIFF:

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ALSO PRESENT:

DANA CAMPBELL, Videographer

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1 Q. What is your -- what are your issues with
2 Ludwig versus the 386 patent?

3 A. The Ludwig patent doesn't talk about memory
4 modules in the way that they are defined in the 386
5 patent. The Ludwig patent talks about replacing
6 individual devices with a collection of devices. So it
7 would be akin to row placing an individual DRAM device
8 within the memory module with a Ludwig-style device.
9 So they are talking about two very, very different
10 things, if you will. That is my first issue with it.

11 Let's see what else I have. So it,
12 therefore, doesn't discuss ranks. It's talking about
13 individual chips and replacing one chip with a stack of
14 chips. Therefore, there can be no concept of a
15 collection of memory devices in the sense of a rank.

16 MR. PERRY: Okay. Let's -- I don't want to
17 spend a lot of time on that one.

18 THE WITNESS: Okay.

19 (Whereupon, Turley Deposition Exhibit 14 was
20 marked for identification and attached to the
21 transcript.)

22 BY MR. PERRY:

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1 Q. Let me show you what I have just marked as
2 Exhibit 14, which is a copy of the United States patent
3 6,961,281 to Wong, et al, entitled Single Rank Memory
4 Module for Use in a Two Rank Memory Module System,
5 bearing production numbers GNET 001298 through -109.
6 Have you seen a copy of this before?

7 A. Yes, I have.

8 Q. What are your issues with the Wong 281 patent
9 versus the 386 patent?

10 A. Wong's disclosure -- this particular Wong
11 disclosure talks about using fewer ranks in place of a
12 greater number of ranks. So it's essentially the
13 opposite situation from what we have been describing in
14 the 386 patent. So it's going in the wrong direction,
15 if you will, or it's teaching away from the particular
16 teachings of the 386 patent.

17 Let's see what else I have here. I think
18 like the Dell 74 patent, this is -- I'm sorry. Hold
19 on. I'm on the wrong section. The logic element, to
20 the extent that there is a logic element in this, does
21 not generate commands.

22 Q. What are you referring to as the logic

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1 element in the 281 patent, Exhibit 14?

2 A. Let's see. So what I understand it to be is
3 the element labeled a control circuit, which in
4 Figure 3 would be number 330. Let's see if it is
5 elsewhere. So it is generating chip select and
6 address 12 signals based upon its inputs. Again, not
7 generating command signals.

8 Q. One of ordinary skill in the art seeing
9 Figure 3 and the accompanying disclosure going from two
10 inputs to one output, doesn't that allow the person of
11 ordinary skill to go from one to two fairly easily?

12 A. I don't think so.

13 Q. Why not?

14 A. Providing fewer address signals is much
15 easier than providing additional address signals than
16 would otherwise be required.

17 Q. But you have command signals coming out of
18 the buffer 320 --

19 A. Correct.

20 Q. -- going to each of the memory elements,
21 correct?

22 A. Correct.

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1 Q. Would you characterize those as command
2 signals?

3 A. Yes. In particular, referring to the RAS and
4 the write enable signals and the CAS signal.

5 Q. And out of the control circuit 330, you have
6 the chip select signal, correct?

7 A. Correct.

8 Q. And that goes to the entirety of the output
9 of devices -- of the memory devices, I should say?

10 A. I need to look in detail and see exactly how
11 that's connected, if I may.

12 MR. PERRY: Sure.

13 A. Figure 3. It appears it is applied to all
14 the memory elements and banks, the element that is
15 called -- labeled bank 0.

16 Q. So you have command signals going to all of
17 them, and you have the chip selects going to all of
18 them, correct?

19 A. Correct.

20 Q. What does AD12 refer to?

21 A. I'm presuming it refers to an address bit,
22 bit number 12.

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1 Q. Do you know if that is the highest order
2 address bit?

3 A. No, it is not.

4 Q. Do you know how AD12 is being used?

5 A. I need to check. So on the top of Column 7,
6 the patent states: Further since address signals AD12
7 and AD13 are used as memory device internal bank select
8 signals BS0 and BS1, an AD12 signal must be generated
9 on memory module 100B.

10 So that would imply to me that address signal
11 AD12 is used as memory device signal BS0.

12 Q. So out of the control circuit 330 in
13 Figure 3, you have got a chip select and effectively a
14 bank select coming out as AD12, correct?

15 A. Correct, bank select 0.

16 Q. That allows you to, then, not only select
17 what specific memory device but also the bank within
18 the memory device?

19 A. Well, I believe, if I'm reading this diagram
20 correctly, their bank relates not to the internal bank
21 definition that we have been using earlier of DRAM
22 devices, but rather to a collection of DRAM devices.

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1 Q. So bank would more likely be associated with
2 our use of rank?

3 A. With our use of rank, correct.

4 Q. So you have got a chip select signal and rank
5 select signal coming out, effectively?

6 MR. HANSEN: Objection. Mischaracterizes
7 testimony.

8 A. Well, the chip select signal is selecting
9 bank 0, or as we are calling it rank 0. The chip
10 select enables each of those memory devices 310.

11 BY MR. PERRY:

12 Q. And the AD12 signal is then doing what?

13 A. That is a good question. I need to read
14 further to find out how BS0 is used. Well, I think
15 that AD12 would also be selecting or deselecting
16 bank 0, based upon this definition, that AD12 is
17 equated to the bank select 0 bit.

18 BY MR. PERRY:

19 Q. This patent also describes, and actually
20 illustrates, a serial presence device, correct?

21 A. Yes, it does.

22 Q. And that serial presence device is connected

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1 then different kinds -- many different kinds of DRAM.

2 Q. And so we know we are on the same page here,
3 what is your understanding of the definition of a bank
4 as used in the context of memory in the 386 patent?

5 MR. HANSEN: Objection. Assumes facts not in
6 evidence.

7 A. I don't think the 386 patent directly
8 addresses ranks as a discussion topic. It addresses it
9 from the perspective of providing bank address
10 information.

11 BY MR. PERRY:

12 Q. When you say it doesn't address rank, you
13 meant bank?

14 A. Did I say rank?

15 MR. PERRY: Yes.

16 A. Oh, my goodness. I'm sorry. I don't think
17 it addresses -- discusses banks, per se, other than to
18 the extent that it defines the number of bank address
19 bits that are used to access a device -- a memory
20 device.

21 Q. Outside of the 386, what do you understand a
22 bank to be in memory?

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1 A. I understand a bank to be a subunit or a
2 subaddressable unit of a memory device. So a given
3 memory device is organized into a set of banks.

4 Q. Could a bank actually consist of portions of
5 more than one memory device?

6 A. Not that I'm aware of.

7 MR. PERRY: Okay.

8 A. Let me just qualify that. That's based upon
9 my general knowledge and understanding of DRAM devices,
10 not in the context of the 386 patent, because I don't
11 think it mentions that at all.

12 Q. And can the memory devices that are -- or --
13 well, strike that. Your position is that you can't
14 have a bank that consists of more than one memory
15 device, correct?

16 A. A bank is internal to a memory device. So,
17 therefore, a bank by definition, could not -- again, in
18 the context of my general knowledge of DRAM devices.
19 So a bank cannot span multiple memory devices.

20 Q. When you say can't span multiple DRAM
21 devices -- strike that. When you say it can't span
22 multiple devices, are you talking about devices being

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1 DRAMs or RAM?

2 A. So I'm specifically talking about DRAM
3 devices, and just in general, DRAM devices in general,
4 not in the context of any patent or technology that
5 we've talked about. The definition, as I understand a
6 bank, is that it is a subelement of a memory device
7 and, therefore, would be -- would not be capable of
8 spanning multiple memory devices.

9 Q. If I were to take off the limitation -- if
10 there was a limitation -- to DRAM devices, is there
11 anything that you understand a bank to be within a
12 normal memory device?

13 A. Banks are, as a construct -- I'm only
14 familiar with them in the context of a DRAM device. So
15 the RAM devices that I have looked at, for example,
16 were not organized into banks.

17 Q. Now, we talked a little bit before about this
18 word generating --

19 A. Yes.

20 Q. -- in the claim. As soon as I find my
21 patent, I will get back to that. Oh, boy. Here we
22 go. Do you understand the word generating here to have