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IN THE UNITED STATES DISTRICT COURT
FOR THE NORTHERN DISTRICT OF CALIFORNIA

U.S. ETHERNET INNOVATIONS, LLC,

Plaintiff,

v.

ACER, INC., et al.,

Defendants.

and

ATHEROS COMMUNICATIONS, INC., et
al.,

Intervenors.

No. C 10-3724 CW

ORDER ON SUMMARY
JUDGMENT MOTIONS

(Docket Nos. 1133
and 1167)

U.S. ETHERNET INNOVATIONS, LLC,

Plaintiff,

v.

AT&T MOBILITY, LLC, et al.,

Defendants.

No. C 10-5254 CW

ORDER ON SUMMARY
JUDGMENT MOTIONS

In this consolidated patent infringement case, Plaintiff U.S. Ethernet Innovations, LLC (USEI) moves for summary judgment on a number of discrete issues: infringement of claim 21 of the '872 patent against Intel, Intel's intentional copying of the patented inventions, validity of the '872 and '094 patents in view of the SONIC prior art reference, and Defendants' claims of inequitable

1 conduct.¹ Defendants and Intervenor (collectively, Defendants)
2 oppose the motion and affirmatively move for summary judgment on
3 the issues of damages, non-infringement of the '313 patent,
4 anticipation of certain claims of the '872 and '094 patents by the
5 Intel 82593 prior art reference, anticipation of all asserted
6 claims of the '872 and '094 patents by the SONIC prior art
7 reference, non-infringement of the '459 patent, invalidity of
8 certain '313 and '459 patent claims under § 112, and issues
9 specific to AT&T Services (ATTS), Marvell (MSI), Apple, and
10 Atheros/Sigma/ATTS. The motions were heard on August 14, 2014.
11 Having considered the parties' submissions and the arguments of
12 counsel, the Court grants some motions and denies others, and
13 grants some motions in part.
14

15 BACKGROUND

16 3Com Corporation, USEI's predecessor-in-interest, developed
17 ethernet technology in the 1980s and 1990s. In the early 1990s,
18 3Com obtained the four patents-in-suit: U.S. Patent Nos. 5,434,872
19 (the '872 patent) (Apparatus for automatic initiation of data
20 transmission), 5,732,094 (the '094 patent) (Method for automatic
21 initiation of data transmission), 5,307,459 (the '459 patent)
22 (Network adapter with host indication optimization), and 5,299,313
23 (the '313 patent) (Network interface with host independent buffer
24 management).
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27 ¹ Defendants have withdrawn their inequitable conduct claims.
28 Thus, the Court need not address this issue.

1 The patents-in-suit relate to the field of network interface
2 controllers/adapters for managing the transmission and reception
3 of data between a host computer system and a communication
4 network. '313 patent, Field of the Invention. Typically, these
5 controllers manage the transfer of data between the host computer
6 system and the communication network, relieving the host computer
7 to perform other tasks. Id., Description of Related Art. Using
8 such a network controller, a sender may transmit "packets" or
9 "frames" of data across a communication network. '872 patent,
10 Description of Related Art. The frames of data must be organized
11 according to the network "protocol" before transmission. Id.
12 Some network adapters include dedicated transmit buffers, which
13 can download data of a frame before they are transmitted. Id. A
14 dedicated transmit buffer allows the host computer system to
15 attend to other tasks while the data frame is being processed and
16 transmitted. Id. If frame transmission is cancelled, the data
17 may be retained in the transmit data buffer until the sending
18 system tries to transmit the frame again. Id.

19 On October 9, 2009, USEI filed suit in the Eastern District
20 of Texas against sixteen computer maker defendants,² alleging that
21 they were manufacturing and selling desktop and laptop computers
22

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25 ² Acer, Inc., Acer America Corporation, Apple, Inc., ASUS
26 Computer International, Asustek Computer, Inc., AT&T Services,
27 Inc., Dell, Inc., Fujitsu Ltd., Fujitsu America, Inc., Gateway,
28 Inc., Hewlett Packard Co., Sony Corporation, Sony Corporation of
America, Sony Electronics, Inc., Toshiba Corporation, Toshiba
America, Inc., and Toshiba America Information Systems, Inc.

1 which incorporated chips supplied by others that practice certain
2 ethernet technology, thereby infringing the four patents-in-suit.
3 That case was subsequently transferred to this district and given
4 Case No. 10-3724 (the Acer case). On March 10, 2010, USEI filed a
5 separate suit in the Eastern District of Texas against the
6 retailer Defendants,³ alleging infringement of the same four
7 patents-in-suit. That case was subsequently transferred to this
8 district and given Case No. C 10-5254 (the AT&T case). Chip
9 suppliers, including Intel, Marvell, Atheros, and Sigma, who
10 designed and provided chips to Defendants, successfully moved to
11 intervene in both cases. The cases against the retailer
12 Defendants and ATTS were stayed.

14 The Court has issued two claim construction orders. See Case
15 No. C 10-3724, Docket Nos. 586 and 634; Case No. C 10-5254, Docket
16 Nos. 331 and 379.

18 LEGAL STANDARDS

19 Summary judgment is appropriate only where the moving party
20 demonstrates there is no genuine dispute as to any material fact
21 such that judgment as a matter of law is warranted. Fed. R. Civ.
22 P. 56(a); Celotex Corp. v. Catrett, 477 U.S. 317, 323 (1986).
23 Material facts are those that might affect the outcome of the
24 case, as defined by the framework of the underlying substantive
25

26 ³ AT&T, Inc., Barnes & Noble, Inc., Claire's Stores, Inc.,
27 J.C. Penney Company, Inc., Sally Beauty Holdings, Inc., and Home
28 Depot U.S.A., Inc.

1 law. Anderson v. Liberty Lobby, Inc., 477 U.S. 242, 248 (1986).

2 A dispute is genuine if the evidence is such that a reasonable
3 jury could return a verdict for either party. Id.

4 The moving party bears the initial burden of informing the
5 district court of the basis for its motion and identifying those
6 portions of the pleadings, discovery, and affidavits that
7 demonstrate the absence of a disputed issue of material fact.
8 Celotex, 477 U.S. at 323. In opposing the motion, the non-moving
9 party may not rely merely on the allegations or denials in its
10 pleadings, but must set forth "specific facts showing that there
11 is a genuine issue for trial." Anderson, 477 U.S. at 248 (citing
12 Fed. R. Civ. P. 56(e)). The court must construe the evidence in
13 the light most favorable to the non-moving party, making all
14 reasonable inferences that can be drawn. Matsushita Elec. Indus.
15 Co., Ltd. v. Zenith Radio Corp., 475 U.S. 574, 587 (1986); Intel
16 Corp. v. Hartford Accident & Indem. Co., 952 F.2d 1551, 1558 (9th
17 Cir. 1991); Eisenberg v. Ins. Co. of N. Am., 815 F.2d 1285, 1289
18 (9th Cir. 1987).

21 DISCUSSION

22 I. Anticipation of the asserted claims of the '872 and '094
23 patent by the SONIC prior art reference

24 A. USEI's motion

25 USEI moves for summary adjudication that the SONIC reference
26 cannot anticipate the '872 and '094 patents (the "Early Transmit"
27 patents), because it lacks a buffer memory of a certain minimum
28

1 size as required by the balance of the claim language. Defendants
2 disagree, and cross-move for summary judgment that the asserted
3 claims are anticipated by the SONIC prior art.

4 Patents are presumed valid, and the presumption may only be
5 overcome by clear and convincing evidence. Microsoft Corp. v. i4i
6 Ltd. P'ship, 131 S. Ct. 2238, 2252 (2011). "The burden of
7 establishing invalidity of a patent . . . shall rest on the party
8 asserting such invalidity." 35 U.S.C. § 282(a). Title 35 U.S.C.
9 § 102 establishes the various grounds for invalidation of patents
10 based on anticipation by prior art. "Anticipation requires the
11 presence in a single prior art disclosure of all elements of a
12 claimed invention arranged as in the claim." Therasense, Inc. v.
13 Becton, Dickinson and Co., 593 F.3d 1325, 1333 (Fed. Cir. 2010)
14 (quoting Connell v. Sears, Roebuck & Co., 722 F.2d 1542, 1548
15 (Fed. Cir. 1983)).

16
17
18 There is no dispute that SONIC is prior art pursuant to 35
19 U.S.C. § 102. SONIC is referred to in the Description of Related
20 Art sections of the '872 and '094 patents as "representative prior
21 art." There is also no dispute that the SONIC device contains a
22 thirty-two byte buffer memory, not big enough to hold the smallest
23 ethernet data frame, which is sixty-four bytes in size.

24
25 USEI contends that the plain language of the '872 and '094
26 patents demonstrates that the buffer memory must be big enough to
27 hold an entire ethernet frame. For example, USEI points to claim
28 1 of the '872 patent, which calls for: "initiating transmission of

1 the frame prior to transfer of all the data of the frame to the
2 buffer memory from the host computer." USEI then points to claim
3 21, which requires "logic which initiates transmission of the
4 frame from the buffer memory to the medium access controller prior
5 to transfer of all of the data of the frame from the buffer
6 memory, including logic which initiates transmission of the frame
7 when no complete frame of data is present in the buffer memory."
8 USEI finally refers to the Court's construction of "buffer memory"
9 as "memory for the temporary storage of data" to argue that, taken
10 as a whole, the buffer memory of the patented invention must be
11 capable of holding a complete minimum-sized ethernet data frame
12 from the host computer "all at one time."

14 USEI's argument is unpersuasive. First, the plain language
15 of the claims says nothing about the buffer memory's ability to
16 hold a complete frame of data. Instead, it states more or less
17 the opposite -- that a complete frame need not be downloaded into
18 buffer memory before transmission can occur. The claim language
19 USEI points out supports only the notion that a complete download
20 of a frame need not occur. In other words, the language does not
21 require that the buffer memory have the capacity to store all of
22 the data of a frame at once, only that the transmission of the
23 frame away from the buffer memory is initiated before all of the
24 data of the frame is fully transferred to the buffer memory.

25 USEI's own evidence of the specification, noting the disadvantages
26 of prior art using a dedicated transmit buffer that accommodated a
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1 full data frame, actually undermines USEI's contention; if the
2 specification criticized the use of full frame capacity, that
3 would indicate that the invention itself did not require full
4 frame capacity.

5 Moreover, the Court construed the term "buffer memory" to
6 mean "a memory for temporary storage of data" and did not impose
7 any extraneous storage requirements on buffer memory. USEI
8 previously made a similar argument that "the buffer memory is able
9 to retain a frame of data that has been transmitted." The Court
10 rejected this argument, finding that such additional language
11 would add a limitation that is not required by the specification.
12 Docket No. 586 at 21. Similarly, USEI's present attempt to infer
13 a size requirement is simply not justified by the claim language,
14 the specification, or any other evidence.

15
16 USEI does not present any evidence to support a finding that
17 SONIC does not anticipate the '872 and '094 patents. Therefore,
18 summary judgment for USEI on this point is not warranted.
19 Instead, as will be discussed below, summary adjudication of the
20 issue is granted for Defendants.

21
22 B. Defendants' cross motion

23 Because Defendants also move affirmatively that SONIC
24 anticipates the asserted claims of the '872 and '094 patents, the
25 Court turns to the other arguments they advance, all of which they
26 must prove by clear and convincing evidence in order to prevail.
27
28 Microsoft Corp., 131 S. Ct. at 2252-53.

1 To show anticipation, Defendants refer to Dr. Wicker's
2 report, which provides invalidity analysis and invalidity claim
3 charts that detail element-by-element how SONIC satisfies each and
4 every asserted claim limitation in the '872 and '094 patents. See
5 Constant Decl. Ex. 14, Wicker Rpt. at ¶¶ 554-675, Exhs 9, 11.
6 This evidence is largely unrefuted by USEI. USEI instead pins its
7 substantive defense on its contention that the balance of the
8 claim language imposes a lower limit on the buffer memory capacity
9 -- that the buffer memory, as claimed, must be large enough to
10 hold a full-size ethernet data frame, which has a minimum size of
11 sixty-four bytes; SONIC's thirty-two byte buffer memory cannot
12 satisfy the "buffer memory" limitation as claimed. In essence,
13 USEI does not dispute any relevant facts regarding the alleged
14 anticipating SONIC prior art, but only disagrees over an
15 interpretation of the claim language. This renders the
16 anticipation issue one of claim construction, which is a question
17 of law. Markman v. Westview Instruments, Inc., 517 U.S. 370, 384
18 (1996).
19
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21 After reviewing the claim language and the specification, the
22 Court finds no justification to require that the "buffer memory"
23 of the "Early Transmit" patents be capable of holding of a
24 complete minimum-sized ethernet data frame all at one time. As
25 the Court detailed above, the plain language of the claims says
26 nothing about the buffer memory's ability to hold a complete frame
27 of data. Instead, it states that a complete frame need not be
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1 downloaded into buffer memory before transmission can occur.
2 Nothing in the specification contradicts this understanding.
3 Accordingly, the Court grants Defendants' motion for summary
4 adjudication that SONIC anticipates the asserted claims of the
5 '872 and '094 patents. Because the Court finds that the asserted
6 claims of the '872 patent are invalid due to anticipation by the
7 SONIC prior art, the Court need not decide USEI's motion for
8 summary judgment of infringement of claim 21 of the '872 patent.
9

10 II. Whether Intel intentionally copied the patented invention,
11 precluding any equitable defense

12 USEI contends that ample evidence exists to show that Intel
13 copied the patented technology, which should prevent Intel from
14 asserting any equitable defense. See, e.g., A.C. Aukerman Co. v.
15 R.L. Chaides Constr. Co., 960 F.2d 1020, 1033 (Fed. Cir. 1992) ("A
16 patentee may also defeat a laches defense if the infringer 'has
17 engaged in particularly egregious conduct which would change the
18 equities significantly in plaintiff's favor.' Conscious copying
19 may be such a factor weighing against the defendant.") USEI
20 presents evidence that Intel began testing and discussing 3Com's
21 ethernet technology in 1992. For example, USEI has proffered
22 internal Intel emails discussing the value of these accused
23 infringing technologies and how they might be implemented in
24 upcoming products. See Nation Decl. Exs. E., F.

25
26 Intel disagrees, arguing that USEI's allegations concern the
27 copying of a 3Com product (the Etherlink III) that USEI's own
28

1 experts could not even identify or describe, much less compare to
2 the asserted claims. Further, Intel contends that USEI's experts
3 never compared the asserted claims to the Intel product (the
4 82595TX) that was alleged to be the result of Intel's intentional
5 copying.

6 In order to establish that Intel intentionally copied the
7 patented inventions, USEI must first show that the product
8 allegedly copied by Intel embodied the asserted claims. Without
9 such a showing, the allegations of copying are irrelevant. See,
10 e.g., Amazon.com, Inc. v. Barnesandnoble.com, Inc., 239 F.3d 1343,
11 1366 (Fed. Cir. 2001) ("[E]vidence of copying Amazon's '1-Click'
12 feature is legally irrelevant unless the '1-click' feature is
13 shown to be an embodiment of the claims.").

14 The proffered internal Intel emails refer to "Parallel
15 Tasking," a 3Com marketing term describing a commercial product
16 (the "EtherLink III" adapter) that 3Com released in 1992. USEI
17 fails to provide any evidence to show that the "Parallel Tasking"
18 EtherLink III adapter embodies each and every element of the
19 asserted claims or practices them. USEI's experts admit that they
20 have not looked into whether the EtherLink III practiced any of
21 the asserted claims. See Constant Decl. Ex. 6, Mitzenmacher Depo.
22 at 290:16-293:19; Ex. 10, Conte Depo. at 79:1-24. Without such a
23 showing, to the extent that USEI's motion asserts intentional
24 copying, it must be denied. USEI also contends, in this motion,
25 that Defendants, including Intel, engaged in litigation misconduct
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1 by paying critical fact witnesses to prevent them from speaking to
2 USEI. The Court has already denied sanctions regarding these
3 actions and addressed accessibility concerns regarding this
4 witness. Docket Nos. 866, 900. Thus USEI's request to bar Intel
5 from asserting any equitable defense is denied.

6 III. Non-infringement of the '313 patent by any of the accused
7 products

8 Claims 1 and 13 are the only asserted independent claims of
9 the '313 patent. Defendants move for summary adjudication that no
10 accused product infringes claim 1 of the '313 patent because
11 (1) none of the accused products practices "network interface
12 means"; (2) none of the accused products satisfies the requirement
13 of "buffer memory outside of the host address space;" and (3) none
14 of the accused products practices "host interface means."
15 Defendants further contend that no accused product infringes claim
16 13 because USEI failed to identify any accused product that
17 includes the structures identified by the Court as corresponding
18 to the "host interface means" or the "network interface means"
19 limitation.
20

21 A. "Network interface means" in claim 1
22

23 Claim 1 of the '313 patent reads:

24 An apparatus for controlling communication between a host
25 system and a network transceiver coupled with a network,
26 wherein the host system includes a host address space,
comprising:

27 a buffer memory outside of the host address space;
28

1 host interface means, sharing the host address space
2 with the host, for managing data transfers between the
3 host address space and the buffer memory in operations
transparent to the host system; and

4 network interface means, coupled with the network
5 transceiver, for managing data transfers between the
buffer memory and the network transceiver.

6 Defendants contend that none of the accused products
7 practices "network interface means" as construed by the Court.

8 Claim 1 of the '313 patent recites "network interface means,
9 coupled with the network transceiver, for managing data transfers
10 between the buffer memory and the network transceiver." The Court
11 found that "network interface means" is a means-plus-function term
12 governed by § 112 ¶ 6. First Claim Construction Order, Docket No.
13 586 at 12. The Court construed "network interface means" to
14 perform the function of "managing data transfers between the
15 buffer memory and the network transceiver" and the corresponding
16 structures to be "in Figure 3, Network interface logic 104, and
17 equivalents." Second Claim Construction Order, Docket No. 634 at
18 17. Figure 3 of the '313 patent shows that the "network interface
19 logic 104" is made up of "XMIT DMA LOGIC 109" and "RECEIVE DMA
20 LOGIC 110." The Court elaborated on its construction by pointing
21 to the specification, which states the "network interface logic
22 104 includes the transmit DMA logic 109 responsive to descriptors
23 stored in the adaptor memory 103, for moving data out of the
24 adapter memory to the network transceiver 105." Id.; '313 Patent,
25 10:3-11.
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1 Defendants contend that the accused infringing products do
2 not "transmit DMA logic responsive to descriptors stored in the
3 adaptor memory" because all accused products move data from the
4 buffer memory onto the network irresponsive to transmit
5 descriptors stored in adapter memory. Kunz Decl. at ¶¶ 19-23;
6 Carkin Decl. at ¶ 7; McCauley Decl. Ex. 1, Lin Rpt. at ¶¶ 156-169;
7 Hu Decl. Ex. 1, Lin Rpt. for Sigma at ¶¶ 81-91, 152-162. USEI
8 responds that, to prove infringement under the Court's
9 construction, all it needs is to identify a "network interface
10 logic 104" that performs the function of "managing transfers of
11 data from buffers in the independent memory 103 and the network
12 transceiver 105"; it does not need to identify further the
13 corresponding structure to "transmit DMA logic 109 responsive to
14 descriptors stored in adapter memory for moving data out of the
15 adapter memory to the network transceiver."

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18 Thus, the debate hinges on what is required to show
19 infringement of "network interface means," a term the Court found
20 to be governed by § 112 ¶ 6. Literal infringement of a claim
21 limitation governed by § 112 ¶ 6 requires that the relevant
22 structure in the accused device (1) perform the identical function
23 recited in the claim, and (2) be identical or equivalent to the
24 corresponding structure in the specification. See Applied Med.
25 Resources Corp. v. United States Surgical Corp., 448 F.3d 1324,
26 1333 (Fed. Cir. 2006). Defendants do not dispute that the
27 identified structures in the accused products perform the
28

1 identical function of "managing data transfers between the buffer
2 memory and the network transceiver." Defendants also do not
3 dispute that the corresponding structure in the specification is
4 the network interface logic 104 shown in Fig. 3, which includes
5 transmit DMA logic 109 that is responsive to descriptors stored in
6 the adapter memory for moving data out of the adapter memory to
7 the network transceiver. In fact, Dr. Mitzenmacher confirmed that
8 the Court's construction requires just such logic. Constant Decl.
9 Ex. 6, Mitzenmacher Depo. at 163:21-164:13. Instead, the parties
10 dispute whether the identified structures in the accused products
11 are identical or equivalent to the corresponding structure in the
12 specification. In this regard, Dr. Mitzenmacher fails to proffer
13 any evidence that the identified structures in the accused
14 products are identical or equivalent to the corresponding
15 structure identified by the Court. For example, in his initial
16 Intel Report, Dr. Mitzenmacher identifies the MAC core component
17 in Intel Gigabit products as the "network interface means" but
18 fails to identify any DMA logic that is "responsive to descriptors
19 stored in the adapter memory for moving data out of the adapter
20 memory to the network transceiver." Constant Decl. Ex. 7,
21 Mitzenmacher Intel Rpt. at ¶ 239. In fact, Dr. Mitzenmacher
22 concedes that he did not specifically identify any such DMA logic
23 in the MAC core component. Nation Decl. Ex. 41, Mitzenmacher 5/30
24 Depo. at 377:20-381:3. Likewise, Dr. Mitzenmacher's report for
25 MSI makes no mention of any structure in the accused products that
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1 is "responsive to descriptors stored in adapter memory for moving
2 data out of adapter memory to a network transceiver." Flynn-
3 O'Brien Decl. Ex. 6, Mitzenmacher Marvell Rpt. at ¶ 69, Ex. 8,
4 Mitzenmacher Depo. at 626:12-22. As an alternative, USEI refers
5 to Dr. Mitzenmacher's Supplemental Reports on how the structures
6 identified in his initial reports are equivalent to the "transmit
7 DMA logic 109 that is responsive to descriptors stored in the
8 adapter memory for moving data out of the adapter memory to the
9 network transceiver." However, the Court has not allowed these
10 supplemental reports. As a result, USEI is foreclosed from
11 arguing that the structures identified in Dr. Mitzenmacher's
12 initial reports are equivalent to the "transmit DMA logic 109."
13 Accordingly, because no structure in any accused product infringes
14 the "network interface means" limitation of claim 1 of the '313
15 patent, summary judgment of non-infringement by any of the accused
16 products of claim 1 of the '313 patent is appropriate.

19 B. "Buffer memory outside of host address space" in claim 1

20 Defendants contend that USEI fails to make a showing that the
21 limitation "a buffer memory outside of the host address space" is
22 met because the identified buffer memory in the accused Intel
23 products can be accessed by the host under some circumstances,
24 which implies that the buffer memory is not "outside of the host
25 address space."
26

27 In his infringement report against Intel, Dr. Mitzenmacher
28 identifies first-in-first-out buffers (FIFOs) in the accused Intel

1 products as the alleged "buffer memory outside of the host address
2 space" recited in claim 1. Constant Decl. Ex. 7, Mitzenmacher
3 Intel Rpt. at ¶ 230. However, Dr. Mitzenmacher concedes that "the
4 Intel technical documentation for at least some of these products
5 allows for direct addressing to the data FIFO buffers by the host
6 specifically for diagnostic purposes." Id. at ¶ 231. These FIFOs
7 in the accused Intel products do not meet the "buffer memory
8 outside of the host address space" requirement because they are
9 accessible by the host system and, thus, lie within the host
10 address space. USEI contends that these FIFOs are only accessible
11 by the host during diagnosis but are inaccessible to the host
12 during normal data transmission, thereby rendering them "outside
13 of the host address space" during the relevant time. Id. USEI's
14 contention fails as a literal infringement argument; the buffer
15 memory can either be inside or outside the host address space, but
16 not both. To the extent that USEI argues that the FIFOs in the
17 accused Intel products are equivalent to "buffer memory outside of
18 the host address space," that is a doctrine of equivalents
19 argument, one for which USEI has failed to proffer any evidence.
20 Therefore, summary judgment of non-infringement of claim 1 of the
21 '313 patent by the accused Intel products is appropriate for this
22 reason as well.

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26 Defendants further contend that Dr. Mitzenmacher improperly
27 identifies two distinctly different "buffer memories" in each
28 accused product for different limitations in claim 1, even though

1 the claim only mentions one "buffer memory." For example, Dr.
2 Mitzenmacher identifies "packet buffer data FIFO buffers" in the
3 accused Intel products as the "buffer memory outside the host
4 address," but identifies "transmit and receive descriptor ring
5 buffers" as the "buffer memory" of the "host interface means."
6 Id. at 230, 233. Similarly, for each accused MSI product, Dr.
7 Mitzenmacher identifies the "MAC Rx and Tx FIFOs" as the "buffer
8 memory outside of the host address space," but the combination of
9 the "MAC Rx and Tx FIFOs" and the "PFU Rx and Tx FIFOs" as the
10 "buffer memory" of the "host interface means." Flynn-O'Brien
11 Decl. Ex. 6, Mitzenmacher Marvell Rpt. at ¶¶ 61-67. USEI does not
12 dispute this showing, but instead argues that this is covered by
13 claim 1.
14

15 Claim 1 only recites one buffer memory in the "host interface
16 means," which is for "managing data transfers between the host
17 address space and the buffer memory," a reference to the "buffer
18 memory outside of the host address space." Therefore, to show
19 literal infringement, USEI must identify one "buffer memory" that
20 performs the claim function. To the extent that USEI argues that
21 the two identified buffer memories are equivalent to "the buffer
22 memory" recited in the claim, that requires a showing of
23 equivalency, for which USEI has failed to proffer any evidence.
24 Therefore, summary judgment of non-infringement of claim 1 of the
25 '313 patent by the accused Intel and MSI products is appropriate
26 for this reason as well.
27
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1 C. "Host interface means" in claim 1

2 Claim 1 contains the limitation of "host interface means,"
3 which the Court construed as having the function of "managing data
4 transfer between address spaces on the host system bus and the
5 buffer memory in operations performed independently of management
6 by the host system." First Claim Construction Order, Docket No.
7 586 at 10-11. Defendants contend that the Court's construction
8 that the data transfer must be "performed independently of
9 management by the host system" dictates that the host system
10 cannot be involved in data transfers. As a result, Defendants
11 argue no infringement can be shown because the host systems in all
12 accused products are involved in managing the data transfers
13 between the host system and the network adapter by writing
14 descriptors to a queue in the host system's memory (i.e., the
15 "host address space.") Defendants' Motion and Opposition, Docket
16 No. 1167-3 at 17.

17
18
19 Because, as discussed above, the Court finds that claim 1 of
20 the '313 patent is not infringed for other reasons, the Court need
21 not address this issue.

22 D. "Host interface means" in claim 13

23 Defendants contend that USEI fails to apply the Court's
24 construction of the "host interface means" in claim 13 of the '313
25 patent to identify the relevant structures in the accused products
26 and, instead, improperly applies the construction from claim 1.
27

28 Claim 13 reads:

1 An apparatus for controlling communication between a host
2 system and a network transceiver coupled with a network,
3 wherein the host system includes a host address space,
4 comprising:

5 a buffer memory outside of the host address space,
6 including a transmit buffer and a receive buffer;

7 host interface means, sharing host address space
8 including a prespecified block of host addresses of
9 limited size defining a first area and a second area, and
10 coupled with the buffer memory, for mapping data
11 addressed to the first area into the transmit buffer,
12 mapping data in the receive buffer into the second area,
13 and uploading data from the receive buffer to the host;
14 and

15 network interface means, coupled with the network
16 transceiver and the buffer memory, for transferring data
17 from the transmit buffer to the network transceiver and
18 mapping data into the receive buffer from the network
19 transceiver.

20 Unlike claim 1, which recites a "host interface means" that
21 performs a single function of "managing data transfers between the
22 host address space and the buffer memory in operations transparent
23 to the host system," claim 13 recites three functions for the
24 "host interface means," namely, "mapping data addressed to the
25 first area into the transmit buffer," "mapping data in the receive
26 buffer into the second area," and "uploading data from the receive
27 buffer to the host." Second Claim Construction Order, Docket No.
28 634 at 16. The Court identified separate corresponding structures
for each identified function, including an XMIT AREA register,
transfer descriptor logic; an XFER AREA register, upload logic;
and an upload DMA module, respectively. Id.

1 USEI fails to base its infringement analysis on the Court's
2 construction for claim 13, but instead applies the construction
3 from claim 1. See Constant Decl. Ex. 53, Mitzenmacher Intel Base
4 Rpt. at ¶ 250. USEI contends that Dr. Mitzenmacher's reports
5 identify structures in the accused products that perform the
6 functions recited by the Court for the "host interface means"
7 element of the '313 patent. Nation Decl. Ex. 35, Mitzenmacher
8 5/29 Depo. at 168:6-172:14, 175:8-21. However, the record does
9 not support USEI's contention. Claim 13 clearly recites three
10 functions for "host interface means" but USEI fails specifically
11 to identify structures in the accused device that perform these
12 functions. Literal infringement of a claim limitation governed by
13 § 112 ¶ 6 requires that the relevant structure in the accused
14 device (1) perform the identical function recited in the claim,
15 and (2) be identical or equivalent to the corresponding structure
16 in the specification. Applied Med. Resources, 448 F.3d at 1333.
17 USEI fails to show even the first requirement that the relevant
18 structure in the accused device perform the identical function
19 recited in the claim, let alone the second requirement that the
20 relevant structures be identical or equivalent to the
21 corresponding structures. Therefore, USEI fails to show an issue
22 of fact regarding infringement of claim 13 of the '313 patent and,
23 thus, summary judgment of non-infringement of that claim by any of
24 the accused products is warranted.
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1 IV. Anticipation of claim 21 of the '872 patent and claims 9, 28,
2 and 39 of the '094 patent by the Intel 82593 prior art
reference

3 Defendants move for partial summary adjudication of
4 anticipation under 35 U.S.C. § 102(a) and (b), contending that
5 Intel's 82593 chip is prior art that satisfies every limitation of
6 claim 21 of the '872 patent and claims 9, 28, 39 of the '094
7 patent. However, as discussed above, the Court grants summary
8 adjudication of invalidity of all the asserted claims of the '872
9 and '094 patents due to the SONIC prior art reference. Thus, the
10 Court need not address this issue.

12 V. Non-infringement of the '459 patent by any of the accused
13 products

14 Claims 1 and 44 are the only asserted independent claims of
15 the '459 patent, and they are asserted only against Intel (claim
16 1) and HP (claims 1 and 44).

17 A. "Means for comparing"

18 Defendants contend that USEI's infringement reports regarding
19 Intel and HP fail to establish infringement because they ignore
20 that the "means for comparing" recited in the claims is a means-
21 plus-function element governed by § 112 ¶ 6 and do not address any
22 of the corresponding structures in the '459 patent that the Court
23 identified for such means (e.g., blocks 224 and 318, interrupt
24 controller 60), much less show that such structures are satisfied
25 by the accused Intel or HP products. Constant Decl. Ex. 12,
26 Crayford Rpt. at ¶¶ 859-861.
27
28

1 As noted above, literal infringement of a claim limitation
2 governed by § 112 ¶ 6 requires that the relevant structure in the
3 accused device (1) perform the identical function recited in the
4 claim, and (2) be identical or equivalent to the corresponding
5 structure in the specification. Applied Med., 448 F.3d at 1333.

6 Claim 1 of the '459 patent reads:

7 An apparatus for transferring a data frame between a network
8 transceiver, coupled with a network, and a host system which
9 includes a host processor and host memory, the apparatus
10 generating an indication signal to the host processor
11 responsive to the transfer of the data frame, with the host
processor responding to the indication signal after a period
of time, comprising:

12 a buffer memory for storing the data frame;

13 network interface logic for transferring the data frame
14 between the network transceiver and the buffer memory;

15 host interface logic for transferring the data frame between
16 the host system and the buffer memory;

17 threshold logic for allowing the period of time for the host
18 processor to respond to the indication signal to occur during
the transferring of the data frame, wherein the threshold
logic includes,

19 a counter, coupled to the buffer memory, for counting the
20 amount of data transferred to or from the buffer memory;

21 an alterable storage location containing a threshold
22 value; and

23 means for comparing the counter to the threshold value in
24 the alterable storage location and generating an
25 indication signal to the host processor responsive to a
comparison of the counter and the alterable storage
location.

26 Claim 44 contains more or less the same language for "means
27 for comparing."
28

1 The Court construed "means for comparing" to have two
2 functions: (1) "comparing the counter to the threshold value in
3 the alterable storage location"; and (2) "generating an indication
4 signal to the host processor." The Court found that the block
5 labeled 224 in Fig. 14 and 318 in Fig. 21 performs the first
6 function. Second Claim Construction Order, Docket No. 634 at 10-
7 11. The Court found that the functional components labeled
8 "Interrupt Controller 60" shown in Fig. 4, together with "Early
9 Rcv Control 225" in Fig. 14, perform the second function. Id.

11 USEI argues that Dr. Mitzenmacher "identifies structures
12 performing the required functions taking into account the Court's
13 claim construction in his original Infringement Reports," but his
14 report merely identifies a portion of the Intel source code of the
15 accused products performing the comparison function without
16 identifying any structure corresponding to the structures
17 specified in the Court's construction. Constant Decl. Ex. 7,
18 Mitzenmacher Intel Rpt. at ¶ 210; Constant Decl. Ex. 12, Crayford
19 Rpt. at ¶¶ 859-61. Similarly, for the accused HP products, Dr.
21 Mitzenmacher simply opines that the recited function is performed,
22 without regard to the corresponding structure required by the
23 Court's claim construction. Declaration of Cameron A. Zinsli
24 (Zinsli Decl.), Ex. 2, Mitzenmacher HP Rpt. at ¶¶ 119, 120. This
25 is not sufficient; USEI must identify structures in the accused
26 product that are either identical or equivalent to the
27 corresponding structures identified by the Court. Applied Med.,

1 448 F.3d at 1333. As an alternative, USEI points to Dr.
2 Mitzenmacher's Supplemental Reports for evidence that the
3 proffered source code is at least equivalent to that required by
4 the Court. However, these reports have been excluded. Therefore,
5 USEI is foreclosed from arguing that the identified source code is
6 equivalent to the corresponding structures required by the Court.
7 Accordingly, summary judgment of non-infringement of claims 1 and
8 44 of the '459 patent by the accused Intel and HP products is
9 granted.
10

11 B. "Look-ahead threshold logic"

12 Intel separately contends that claim 1 of the '459 is not
13 infringed because Intel's accused products do not satisfy "means
14 for comparing" in that they do not contain the "look-ahead
15 threshold logic" required by the Court's construction. However,
16 as discussed above, given that summary adjudication of non-
17 infringement of claims 1 and 44 of the '459 patent by the accused
18 Intel and HP products is granted, the Court need not address
19 whether Intel's products do not infringe claim 1 for this
20 additional reason.
21

22 C. "Threshold value"

23 In addition, Defendants contend that claims 1 and 44 of the
24 '459 patent are not infringed because the accused products do not
25 satisfy "an alterable storage location containing a threshold
26 value" limitation in claim 1 and "an alterable storage location
27 containing a transfer threshold value" limitation in claim 44.
28

1 Again, as discussed above, given that summary adjudication of
2 non-infringement of claims 1 and 44 of the '459 patent by the
3 accused Intel and HP products is granted for other reasons, the
4 Court need not decide this issue.

5 VI. Invalidity under § 112 of claim 13 of the '313 patent and
6 claim 1 of the '459 patent

7 Defendants contend that nothing in the '313 or '459 patents
8 suggests a single structure for performing the functions recited
9 for the "host interface means" of claim 13 of the '313 patent and
10 the "means for comparing" of claim 1 of the '459 patent, and ask
11 the Court to invalidate the claims as indefinite under 35 U.S.C.
12 § 112. However, as discussed above, the Court grants summary
13 adjudication of non-infringement of claim 13 of the '313 patent
14 and claim 1 of the '459 patent. Thus, the Court need not decide
15 this issue.

17 VII. Exclusion of the unreliable opinion of USEI's damages
18 expert, Walter Bratic

19 Defendants contend that USEI cannot prove damages, because
20 its expert, Mr. Bratic, used unreliable methods, unreasonable
21 inferences and speculation to reach his damages conclusions and,
22 thus, his testimony should be excluded.

23 However, given the findings in this order, this motion is
24 moot, and the Court need not address it.

25 VIII. ATTS' motion for partial summary judgment of no damages or,
26 alternatively, to limit the AT&T royalty base

27 ATTS moved for summary judgment to limit the AT&T royalty
28 base to the number of Sigma chips purchased during the relevant

1 time period. Given the other findings in this order, this motion
2 is moot, and the Court need not address it.

3 IX. MSI's motion for partial summary judgment to exclude foreign
4 non-party sales from USEI's asserted damages base

5 MSI contends that the damages USEI claims against it are
6 improper in that they include Yukon chips that are manufactured
7 abroad by third-party foundries or offered for sale and sold
8 abroad by non-party Marvell Asia Pte. Ltd. (MAPL), a Singapore
9 corporation that is a legal entity distinct from MSI. Declaration
10 of Joseph Kuo (Kuo Decl.) at ¶¶ 9, 10. However, given the other
11 findings in this order, the Court need not address this issue.

12 X. Apple's motion for partial summary judgment of non-
13 infringement of claims 1, 9, 12 and 28 of the '094 patent

14 USEI accuses certain Apple products of infringing method
15 claims 1, 9, 12, and 28 of the '094 patent based solely on its
16 inclusion of GEM ethernet technology supplied by Sun Microsystems.
17 Declaration of Christopher Cravey (Cravey Decl.) Ex. 1,
18 Mitzenmacher Apple Rpt. at ¶¶ 52-84. Apple contends that it does
19 not infringe these method claims because it has always disabled
20 the accused infringing "Early Transmit" feature in the Sun GEM
21 ethernet technology, thus rendering use of the accused infringing
22 feature impossible. Cravey Decl. Ex. 3, Seifert Rpt. at ¶¶ 48-52,
23 54-57, and 64-69.

24 Because the Court grants summary adjudication of invalidity
25 of all the asserted claims of the '094 patent due to the SONIC
26 prior art reference, the Court need not address this issue.

1 XI. Atheros, Sigma and ATTS's motion for partial summary judgment
2 of non-infringement of the '313 patent

3 In construing the '313 patent's claim 1 element, "host
4 interface means," the Court found that the function of "managing
5 data transfers between the host address space and the buffer
6 memory in operations transparent to the host system" necessarily
7 includes the function of remapping a section of the host address
8 space in the host system to the buffer memory. Second Claim
9 Construction Order, Docket No. 634 at 13. Atheros, Sigma and ATTS
10 contend that Dr. Mitzenmacher's report does not provide any
11 analysis to indicate that these Defendants' accused products
12 practice the claims under the Court's construction. Sigma and
13 ATTS argue that the same is true for the claims dependent on claim
14 1 in the '313 patent, as well as claim 13 and its dependent
15 claims.
16

17 However, as discussed above, the Court grants summary
18 adjudication of non-infringement of the asserted claims of the
19 '313 patent by any of the accused products. Thus, the Court need
20 not address this issue.
21

22 CONCLUSION

23 As discussed above, the Court has adjudicated the status of
24 each asserted claim of the patents-in-suit as follows:

25 The Court (1) DENIES USEI's motion for summary adjudication
26 of non-anticipation of the asserted claims of the '872 or '094
27 patents by the SONIC prior art reference, and instead GRANTS
28

1 Defendants' motion for invalidity of the asserted claims of the
2 '872 or '094 patents in view of the SONIC prior art reference;
3 (2) DENIES USEI's motion for summary judgment against Intel, and
4 Defendants using Intel chips, of infringement of claim 21 of the
5 '872 patent as moot; and (3) DENIES USEI's motion for summary
6 judgment that Intel may not present any equitable defense because
7 it intentionally copied USEI's patented invention.
8

9 With regard to Defendants' motions for summary judgment, the
10 Court GRANTS the following motions: (1) for summary adjudication
11 that SONIC anticipates the asserted claims of the '872 and '094
12 patents; (2) for summary adjudication of non-infringement of
13 claims 1 and 13 of the '313 patent by any of the accused products;
14 and (3) for summary adjudication of non-infringement of claims 1
15 and 44 of the '459 patent by the Intel and HP accused products.
16

17 The Court DENIES the following Defendants' motions as moot:
18 (1) to exclude Mr. Bratic's expert testimony regarding all four
19 patents-in-suit as moot; (2) for summary adjudication of
20 anticipation of claim 21 of the '872 patent by the Intel 82593
21 chip prior art; (3) for summary adjudication of anticipation of
22 claims 9, 28 and 39 of the '094 patent by the Intel 82593 chip
23 prior art; (4) for summary judgment of invalidity, under § 112, of
24 claim 13 of the '313 patent and claim 1 of the '459 patent;
25 (5) MSI's motion for partial summary judgment to exclude foreign
26 non-party sales from USEI's asserted damages base; (6) Apple's
27 motion for summary adjudication of non-infringement of claims 1,
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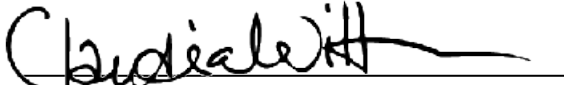
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9, 12 and 28 of the '094 patent; and (7) Atheros, Sigma and ATTS's motion for partial summary judgment of non-infringement of the '313 patent.

Accordingly, all of the asserted claims of the patents-in-suit are resolved in favor of Defendants. The Clerk of the Court shall enter judgment in favor of Defendants, who shall recover costs from USEI.

IT IS SO ORDERED.

Dated: November 7, 2014



CLAUDIA WILKEN
United States District Judge