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IN THE UNITED STATES DISTRICT COURT
FOR THE NORTHERN DISTRICT OF CALIFORNIA
SAN JOSE DIVISION

HYNIX SEMICONDUCTOR INC., HYNIX SEMICONDUCTOR AMERICA INC., HYNIX SEMICONDUCTOR U.K. LTD., and HYNIX SEMICONDUCTOR DEUTSCHLAND GmbH,

Plaintiffs,

v.

RAMBUS INC.,

Defendant.

No. C-00-20905 RMW

ORDER DENYING HYNIX'S MOTION FOR A NEW TRIAL ON INVALIDITY BASED ON OBVIOUSNESS AND ANTICIPATION

[Re Docket Nos. 2073, 2087, 2954]

Following a trial on infringement and validity, the jury returned a verdict that Hynix[1] infringed certain Rambus patents and that Hynix had not proven that those patents were invalid. Docket No. 2054 (Apr. 26, 2006). The court deferred ruling on post-trial motions from the patent trial until a jury determined Hynix's antitrust and fraud claims. On March 26, 2008, a different jury found that Rambus did not monopolize various technology markets or commit fraud. Docket No. 3613. The court has denied Hynix's motion for a new trial with respect to those claims. *Hynix Semiconductor Inc. v. Rambus Inc.*, 2008 WL 2951341 (N.D. Cal. Jul. 24, 2008).

[1] The court collectively refers to the four Hynix entities as "Hynix."

The court now returns to the post-trial motions from the patent case. This order addresses Hynix's filings in support of a motion for a new trial on anticipation and obviousness.[2] Rambus opposes the motion. The court has reviewed the papers and considered the arguments of counsel. For the reasons set forth below, the court denies the motion for a new trial.

I. RAMBUS'S MOTION TO STRIKE

After the jury returned its verdict in favor of Rambus, the parties and the court discussed a time line for resolving post-trial motions. Hynix represented that it would file "final versions" of all its motions by May 5, 2006. Tr. 3492:23-3294:24. Come May 5, Hynix filed a "Notice of Motion and Motion For a New Trial On Invalidity Based on Prior Art" that lacked any legal argument other than noting that a memorandum of points and authorities would be following "forthwith" and that Hynix "reserve[d] its right to bring other appropriate post-verdict motions within 10 days after judgment has been entered[.]" Eleven days later, Hynix filed its memorandum of points and authorities in support of its motion for a new trial. Rambus opposed the motion in a timely manner, and there is no indication that Rambus's opposition was prejudiced by Hynix's delinquent filing.

Nonetheless, Rambus has moved to strike the motion for failure to comply with the briefing schedule set by the court. While Hynix offers no explanation for its failure to file its motion according to the court's deadline, it appears to have had no impact, let alone a prejudicial impact, on Rambus. As Rambus has not been harmed, the court denies Rambus's motion to strike and will decide the motion on the merits. This ruling should not be construed as any suggestion that the court will relieve parties from deadlines in the future. The court will also consider the supplemental briefing by the parties on the effect of *KSR Int'l Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1741 (2007).

II. LEGAL STANDARD FOR A NEW TRIAL

After a jury has returned its verdict, the court may grant a new trial "for any reason for which a new trial has heretofore been granted in an action at law in federal court." Fed. R. Civ. P.

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[2] By Hynix's filings, the court refers to its original notice of motion, its later-filed memorandum of points and authorities, and its three rounds of supplemental briefing filed on July 6, 2007, January 4, 2008, and April 25, 2008.

59(a)(1)(A). Hynix's motion for a new trial rests on a number of grounds, but focuses on arguing that the verdict was against the weight of the evidence. Such a motion may be granted if "the verdict is contrary to the clear weight of the evidence[.]" *United States v. 4.0 Acres of Land*, 175 F.3d 1133, 1139 (9th Cir. 1999). "[A] district court may not grant or deny a new trial merely because it would have arrived at a different verdict." *Id.* While there is no formulaic test for determining whether a verdict is contrary to the clear weight of the evidence, "[i]f, having given full respect to the jury's findings, the judge on the entire evidence is left with the definite and firm conviction that a mistake has been committed, it is to be expected that he will grant a new trial." *Landes Constr. Co., Inc. v. Royal Bank of Canada*, 833 F.2d 1365, 1372 (1987). In forming that conviction, the court may consider the credibility of witnesses and persuasiveness of the evidence. *Id.*

III. THE CVAX AND iRAM REFERENCES

Hynix's motion attacks the jury's finding that the following claims were not obvious: claims 24 and 33 of U.S. Patent No. 6,034,918, claim 33 of U.S. Patent No. 6,324,120, claims 9, 28, and 40 of U.S. Patent No. 6,426,916, and claim 16 of U.S. Patent No. 6,452,863.[3] The claimed inventions are memory devices and methods of operating memory devices that implement a variety of interface features that regulate the connection between the DRAM and the bus. Hynix moves for a new trial with respect to whether these claims are obvious in light of admitted trial exhibits 2049 and 2063, the CVAX prior art references, and admitted trial exhibit 2385, the iRAM prior art reference which supplied a purported motivation to combine the CVAX references. Due to the complex nature of these issues, the court begins by considering the impact of the references on a single claim.

A. Rambus's Claim 24 of the '918 Patent

The '918 patent's claim 24 depends from claim 18, which recites a method of operating a synchronous memory device. In general terms, the method of claim 18 begins by requiring the memory device to receive an external clock signal. The method next requires the device to receive "block size information" from a controller. The block size information defines how much data

[3] The court refers to these patents throughout this order by their final three digits.

should be output during a read operation. The next step of the method involves receiving a request for such a read operation and then synchronously outputting the defined amount of data.

Claim 24 further limits the method by including the use of an access time register to the memory device. The access time register stores a value ("delay time code") that represents a number of clock cycles that elapse between when the device receives the read request and when it outputs the block of data. Colloquially, claim 24 recites the implementation of block data transfers governed by a programmable read latency that is stored in a register on a DRAM. The full text of claim 24 (with claim 18 incorporated) reads:

> A method of operation of a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method of operation of the memory device comprises:
>
> receiving an external clock signal;
>
> receiving first block size information from a bus controller, wherein the first block size information defines a first amount of data to be output by the memory device onto a bus in response to a read request;
>
> receiving a first request from the bus controller; and
>
> outputting the first amount of data corresponding to the first block size information, in response to the first read request, onto the bus synchronously with respect to the external clock signal.
>
> further including storing a delay time code in an access time register, the delay time code being representative of a number of clock cycles to transpire before data is output onto the bus after receipt of a read request and wherein the first amount of data corresponding to the first block size information is output in accordance with the delay time code.

'918 Patent, col. 26, ll. 13-24; 61-67.

B. The CVAX References

At trial, Hynix offered two articles that it refers to as the "CVAX references." Trial Tr. 1820:2-1821:5 (Mar. 30, 2006). The first article was written by David K. Morgan. Tr. Ex. 2049. It appeared in the August 1988 issue of *Digital Technical Journal*[4] and was titled "The CVAX

[4] *Digital Technical Journal* was an internal publication of Digital Equipment Corporation. *See* Docket No. 2002, Ex. C at 3 (testimony of David Morgan played at trial). Though the journal was not available outside of DEC, Mr. Morgan testified that DEC did not restrict the journal's circulation and that he discussed articles in it with people outside of the company. *Id.* Rambus does not oppose

CMCTL – A CMOS Memory Controller Chip." *Id.* The second article, "Overview of the MicroVAX 3500/3600 Processor Module," was written by Gary P. Lidington and appeared in the same issue of *Digital Technical Journal*. Tr. Ex. 2063. Hynix's technical expert, David Taylor,[5] testified about the scope of the CVAX references' disclosures.

The papers describe parts of the CVAX memory system, a computer system manufactured and sold by Digital Equipment Corporation. Trial Tr. 1818:7-9 (Mar. 30, 2006). Mr. Taylor presented his testimony to the jury by showing a series of slides with excerpted quotes from the two papers. He focused on the papers' discussion of the CMCTL, the CVAX system's memory controller. *Id.* at 1818:18-21. Before continuing, it is critical to distinguish between a memory controller like the CMCTL and the "synchronous memory device" that "includes a plurality of memory cells" recited in Rambus's claim. A memory controller is a chip that mediates between a central processing unit and a memory to make operations more efficient. Because memory controllers (including the CMCTL) typically lack memory cells, Hynix does not argue that the CVAX references anticipate Rambus's claims. As discussed in more detail below, Hynix contends that a person of ordinary skill would have found it obvious to combine the functionality of the CMCTL with a DRAM.

The Morgan reference disclosed that the controller possessed a programmable mechanism "for varying the PMI transition timing for CVAX bus cycles less than 100 nanoseconds." *Id.* According to Mr. Taylor, this suggested that the CMCTL could be programmed with "a parameter related to access time." *Id.* at 1818:22-1819:5. Mr. Taylor then quoted from the Lidington CVAX reference describing a single bit parameter in the controller for specifying a number of cycles before allowing access to the DRAMs included in the CVAX memory system. *See id.* at 1819:6-17 (quoting from Tr. Ex. 2063.0004, second column). Following this discussion, Mr. Taylor confirmed

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Hynix's motion on the basis of the public availability of the CVAX references.

[5] Mr. Taylor has a Master's Degree in electrical engineering and extensive industry experience with designing memory devices, including a stint at Hynix's predecessor Hyundai designing the earliest Hynix SDRAM products at issue in this case. *See generally* Trial Tr. 1685:17-1609:2 (Mar. 29, 2006).

that the CMCTL operated in a synchronous fashion. *Id.* at 1819:20-1820:20.

Mr. Taylor also testified about block operations in the CVAX memory system. *See id.* at 1840:24-1841:22. He pointed out that the Morgan reference describes the system's ability to transfer "up to four bytes of data" at a time. *Id.* at 1841:10-11 (citing Tr. Ex. 2049.0004, first column). Likewise, he showed that the Lidington reference disclosed that "[t]he size of the transfer is encoded in bits 31 through 30 of the physical address (up to four longwords)." *Id.* at 1841:15-18 (quoting Tr. Ex. 2063.0004, first column). According to Mr. Taylor, bits 31 and 30 enabled the CVAX system to make block data transfers of four different sizes. *Id.* at 1841:19-22.

Robert Murphy, Rambus's technical expert, disputed some aspects of Mr. Taylor's testimony. He noted that in the CVAX memory system, the DRAMs did not receive an external clock signal, nor did they receive block size information. Trial Tr. 2649:8-11 (Apr. 10, 2006). Mr. Murphy did not disagree that the CMCTL (CVAX's memory controller) received an external clock signal and block size information.

Mr. Murphy also testified that the CVAX references "[don't] disclose an access time register." *Id.* at 2649:11-12; 2659:14-15. Mr. Murphy never explained his basis for this opinion, nor how Mr. Taylor erred in reading the CVAX references. Rambus attempts to buttress Mr. Murphy's testimony by contending that the testimony of David Morgan shows that Hynix failed to prove that the CVAX references disclose an access time register. In full, Mr. Morgan testified as follows:

> Q: If the [private memory interconnect] cycle select bit in the CVAX memory controller is set to zero, based on that particular DRAM being put in the system, what will be that particular DRAM's RAS access time in that situation?
> A: ***The DRAM that you – that's on the memory board has a fixed access time. The memory controller can't change that.*** Okay?
> Q: Yes.
> A: And what the private memory select bit does is add cycles to the private memory interconnect to – or subtract cycles from the private memory interconnect cycle time to match to the speeds of the RAMs that are out there.
> Q: Okay.
> A: And the timing is multiple cycles of the CVAX pin bus.
> Q; Okay. I think I understand that.
> A: So what I was reacting to was the notion that – I think the notion that the

> memory controller is changing the access time of the DRAMs. And that's why I was getting confused. It does not do that.

Docket No. 2002, Ex. F at 2 (emphasized portion quoted by Rambus). Rambus's opposition characterizes this testimony as Mr. Morgan stating that "CVAX lacked an 'access time register.'" Opp'n at 10, fn.18. Rambus reads too much into the testimony. Mr. Morgan testified that the bit on the CVAX memory controller could not change the access time of the DRAM, but his testimony *confirms* that the memory controller contained a mechanism for adjusting the controller's time to access the DRAMs in clock cycles to permit it to adapt to different types of DRAMs. *Accord id.* at 1 (explaining that the CVAX system was designed to interface with multiple generations of DRAMs).

Unresolved by this testimony presented by both Hynix and Rambus is whether this bit is "representative of a number of clock cycles to transpire before data is output onto the bus after receipt of a read request." Mr. Taylor's rebuttal testimony repeats that the CVAX references disclose an "access time register," *see* Trial Tr. 3152:9-3153:15 (Apr. 12, 2006), but his testimony does not explain how the bit represents an amount of time that transpires between receiving a read request and outputting data. It appears from Mr. Morgan's testimony that the purpose of the private memory select bit was to permit the CMCTL to operate with various DRAMs, not to control the amount of time between receiving a read request and outputting data. On the other hand, the private memory select bit seems to have affected the amount of time between receiving requests for memory operations, like a read request, and completing them.

C. The iRAM Reference and Its Motivation to Combine

Hynix contends that a person of ordinary skill would have combined the features of the CMCTL memory controller with a DRAM based on the teaching of admitted trial exhibit 2385, the "iRAM reference." Trial Tr. 1843:2-13 (Mar. 30, 2006). The iRAM reference is Intel's 1985 Memory Components Handbook, and Hynix specifically relies on page 3-433, which states:

> A sensible alternative is to integrate the memory controller circuits into the memory – completely freeing the CPU of this task. While this approach places an additional burden on the device designer, it greatly simplifies the task of the system designer by eliminating the design problems associated with refresh and timing. This permits

> a very simple interface to the CPU and yet provides guaranteed refresh, optimized timing, and minimal hardware support requirements.
>
> A microprocessor integrates all the components of a central processing unit into one device. An iRAM integrates all the components of a dynamic RAM memory system into a single device. This is unlike the pseudostatic or quasi-static RAM devices which only incorporate a portion of the refresh circuitry onto the memory chip and still require much control from the CPU. The integration used in the iRAM includes the refresh timer, refresh address control and counter, address multiplexing, and memory cycle arbitration as well as an 8-bit wide memory array.

Trial Ex. 2385, 3-433.

At trial, Mr. Taylor testified that iRAM would motivate a person of ordinary skill to integrate "memory controller functions into the memory." *See* Trial Tr. 1835:2-8 (Mar. 30, 2006). Other than this statement, he provided minimal substantive testimony about the reference and its teachings. Mr. Taylor never read these passages into the record. Indeed, the sum of his testimony introducing iRAM to the jury and why it would motivate a person of ordinary skill to add memory controller functionality to a DRAM spanned just over two minutes. *Id.* at 1834:2-1835:14.

Rambus pounced on this gap. *See* Trial Tr. 2533:18-2535:15 (Apr. 6, 2006). Mr. Murphy testified that a person of ordinary skill would not have felt motivated to add the functionality of the CMCTL to a DRAM. *Id.* at 2533:18-2534:8. He explained that at the time of the invention, the industry strove to add as much memory to a computer system as possible, and it did so by using a "single memory control chip and it would talk to as many DRAMs as they could design to fit in the specs of that system." *Id.* at 2534:6-8. With respect to iRAM, Mr. Murphy went into detail:

> iRAM does suggest combining a particular function with memory, and it does it in a way where it's targeting a particular type of small system that normally used static RAMs and says that if you combine the refresh circuitry on to a DRAM, that it would be appropriate for very small systems. However, the document's pretty clear, and if you would pull up [trial exhibit] 2385, page 28, and highlight the first sentence. . . . It says: "integrated RAMs are primarily intended for use in microprocessor memories usually less than or approximately equal to 64k bytes while standard DRAMs with a separate controller are most cost effective in larger memories." And so one of the things that this tells one of ordinary skill in the art and what one of ordinary skill in the art knew at the time is that just the addition of one feature, the refresh feature, made this part not compatible with the cost goals of a large memory system and, therefore, these products were only targeted to replace SRAMs.

Id. at 2534:14-2535:15. It bears noting that Mr. Murphy did not deny that iRAM suggested adding

memory controller functionality to a DRAM. He instead drew upon the language in the iRAM reference to emphasize that doing so was not cost-effective with larger memories.

In Hynix's response to Rambus's rebuttal case, Hynix attempted to rehabilitate the iRAM reference, and Mr. Taylor provided a more detailed explanation of iRAM's teaching. *See* Trial Tr. 3147:13-3150:12 (Apr. 12, 2006). Mr. Taylor showed that the iRAM integrated more than just refresh circuitry onto the memory; it also added memory controller functions. *Id.* at 3148:9-3149:24. Mr. Taylor emphasized that iRAM shows the motivation to combine memory controller and DRAM functionality not just in the abstract, but in a commercial product. *See id.* at 3150:10-12 ("And that form of suggestion is the highest form of suggestion that anyone could possibly provide.").

D. Analysis of the New Trial Motion Regarding Claim 24 of the '918 Patent

Hynix bore the burden of persuasion at trial of proving by clear and convincing evidence that claim 24 would have been obvious to a person of ordinary skill in the art. Before reaching the quality of the evidence, the court must address a threshold challenge raised by Rambus.

Setting forth evidence that proves invalidity is no small matter. In *Koito Manufacturing Co. v. Turn-Key-Tech, LLC*, the Federal Circuit reversed the denial of the patentee's motion for judgment as a matter of law, which argued that there was a failure to adduce sufficient evidence of anticipation. 381 F.3d 1142 (Fed. Cir. 2004). The court held that "general and conclusory testimony . . . does not suffice as substantial evidence of invalidity." *Id.* at 1152. It explained that substantial evidence "typically" takes the form of "testimony from one skilled in the art and must identify each claim element, state the witnesses' interpretation of the claim element, and explain in detail how each claim element is disclosed in the prior art reference." *Id.* (quoting *Schumer v. Lab. Computer Sys., Inc.*, 308 F.3d 1304, 1315-16 (Fed. Cir. 2002)). Introducing the prior art reference into evidence is *not* a substitute; a challenger must "articulate how [a prior art] reference anticipates or makes obvious the [claim at issue]." *Id.* In *Koito*, the trial court relied on a prior art reference about which there had been no testimony in upholding a jury's verdict of obviousness. *Id.* at 1151-52. The Federal Circuit reversed and remanded for the trial court to "review the trial testimony and evidence, especially that regarding the plastic cassette technology, to determine whether Koito provided clear

and convincing evidence to the jury on the issue of anticipation and obviousness to render the '268 patent invalid." *Id.* at 1153,

The Federal Circuit's discussion of the "typical" form of evidence suggests that it *might* be possible to support a finding of invalidity without detailed testimony as to each claim limitation in some unusual case. The current case does not appear to be one. The obviousness inquiry turns on consideration of the "interrelated teachings of multiple [references]." *KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1740 (2007). This allows the court to determine whether the was an "apparent reason to combine the known *elements* in the fashion claimed by the patent at issue." *Id.* at 1741 (emphasis added). Without specific testimony about what limitations or "elements" of a claimed invention also appear in a prior art reference, it is impossible to determine whether or not an element of an invention was known in the prior art. Thus, in a case such as this one, the court believes that evidence sufficient to support a finding that a prior art reference discloses a limitation (or all limitations) of a claimed invention must include testimony explaining what the reference discloses. This testimony must not be "general and conclusory." *Koito*, 381 F.3d at 1152; *but see Arthur A. Collins, Inc. v. N. Telecom Ltd.*, 216 F.3d 1042, 1047-48 (Fed. Cir. 2000) (suggesting that conclusory opinion testimony is permitted at trial under Federal Rule of Evidence 705 because "the opposing party can challenge the factual basis of the expert's opinion during cross-examination").

Rambus argues that Hynix's motion for a new trial must fail because Hynix did not meet its burden of producing evidence on a limitation-by-limitation basis. According to Rambus, because Hynix failed to produce evidence sufficient to support a jury finding in its favor, the court cannot find that the "clear weight" of the evidence favors Hynix. Hynix's reply brief fails to respond to this argument. Rambus raised this argument at a hearing on the motion, Hrg. Tr. 78:24-80:17 (Jun. 27, 2006), and again, Hynix failed to respond, *see id.* at 86:1-89:9. Rambus's argument has persuasive force, but the court need not hold that a party cannot as a matter of law receive a new trial even if it failed to adduce sufficient evidence at trial to support a verdict in its favor.

Simply put, the court is not persuaded that the jury's verdict regarding claim 24 is against the clear weight of the evidence. Reviewing the record, the court is left with the firm conviction that

much of the evidence elicited at trial appears to have little persuasive weight. Mr. Taylor's testimony floated "at a high level," Hrg. Tr. 86:14-15 (Jun. 27, 2006), often quoting single lines of documents and moving on to a conclusion with little analysis. For example, what effect does the private memory select bit have on read operations in the CVAX computer system? The testimony does not provide a clear answer, and without one, the court cannot conclude that the "clear weight" of the evidence shows that CVAX discloses an access time register that stores a delay time code.

As a second example, why would iRAM motivate one of ordinary skill in the art to place controller circuitry on a DRAM when it explicitly states that "standard DRAMs with separate controllers are more cost effective in larger memories"?[6] To be sure, a prior art reference "is no less anticipatory if, after disclosing the invention, the reference then disparages it." *Celeritas Techs., Ltd. v. Rockwell Int'l Corp.*, 150 F.3d 1354, 1361 (Fed. Cir. 1998). But Hynix did not rely on iRAM to disclose a limitation of a claimed invention. Hynix relied on iRAM to prove that a person of ordinary skill would have considered it obvious to add elements of a memory controller to a DRAM. The "clear weight" of the evidence about iRAM does not support this conclusion. Considering the reference and the testimony about it, the court is inclined to believe that a person of ordinary skill familiar with iRAM would have been discouraged to add controller circuitry to a DRAM.

In sum, the court does not possess a "definite and firm conviction" that the jury erred. The court therefore denies Hynix's motion for a new trial with respect to the obviousness of claim 24. Claims 9, 28, and 40 of U.S. Patent No. 6,426,916 contain access time register limitations similar to claim 24 of the '918 patent. The court denies the motion for a new trial on obviousness with respect to these claims as well. Claim 33 of U.S. Patent No. 6,034,918, claim 33 of U.S. Patent No. 6,324,120, and claim 16 of U.S. Patent No. 6,452,863 do not include "access time register" limitations. Nonetheless, Hynix's arguments regarding them rely on the persuasiveness of iRAM's motivation to combine aspects of controller circuitry (like that in the CMCTL) and a standard DRAM. The court lacks a definite and firm conviction that the jury erred with respect to these

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[6] iRAM defined "larger memories" as those larger than 64 kilobytes. The memories involved in this case ranged from the dozens to hundreds of megabytes.

claims.

IV. THE REDWINE REFERENCE

Hynix next argues that the evidence clearly weighs against the jury's verdict with respect to whether or not claims 32 and 36 of U.S. Patent No. 6,378,020 were anticipated by U.S. Patent No. 4,330,852, the "Redwine patent."

A. Claims 32 and 36 of the '020 Patent

Claims 32 and 36 are dependent claims that share many limitations. Claim 32 depends from claim 31, which depends from claim 30. Claim 36 depends from claim 35, which also depends from independent claim 30. As both claims incorporate claim 30, they share the following limitations:

> An integrated circuit device comprising:
>
> input receiver circuitry to sample an operation code synchronously with respect to a first transition of an external clock signal, the operation code specifying a read operation; and
>
> output driver circuitry to output data in response to the operation code, wherein: the output driver circuitry outputs a first portion of data in response to a rising edge transition of the external clock signal; and
>
> the output driver circuitry outputs a second portion of data in response to a falling edge transition of the external clock signal.

'020 Patent, col. 28, ll. 4-18. Thus, both claims at issue recite the need for input receiver circuitry that samples an operation code. Generally, the claim recites an integrated circuit device that synchronously receives requests for a read operation and then outputs data in response on both edges of the clock signal. Rambus contends that this claim covers DRAMs that use "dual-edged clocking."

Claim 32 adds two limitations, namely that the integrated circuit device include "a memory array having a plurality of memory cells" and that the input receiver circuitry also receive "address information" and that it do so "synchronously with respect to the external clock signal." Claim 36 also adds two limitations, but of a different nature. Claim 36 requires the integrated circuit device to possess "a clock alignment circuit to receive the external clock signal" and that this circuit "generate[] an internal clock signal" and the output driver circuitry "outputs data in response to the internal clock signal." Effectively, claim 32's additional limitations restrict it to covering synchronous memory devices that use dual-edged clocking. Claim 36 is drawn toward a broader

class of devices that combine dual-edged clocking with the use of a "clock alignment circuit" that dictates when the device outputs data.

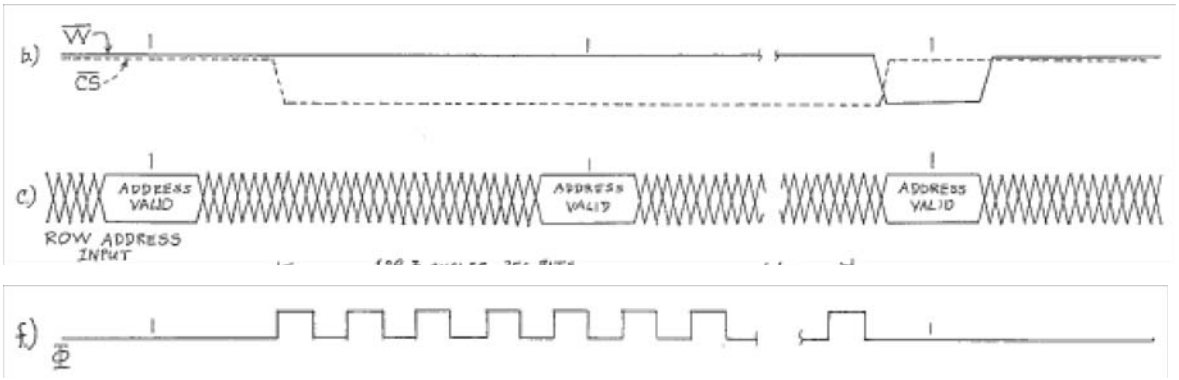
B. The Redwine Reference and Hynix's Summary Judgment Motion

U.S. Patent No. 4,330,852, titled "Semiconductor Read/Write Memory Array Having Serial Access" issued on May 18, 1982 to Donald J. Redwine, Lionel S. White, Jr., and G. R. Mohan Rao and was assigned to Texas Instruments, Inc. Hynix contends that Redwine anticipates both claim 32 and claim 36. It previously moved for summary judgment of invalidity, arguing that Redwine anticipated claim 32 and rendered claim 36 obvious when combined with another patent. The court denied Hynix's motion for summary judgment, but accepted Hynix's arguments that Redwine disclosed many of the limitations of the two claims. *See* Docket No. 1789 (Mar. 9, 2006). The court then precluded Rambus from arguing that Redwine did not disclose those limitations at trial. *See* Docket No. 2026, Ex. 3 (Apr. 18, 2006) (email from Judge Ronald Whyte of March 29, 2006).

C. The Trial Testimony About Redwine and What It Discloses

At trial, the Redwine patent was admitted into evidence as trial exhibit 2022. Trial Tr. 1777:18-1778:7 (Mar. 30, 2006). Mr. Taylor opined that "claim 32 of the '020 patent is rendered invalid by the Redwine reference" because "all of the elements are found in [Redwine]." *See id.* 1771:9-16. He shared a similar opinion with respect to claim 36. *See id.* 1771:23-1772:4. Mr. Taylor then presented a series of slides explaining the basis for these conclusions, focusing on the reasons he believed that Redwine disclosed outputting data on both edges of the clock signal and a "clock alignment circuit." *See id.* 1778:9-1784:14. Two hours later, he presented conclusory testimony that each limitation of claim 32 was disclosed by Redwine. *See id.* 1860:16-1862:5 ("And we have to go through each of the elements because that's what the test requires, so let's do that."). In his summary testimony, Mr. Taylor submitted without explanation that Redwine disclosed "input receiver circuitry to sample an operation code synchronously with respect to a first transition of an external clock signal." *Id.* 1861:15-17. Rambus's cross-examination of Mr. Taylor did not challenge the factual basis for his opinion, but hammered on the fact that the Patent Office considered Redwine before issuing the '020 patent. *Id.* 1914:22-1917:25.

In rebuttal, Rambus's expert Mr. Murphy testified that Redwine could not anticipate claims 32 and 36 because it did not disclose input receiver circuitry that *sampled* an operation code. Trial Tr. 2535:22-2538:2 (Apr. 6, 2006); 2633:4-2636:4 (Apr. 10, 2006). Mr. Murphy explained that Redwine disclosed *sensing* an operation code ("the W signal"). Putting Mr. Murphy's testimony in context requires examining three graphs from Figure 2 of Redwine, which display the status of the W signal (a read/write switch), the row address input, and Φ (the external clock signal) respectively:



Mr. Murphy distinguished sampling a signal from sensing it by reference to how Redwine measured the status of W and the row address input, as follows:

> A: So in row C, we see a signal that is sampled. It's a signal that the device looks at a certain point in time to determine whether the value on that line is a high or a low, and that would be the address valid areas. And then after that occurs, the line is cross-hatched, indicating that the part doesn't care whether that signal moves around because it's simply not looking at that point in time. And that was in contrast with the W bar signal in row B, and what is shown in row B is that the W bar signal is held at a particular state throughout most of the cycle. And then it changes. It transitions from high to low and then stays low for a while, and then goes high and stays high. And the difference in the drawing would indicate to one of ordinary skill in the art that that is a signal that is not sampled at a particular point in time. It's looked at for the whole period because it's indicated that for the whole time there, it's in a particular value and it's assumed to be the value that they need for the operation of the device.
>
> Q: And what would happen if the W signal were not held high during a read?
>
> A: The device would not operate correctly.
>
> Q: So is the W signal sampled or sensed?
>
> A: The W signal is sensed.

Id. 2633:17-2634:19. Mr. Murphy provided the following analogy to explain his distinction between sensing and sampling a signal:

> Q: Give us an example, a lay example of the difference between sensing and sampling, if you will.
>
> A: A good example would be let's say you're interested in knowing when the mail arrived in your mailbox. So you got up in the morning, you had breakfast, and you walked out to the front of the house and sat by a window where you could see the mailbox. And you looked at the mailbox continuously and looked and looked and looked until you actually saw the postal carrier bring the mail, put it in the mailbox, and you would sense exactly at that point that the mail was in the box. Sampling is different. An example of that would be, again, you're interested in whether the mail had arrived. You get up in the morning, have breakfast. Perhaps you look at the clock and say it's 8:00 o'clock, I'll go check the mailbox. You walk to the front door. You open the front door, lift the box to see if there's mail. At that point there's no mail. You close the box. You close the door. You go about your business. You don't care whether there's mail in the box. You checked it at 8:00 o'clock. You might check again at 9:00 o'clock or 10:00 o'clock or whatever schedule you pick, but you're simply going and sampling to see if the mail is there at a certain point in time. And then the rest of the time, you just don't care. You don't care if the mail is there or not yet. You only sample it at a particular time.

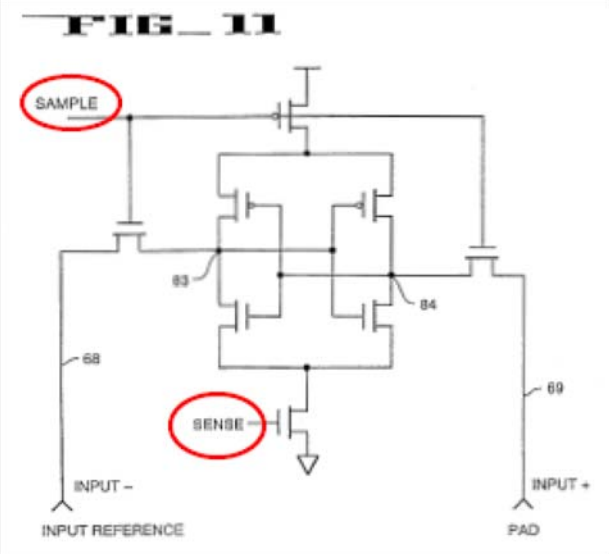
Id. 2634:20-2636:1. Hynix did not cross-examine Mr. Murphy on this point. *See id.* 2753:7-10 (Apr. 11, 2006).

Mr. Taylor testified in response that Mr. Murphy's distinction was inaccurate. *See* Trial Tr. 3140:4-3142:14 (Apr. 12, 2006). Specifically, Mr. Taylor stated that Redwine makes no distinction between "sensing" and "sampling" and quoted from the patent specification that "the proper sequence is selected by sensing the W/ command at the start of a cycle, just as an address is sensed . . . ." *Id.* 3141:14-3142:1 (quoting U.S. Patent No. 4,330,852, col. 7, ll. 47-49). According to Mr. Taylor, "the patent is telling you it's doing the same thing to the W pin as it's doing to the address pins." *Id.* 3142:9-14. Mr. Taylor couched his testimony in Redwine's use of the word "sense," not in whether sampling and sensing are meaningfully different to a person of skill in the art.

The full scope of the evidence in this case sheds little light on whether there is a meaningful

difference between "sensing" a signal and "sampling" it.[7] Mr. Taylor's expert testimony is no better than Mr. Murphy's. Both experts rendered conclusory opinions and struck the court as too beholden to their sides to offer persuasive testimony.

The court is left with a suspicion that the distinction drawn by Mr. Murphy, and accepted by the jury, is not meaningful. The '020 patent's specification appears to discuss the distinction between sensing and sampling signals, and it appears to distinguish them differently. One portion of the specification discusses the internal DRAM circuitry between the memory cells and the bus interface pins. *See* '020 Patent, col. 20, l. 20 - col. 24, l. 49 (discussing the DRAM device interface, particularly the input/output circuitry and the DRAM column access). The preferred input/output circuitry connects two input receivers to each pin on the device (which in turn connect to the bus lines). *Id.*, col. 20, ll. 43-52. The pair of input receivers alternate the clock cycles on which they "sample" the inputs. *Id.*, col. 20, ll. 51-52.[8] Drs. Farmwald and Horowitz hold out the "standard clock DRAM sense amp" as being able to satisfy most of the constraints placed on the memory device's input receiver circuitry. *See id.*, col. 21, ll. 18-32. A diagram of this standard sense amp, Figure 11 (shown at right with emphasis added), has distinct connections for "sense" and "sample." In standard operation, the "sense amp goes from sense to sample," which creates the need to



[7] The issue was not raised by the parties' claim construction statement in this case. *See generally* Docket No. 326 (Sept. 12, 2003). In *Rambus Inc. v. Hynix Semiconductor, Inc.*, C-05-00334, the court construed the term "sample" as to "ascertain at a discrete point in time," but no party raised the possibility of a distinction between "sensing" a signal and "sampling" it. 569 F. Supp. 2d 956, 987-88 (N.D. Cal. 2008) (listing proffered constructions).

[8] The preferred embodiment requires multiple input receivers because it takes time for the input receiver to convert the "low-voltage" signal received from the bus into a "full value CMOS logic signal" that the DRAM can interpret. *See* '020 patent, col. 20, ll. 52-64. The difficulty arises from the frequency of the bus increasing so much that new data arrives faster than the input receiver can resolve it; hence the need for multiple input receivers to switch off on sampling the bus. *See id.*

discharge excess capacitance from the circuit (a problem the inventors strive to address). *See id.*, col. 21, ll. 25-32. This discussion strongly suggests that there is a meaningful distinction between sensing and sampling to a person of skill in the art, and that the sense amp in the DRAM's input receiver circuitry does both. This leaves the question, however, of what is a sense amp doing when it is sensing and what is it doing when it is sampling?

Considering the specification as a whole, the court suspects the difference is that the input/output circuits "sense" information when that information is coming from the memory cells and "sample" information when it is coming from the bus. For example, the inventors use the verb "sense" when discussing how precharging allows the "column sense amps to *sense* data quickly" and how page mode access creates efficiency by leaving the data stored in the memory cells in the sense amps, and thus "the DRAM does not need to wait for the data *to be sensed* (it has been *sensed* already) and access time for this data is much shorter than normal access time." *Id.*, col. 10, ll. 13-37 (emphasis added). These are the only instances in which the inventors used "sense" as a verb. On the other hand, the inventors use the verb "sample" to refer to obtaining information from the bus, be it the clock signal, *id.*, col. 19, ll. 27-29, or the bus lines, *id.*, col. 21, ll. 48-52. *See also id.*, col. 22, ll. 49-53 (referring to "input sampler" circuitry); col. 23, ll. 4-7 (same); col. 23, ll. 34-39 (contrasting the time needed to "drive" data onto the bus versus the time needed to "sample" data from it). In other words, it appears that the distinction between "sensing" and "sampling" refers to the source of the information being obtained by the input/output circuitry. On the other hand, the distinction may arise from how the sources of the different signals send information. A memory cell in a DRAM shares its information by discharging its capacitance onto a bitline, and the sensing circuit then amplifying that voltage differential. The bus seems to deal with stronger voltages that do not require such amplification, perhaps allowing the input receiver to "sample" it instead of "sensing" it.

The court's confusion arises from the lackluster quality of the evidence in the record about these technologies. As the record stands, the court is left with a suspicion that Mr. Murphy's distinction between "sensing" and "sampling" is not that of one of skill in the art (like Drs.

Farmwald and Horowitz). Because both the operation code in Redwine comes from the bus, it might be more appropriate to say that the signal is "sampled," not "sensed," and that Redwine does meet the limitation of claim 32 singled out by Mr. Murphy as not being met.

But a suspicion is substantially less than a clear conviction. Without a "firm and definite conviction" that the jury made a mistake, the court cannot order a new trial. Accordingly, Hynix's motion for a new trial regarding the anticipation of claim 32 is denied. Because claim 36 recites the same "sample an operation code" limitation, the court denies Hynix's motion with respect to claim 36 as well.

V. THE LOFGREN REFERENCE, IN LIGHT OF REDWINE

Hynix's final argument focused on the prior art is that the clear weight of the evidence favored finding claim 34 of U.S. Patent No. 5,915,105 invalid in light of Redwine and the "Lofgren reference," U.K. Patent Application No. GB 02197553 A.

A. Claim 34 of the '105 Patent and Its Limitations

Claim 34 of the '105 patent incorporates independent claim 31. With the text of claim 31 included, claim 34 recites the following memory device:

> A synchronous memory device having at least one memory section which includes a plurality of memory cells, the memory device comprises:
>
> internal clock generation circuitry to generate a first internal clock signal and a second internal clock signal, wherein the internal clock generation circuit generates the first and second internal clock signals using at least a first external clock;
>
> an output driver, coupled to the internal clock generation circuitry, the output driver outputs data on a bus in response to the first and second internal clock signals and synchronously with respect to at least the first external clock signal[;]
>
> further including clock receiver circuitry to receive the first external clock and wherein the internal clock generation circuitry includes delay locked loop circuitry, coupled to the clock receiver circuitry, to generate the first internal clock signal and the second internal clock signal using at least the first external clock.

'105 Patent, col. 28, ll. 51-63; col. 29, ll. 9-15. Colloquially, the claim recites a memory device that uses a delay locked loop to control when the device outputs data, or, in Rambus's parlance, "on-chip DLL."

Hynix moved for summary judgment that the claim is invalid as obvious in light of the

teachings of Redwine and Lofgren. The court denied summary judgment, but held that Hynix had established that Redwine disclosed the three limitations of incorporated claim 31, leaving only the final limitation in dispute. *See* Docket Nos. 1789, 13-15 (Mar. 9, 2006); 2026, Ex. 3 (Apr. 18, 2006) (email from Judge Ronald Whyte of March 29, 2006).

As conceded by Mr. Murphy at trial, the final "delay locked loop" limitation of claim 34 was disclosed in the Lofgren reference. Trial Tr. 2639:22-2640:11. Mr. Murphy disputed whether a person of ordinary skill would have combined these references to arrive at claim 34, bringing the court to the present dispute.

B. Testimony Regarding the Combination of Redwine and Lofgren

Mr. Taylor testified that Lofgren, admitted as Trial Exhibit 2012, disclosed a delay locked loop, that is, a "variable delay line that uses feedback to vary the amount of the delay on the delay line and generating a signal having a controlled timing relationship relative to another signal." Trial Tr. 1794:19-1795:12; 1797:7-1799:1 (Mar. 30, 2006). He also testified that Lofgren provides a "clear suggestion" to add a delay locked loop to a DRAM. *Id.* 1799:2-1800:4. Specifically, Lofgren's background states that "delay lines are also used to provide optimum timing for control of high speed dynamic RAM devices, which comprise the main memory of virtually all personal computers." Trial Ex. 2012, col. 1, ll. 14-18.

Mr. Murphy minimized Lofgren's significance. Trial Tr. 2640:3-15. He opined that Lofgren teaches using a DLL to control DRAMs, but that it did not disclose placing a DLL on a DRAM. *Id.* He explained that Lofgren discusses delay lines generally, and that all of the delay lines it discusses were kept off of the DRAM. *Id.* 2640:21-2642:24. He also claimed that by illustrating the external use of delay lines, Lofgren taught away from combining the DLL with the DRAM. *Id.* 2651:5-12.

Hynix's cross-examination of Mr. Murphy on this point adds some clarity. *See generally id.* 2813:14-2821:25. It appears from Mr. Murphy's testimony that Lofgren does not disclose where to place the DLL circuit, and that based on his experience, Mr. Murphy believed that a person of ordinary skill reading Lofgren would have kept Lofgren's DLL off of the DRAM. *Id.*

This exchange triggered a lengthy inquiry into how engineers design circuits and move them

from one context to another. *See generally id.* 2826:9-2832:13 ("Isn't it true, Mr. Murphy, that in the electrical engineering field there is a built-in motivation to combine circuits from one kind of semiconductor to another kind of semiconductor?"). Mr. Murphy conceded that engineers routinely combine different pieces of circuitry. *Id.* 2826:13-2827:10. But to Mr. Murphy, the challenge of electrical engineering is that "it's not necessarily easy to figure out whether adding a particular piece of circuitry to another integrated circuit is necessarily going to give you a benefit or just be a detriment." *Id.* 2831:6-10.[9]

This testimony strikes at the heart of this case. Many of Rambus's claims are drawn toward combinations of prior art circuitry that Drs. Farmwald and Horowitz added to a DRAM's interface, making the DRAM interface more expensive and complex. The court is generally persuaded by the testimony that there is a strong, inherent motivation and incentive to combine existing pieces of circuitry. Yet though this motivation exists, the court also credits Mr. Murphy's testimony that it is not easy to recognize when making such combinations will yield benefits, as opposed to messy, expensive complexity.

Here, Hynix presented evidence as to two motivations to combine Lofgren with the teachings of Redwine. One was the ambivalent statement in Lofgren that delay lines are often used with DRAMs, but Lofgren said nothing one way or the other about placing such circuits on the DRAM. The second was the engineer's inherent motivation to combine circuits. Given the testimony and summary judgment order about which limitations were disclosed in Redwine and Lofgren, the jury's verdict that claim 34 would not have been obvious clearly implies that the jury found that a person of ordinary skill in the art would not have felt a motivation or pressure to combine these features. The court may have reached a different conclusion on this underlying factual question, as it strikes the court as a close call. The closeness of the question, however, compels the court to deny the motion, as the court may only grant a motion for new trial if the jury's finding is against the clear weight of the evidence. The jury's verdict as to claim 34 was not.

[9] Mr. Taylor's testimony in response was limited to testifying that Lofgren does not contain a limit on whether to place its DLL on or off the DRAM. Trial Tr. 3146:4-12.

VI. TWO CHALLENGED EXHIBITS

Hynix takes issue with the court's admission of two exhibits, arguing that they prejudiced Hynix and merit granting a new trial. The first is trial exhibit 5640A. Exhibit 5640A was a redacted article announcing that Dr. Horowitz received an IEEE Solid-State Circuits Technical Field award. As the court noted in ruling on the objection at trial, the article does not constitute hearsay because it was admitted not for its truth, but as a proper secondary consideration of nonobviousness in the form of praise from others in the industry. *See Graham*, 383 U.S. at 17-18; *see also Muniauction, Inc. v. Thomson Corp.*, 532 F. 3d 1318, 1327 (Fed. Cir. 2008). The court recognized that the article discussed Dr. Horowitz's work concerning integrated circuits in respects other than memory interfaces. Accordingly, the court redacted substantial portions of the article, save the discussions of his contributions specifically related to memory interfaces and bandwidth. The court believes it struck the proper balance in permitting Rambus to present evidence relevant to secondary indicia of nonobviousness while shielding Hynix from the unfair prejudice of permitting the jury to hear about Dr. Horowitz's work with no relation to the technologies at issue.

Hynix also contends that trial exhibit 5218 was improperly admitted because it was not properly authenticated. Exhibit 5218 was a memo drafted by S.B. Kil, a Hynix employee, discussing the excellence of the design and operation of the RDRAM and two of the specific features at issue in this case. As the court stated in overruling Hynix's objection to Exhibit 5218, the court found that there was sufficient authentication even though Kil was not available to testify. *See* Trial Tr. 2555:9-21 (Apr. 7, 2006); *see also id.* 2590:3-2593:23 (colloquy about authentication and Rambus's promise not to argue that the exhibit showed copying). Rambus presented Kil's deposition testimony of his role of performing technical evaluations at Hynix during the relevant time, the memo was produced by Hynix, a senior Hynix employee testified that the memo appeared to be a Hynix document, and Hynix does not otherwise contest its authenticity. *See* Trial Tr. 2615:12-19. Finally, Exhibit 5218 discusses some of the features of the claims-in-suit. *See* Trial Ex. 5218 at 13. The memo recognized Rambus's technology and is thus relevant indicia of nonobviousness in the

form of praise in the industry.[10]

The court finds that Exhibits 5640A and 5218 were properly admitted for the reasons stated at trial and, accordingly, provide no basis for a new trial.

VII. OBVIOUSNESS AND *KSR*

As discussed above, Hynix's original new trial motion on obviousness focused on the weight of the evidence. In its three supplemental filings, Hynix contends that the court's instruction and verdict form failed to comply with the law on obviousness as defined by the Supreme Court in *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727 (2007) which came down a little over a year after the verdict in the patent trial.

A. The Obviousness Instruction

Hynix contends that the *KSR* decision justifies a new trial because the court's instruction and verdict form, despite being in conformance with the jury instructions and special verdict form requested by Hynix, were erroneous and prejudicial to Hynix under the rationale of *KSR*. The court gave the following instruction defining obviousness:

> **Obviousness - Definition**
>
> A patent claim is invalid if the claimed invention would have been obvious to a person of ordinary skill in the field at the time the application was filed (in this case, April 18, 1990 for all the Rambus Patents-in-Suit). This means that even if all of the requirements of the claim cannot be found in a single prior art reference that would anticipate the claim, a person of ordinary skill in the field (in this case the field of integrated circuit memory design) who knew about all this prior art would have come up with the claimed invention. ***The claimed invention is not obvious unless there was something in the prior art or within the understanding of a person of ordinary skill in the field that would suggest the claimed invention.*** You must be careful not to determine obviousness using the benefit of hindsight. You should put yourself in the position of a person of ordinary skill in the field at the time the invention was made. You should not consider what is known today or what is learned from the teaching or disclosure of the Rambus patents themselves.
>
> Your conclusion about the question of whether a claim is obvious must be based on several factual decisions that you must make. First, you must decide the scope and content of the prior art. Second, you must decide what difference, if any, exists between the claim's requirements and the prior art that has been presented to you. Third, you must decide the level of ordinary skill in the field that someone

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[10] Hynix argued strenuously that because Mr. Kil was not available to testify, Rambus should not be permitted to introduce his memo into evidence. *See* Trial Tr. 2588:12-2591:14 (Apr. 7, 2006). To be sure, Mr. Kil was beyond the court's subpoena power and Hynix could not force him to appear to testify. But Mr. Kil worked for Hynix, and Hynix noticed his deposition. *See id.* The court is thus less sympathetic to Hynix's plea that it could not get Mr. Kil's testimony about the document.

would have had at the time the claimed invention was made. Finally, you may consider any evidence with respect to the following:

(1) commercial success resulting from the merits of the claimed invention;
(2) any long felt need for the solution provided by the claimed invention;
(3) unsuccessful attempts by others to find the solution provided by the claimed invention;
(4) unexpected superior results from the claimed invention; and
(5) acceptance by others of the claimed invention as shown by praise from others in the field or from the licensing of the claimed invention.

The presence of any of the above five factors may be an indication that a claimed invention would not have been obvious at the time it was made. However, before any particular factor may be considered as evidence of nonobviousness, you must first determine that there is a direct relationship between the evidence of that factor and the claimed invention. The importance of any of the above five factors to your decision on whether the claimed invention would have been obvious is up to you.

Docket No. 2050 (emphasis added). Hynix's argument focuses on the emphasized wording in the instruction.

B. Applicability of Invited Error Principle

Federal Rule of Civil Procedure 51(d)(1)(A) imposes strict limits on a party's right to complain that the court erred in instructing the jury. To move for a new trial based on an error in the court's instruction on obviousness, a party must show that it properly objected to the instruction the court gave. Fed. R. Civ. P. 51(d)(1)(A). Rambus argues that Hynix's "invited error" should end the court's inquiry, citing the Federal Circuit's decision in *Cordis Corp. v. Medtronic Ave, Inc.*, 511 F.3d 1157 (Fed. Cir. 2008), which involved a request for a new trial based on *KSR*'s impact on the law of obviousness. "[E]ven in the case of a change in the law, the Supreme Court has held that the plain error standard applies to a jury instruction to which no objection was made." *Id.* at 1172.[11] The Federal Circuit cited the criminal case of *Johnson v. United States*, 520 U.S. 461, 465-66 (1997) as the authority for its statement. Ninth Circuit law, however, appears to make an exception to Rule 51(d)(1)(A) where the court's instruction is consistent with controlling law as it existed at the time the instruction was given. "No exception is required when it would not have produced any results in the trial court because a solid wall of Circuit authority then foreclosed the point." *Robinson v.*

[11] The Federal Circuit's decision does not control the outcome here because it applies the case's regional circuit's law to matters that are not unique to patent law. In *Cordis*, it applied Third Circuit law. 511 F.3d. at 1172.

Heilman, 563 F.2d 1304, 1307 (9th Cir. 1977) (internal citation omitted). Whether *Johnson* limits the rule from *Robinson* to cases only where there is plain error is unclear. However, the court does not need to reach that issue because it finds that the instruction given was in substantial conformance with *KSR*.

C. The Obviousness Instruction Accords with *KSR*

Hynix first suggests that the court erred by instructing the jury that Rambus's claims were "not obvious unless there was something in the prior art . . . that would suggest the claimed invention." Hynix Supp. Brief at 3:9-11; 7:11-12. Hynix submits that this instruction "directly contradicts" the Supreme Court's rejection of a strict requirement that a teaching, suggestion, or motivation to combine references must be explicit in the prior art. *Id.* at 7:14-15.

Hynix's "direct contradiction" stems from its use of an ellipsis to remove critical language from the court's instruction. The quoted sentence reads in full: "The claimed invention is not obvious unless there was something in the prior art *or within the understanding of a person of ordinary skill in the field* that would suggest the claimed invention." (omitted portion emphasized). This instruction is significantly broader than the "rigid and mandatory" test rejected in *KSR* because the jury was also instructed to consider a person of ordinary skill's "understanding" in deciding whether Rambus's claimed inventions were obvious. This instruction captures *KSR*'s overarching insight that obviousness be approached "expansively" and "flexibly." *See KSR*, 127 S. Ct. at 1739-40. By instructing the jury that any suggestion within the person of ordinary skill's "understanding" could support a finding of obviousness, the jury was free to consider any evidence that might have led a person of ordinary skill to make Rambus's claimed inventions. Indeed, Hynix proffered such evidence during its cross-examination of Mr. Murphy regarding an electrical engineer's ability to combine circuits. Read in its entirety, the court cannot agree that its instruction required an explicit motivation to combine and does not believe the instruction "directly contradicts" *KSR*.

Hynix also finds fault in testimony at trial about whether the prior art contained a teaching, suggestion, or motivation to combine the elements of Rambus's claimed inventions and whether the references "teach away" from Rambus's claimed inventions. Hynix does not explain why any of this

testimony compels a new trial. Nor can it. *KSR* rejected the use of a rigid teaching, suggestion, or motivation test as the only avenue to obviousness. It did not, however, reject using a teaching, suggestion, or motivation analysis. On the contrary, it considered such an inquiry, and testimony pertinent to it, "helpful" in deciding whether an invention is obvious. *See KSR*, 127 S.Ct. at 1241. The fact that Rambus put on testimony that no suggestion to combine existed in the prior art was appropriate and does not justify granting a new trial.

Hynix next argues that *KSR* holds that a combination of known elements is obvious if that combination is within the "common sense" of a person of ordinary skill in the art. *KSR* holds that where market pressure makes something "obvious to try," it "is likely the product not of innovation but of ordinary skill and common sense." *Id.* at 1742. From this, Hynix complains that the court's instruction did not allow the jury to find that Rambus's inventions were within the "common sense" of a person of ordinary skill. But the phrase "within the understanding of a person of ordinary skill in the field" says as much. Inserting Hynix's requested "common sense" in place of the word "understanding" used in the actual instruction shows the emptiness of Hynix's argument. Simply put, there is no meaningful distinction between the instruction given based upon Hynix's proposed instruction and the language Hynix now argues should have been used.

Finally, Hynix argues that *KSR* requires the court to instruct the jury that a "combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." 127 S.Ct. at 1739. Indeed, that an easily-made combination of familiar elements must generate some synergy to be non-obvious is clear from the Court's discussion of its various precedents. *Id.* at 1739-40. That the Court's discussion focused on a long line of Supreme Court precedent is significant. As discussed, Rule 51 provides a possible exception for a failure to object where there has been a supervening change in the law. But the Court did not change the law in this respect. The Supreme Court's emphasized its "over a half century" of obviousness jurisprudence. *See id.* at 1739. To the extent *KSR* changed the law, it rejected the rigid application of the "teaching, suggestion, or motivation" test for proving obviousness — and nothing more. *See Takeda Chemical Industries, Ltd. v. Alphapharm Pty., Ltd.*, 492 F.3d 1350, 1356-57 (Fed. Cir.

2007); *Cordis*, 511 F.3d at 1172; *cf. Roche Palo Alto LLC v. Apotex, Inc.*, 526 F. Supp. 2d 985, 996-97 (N.D. Cal. 2007) (considering, but not deciding, whether *KSR* changed the law enough to prevent issue preclusion and noting that "*KSR*'s actual holding was narrow, as it was limited to the Federal Circuit's application of the TSM test in the matter before it, and did not purport to overrule or overturn any other decisions").

Hynix cannot escape two facts: one, that the court largely used Hynix's proposed obviousness instruction, and two, that Hynix made no objection to the absence of the language it now seeks. Rule 51 does not permit review of a jury instruction in these circumstances.

Further, the court did tell the jury that it could consider whether the claimed invention had "unexpected superior results." Although the jury was told that this secondary factor "may be an indication that a claimed invention would not have been obvious at the time it was made," it certainly implies that predictable results do not suggest nonobviousness. The instruction as given was not error nor can Hynix claim it was incomplete absent an objection at the time it was given. *See Cordis*, 511 F.3d at 1172.

D. The Special Verdict Form on Obviousness

Hynix also asserts error in the jury's verdict form and argues that this error mandates a new trial. The alleged error arises from the form of the interrogatory posed to the jury, namely, "Has Hynix proven that it is highly probable that any of the following claims are invalid because the claimed invention would have been obvious at the time the invention was made to a person having ordinary skill in the art?" The jury was then asked to write yes (for "obvious") or no (for "not obvious") next to each claim at issue. Hynix urges that the court cannot determine whether Rambus's claimed inventions were obvious based on this single question because the jury's answer supplies no factual findings.

Admittedly, this question sheds little light on the jury's underlying factual findings regarding the question of obviousness. This opacity has led the Federal Circuit to disfavor posing only the ultimate issue of obviousness to the jury. *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1356 (Fed. Cir. 2001) (criticizing the "black box" jury form); *Am. Hoist & Derrick Co. v. Sowa & Sons,*

Inc., 725 F.2d 1350, 1360-61 (Fed. Cir. 1984). But Hynix overlooks a critical fact: this verdict form was proposed by Hynix.[12] Detre Decl., Ex. A. A party waives any objection to its own verdict form. *Mitsubishi Elec. Corp. v. Ampex Corp.*, 190 F.3d 1300, 1304 (Fed. Cir. 1999) (finding waiver where appellant's proposed verdict form did not separate bases for invalidity); *Hoechst Celanese Corp. v. BP Chemicals Ltd.*, 78 F.3d 1575, 1581 (Fed. Cir. 1996) (finding waiver where appellant's proposed verdict form merged literal infringement and infringement by the doctrine of equivalents).

Perhaps recognizing the lurking issue of waiver, Hynix suggests that *KSR* changed the law with respect to obviousness by requiring that the jury make specific factual findings. But *KSR* made no such change. The Court's holding was limited to rejecting the rigid use of a teaching, suggestion, motivation test for obviousness. In *dictum*, the Court suggested that a trial court should consider a variety of factual issues like the level of skill in the art, the person of ordinary skill's background knowledge, and the state of the marketplace at the time of the invention. *See KSR*, 127 S.Ct. at 1740-41. It then noted that "[t]o facilitate review, this analysis *should* be made explicit." *Id.* at 1741 (emphasis added). Even were this a holding, it is not a change. The Federal Circuit has long clamored for district courts to use detailed special verdict forms to aid its review of the legal question of obviousness. *McGinley*, 262 F.3d at 1356; *Am. Hoist & Derrick Co.*, 725 F.3d 1360-61; *cf. In re Kahn,* 441 F.3d 977, 988 (Fed. Cir. 2006) (cited in *KSR* and discussing appellate review of PTO rejections on obviousness grounds). Knowing this, Hynix gambled by proposing a condensed interrogatory on obviousness. It was not compelled to do this by the existing law; in fact, it was discouraged from doing so. Perhaps it did not want the jury to have to think too hard about secondary considerations. Maybe it wanted to foreclose appellate review had it won. Nonetheless, Hynix took its chances, and it lost. Hynix has waived any issue with respect to the verdict form.

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[12] Despite the encouragement from the Federal Circuit, it is not an uncommon practice for parties to propose and the court to only ask the jury the ultimate obviousness question.

VIII. ORDER

For the foregoing reasons, the court denies Rambus's motion to strike and denies Hynix's motion for a new trial with respect to anticipation and obviousness.

DATED: 1/16/2009

RONALD M. WHYTE
United States District Judge

Notice of this document has been electronically sent to counsel in: C-00-20905.

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Dated: 1/16/2009

TSF

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