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E-filed: 12/15/2008

IN THE UNITED STATES DISTRICT COURT
FOR THE NORTHERN DISTRICT OF CALIFORNIA
SAN JOSE DIVISION

RAMBUS INC.,

Plaintiff,

v.

HYNIX SEMICONDUCTOR INC., HYNIX
SEMICONDUCTOR AMERICA INC.,
HYNIX SEMICONDUCTOR
MANUFACTURING AMERICA INC.,

SAMSUNG ELECTRONICS CO., LTD.,
SAMSUNG ELECTRONICS AMERICA,
INC., SAMSUNG SEMICONDUCTOR, INC.,
SAMSUNG AUSTIN SEMICONDUCTOR,
L.P.,

NANYA TECHNOLOGY CORPORATION,
NANYA TECHNOLOGY CORPORATION
U.S.A.,

Defendants.

No. C-05-00334 RMW

ORDER GRANTING IN PART AND
DENYING IN PART RAMBUS'S MOTION
TO STRIKE; DENYING MOTION FOR
SUMMARY JUDGMENT No. 1 OF
INVALIDITY; AND STRIKING MOTION
FOR SUMMARY JUDGMENT No. 2 OF
INVALIDITY

[Re Docket Nos. 2406, 2458, 2533]

RAMBUS INC.,

Plaintiff,

v.

SAMSUNG ELECTRONICS CO., LTD.,
SAMSUNG ELECTRONICS AMERICA,
INC., SAMSUNG SEMICONDUCTOR, INC.,
SAMSUNG AUSTIN SEMICONDUCTOR,
L.P.,

Defendants.

No. C-05-02298 RMW

[Re Docket Nos. 1251, 1286, 1327]

ORDER GRANTING IN PART AND DENYING IN PART RAMBUS'S MOTION TO STRIKE; DENYING MOTION FOR
SUMMARY JUDGMENT No. 1 OF INVALIDITY; AND STRIKING MOTION FOR SUMMARY JUDGMENT No. 2 OF
INVALIDITY — C-05-00334 RMW; C-05-02298-RMW; C-06-00244-RMW

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RAMBUS INC.,
Plaintiff,
v.
MICRON TECHNOLOGY, INC., and
MICRON SEMICONDUCTOR PRODUCTS,
INC.
Defendants.

No. C-06-00244 RMW
[Re Docket Nos. 1490, 1525, 1562]

Rambus has accused the Manufacturers¹ of infringing various patents. Trial is scheduled for January 19, 2009. Pursuant to a case management deadline for filing summary judgment motions, the Manufacturers have filed two motions for summary judgment of invalidity pursuant to 35 U.S.C. § 102(b). Rambus opposes both motions. Rambus also moves to strike the two motions for violating a case management order. The court has reviewed the papers and considered the arguments of counsel. For the following reasons, the court grants Rambus's motion to strike the Manufacturers' summary judgment motion no. 2 and the court does not consider it. The court denies Rambus's motion to strike the Manufacturers' summary judgment motion no. 1. The court denies the Manufacturers' motion for summary judgment no. 1.

I. RAMBUS'S MOTION TO STRIKE

Before turning to the Manufacturers' motions for summary judgment of invalidity, the court must address Rambus's motion to strike those motions.

A. Background

On April 24, 2007, the court entered a joint case management order "to adopt special procedures for managing the complex issues and multiple parties in future proceedings" in these cases. *E.g., Rambus Inc. v. Hynix Semiconductor, Inc.*, C-05-00334, Docket No. 174 at 1 (N.D. Cal. Apr. 24, 2007). The order included a schedule for trying Rambus's patent claims and the Manufacturers' defenses. *Id.*, at 2 & Attach. C. The schedule set deadlines for filing infringement

¹ The court collectively refers to the Hynix, Micron, Nanya, and Samsung entities in this suit as "the Manufacturers."

1 contentions, a joint claim construction statement, claim construction briefs, and "summary judgment
2 motions that depend on claim construction issues." *Id.*, Attach. C. At the deadline for filing such
3 summary judgment motions, Rambus filed motions for summary judgment of infringement and the
4 Manufacturers filed motions for summary judgment of non-infringement and invalidity pursuant to
5 35 U.S.C. § 112.

6 The court issued another scheduling order as the trial date approached. *See* Docket No. 1963
7 (Jul. 16, 2008). The order set a deadline for dispositive motions. It explained that:

8 Given these cases' histories, a few deadlines may require clarification. A
9 "dispositive motion" is a motion for summary judgment that disposes of a portion of
10 the case. The court will *not* entertain any dispositive motion that turns on an issue
11 of claim construction. Such motions were supposed to be filed on October 5, 2007.
12 *See* Joint Case Management Order, Attachment C (Apr. 24, 2007).

13 *Id.* at 3 (emphasis in original).

14 On October 24, the Manufacturers filed two motions for summary judgment of invalidity
15 pursuant to 35 U.S.C. § 102(b). The first motion's introduction argues that:

16 Rambus asked the Court to construe its claims broadly. Under the constructions it
17 requested, and which the Court adopted, the five claims at issue on this motion
18 indisputably read directly on the Bennett prior art. Because there is no genuine issue
19 of fact for the jury, the Court should resolve these claims against Rambus before
20 trial.

21 Docket No. 2406, 2:5-8 (Oct. 24, 2008). The second motion similarly argues that "each and every
22 limitation of the asserted claims are present in the Novak patent. . . . There is no genuine issue of
23 material fact regarding the disclosure of the relevant limitations in Novak." Docket No. 2458, 1:8-
24 13 (Oct. 24, 2008).

25 **B. Analysis**

26 Rambus moves to strike the Manufacturers' two motions for summary judgment for violating
27 the court's scheduling orders. The Manufacturers first argue that the motions do not "turn on issues
28 of claim construction" because the motions "do not require the Court to resolve an issue of claim
construction." The court disagrees. "[I]t is axiomatic that that which would literally infringe if later
anticipates if earlier." *Bristol-Myers Squibb Co. v. Ben Venue Laboratories, Inc.*, 246 F.3d 1368,
1378 (Fed. Cir. 2001). The parties clearly understood that the court's order set a deadline for filing

1 motions for summary judgment of infringement and non-infringement that turn on the interpretation
2 of a claim term. Anticipation involves the same inquiry as infringement; there is no reason to
3 believe that one "turns on issues of claim construction" while the other does not.

4 The Manufacturers next argue that the court's order could not have contemplated its motions
5 for summary judgment of invalidity because as of the court's deadline final invalidity contentions
6 were not yet due and discovery had not yet closed. The Manufacturers argue that even if this
7 interpretation is wrong, it was reasonable and their failure to file their two motions timely should be
8 forgiven. This argument fails because there is nothing inherently unfair about requiring motions that
9 depend on how claims are interpreted to be filed before final contentions or before all discovery is
10 completed. If the Manufacturers believed they needed additional time, they could have filed a
11 motion asking for relief from the deadline. This argument also cannot explain why the parties acted
12 as though motions for summary judgment of infringement and non-infringement were due in
13 October 2007. Finally, and most importantly, the argument overlooks the court's well-known desire
14 to grapple with issues of infringement and validity while simultaneously addressing claim
15 construction. Indeed, the court remarked on the Manufacturers' failure to file motions for summary
16 judgment of invalidity and the difficulties that failure created in understanding the scope of the
17 parties' claim construction dispute. *Rambus Inc. v. Hynix Semiconductor, Inc.*, 569 F. Supp. 2d 946,
18 971 (N.D. Cal. 2008) ("This leaves the court to speculate as to why this dispute is material. Either
19 this dispute is about nothing, or the Manufacturers are suggesting that the court construe a claim so
20 broadly that it is invalid. This uncertainty defeats the purpose of the court's case management
21 order."). If there could be any doubt about the meaning of the court's case management order, this
22 passage in the claim construction order made it clear that the deadline for filing such motions had
23 passed. Because the Manufacturers' interpretation of the court's order is not reasonable, the court
24 rejects it.

25 Of course, a party may seek relief from a case management order upon a showing of good
26 cause. *Zivkovic v. S. Cal. Edison Co.*, 302 F.3d 1080, 1087-88 (9th Cir.2002); *Hynix Semiconductor*
27 *Inc. v. Rambus Inc.*, 250 F.R.D. 452 (N.D. Cal. 2008). The court therefore treats the Manufacturers'

1 motions for summary judgment as implicitly requesting relief from the court's case management
2 orders. *Cf. United States v. 1982 Sanger 24' Spectra Boat*, 738 F.2d 1043, 1046 (9th Cir.1984)
3 ("The moving party's label for its motion is not controlling. Rather, the court will construe it,
4 however styled, to be the type proper for relief requested.").

5 The Manufacturers' first motion for summary judgment asserts that U.S. Patent No.
6 4,734,909 anticipates some of Rambus's claims. The Manufacturers point out that the patent was not
7 cited in the prosecution history of Rambus's patents, and suggest that they did not discover the
8 patent's applicability to this case until July 25, 2008. *See* Decl. of Michael Eisenberg, Docket No.
9 2393 ¶ 2 (Oct. 24, 2008) ("I discovered U.S. Patent No. 4,734,909 (the "Bennett Patent") on or
10 around July 25, 2008 while reviewing prior art."). Though the Eisenberg Declaration does not
11 clearly state that *the Manufacturers* were unaware of the Bennett patent until July 25, 2008, it does
12 support the inference that the Manufacturers did not know of the Bennett patent when the October
13 2007 summary judgment filing deadline passed. *Accord* Tr. 73:20-74:25 (Dec. 10, 2008)
14 (representations by Messrs. Berezin and Powers that the Manufacturers did not find Bennett until
15 after October 2007). Because the Manufacturers could not have filed their motion for summary
16 judgment with respect to the Bennett patent by the deadline set by the court, the Manufacturers have
17 established good cause for relief with respect to the Bennett motion.

18 The Manufacturers do not attempt a similar showing with respect to the Novak patent, U.S.
19 Patent No. 4,663,735. Nor could they. Multiple Rambus patents-in-suit disclose the Novak patent
20 as a cited reference. *See, e.g.*, U.S. Patent Nos. 6,266,285 (page 2); 6,314,051 (page 1); 6,324,120
21 (page 2). The Manufacturers did not have to "discover" the Novak patent or its importance to the
22 Farmwald/Horowitz patents-in-suit; the patent prosecution process had already done so. The
23 Manufacturers' failure to make their arguments based on the Novak patent in a diligent and timely
24 manner dooms their implied effort to seek relief from the case management order's deadline. *See*
25 *Johnson v. Mammoth Recreations, Inc.*, 975 F.2d 604, 610 (9th Cir.1992).

26 Accordingly, the court denies Rambus's motion to strike with respect to the Manufacturers'
27 first motion for summary judgment and grants Rambus's motion with respect to the Manufacturers'

28 ORDER GRANTING IN PART AND DENYING IN PART RAMBUS'S MOTION TO STRIKE; DENYING MOTION FOR
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1 second. The Manufacturers may of course make their invalidity arguments based on Novak at trial.
2 Their failure to comply with the court's case management order, however, forfeits their right to bring
3 a summary judgment motion and precludes them from making their Novak arguments at this
4 juncture.

5 II. LEGAL STANDARD

6 A. Summary Judgment

7 Ninth Circuit law governing summary judgment procedures applies because this procedural
8 law does not relate to substantive patent law principles. *In re Cygnus Telecomm'ns Tech., LLC,*
9 *Patent Litig.*, 536 F.3d 1343, 1351-52 (Fed. Cir. 2008). Because a patent claim is presumed to be
10 valid, the Manufacturers bear the burden of persuasion at trial as to whether or not each asserted
11 claim is invalid. 35 U.S.C § 282. Thus, as movants, the Manufacturers bear the burden of
12 producing evidence showing that the reference in question discloses each limitation of each claim
13 that the Manufacturers argue is invalid.

14 If the Manufacturers fail to meet this burden of production, Rambus need not produce
15 anything to defeat summary judgment. *Nissan Fire & Marine Ins. Co., Ltd. v. Fritz Companies,*
16 *Inc.*, 210 F.3d 1099, 1102-03 (9th Cir. 2000). If the Manufacturers satisfy this burden of production,
17 Rambus must produce evidence such that a jury, drawing all inferences in favor of Rambus, could
18 find that the reference does not anticipate the claim at issue. *Id.* If Rambus produces such evidence,
19 the motion must be denied. *Id.* A failure by Rambus to adduce such evidence, however, entitles the
20 Manufacturers to summary judgment. *Id.*

21 A mere disagreement between experts is not sufficient to raise a triable issue of fact. An
22 expert's opinion must be supported by facts to support or defeat a motion for summary judgment.
23 The Federal Circuit has held that an expert's "unsupported conclusion" as to whether there is
24 infringement or whether a claim limitation is satisfied is not sufficient. *Arthur A. Collins, Inc. v. N.*
25 *Telecom Ltd.*, 216 F.3d 1042, 1046-48 (Fed. Cir. 2000). Instead, the expert must "set forth the
26 factual foundation for his opinion – such as a statement regarding the structure in the accused
27 product – in sufficient detail for the court to determine whether that factual foundation would

1 support a finding of infringement under the claim construction adopted by the court, with all
2 reasonable inferences drawn in favor of the non-movant." *Id.* at 1047-48. This requirement is not
3 unique to the issue of infringement. It is based on Rule 56(e)(1)'s requirement that supporting or
4 opposing declarations "be made on personal knowledge, set out facts that would be admissible in
5 evidence, and show that the affiant is competent to testify[.]" Thus, the stringent requirement
6 discussed in *Arthur A. Collins* applies equally to motions addressing invalidity. This standard is
7 important here because the parties rely solely on the declarations of their technical experts to support
8 or oppose the Manufacturers' motion for summary judgment.

9 **B. Anticipation**

10 A patent claim is invalid if the claimed invention was described in a printed publication more
11 than a year prior to the patent's application date. 35 U.S.C. § 102(b). Here, the parties agree that the
12 Bennett patent is a printed publication and that it predates by more than one year the filing of the
13 original application for all of the claims-in-suit. The only dispute is whether the Bennett patent
14 describes each of the claimed inventions.

15 This dispute raises a question of fact. *Scripps Clinic & Research Foundation v. Genentech,*
16 *Inc.*, 927 F.2d 1565, 1576 (Fed. Cir. 1991). A reference anticipates a claim if it includes *all* of the
17 claim's elements or limitations. *Id.* The reference's disclosure of each limitation need not be
18 explicit; a limitation may be inherently disclosed if the prior art "necessarily functions" in accord
19 with the inherent limitation. *Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375-76 (Fed. Cir.
20 2005). Frequently, this occurs because "[a] patent need not teach, and preferably omits, what is well
21 known in the art." *Spectra-Physics, Inc. v. Coherent, Inc.*, 827 F.2d 1524, 1534 (Fed. Cir. 1987).
22 This is not to suggest, however, that an inherently disclosed limitation *must* be well-known to one of
23 ordinary skill. *MEHL/Biophile Int'l Corp. v. Milgraum*, 192 F.3d 1362, 1365 (Fed. Cir. 1999)
24 ("Inherency is not necessarily coterminous with the knowledge of those of ordinary skill in the art.").

25 In practice, the anticipation inquiry is identical to the infringement inquiry, albeit with a clear
26 and convincing standard of evidence. *Bristol-Myers Squibb*, 246 F.3d at 1378. Though it is a
27 question of fact, anticipation, like infringement, is amenable to summary judgment where there is no

1 issue of material fact regarding the reference's disclosure. *Scripps*, 927 F.2d at 1576; *see, e.g.*,
2 *Golden Bridge Tech., Inc. v. Nokia, Inc.*, 527 F.3d 1318 (Fed. Cir. 2008) (affirming summary
3 judgment of anticipation); *Leggett & Platt, Inc. v. VUTEk, Inc.*, 537 F.3d 1349 (Fed. Cir. 2008)
4 (same). This suggests that summary judgment may often be appropriate due to the scarcity of
5 genuine disputes over the content of a disclosure or operation of a device. Nonetheless, "[t]rial by
6 document is an inadequate substitute for trial with witnesses, who are subject to examination and
7 cross-examination in the presence of the decision-maker." *Scripps*, 927 F.2d at 1578. This
8 admonition carries particular weight with respect to this motion because of the age (over 26 years
9 old), size (hundreds of pages), and complexity of the allegedly anticipating reference. Where no
10 testimony explains the contents or context of this reference, the court declines to enter summary
11 judgment. *Cf. Invitrogen Corp. v. Clontech Labs., Inc.*, 429 F.3d 1052, 1068-69 (Fed. Cir. 2005)
12 ("Unsubstantiated attorney argument regarding the meaning of technical evidence is no substitute for
13 competent, substantiated expert testimony. It does not, and cannot, support [a party's] burden on
14 summary judgment."); *Biotec Biologische Naturverpackungen GmbH & Co. KG v. Biocorp, Inc.*,
15 249 F.3d 1341, 1353 (Fed. Cir. 2001) (rejecting the argument that "that [defendants are] under no
16 obligation to explain their theories of invalidity" and holding that "[i]t is not the trial judge's burden
17 to search through lengthy technologic documents for possible evidence").

18 III. THE BENNETT PATENT

19 The Manufacturers must establish facts that show that the Bennett patent discloses each
20 limitation of each claim that the Manufacturers argue is invalid. To meet their burden, the
21 Manufacturers rely on their technical expert Joseph McAlexander, an electrical engineer, to explain
22 DRAM technology and the voluminous Bennett patent. Rambus relies on its technical expert,
23 Robert J. Murphy, also an electrical engineer, to rebut the Manufacturers' showing. Because the
24 Manufacturers must make a *prima facie* showing that the Bennett patent discloses each limitation of
25 a claim, the court's analysis begins with the Manufacturers' proffer of evidence as to each allegedly
26 invalid claim.

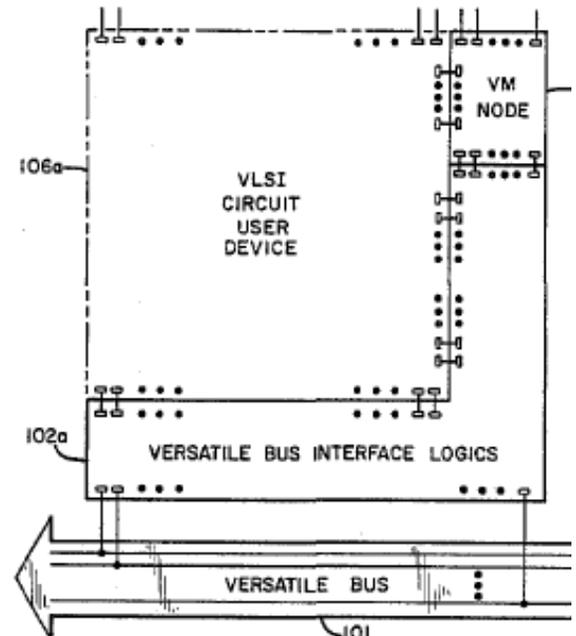
27 A. An Overview of the Bennett Patent

28 ORDER GRANTING IN PART AND DENYING IN PART RAMBUS'S MOTION TO STRIKE; DENYING MOTION FOR
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1 U.S. Patent No. 4,734,909 (hereinafter "Bennett") uses 254 pages of figures and 282 columns
2 of text to disclose a versatile bus interface. Due to the complexity of the information it contains,
3 some basic overview is necessary.

4 **1. The Versatile Bus Interface and Configuration Register**

5 The Bennett inventors sought to provide "a scheme and an apparatus of bused digital
6 communications interconnection, especially as between numbers of very large scale integrated
7 (VLSI) circuit devices [with so many virtues] that it will become an interface standard embraced by
8 diverse designers of myriad devices." Bennett, col. 12, ll. 14-25. The new interface placed its logic
9 directly "upon the same chip substrate" as the very
10 large scale integrated circuit (VLSIC) devices that
11 it connected. *Id.*, col. 12, ll. 28-32. The interface
12 consisted of a set of pins that connected to the
13 Versatile Bus and an optional second set of pins
14 that connect to a maintenance processor that
15 supplies, among other things, initial settings for
16 each VLSIC device. *Id.*, col. 12, ll. 32-45. This
17 placement of the Bennett interface on the same
18 chip as the VLSIC device is shown in the block
19 diagram (a cropped version of Figure 1 of the



20 patent) at right. The VLSIC device appears in the upper left, while the first set of pins consisting of
21 the bus interface appear on the bottom (and connect to the bus) while the optional, second set of
22 pins appears in the upper right (and do not connect to the bus).

23 An important goal of the inventors was to create a flexible interface. *Id.*, col. 15, l. 22 - col.
24 17, l. 54; col. 35, ll. 31-34. The Versatile Bus maintained a standard voltage level and clock
25 frequency, but permitted a variety of other features to be configured to meet a designer's wishes. *Id.*,
26 col. 35, ll. 34-44. It accomplished this by placing a configuration register on each device in the
27 environment. *Id.*, col. 35, ll. 44-51. The configuration register could be set when the device was

1 made (and then never changed). *See id.*, col. 35, ll. 48-50. Alternatively, the configuration register
2 could connect to a maintenance processor through the optional second set of pins (the "VM Node
3 maintenance interface"). *Id.*, col. 35, ll. 50-54. This second interface to the maintenance processor
4 permitted the configuration register to be set or reset as desired. *Id.*

5 The preferred embodiment of the Versatile Bus interface required 37 pins to connect each
6 VLSIC device in the environment to a Versatile Bus, though the interface permitted devices to
7 employ as few as 3 pins and still access the Versatile Bus. *Id.*, col. 36, ll. 62-68;² col. 45, l. 49 - col.
8 46, l. 17. Eight basic parameters (or "primitives") governed the interface. *Id.*, col. 37, l. 63 - col. 38,
9 l. 35. The parameters were: (1) number of arbitration lines per group (and pins so devoted); (2)
10 number of arbitration groups; (3) arbitration choices; (4) number of slave ID/function parameters
11 (and pins so devoted); (5) number of slave ID/function cycles; (6) number of wait lines (and pins do
12 devoted); (7) number of data lines (and pins so devoted); and (8) number of data bits. *Id.*, col. 38, ll.
13 21-35.

14 Each primitive was set by the value of three binary cells in the configuration register (thus
15 permitting each parameter to have up to 2³ or 8 settings). *Id.*, col. 38, ll. 56-60. In other words, the
16 configuration register contained 24 binary cells that contained the values of the eight interface
17 parameters. *See id.* As discussed, the register could be hard-wired with certain parameter values.
18 *Id.*, col. 38, ll. 61-65. The inventors preferred, however, to connect the configuration register's 24
19 cells through the VM Node interface to the maintenance processor to allow these values to be
20 changed. *Id.*, col. 38, l. 64 - col. 39, l. 9.

21 Throughout the Bennett patent, the inventors refer to different Versatile Bus configurations
22 by an 8-digit string of numbers, with each digit ranging from one to six. For example, the preferred
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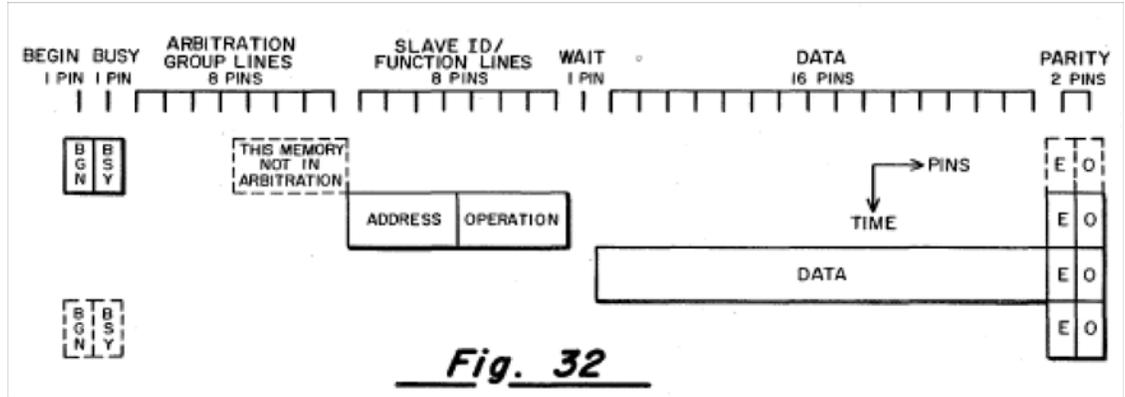
24 ² The inventors considered existing package technology of the time and envisioned
25 placing three distinct and complete interfaces on each device to permit the device to connect to three
26 different busses. *Id.*, col. 36, ll. 62-68. This explains the inventors' later comment that "a VLSIC chip
27 has on the order of 100 pins." *Id.*, col. 66, ll. 65-68. In that portion of the Bennett specification, the
28 inventors remarked that adding a pin to receive a clock signal was a negligible addition to the
complexity of the device. *See id.* Their discussion assumed that the VLSIC device maintained three
separate bus interfaces.

1 embodiment of the Versatile Bus is 55255355. *See, e.g.*, col. 38, ll. 48-50. Each digit of the eight-
2 digit string refers to the value of one of the eight interface parameters or primitives. The key to
3 interpreting the values of each primitive appears in Figure 3 of the Bennett patent. Thus, the fourth
4 digit (slave ID/function lines) dictates how many pins the device has dedicated to sending slave ID
5 and function information; it ranges from "multiplexed" (with arbitration and wait information) when
6 the value is 1 to eight dedicated pins when the value is 5 (as it is in the preferred embodiment). *See*
7 *id.*, Fig. 3. Likewise, the seventh digit dictates the number of data pins and ranges from one
8 (parameter value of 1) to 16 (parameter value of 5). *Id.*

9 It is critical to note that devices in the Versatile Bus interface system need not possess the
10 maximum range of functionality. *See id.*, col. 37, l. 60 - col. 38, l. 5. Any device that can
11 accommodate a certain value of a primitive can also operate at all lower values. *Id.* Thus, a device
12 designer could build a device with as many as 16 data pins, but that device could operate using only
13 one of the data pins if the Versatile Bus environment so required. What made the Versatile Bus
14 "versatile" was that it was "always possible to find a value for each primitive that [was] supported by
15 all the chips that are to be used together, and therefore there [was] always some Versatile Bus
16 configuration that will allow their interconnection." *Id.*, col. 38, ll. 1-6.

17 A final word on the interplay between parameters VII and VIII is necessary to understand the
18 parties' invalidity arguments. As discussed, parameter VII dictates the number of data pins that will
19 be used in the Versatile Bus configuration. *See id.*, col. 16, ll. 59-63. Parameter VIII dictates the
20 number of data bits in a single data word. *Id.*, col. 16, ll. 63-68. These parameters depend on each
21 other; they are not independent because Parameter VIII depends on Parameter VII. *Id.*, col. 17, ll. 1-
22 19; col. 82, ll. 10-16. The number of data lines (Parameter VII) must be less than or equal to the
23 number of bits in a data word (Parameter VIII). *Id.*, col. 82, ll. 10-16. In practice, the Bennett
24 patent's illustrations overwhelmingly configure parameters VII and VIII to the same value to ensure
25 that the entire data word can be transferred in one clock cycle. *See, e.g., id.*, col. 85, l. 67 - col. 86, l.
26 4 (same values in multiplexed operations illustrations); col. 92, l. 32 - col. 96, l. 42 (same value in
27 every sample memory operation). Nonetheless, the number of data lines can be less than the number

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46, l. 53 - col. 47, l. 17. The BEGIN signal going high indicates the start of a transaction. *Id.* The BUSY signal effectively means "the bus will be busy next cycle." *See id.* When the BUSY signal is high, the transaction is ongoing; when it goes low, the transaction terminates on the next clock cycle. *See id.* In this simple memory operation, the BUSY signal remains low, indicating that a second operation (not shown) could begin on the next clock cycle. *Id.*, col. 92, ll. 56-63.³ The memory device in this sample operation is a slave device (i.e., it cannot take control of the bus) and it therefore ignores the simultaneous signals sent over the arbitration bus lines. *Id.*, col. 92, l. 63 - col. 93, l. 1.⁴

On the second clock cycle, the memory device receives address and "operation" information over the slave ID/function pins. *Id.*, col. 93, ll. 12-26. In this sample operation, the inventors partition the field of information equally (and arbitrarily) into address and operation. *Id.* This example implicitly contemplates a small enough memory that four bits of address information suffice to identify which memory array to read data from or write data into. *See id.* Having selected the address in memory and determined the type of operation, the memory device can send or receive

³ The memory devices in the Bennett system can accomplish different aspects of multiple operations simultaneously. In other words, the Bennett memory devices "pipeline" operations, leading to higher bus utilization and faster operation.

⁴ Activity is shown on only 4 of the arbitration pins because the Versatile Bus configuration of this example is a 42252255, a lower configuration than the preferred embodiment configuration. *Id.*, col. 92, ll 31-36. As shown in Figure 3, a parameter I value of 4 implies that there are only 4 arbitration pins connecting to the bus.

1 data on the third clock cycle and effectively⁵ complete the transaction. *Id.*, col. 93, ll. 27-28.

2 The sample operation shown above occurred in a 42252255 bus configuration. Figure 33
 3 depicts a similar sample operation, but this time in a 43112244 bus configuration. *Id.*, col. 93, ll. 56-
 4 58. The configuration is meant to highlight the Versatile Bus's capacity to multiplex various types
 5 of information. *See id.*, col. 93, l. 56 - col. 94, l. 8. For example, parameter IV (the number of slave
 6 ID/function lines) is equal to one, i.e., it is programmed to multiplex slave ID and function
 7 information over the data lines. *Id.* Parameter VII is equal to four, i.e., the configuration uses eight
 8 data lines. *See id.* When the slave ID/function information is multiplexed, the system transmits
 9 slave ID/function information over Parameter VII's number of data lines. *Id.*, col. 94, ll. 2-5. This
 10 produces the sample memory operation shown below (using the same x-axis as Figure 32):

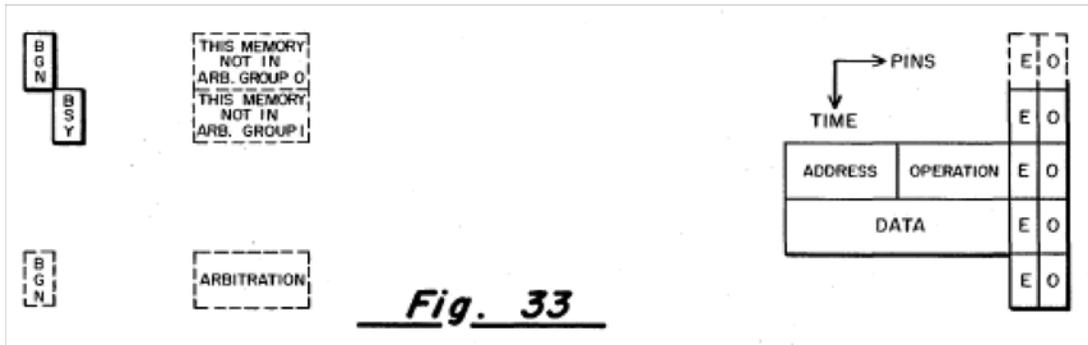


Fig. 33

17 As desired, the slave ID/function information arrives at the memory device over the configuration's
 18 eight data pins. The memory device sends or receives data on the following clock cycle. As in the
 19 prior configuration, parameter VI (the number of wait lines) is set to 2, i.e., "no wait lines are
 20 employed." *Id.*, col. 94, l. 2.

21 **3. Block Memory Operations**

22 The Versatile Bus interface also supported "block" read and write operations. Instead of
 23 transferring a single data word, block operations permitted an operation that could continue
 24 indefinitely. *See id.*, col. 17, ll. 19-29 (noting that the potential for "millions of data words" to flow

26 ⁵ The rightmost pins convey parity information that allows the devices to check for errors
 27 in the transmission of information. The parity bits lag their corresponding information by one clock
 28 cycle. *Id.*, col. 93, ll. 28-46. Thus, even after the data is sent or received on the third clock cycle, parity
 information related to the data is being sent on the fourth clock cycle.

1 as block data "most emphatically" lacks relationship to the values of Parameters VII and VIII). To
2 trigger a block operation, the master sent an address and an integer to the memory device. *Id.*, col.
3 91, ll. 54-55. In a read operation, the memory device transmitted the first data word from the
4 address. *Id.*, col. 91, ll. 56-57. The memory device then added the integer to the first address to
5 obtain a second address and transmitted the second data word from the second address. *Id.*, col. 91,
6 ll. 57-59. The memory device continued to operate in a loop by adding the same integer to the most
7 recent address and transmitting data words indefinitely. *See id.* The block read operation only
8 terminated when the master deactivated the BUSY line. *Id.*, col. 91, ll. 56-61. A similar protocol of
9 adding an integer to the most recent address permitted block write operations. *Id.*, col. 91, ll. 62-68.

10 4. The WAIT Signal's Role in Operations

11 In the Versatile Bus configurations discussed above, parameter VI (the number of wait lines)
12 was set to 2, which corresponds to omitting the WAIT signal from the configurations. *See Bennett,*
13 *Fig. 3.* In configurations that omit a wait line (parameter VI equal to 2), slave devices must accept
14 transactions. *Id.*, col. 77, ll. 26-29. The inventors' preferred embodiment of the Versatile Bus
15 interface either excluded the WAIT line or included a single pin for transmitting WAIT information.
16 *Id.*, col. 76, ll. 1-4. The general purpose of the WAIT signal is to allow a slave device to signal to
17 the master device that it is not "absorbing" the information being sent in the pending transaction.
18 *Id.*, col. 76, ll. 24-30. A WAIT signal of zero informs the master that the slave device will accept the
19 transaction. *Id.*, col. 75, ll. 62-65. A WAIT signal of one (or high) indicates a problem, but the
20 inventors left the precise meaning of the WAIT signal open to future system designers, with a few
21 suggested conventions. *Id.*, col. 76, ll. 7-24.

22 The decision to multiplex the WAIT signal or to send it over a separate pin can have a
23 curious impact on the overall timing of operations. This impact appears in Figures 25a and 25b,
24 reproduced below:

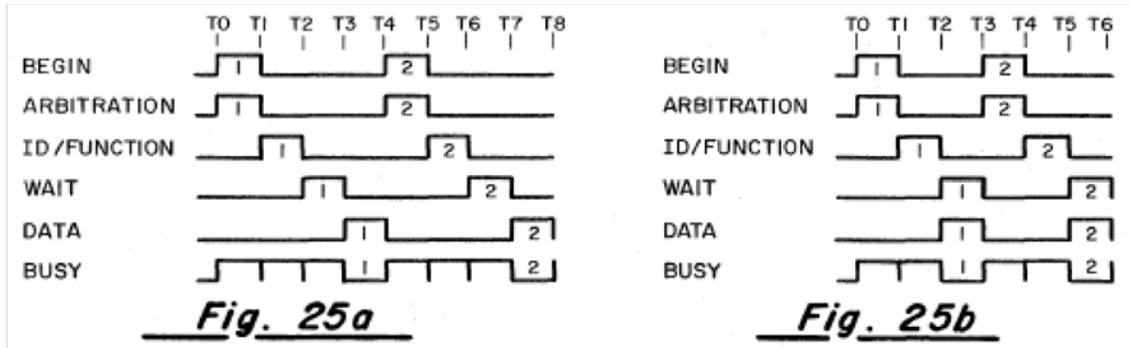


Figure 25a depicts a Versatile Bus configuration of 122121XX. *Id.*, col. 85, ll. 49-59.

Parameters I, IV, and VI all equal 1, meaning that arbitration, ID/function, and wait information are all multiplexed over the data pins. *See id.*, col. 86, ll. 4-9. Fig. 3. Parameters II and V are selected to ensure that the arbitration and ID/function phases of an operation each require one clock cycle. *Id.*, col. 85, l. 67 - col. 86, l. 4. Likewise, setting parameter VII to equal parameter VIII ensures that all data is transferred over one clock cycle. *Id.* Thus, a completely multiplexed operation takes four complete cycles: one for arbitration, one for ID/function, one for wait information, and one for data. *Id.*, col. 86, ll. 27-30.

Figure 25b depicts the timing of an operation with configuration 122123XX. *Id.*, col. 85, ll. 31-41. The only difference in the configuration is the change in parameter VI from 1 to 3. In other words, Figure 25b uses a dedicated wait pin instead of multiplexing wait information over the data lines. *Id.* This permits the slave devices to transmit wait information at the same time that data is transmitted, reducing the total operation time to three clock cycles. *Id.*, col. 86, ll. 37-41.

B. Claim 16 of U.S. Patent No. 6,266,285

1. The Asserted Claim

The Manufacturers assert that the Bennett patent anticipates claim 16 of U.S. Patent No. 6,266,285. The claim generally recites a method of operating a memory device involving: (1) receiving an external clock signal, (2) receiving a delay time value and storing it in a register, (3) receiving a request for a write operation, and finally (4) sampling data in response to the write operation after the delay time transpires. Rambus colloquially refers to this claim as covering the

1 implementation of programmable write latency. The full text of the claim follows, with the
2 language of the claim from which it depends incorporated in brackets:

3 [[A method of operation in a memory device having a section of memory which
4 includes a plurality of memory cells, the method comprising:

5 receiving an external clock signal;

6 receiving a request for a write operation synchronously with respect to the external
clock signal; and

7 sampling data, in response to the request for a write operation, after a programmable
8 number of clock cycles of the external clock signal transpire.]]

9 [further including storing a value which is representative of the programmable
10 number of clock cycles of the external clock in a programmable register on the
memory device.]

11 further including receiving a set register request, wherein in response to the set
register request, the memory device stores the value in the register.

12 2. The Evidence With Respect to Each Limitation

13 In this section, the court determines whether the Manufacturers have met their burden of
14 producing clear and convincing evidence showing that the Bennett patent discloses each limitation
15 of claim 16. The court also determines whether Rambus has rebutted this showing and whether the
16 Manufacturers have carried their burden of persuasion with respect to each limitation.

17 a. A Memory Device

18 Mr. McAlexander states that the Bennett patent discloses a memory device. Lee Decl., Ex. 3
19 at C-7 (hereinafter "Bennett Chart"). He points to various portions of the Bennett patent that
20 describe the different users of the patent's new bus interface. *See id.* For example, the Bennett
21 patent describes its interface as "intended to be built with a CPU, IOC, Memory, or similar User
22 device for signal and data exchange." Bennett, col. 35, ll. 60-62. The Bennett patent again defines a
23 "User" in its bus interface as "the logics (e.g., a central processor or a memory or whatever) which
24 communicates through the Versatile Bus Interface Logics, such as are taught by this specification,
25 onto the Versatile Bus." *Id.*, col. 40, ll. 52-55. The Bennett patent further lists the memory
26 operations that must be defined in the bus interface to "avoid a flexibility stifling proliferation of
27 memory interfaces." *See id.* col. 90, l. 42 - col. 92, l. 8.

1 Mr. McAlexander further asserts that "[t]he VLSI memory device of Bennett necessarily
2 includes memory cells." Bennett Chart, C-7. Mr. McAlexander does not explain why, but this is
3 clear from the nature of memory devices and would be immediately clear to one skilled in the art. A
4 "memory cell" stores a single bit of information. The Bennett patent discusses memory operations
5 involving accepting addresses to different portions of the memory. *See, e.g.*, Bennett, col. 91, ll. 54-
6 61 ("The first word is read at the specified address. The subsequent words' addresses are found by
7 adding the integer to the address of the most recently read word."). The need for multiple addresses
8 implies a memory with a "plurality" of memory cells.

9 Rambus disagrees that Bennett discloses a "memory device" as construed by the court.
10 Rambus urges that a person of ordinary skill in the art would read Bennett and understand that it
11 "did not intend for the memory devices used with its invention to be implemented as VLSIC
12 devices." Opp'n at 2-3. Rambus supports this assertion by reference to a declaration from Mr.
13 Murphy.

14 Mr. Murphy first points to a discussion in Bennett referring to an example of operations with
15 large memories. There, Bennett discusses the possibility of transmitting information to a "large
16 memory of up to 2^{32} addresses of 32 bit words[.]" Bennett, col. 95, ll. 58-59. Mr. Murphy points out
17 that even today (26 years after the Bennett patent application was filed) no single chip can hold that
18 amount of memory. Murphy Decl., Ex. A ¶ 4 (hereinafter "Murphy Report"). Mr. Murphy opines
19 that in 1982 such a memory of that capacity would fill a medium-sized room and comprise
20 thousands of memory cards. *Id.* Therefore, Mr. Murphy believes that a person of ordinary skill in
21 the art would not understand Bennett's "memory devices" as existing on a single VLSIC chip.

22 Mr. Murphy supports his position by latching onto Bennett's discussion of the theoretical
23 maximum-size memory device that its Versatile Bus could accommodate. But read in the context of
24 the patent, it is clear that the discussion of this "large memory" is meant to illustrate the flexibility of
25 the bus interface, not to suggest that Bennett contemplates that all memory devices designed for use
26 in its system should be so large. Rambus's emphasis on Bennett's discussion of "large memories"
27 also fails to account for Bennett's discussion of memory operations with "relatively small fast

1 memories." *See* Bennett, col. 92, l. 11 - col. 94, l. 23. Mr. Murphy's report ignores this discussion.
2 When asked at the hearing about the distinction between Bennett's "small fast" memories and its
3 "large memories," Rambus answered, "a small fast memory is also a memory board but not
4 containing as many chips and so capable of faster operation than what Bennett refers to as a large
5 memory." Tr. 100:15-22 (Dec. 10, 2008). Because Mr. Murphy does not establish this distinction,
6 Rambus attempted to support this distinction by repeating two arguments, which the court rejects in
7 detail below. Thus, even if Rambus has raised an issue of fact as to whether Bennett's "large
8 memory" devices are not the "memory devices" of Rambus's claims, Rambus has not raised an issue
9 of fact as to whether the Bennett patent discloses "small fast" memories that are the "memory
10 devices" of Rambus's claims.

11 The rejected arguments mentioned above both result from reading short passages of the
12 specification and ignoring their context. Mr. Murphy points out a discussion in the background
13 section of the patent where the inventors wrote that "[a]n efficient interconnect system cannot saddle
14 simple interconnects with the coordination overhead required for the complex ones." Murphy
15 Report ¶ 5 (citing Bennett, col. 8, ll. 10-12). Mr. Murphy states that "simple interconnects" refers to
16 memory chips, and therefore the Bennett patent's discussions of "memories" must exclude simple
17 memory chips. *Id.* Mr. Murphy misconstrues the Bennett patent. In this discussion, the Bennett
18 inventors explain the basic problems that must be solved by an ideal bus interface. *See generally*
19 Bennett, col. 7, l. 22 - col. 8, l. 12. One feature of an efficient bus interface (to the Bennett
20 inventors) is low overhead, i.e., not "saddling" simple devices with complex interfaces. The Bennett
21 inventors therefore disclosed a flexible system that operates at the lowest common denominator
22 configuration, but that can operate at high levels of complexity if the device environment only
23 includes complex devices. Mr. Murphy errs by equating this problem to be solved by the invention
24 with a limitation on the memory devices that use the inventive bus interface.

25 Mr. Murphy next points out that memory chips in 1982 "had on the order of 16 pins."
26 Murphy Report ¶ 6. He then notes that Bennett discloses that a VLSIC chip "has on the order of 100
27 pins." Bennett, col. 66, ll. 65-66. Mr. Murphy concludes that a person of ordinary skill in the art

1 would therefore conclude that the Bennett inventors could not have meant to add the Versatile Bus
2 interface to a memory and increase the pin count so much. Murphy Report ¶¶ 6-8. But as discussed
3 above, the Bennett patent's reference to "on the order of 100 pins" was made in the context of
4 considering existing microprocessor packages. Bennett frequently stresses that the preferred
5 embodiment requires 24 pins for the VM Node interface and 37 pins for the preferred Versatile Bus
6 interface. This total of 71 is not trivial, but the Bennett inventors frequently refer to implementing
7 the Versatile Bus interface with as few as three pins and minimizing the number of pins needed for
8 the VM Node interface. *See* Bennett, col. 118, ll. 15-28 (explaining that adding logic to the devices
9 would reduce the need for VM Node interface pins, but that "reduction of pins . . . is not the subject
10 of this application."). Thus, the preferred memory device interface has *at most* 71 pins, not "on the
11 order of 100 pins." The "on the order of 100 pins" remark in the specification therefore has no
12 bearing on the scale of Bennett's memory devices.

13 Mr. Murphy is correct in pointing out that it would be expensive to make memory chips that
14 implement the Versatile Bus interface. But his focus on the expense of implementing the Versatile
15 Bus interface on a memory device is irrelevant. "A reference is no less anticipatory if, after
16 disclosing the invention, the reference then disparages it." *Celeritas Techs., Ltd. v. Rockwell Int'l*
17 *Corp.*, 150 F.3d 1354, 1361 (Fed. Cir. 1998). It follows that the expense of producing or
18 implementing an anticipatory reference is also irrelevant.

19 Finally, it bears noting that the Bennett inventors were aware of memory cards and referred
20 to them as such when they chose. *E.g.*, Bennett, col. 37, ll. 26-36. The inventors disparaged the
21 existing computer busses and the "many cards [that] can be placed on the bus and communicate
22 among themselves." *Id.*, col. 37, ll. 26-28. The Bennett inventors hoped that a versatile bus
23 connecting VLSIC chips could omit the "multiunit handshaking that is just so much excess baggage"
24 found in existing busses. *Id.*, col. 37, ll. 37-41.

25 In sum, it is clear that the Bennett inventors sought to disclose a bus interface for use
26 between VLSIC devices, including memory devices. Whether the Versatile Bus interface would
27 have been an expensive addition to such memory chips is irrelevant. The court therefore concludes

1 that the Manufacturers have carried their burden of producing evidence that Bennett discloses a
2 memory device, and that Rambus has failed to rebut this showing.

3 **b. Receiving an External Clock Signal**

4 The next limitation of claim 16 requires the memory device to receive an external clock
5 signal. Mr. McAlexander states that the Bennett patent discloses such a clock signal. Bennett Chart,
6 C-7. He points out that the Versatile Bus interface transmits "[a] clock of approximately equal
7 phases, both within each [sic] 40 nanoseconds, . . . to every interfacing chip on a versatile Bus."
8 Bennett, col. 51, ll. 65-67. Bennett describes in detail the need to choose between a synchronous or
9 asynchronous bus protocol. *Id.*, col. 66, ll. 10-18. After disparaging the existing asynchronous
10 protocols, *see id.*, col. 66, ll. 19-58, the Bennett inventors opted for "a clocked, or synchronous,
11 protocol." *Id.*, col. 66, ll. 59-60. The Manufacturers have therefore met their burden of showing that
12 the Bennett patent discloses "receiving an external clock signal." Rambus does not dispute that the
13 devices featuring the Versatile Bus interface receive an external clock signal. The court therefore
14 concludes that the Manufacturers have shown that the Bennett patent discloses this limitation of
15 claim 16.

16 **c. Receiving a Request for a Write Operation**

17 The method of claim 16 also requires the memory device to "receiv[e] a request for a write
18 operation synchronously with respect to the external clock signal." Mr. McAlexander states that the
19 memory devices in the Versatile Bus interface operate in this manner. Bennett Chart, C-8. Indeed,
20 the Bennett patent's interface employs two clock signals, $\phi 1$ and $\phi 2$, to create a reference signal "to
21 which all communication between the Versatile Bus Interface Logics and the User, and upon the
22 Versatile Bus, is referenced." Bennett, col. 101, ll. 50-54. Furthermore, all signals from the
23 interface logic to a user device (like a memory device) are triggered by the leading edge of one of
24 the clock signals. *See id.*, col. 102, ll. 9-27. As discussed above, various types of requests for a
25 write operation can be sent in the slave ID/function block and received by the Bennett memory
26 devices. The Manufacturers have therefore met their burden of showing that the Bennett patent
27 discloses "receiving a request for a write operation" Rambus does not dispute that the devices

1 featuring the Versatile Bus interface synchronously receive requests for a write operation. The court
2 therefore concludes that the Manufacturers have shown that the Bennett patent also discloses this
3 limitation of claim 16.

4 **d. A Programmable Number of Clock Cycles**

5 The next two limitations of the method of claim 16 require the memory device to "sampl[e]
6 data, in response to the request for a write operation, after a programmable number of clock cycles
7 of the external clock signal transpire" and for the memory device to "stor[e] a value which is
8 representative of the programmable number of clock cycles of the external clock in a programmable
9 register. . . ." The court addresses the limitations together because the parties' dispute turns on
10 whether Bennet discloses the sampling of data after a programmable number of clock cycles
11 transpire.

12 The Manufacturers, through Mr. McAlexander, point to the following pieces of evidence.
13 *See* Bennett Chart, C-8 & C-9. The Versatile Bus interface supports pipelining operations. Bennett,
14 col. 46, ll. 18-20. "Pipelining" refers to breaking a bus transaction into its constituent parts. In the
15 Versatile Bus interface, these parts comprise arbitration, slave ID/function, and wait/data. *See id.*,
16 col. 46, ll. 23-29. The interface uses separate pins for the different types of information. *Id.*
17 Pipelining allows the device to receive the various pieces of information on the separate sets of pins
18 at staggered points in time. *Id.* For example, in the memory operations shown above in Figures 32
19 and 33, the memory device receives arbitration information on a first clock cycle or cycles, slave ID
20 and function information on a second clock cycle, and then data information on a third clock cycle.
21 *See id.*; Figs. 32, 33. The pipelined operations in the Versatile Bus interface can run two to ten
22 operations deep and have a latency of two to ten clock cycles. *Id.*, col. 46, ll. 18-23. The preferred
23 Versatile Bus interface runs a pipeline with a latency of three clock cycles. *Id.*, col. 46, ll. 21-23. It
24 is important to note that this latency refers to the number of clock cycles between the BEGIN signal
25 (the generic signal that indicates that a master wishes to use the bus) and the completion of the data
26 transfer, not the latency between an operation and its completion.

27 With these concepts in mind, Mr. McAlexander points to the example of multiplexed

1 operations in Figures 25a and 25b discussed above. Mr. McAlexander notes that in the 122121XX
2 configuration shown in Figure 25a, the total transaction time is four clock cycles. Bennett Chart, C-
3 8. By changing the value of parameter VI from 1 to 3, i.e., by dedicating a pin to the wait signal and
4 not multiplexing it with data, the device is able to send the wait signal while simultaneously sending
5 or receiving data. This reduce the total transaction time to three clock cycles. *Id.* Of course, the
6 BEGIN signal is not the "request for a write operation" received by a memory device in the Versatile
7 Bus architecture.⁶ A request for a write operation is indicated by information transmitted as part of
8 the slave ID/function block of information. Nevertheless, in Figure 25a, there is a delay of 1 clock
9 cycle between the memory device receiving the request for a write operation and the memory device
10 receiving data. In Figure 25b, there is no delay between receiving the request for a write operation
11 and the memory device's receipt of the data. This difference results from parameter VI in the
12 configuration register being programmed to equal 1 or 3.

13 Rambus responds by pointing out that parameter VI does not equal the time delay between
14 the memory's receiving a request for a write operation and sampling data. The court has already
15 rejected this argument, though at that time it was made by Hynix. *See Hynix Semiconductor, Inc. v.*
16 *Rambus Inc.*, 2008 WL 5100791, *5-*7 (N.D. Cal. Dec. 2, 2008) (rejecting Hynix's non-
17 infringement argument with respect to the programmable register's CAS latency value).

18 The relevant inquiry, as dictated by the text of Rambus's claim, is whether the value is
19 *representative* of the number of clock cycles between the write request and sampling. The court
20 previously held that a stored value was representative of a delay time because the delay time could
21 be expressed as a function the of the stored value. *See id.* Parameter VI (the number of wait lines
22 used in the Versatile Bus configuration) can vary from 1 to 5. It appears that when Parameter VI

23

24 ⁶ This mistake underscores why the second example called out by the Manufacturers' in
25 their motion does *not* illustrate a programmable delay between receiving a request for a write operation
26 and sampling data in response. While the total transaction times in Figures 32 and 33 differ due to how
27 the different configurations process arbitration information, both examples illustrate waiting *zero* clock
28 cycles between receiving a request for a write operation and sampling data in response. In both
examples, the memory devices receive a request for a write operation on clock cycle t , and sample data
in response on clock cycle $t + 1$.

1 equals 1, i.e., when the wait line is multiplexed with the data lines, the "write latency" is one clock
2 cycle because the data cannot be received until the wait signal is sent. It further appears that when
3 Parameter VI equals anything else (2-5), the "write latency" is zero because the configuration either
4 lacks a wait signal or transmits it simultaneously with the data. Obviously, this is not the clear
5 functional relationship that connected the CAS latency value to the delay before the device began to
6 output data in *Hynix*. But the value of Parameter VI still determines the "write latency" that will
7 exist in the Versatile Bus interface's memory operations.

8 However, one value being "representative" of another requires more than a functional
9 relationship between the two. The word "representative" implies some level of recognition by
10 another that the first value indicates or represents the second. The verb "represent" means "[t]o
11 bring clearly and distinctly before the mind, esp. (to another) by description" and "[t]o symbolize, to
12 serve as a visible or concrete embodiment of (some quality, fact, or other abstract concept)." Oxford
13 English Dictionary (2d ed. 1989) (definitions 2a and 6a). In *Hynix*, the evidence showed that the
14 DRAMs' CAS latency value equaled the amount of time before the DRAM made information
15 available to the bus. It was trivial from that to recognize that the CAS latency value also controlled
16 the timing of all other aspects of the DRAM's response to a read operation, namely, when the device
17 began to output data. Here, Mr. Murphy correctly points out that the Bennett interface's eight
18 parameters "do not include the time delay between the receipt of a read or write command and the
19 output or input of the corresponding data." Murphy Report ¶ 12. The Bennett inventors never
20 referred to Parameter VI as embodying a mechanism for controlling the write latency of the
21 Versatile Bus interface's memory operations. Drawing all inferences in favor of Rambus, the value
22 of Parameter VI, i.e., the number of wait lines used in a configuration of the bus interface, would not
23 be recognized as representing the number of clock cycles between receiving a request for a write
24 operation and sampling data in response.

25 Two additional arguments made by Rambus deserve attention because of their tendency to
26 "cloud rather than clarify the central legal issues" regarding Bennett and risk "draw[ing] the [jury's]
27 attention to peripheral matters." *Allen Eng'g Corp. v. Bartell Industries, Inc.*, 299 F.3d 1336, 1356

1 (Fed. Cir. 2002). Rambus argues that "the values in the configuration register do not determine the
2 actual configuration of the device." Murphy Report ¶ 13. Mr. Murphy bases this conclusion on the
3 Versatile Bus interface's requirement that the bus configuration support the least complex device.
4 He states that, "the actual configuration of the device will depend not just on the values in its
5 configuration register, but also the values in the configuration registers of the other components in
6 the system." *Id.* Rambus therefore suggests that a device could have a "3" in its register for
7 parameter VI, but another device could have a value of "2" and the Versatile Bus environment
8 would then operate at the lower value despite the higher value in one of the device's configuration
9 registers. But Rambus and Mr. Murphy appear to confuse the role of the configuration register in
10 the Versatile Bus interface when all of the devices possess programmable configuration registers.
11 Because different devices will have different interface complexities, the maintenance processor
12 programs *all* of the devices in such a bus environment with the same octet of values. The value in
13 the configuration register always determines the actual configuration of the device. Rambus's
14 example does not accurately describe the Bennett bus interface in such an environment.

15 Rambus also suggests that the description of Figures 25a and 25b are purely exemplary and
16 that there is no guarantee that there is a one cycle delay between the request for a write operation
17 and the output of data. Rambus bases this argument on Bennett's statement that "[i]n order to
18 simplify presentation of timing concepts all Arbitration, Slave Identification/Function, and Data
19 activities are assumed to be but one cycle." Bennett, col. 85, ll. 17-19. Rambus's argument fails for
20 two reasons. First, this is not a baseless assumption by the Bennett inventors. The other primitives
21 in the Figure 25 example are selected to ensure that arbitration, slave ID/function, and data all occur
22 in one cycle. In other words, this is not a guess; there is a configuration of the Versatile Bus
23 interface in which this is true. Second, it is irrelevant. That the arbitration, slave ID/function, and
24 data activities are all assumed to last one cycle does not impact the amount of delay *between* the
25 slave ID/function and data activities. That delay is determined by the status of the wait signal.

26 **e. Set Register Request**

27 The final limitation of claim 16 requires the memory device to receive "a set register request,

1 wherein in response to the set register request, the memory device stores the value in the register."
2 Mr. McAlexander states that Bennett discloses a memory device receiving a set register request.
3 Bennett Chart, C-9. He points out that parameter VI is programmed into the configuration register
4 when the devices on the Versatile Bus are initialized. *See* Bennett, col. 35, ll. 48-54. He does not
5 explain how this happens. *See* Bennett Chart, C-9.

6 In their brief, the Manufacturers cite a cryptic portion of Bennett that states:

7 The maintenance processor effectuates the impressing of a pertinent bit pattern upon
8 the configuration register within each Versatile Bus Interface Logics by respectively
9 emplacing a logical Low on signal (L) SCAN/SET ENABLE, a logical Low on
10 signal (L) SCAN/SET SELECT (L=SET), a logical High on signal (H) SEL LOOP
D, and appropriate logical High or Low level of signal (H) SET DATA as a
respective logical "1" or "0" is desired to be set within each bit position of Loop D
as gated by clock ϕ 2.

11 Bennett, col. 125, ll. 46-56. The Manufacturers provide no testimony to explain the significance of
12 the passage, and without any testimony, the court cannot grant summary judgment.

13 3. Conclusion

14 The Manufacturers have failed to meet their burden of producing clear and convincing
15 evidence that the Bennett patent discloses the "set register request" limitation of claim 16 of the '285
16 patent. The Manufacturers have failed to carry their burden of persuasion with respect to the
17 "programmable number of clock cycles" limitations because Rambus has produced evidence in
18 opposition that raises a triable issue of fact. Accordingly, the court denies the Manufacturers'
19 motion for summary judgment with respect to claim 16 of the '285 patent.

20 C. Claim 27 of the '051 Patent

21 1. The Asserted Claim

22 The Manufacturers next assert that the Bennett patent anticipates claim 27 of U.S. Patent No.
23 6,314,051. The claim generally recites a memory device that possesses: (1) clock receiver circuitry
24 for receiving an external clock signal, (2) a programmable register for storing a value representative
25 of the device's write latency, and (3) data input circuit to sample data after the write latency period.
26 Rambus colloquially refers to this claim as covering a device featuring programmable write latency.
27 The full text of the claim follows:

28 ORDER GRANTING IN PART AND DENYING IN PART RAMBUS'S MOTION TO STRIKE; DENYING MOTION FOR
SUMMARY JUDGMENT No. 1 OF INVALIDITY; AND STRIKING MOTION FOR SUMMARY JUDGMENT No. 2 OF
INVALIDITY — C-05-00334 RMW; C-05-02298-RMW; C-06-00244-RMW

1 A memory device having a plurality of memory arrays, wherein each memory array
2 includes a plurality of memory cells, the memory device comprising:

3 clock receiver circuitry to receive an external clock signal;

4 a programmable register to store a value which is representative of a number of clock
5 cycles of the external clock signal to transpire before sampling a first portion of data,
6 wherein the first portion of data is sampled in response to an operation code;

7 and data input receiver circuitry to sample the first portion of data synchronously
8 with respect to the external clock signal.

9 **2. The Evidence With Respect to Each Limitation**

10 The limitations of claim 27 closely resemble some of the limitations of claim 16 of the '285
11 patent. In short, Rambus has raised a triable issue of fact regarding whether Bennett's memory
12 interface's parameter VI is "representative" of "a number of clock cycles of the external clock
13 signal" that must transpire before the memory device samples data. The court therefore denies the
14 Manufacturers' motion for summary judgment with respect to this claim.

15 **D. Claim 43 of the '051 Patent**

16 **1. The Asserted Claim**

17 The Manufacturers also argue that the Bennett patent anticipates claim 43 of the '051 patent.
18 The claim is very general, and recites a synchronous DRAM with (1) input receiver circuitry to
19 sample an operation code synchronously and (2) input receiver circuitry to sample data in response
20 to the operation code after a predetermined number of clock cycles. The full text of the claim
21 follows, with the language of the claim from which it depends incorporated in brackets:

22 [A memory device having a plurality of memory arrays, the memory device
23 comprising:

24 first input receiver circuitry to receive an operation code synchronously with respect
25 to an external clock; and

26 second input receiver circuitry to sample data, in response to the operation code,
27 after a predetermined number of clock cycles of the external clock]

28 wherein the memory device is a synchronous dynamic random access memory.

2. The Evidence With Respect to Each Limitation

The final limitation of claim 43 modifies the preambulatory "memory device" limitation, so the

1 court addresses the two limitations together. The court discussed the arguments regarding the
2 Manufacturers' showing that the Bennett patent discloses a "memory device" above. *See supra* § III-
3 B-2-a.

4 The first difference between the two claims with respect to the "memory device" limitation is
5 that claim 16 recited a memory device with a plurality of memory cells, while claim 43 recites a
6 memory device with a plurality of memory "arrays." During claim construction, the parties agreed
7 that a "memory cell" was "an electronic storage element(s) in a memory array." *Rambus Inc. v.*
8 *Hynix Semiconductor, Inc.*, C-05-00334, Docket No. 254, at 3 (N.D. Cal. Jul. 11, 2007) ("Joint
9 Claim Construction Statement"). But the parties disputed the construction of "memory array." *See*
10 *id.* at Jt. App'x A, 21. Rambus argued that a "memory array" was "a plurality of data storage
11 elements that are arranged in rows and columns." *Id.* The Manufacturers submitted that no
12 construction was necessary. *Id.* Neither party raised the issue of the construction of "memory array"
13 in their briefs or at the claim construction hearing. Nor did any party consider the dispute
14 particularly significant. *See* Docket Nos. 254-4 (ranking the dispute 39th on Rambus's list of
15 priorities), 254-5 (failing to list the dispute on the Manufacturers' list of 47 important claim
16 construction disputes).

17 To the extent the term needs construction, the court agrees with Rambus's construction. The
18 parties agree that a memory cell is a storage element in a memory array. The parties also agree that
19 a "synchronous dynamic random access memory" is "a synchronous semiconductor memory device
20 which includes one or more arrays of DRAM cells." Joint Claim Construction Statement, 3. Thus,
21 the parties agree that an array contains memory cells and that a DRAM contains one or more arrays.
22 This favors Rambus's construction, but does not necessarily explain the rows and columns
23 limitations suggested by Rambus. The extrinsic evidence fills the gap. Memory arrays are
24 "rectangular grids of storage cells with each cell holding one bit of data. . . . [M]emory arrays are
25 organized into *rows* and *columns*." Bruce Jacob, Spencer W. Ng & David T. Wang, *Memory*
26 *Systems: Cache, DRAM*, Dick 316-17 (2008). In light of the parties' agreements, the extrinsic
27 evidence, and silence of the Manufacturers, the court adopts Rambus's construction of "memory

1 array."

2 To establish that Bennett discloses a memory device with a plurality of memory arrays, Mr.
3 McAlexander refers to the "large memory" discussed above. Bennett Chart, C-14. In so doing, he
4 concedes that such a large memory would have been composed of multiple chips, and that each chip
5 would have at least one memory array. *See id.* As discussed above, Rambus has raised a triable
6 issue of fact as to whether the "large memories" of Bennett satisfy the "memory device" limitation of
7 Rambus's claims. While Rambus has not similarly raised a question of fact with respect to Bennett's
8 "small fast memories," Mr. McAlexander does not state whether Bennett's "small fast" memories
9 would have had a plurality of memory arrays. Because the Manufacturers have not produced
10 sufficient evidence on summary judgment to establish that Bennett discloses the slightly different
11 "memory device" of claim 43, the court cannot grant summary judgment.

12 The court must also deny summary judgment because the Manufacturers have not produced
13 sufficient evidence on summary judgment that the Bennett patent discloses a memory device that is
14 a synchronous dynamic random access memory. *See* Bennett Chart, C-16. Mr. McAlexander
15 generally cites Bennett's seven-column discussion of memory operations as disclosing a
16 synchronous DRAM. Those seven columns specifically mention only one type of memory: ROM or
17 read-only memory. *See* Bennett, col. 91, ll. 1-2. Bennett discusses ROMs while explaining the
18 limited number of operations that can be done with a memory device, and it does so to point out that
19 memories like ROMs cannot receive write operations. *See id.* Bennett's discussion thus impliedly
20 discloses some type of memory device that can receive write operations. The jury will have to
21 determine at trial whether that implied disclosure encompasses a dynamic random access memory.

22 Because the court denies the Manufacturers' motion for summary judgment with respect to
23 claim 43 for failure to establish that Bennett discloses the first and fourth limitations of claim 43, the
24 court does not reach whether Bennett discloses the second and third limitations of the claim.
25 Nonetheless, the court notes that Rambus's argument with respect to the second input receiver
26 circuitry appears misplaced. Rambus argues that Bennett does not anticipate claim 43 because
27 Bennett does not disclose "programmable write delay." Claim 43's third limitation recites "input

1 receiver circuitry to sample data, in response to the operation code, after a predetermined number of
2 clock cycles of the external clock." The claim says nothing about varying the predetermined number
3 of clock cycles or storing/programming the number of clock cycles in a register.

4 **E. Claim 16 of the '863 Patent**

5 **1. The Asserted Claim**

6 The Manufacturers also assert that the Bennett patent anticipates claim 16 of U.S. Patent No.
7 6,452,863. The claim generally recites a method of operating a synchronous memory device. The
8 method generally involves (1) the device receiving and "processing" some block size information
9 from a memory controller; (2) synchronously receiving a request for a write operation from the
10 memory controller; and (3) inputting data in response, both synchronously and over more than one
11 clock cycle. Rambus colloquially refers to this claim as covering the implementation of
12 programmable or variable burst length. The full text of the claim follows:

13 [[A method of operation in a synchronous memory device, wherein the memory
14 device includes a plurality of memory cells, the method of operation of the memory
device comprises:

15 receiving first block size information from a memory controller, wherein the memory
16 device is capable of processing the first block size information, wherein the first
block size information represents a first amount of data to be input by the memory
device in response to an operation code;

17 receiving the operation code, from the memory controller, synchronously with
18 respect to an external clock signal; and

19 inputting the first amount of data in response to the operation code]]

20 [wherein inputting the first amount of data includes receiving the first amount of data
21 synchronously with respect to the external clock signal]

22 wherein the first amount of data is sampled over a plurality of clock cycles of the
external clock signal.

23 **2. The Evidence With Respect to Each Limitation**

24 **a. Memory Device**

25 The preamble "memory device" limitation essentially mirrors that in claim 16 of the '285
26 patent. The court previously discussed the arguments regarding the Manufacturers' showing that the
27 Bennett patent discloses a "memory device." *See supra* § III-B-2-a. The only difference in the two

1 "memory device" limitations is that claim 16 of the '863 patent adds a "synchronous" aspect to the
2 limitation. The court determined that Bennett discloses synchronous memory devices in its prior
3 discussion. *See supra* § III-B-2-b (discussing clock receiver circuitry).

4 **b. Receiving Block Size Information**

5 The method of claim 16 of the '863 patents begins with the memory device receiving block
6 size information from a memory controller. "Block size information" means "information that
7 specifies the total amount of data that is to be transferred on the bus in response to a transaction
8 request."

9 Mr. McAlexander states that the Bennett patent discloses receiving block size information
10 from a memory controller. *See Bennett Chart, C-30.* Mr. McAlexander points to two instances
11 where he states that the memory device receives block size information. One does not disclose
12 receiving block size information. The other does.

13 First, the Manufacturers and Mr. McAlexander point to the use of the BUSY signal in the
14 block read and write operations defined by the Bennett inventors and discussed above. But the
15 Manufacturers fail to show how the block read or write operations involve the memory device
16 receiving block size information. On the contrary, the memory devices engaged in block operations
17 in the Versatile Bus interface *never* receive information that specifies the total amount of data to be
18 transferred. The memory devices receive only a request to begin a block operation and the BUSY
19 signal from the master device. The block operation continues indefinitely until the master
20 terminates the BUSY signal. The BUSY signal does not specify a total amount of data to be
21 transferred; it only instructs the DRAM to continue to operate. In pursuing this argument, the
22 Manufacturers lose sight of the difference between block memory operations and the memory
23 device's receipt of block size information. The two are not the same.

24 The Manufacturers next argue that the Bennett memory device receives block size
25 information when it receives parameters VII and VIII during configuration. As discussed,
26 parameters VII and VIII define what the Bennett inventors call "data format." The parameters do
27 not define the length of a block operation. The parameters simply define the dimensions of a single

1 data word. Thus, parameters VII and VIII cannot specify the total amount of data that will be
2 transferred in response to a block read or block write operation. But they do specify the total
3 amount of data to be transferred in response to Bennett's basic, single-word read or write operations.

4 Rambus argues that the fallacy in the Manufacturers' argument is that "the bits they point to
5 do not specify the *number* of data words to be transferred." But the court's construction of "block
6 size information" – "information that specifies the total amount of data that is to be transferred on
7 the bus in response to a transaction request" – does not require the information to specify the number
8 of data words. It only requires the information to specify the *total* amount of data to be transferred.
9 Indisputably, parameters VII and VIII specify the total amount of data that will be transferred in
10 response to two basic types of transaction requests.

11 And even if "block size information" had to specify the number of data words to be
12 transferred, Bennett's parameters VII and VIII do to the same extent that the Farmwald/Horowitz
13 specification's BlockSize[0:3] does. In the preferred embodiment interface of Drs. Farmwald and
14 Horowitz, the block size parameter instructed the DRAM to send or receive 0-7, 8, 16, 32, 64, 128,
15 256, 512, or 1,024 bits of information. *See* U.S. Patent No. 6,426,916, col. 11, ll. 44-67. The
16 preferred embodiment used eight bus data lines. Thus, when the DRAM received block size
17 information, that information also specified the number of data words that would be transferred as
18 well, i.e., 0-7 specified that no complete data words would be transferred, 8 specified that one data
19 word would be transferred, 16 specified that two, and so on. Analogously, when Parameter VII
20 equals VIII, the two parameters "specify" that one data word will be transferred in response to basic
21 read and write operations.

22 There is another wrinkle, however. Unlike Rambus's other asserted claims, Claim 16
23 explicitly requires the presence of a memory controller. Specifically, the method of claim 16
24 requires the memory device to receive the block size information "from a memory controller." In
25 Bennett's Versatile Bus interface, Parameters VII and VIII come from the maintenance processor.
26 Mr. McAlexander does not state one way or the other whether Bennett's maintenance processor is a
27 memory controller. *See* Bennett Chart, C-30. The court must therefore deny summary judgment

1 because the Manufacturers have failed to establish that Bennett anticipates claim 16 of the '863
2 patent by disclosing the memory device's receipt of block size information from a memory
3 controller.

4 It is unclear whether the Manufacturers will be able to establish this at trial. To begin, the
5 parties included "memory controller" among the terms on whose construction the parties could not
6 agree. Joint Claim Construction Statement, Jt. App'x at 22. As with "memory array" though, the
7 parties did not call this dispute to the court's attention during claim construction. Rambus submitted
8 that a "memory controller" is "an integrated circuit device that includes circuitry to direct the actions
9 of one or more memory device." *Id.* This broad construction of the term might encompass the
10 maintenance processor because Bennett's maintenance processor dictates the "data format" of all
11 future memory operations. It does not appear, however, that the maintenance processor directs any
12 other actions of the memory device, i.e., the maintenance processor does not send requests for read
13 or write operations to the memory devices in the Versatile Bus environment. On the other hand, the
14 court cannot adopt the constructions proposed by the Manufacturers. Some Manufacturers proffered
15 constructions incorporating the request packet limitation that the court has rejected. *See Rambus*
16 *Inc. v. Hynix Semiconductor, Inc.*, 569 F. Supp. 2d 946, (N.D. Cal. 2008). Another did not offer a
17 proposed construction because no claim asserted against that Manufacturer included a "memory
18 controller" limitation at that time. Joint Claim Construction Statement, Jt. App'x at 22. Whether the
19 parties still dispute the construction of the term "memory controller" and whether the Bennett
20 maintenance processor is such a "memory controller" remain to be seen.

21 **F. Claim 28 of the '916 Patent**

22 Finally, the Manufacturers also move for summary judgment that the Bennett patent
23 anticipates claim 28 of U.S. Patent No. 6,426,916. The claim generally recites a synchronous
24 memory device that receives block size information and stores a value that is "representative" of a
25 write latency period. The court previously discussed the Manufacturers' failure to carry their burden
26 of persuasion with respect to the write latency limitation. *See supra* § III-B-2-d. Accordingly, the
27 court denies the Manufacturers' motion for summary judgment with respect to claim 28 as well.

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IV. ORDER

For the foregoing reasons, the court grants Rambus's motion to strike the Manufacturers' summary judgment motion no. 2 and the court does not consider it. The court denies Rambus's motion to strike the Manufacturers' summary judgment motion no. 1. The court denies the Manufacturers' motion for summary judgment no. 1.

DATED: 12/15/2008



RONALD M. WHYTE
United States District Judge

1 Notice of this document has been electronically sent to counsel in:
2 C-05-00334, C-05-02298, C-06-00244.

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24 **Dated:** 12/15/2008 TSF
25 Chambers of Judge Whyte