EXHIBIT 1

D7 Pages 26-54

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being transferred to said output of said memory, and	with the '754 Reference. "In response to that, the operation timing signals Φ pa 1 and Φ pa 2 of the sense amplifiers SA 1 and SA 2, which are slower than the above-mentioned word line selection timing signals Φ x 1 and Φ x 2, are generated at the same time too." ['1182 Reference, Page 5, column 1] *See also* Figure 1. The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58] "A semiconductor dynamic memory device comprising: … a plurality of sense amplifying means (18-1 to 18-4; SA1 to SA8) responsive to a control signal input thereto, for selectively activating one sense amplifying means to sense and amplify data on said selected data lines of one of said two column-selected memory blocks, and for selectively

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	activating at least one other sense amplifying means to refresh data to said each memory cell along said selected word lines; ...." ['754 Reference, Page 6:53- 7:5]
(2) a predetermined number of other sense amplifier circuits whose output signals will be transferred next to said output of said memory if said operation continues sufficiently long.	This limitation is met by the '1182 Reference alone or in combination with the '754 Reference. "In response to that, the operation timing signals Φ pa 1 and Φ pa 2 of the sense amplifiers SA 1 and SA 2, which are slower than the above-mentioned word line selection timing signals Φ x 1 and Φ x 2, are generated at the same time too." ['1182 Reference, Page 5, column 1] *See also* Figure 1. The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58]

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	"A semiconductor dynamic memory device comprising: ... a plurality of sense amplifying means (18-1 to 18-4; SA1 to SA8) responsive to a control signal input thereto, for selectively activating one sense amplifying means to sense and amplify data on said selected data lines of one of said two column-selected memory blocks, and for selectively activating at least one other sense amplifying means to refresh data to said each memory cell along said selected word lines; ...." ['754 Reference, Page 6:53- 7:5]
10. The memory of claim 7 wherein:	
said set of locations comprises k subsets S-1, . . . , S-k wherein k is greater than or equal to two, such that, for a positive integer m and for any subset S-i, the contents of m consecutively addressed locations from said subset S-i can be transferred simultaneously to said plurality of sense amplifier circuits; and tARA is measured from the time that an address of the first location to be read out in said operation is made available to said memory to the time when said plurality of sense amplifier circuits develops an output signal indicative of the contents of said first location; and in said operation, time tARA does not exceed m * (k-1) * (tOE), wherein:	This limitation is met by the '1182 Reference. Specifically, the '1182 Reference states: "Although this embodiment is not especially restricted, the memory array is split into two on the left and the right such as M-ARY 1 and M-ARY 2 in its configuration. In the memory arrays M-ARY 1 and M-ARY 2, a column-type (data line) signal line consists of a pair of complementary data lines that have been placed parallel, and the two pairs of complementary data lines will constitute a set; in the diagram they are configured by a double intersecting method arranged to face the horizontal direction. . . . The above column decoder C-DCR deciphers the address signals like those set out below, is synchronized to the data line selection timing signals Φ y, and forms selection signals that are provided to the above-mentioned column switching circuits C-SW1, C-SW2." ['1182 Reference, Page 2, Column 2; *see also*Fig. 2 and Claim 1]
tOE is the time to transfer the contents of any one of said locations from said plurality of sense amplifier	A person of skill in the art would know that this timing relationship would be used when designing the memory disclosed in claim 1.

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circuits to said output.	
11. The memory of claim 8 wherein, in said operation, each location to be read out except the first location to be read out is read out to said output in a shorter time than the first location to be read out.	This limitation is met by the '1182 Reference alone or in combination with any of the '885 Reference or the '587 Reference or the '003 Reference or the '994 Reference or the '199 Reference. Specifically, Figure 3 of the '1182 Reference illustrates this timing. The '885 Reference states: "Circuitry for serial read memory access utilizing a random starting address. Fast read access is provided without upsetting the original data pattern stored in the memory core if the sequential read is terminated in midstream." ['885 Reference, Page 1] The '994 Reference states: "For that reason, even if the address moves serially to the next row and changes, the data itself will be read at high speed t_0. As is evident from the explanation above, as long as serial access continues, the internal data can continue to be read at high speed." ['994 Reference, Page 4, Column 1] "In the specifications, the address access time t_1 is estimated at 150 ns, and t_0 is estimated at the level of 30 ns for simple determination at the number of steps of the gates. In a hypothesis of the worst-case scenario for the current jump command +1 instruction, the jump command would be 3 bytes for the operand +2 data, 1 instruction would be 1 byte. Therefore, the average access time is {150 ns x 1 + 30 ns x 3}/4 = 60 ns. In contrast, the access time is 150 ns when the invention is not used."

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	['994 Reference, Page 4, Column 2] The '587 Reference states: "The reduction in the memory access cycle time from a convention memory access operation, generally represented by the first prefetch with a three clock cycle span between event t1 and t2, is clearly evident when the times are compared to those of the consecutive prefetch operation extending for two clock cycles between corresponding time intervals t3 and t4. Time t2 and t4 identify the first clock interval suitable to initiate succeeding memory access operations." ['587 Reference, Col. 5:63-6:3] The '003 Reference states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage

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	locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41] The '199 Reference states: "However, in some integreated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer. Typically, the access addresses of the 'extra' storage cells differ from the original access address by only one or two bits. However, subsequent accesses to these cells can be accomplished by simply executing additional access cycles without changing the access address. In the art, such memories are referred to as 'nibble mode'. In some other integreated circuit memories, a portion of the original address can be 'assumed' for one (or more) subsequent accesses, so that only the least significant portion of the address needs to be decoded, etc. Thus, once the original access had been completed, subsequent accesses to 'related' storage cells will be significantly quicker." ['199 Reference, Col. 1:13-28]
12. The memory of claim 8 wherein the sequence of locations L1, . . . , Ln is a sequence of increasing order of addresses.	This limitation is met by the '1182 Reference. Specifically, this limitation is described on Page 5 and 6 of the '1182 Reference.
13. The memory of claim 7 wherein in said operation any number of said locations addressed consecutively with wrap around can be read out to said output so that:	This element is met in the '1182 Reference alone or in combination with the '885 Referece. Specifically, the '1182 Reference states that: "When th reading has finished to the column address 1023 in resonse to the above-mentioned address 4, the carrier signals ca for the column-type

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	counter circuit (Y) are produced similarly to what is explained above, and they themselves will be the address 0 and the row-based address will be changed to 6." ['1182 Reference, Page 5, second column] "(5) There is an effect that is obtained whereby high-speed continuous reading is carried out from a random address by incorporating address signals that have been supplied from the external terminal as initial values." ['1182 Reference, Page 6, second column] "(6) Based on (1) to (5) above, there is an effect that is obtained whereby there can be provided a semiconductor memory device that is applicable to a semiconductor memory where picture element data that is large in quantity is repeated to depict high-precision picture images using a display device, such as a CRT, and, therefore, high-speed continuous reading would be presumed to be necessary." ['1182 Reference, Page 6, second column] *See also* Figure 3 and accompanying description on Page 4. The '885 Reference states: "After the last memory address is reached, the access automatically rolls over to the first address." ['885 Reference, Col. 3:1-3] "A method as in claim 5 wherein the sequence of incremented addresses wraps around when the address of the Nth register is reached such that all N registers in the array are read." ['885 Reference, Col. 7:45-48]
the first location to be read out in said operation is read	This element is met by the '1182 Reference alone or in combination with

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out to said output after time tARA+tOE wherein: tARA is measured from the time that an address of said first location is made available to said memory to the time when said plurality of sense amplifier circuits develops an output signal indicative of the contents of said first location; and tOE is the time to transfer the contents of any one of said locations from said plurality of sense amplifier circuits to said output of said memory; and	the '885 Reference or the '994 Reference or the '587 Reference or the '003 Reference or the '199 Reference. Specifically, the '1182 Reference states: "(3) In the expansion serial access mdoe, there is an effect that is obtained whereby all that needs to be done is to change the external terminal because address signals are formed by a built-in address counter circuit, and therefore, it will be very easy for users to handle." ['1182 Reference, Page 6, second column] The '885 Reference states: "An embodiment of circuitry for sequential read access of a serial memory array in accordance with the present invention comprises an address latch which stores an address used to access the memory array to read data from a corresponding data register in the array. The address latch includes a counter which increments the stored address upon receipt of an address increment signal." ['885 Reference, Col. 3:7-14] The '994 Reference states: "For that reason, even if the address moves serially to the next row and changes, the data itself will be read at high speed t_0. As is evident from the explanation above, as long as serial access continues, the internal data can continue to be read at high speed." ['994 Reference, Page 4, Column 1] "In the specifications, the address access time t_1 is estimated at 150 ns, and t_0 is estimated at the level of 30 ns for simple determination at the number of steps of the gates. In a hypothesis of the worst-case scenario

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	for the current jump command +1 instruction, the jump command would be 3 bytes for the operand +2 data, 1 instruction would be 1 byte. Therefore, the average access time is {150 ns x 1 + 30 ns x 3}/4 = 60 ns. In contrast, the access time is 150 ns when the invention is not used." ['994 Reference, Page 4, Column 2] The '587 Reference states: "The reduction in the memory access cycle time from a convention memory access operation, generally represented by the first prefetch with a three clock cycle span between event t1 and t2, is clearly evident when the times are compared to those of the consecutive prefetch operation extending for two clock cycles between corresponding time intervals t3 and t4. Time t2 and t4 identify the first clock interval suitable to initiate succeeding memory access operations." ['587 Reference, Col. 5:63-6:3] The '003 Reference states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col.

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	10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer. Typically, the access addresses of the 'extra' storage cells differ from the original access address by only one or two bits. However, subsequent accesses to these cells can be accomplished by simply executing additional access cycles without changing the access address. In the art, such memories are referred to as 'nibble mode'. In some other integrated circuit memories, a portion of the original address can be 'assumed' for one (or more) subsequent accesses, so that only the least significant portion of the address needs to be decoded, etc. Thus, once the original access had been completed, subsequent accesses to 'related' storage cells will be significantly quicker." ['199 Reference, Col. 1:13-28]
every other location to be read out in said operation is read out to said output within time tOE.	This element is met by the '1182 Reference alone or in combination with the '885 Reference or the '994 Reference or the '587 Reference or the '003 Reference or the '199 Reference. Specifically, the '1182 Reference

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	states: "(3) In the expansion serial access mdoe, there is an effect that is obtained whereby all that needs to be done is to change the external terminal because address signals are formed by a built-in address counter circuit, and therefore, it will be very easy for users to handle." ['1182 Reference, Page 6, second column] The '885 Reference states: "An embodiment of circuitry for sequential read access of a serial memory array in accordance with the present invention comprises an address latch which stores an address used to access the memory array to read data from a corresponding data register in the array. The address latch includes a counter which increments the stored address upon receipt of an address increment signal." ['885 Reference, Col. 3:7-14] The '994 Reference states: "For that reason, even if the address moves serially to the next row and changes, the data itself will be read at high speed t_0. As is evident from the explanation above, as long as serial access continues, the internal data can continue to be read at high speed." ['994 Reference, Page 4, Column 1] "In the specifications, the address access time t_1 is estimated at 150 ns, and t_0 is estimated at the level of 30 ns for simple determination at the number of steps of the gates. In a hypothesis of the worst-case scenario for the current jump command +1 instruction, the jump command would be 3 bytes for the operand +2 data, 1 instruction would be 1 byte.

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	Therefore, the average access time is {150 ns x 1 + 30 ns x 3}/4 = 60 ns. In contrast, the access time is 150 ns when the invention is not used." ['994 Reference, Page 4, Column 2] The '587 Reference states: "The reduction in the memory access cycle time from a convention memory access operation, generally represented by the first prefetch with a three clock cycle span between event t1 and t2, is clearly evident when the times are compared to those of the consecutive prefetch operation extending for two clock cycles between corresponding time intervals t3 and t4. Time t2 and t4 identify the first clock interval suitable to initiate succeeding memory access operations." ['587 Reference, Col. 5:63-6:3] The '003 Reference states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read

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	request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer. Typically, the access addresses of the 'extra' storage cells differ from the original access address by only one or two bits. However, subsequent accesses to these cells can be accomplished by simply executing additional access cycles without changing the access address. In the art, such memories are referred to as 'nibble mode'. In some other integrated circuit memories, a portion of the original address can be 'assumed' for one (or more) subsequent accesses, so that only the least significant portion of the address needs to be decoded, etc. Thus, once the original access had been completed, subsequent accesses to 'related' storage cells will be significantly quicker." ['199 Reference, Col. 1:13-28]
14. The memory of claim 8 wherein said memory is fabricated in an integrated circuit.	This limiation is met by the '1182 Reference. Specifically, the '1182 Reference states: "Shown in FIG. 1 is a block diagram of a dynamic-type RAM in which the invention has been applied. The circuit component that constitutes the circuit blocks in the diagram is not especially restricted by the manufacturing technology for a semicondcutor integrated circuit that is

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	known in the industry; however, it is formed on a semiconductor substrate such as single crystal silicon." ['1182 Reference, Page 2, second column]
20. An integrated memory comprising:	Although a preamble is normally not limiting, should this preamble be limiting, this element is met in the '1182 Reference. Specifically, the '1182 Reference states that:
an array of memory locations, the array comprising a plurality of subarrays, each subarray comprising a predetermined number of groups of columns of the memory locations such that for any given column position in a group, the memory locations in any given row in the columns at said given position in the groups of the subarray have consecutive addresses;	This limitation is met by the '1182 Reference. Specifically, the '1182 Reference states: "Although this embodiment is not especially restricted, the memory array is split into two on the left and the right such as M-ARY 1 and M-ARY 2 in its configuration." ['1182 Reference, Page 2, second column] "Thereafter, when high-level clock signals are supplied to the external clock signals [CL bar], the address counter circuit COUNT receives the above-mentioned clock signals Φ and performs a+1 step operation. In that instance, the column-based counter circuit (Y) forms the carrier signals ca by the above-mentioned step operation, and that itself will be at address 0. In addition, the row-based address will change to 5." ['1182 Reference, Page 5, first column] "(3) In the expansion serial access mode, there is an effect that is obtained whereby all that needs to be done is to change the external terminal because address signals are formed by a built-in address counter circuit, and, therefore, it will be very easy for users to handle." ['1182 Reference, Page 6, second column] *See also* description of operation on Page 5; Figure 1 and Claim 1.

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one X-decoder for each subarray;	This limitation is met by the '1182 Reference. Specifically, the '1182 Reference states: "The row address decoders R-DCR 1 and R-DCR2 decipher the above-mentioned address signals x0-xm and form the selection signals of the word line, are synchronized to the word line selection timing signals Φx1 and Φx2, and perform the selection operation of a one word line of the memory arrays M-ARY 1 and M-ARY 2 and dummy word line. ['1182 Reference, Page 3, first column] Further, the '1182 Reference could be combined with any of the '596 Reference or the '297 Reference or the '495 Reference to meet this limitation.
one X-register for each X-decoder;	This element is met in the '1182 Reference alone or in combination with any of the '937 Reference or the '495 Reference or the '021 Reference. Specifically, the '1182 Reference states that: "Specifically, address signals that have been provided from an external terminal in accordance with operation mode signals that have been designated from specified external control signals are incorporated as the initial values; there is an address counter circuit that performs a stepping operation based on the pulse that has been provided from the external terminal; the address signals that have been formed by the above-mentioned address counter circuit in accordancd with the above-mentioned operation mode signals are relayed to an address decoder via a multiplexer; and in accordance with the address signals formed by the above-mentioned address counter circuit, column selection operations for

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	the other memory array where the word line is already in a state of selection is performed upon completion of the final selection of addresses for one of the memory arrays during column selection for the memory array that has been partitions into two." ['1182 Reference, first and second column; *see also* Fig. 1; *see also* Claim 1] To the extent AMD reads this limitation on the Samsung devices, this '1182 Reference meets this limitation. The '937 Reference states: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42] The '495 Reference states: "The register 70a, 70b, 70c or 70d selected by the block decoder 50 holds 8-bit address codes ARC0-ARC7 supplied in synchronism with the row selection signal RAS. Since the holding of the address codes ARC0-ARC7 will be maintained even after access is shifted to another cell array

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	block, these registers 70a-70d store respectively the address codes ARC0-ARC7 of the last access in the cell array blocks 10a-10d and supply them to the selectors 80a-80d which also receive the address codes ARC0-ARC7 supplied in synchronism with the row selection signal RAS and introduce them to the row decoders 20a-20d." ['495 Reference, Col. 4:25-37] The '021 Reference states: "Since the low-speed large-capacity memories 11, 12, 13, 14 performing the 4-way interleave operation are shifted in access timing usually by one cycle from each other, the memories 11-14 are provided respectively with registers 23-26 each for holding an address." ['021 Reference, Col. 4:5-9] Further, the '1182 Reference could be combined with any of the '596 Reference or the '297 Reference or the '495 Reference to meet this limitation.
one Y-decoder for each subarray;	This limitation is met by the '1182 Reference alone or in combination with any of the '937 Reference or the '495 Reference or the '021 Reference. Specifically, the '1182 Reference states: "In addition, the center is a column decoder C-DCR, and here is one pair of common complementary data lines CD1 and CD2 that run in the vertical direction left and right. As a result, column switching circuits C-SW1 and C-SW2 that connect the complementary data lines connect the complementary data lines and the common data lines that correspond to the addresses." ['1182 Reference, Page 2, second column] "The main amplifiers MA 1, MA 2 are in an operative state in accordance

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	with the timing signals Φ ma1 and Φ ma2, and they perform the operation of amplification of signals that have been read to the common complementary data lines CD1, CD2." ['1182 Reference, Page 3, second column] Further, the '937 Reference teaches the use of a plurality of decoders as well as the use of a single decoder for performing the same function. [Figs. 3 and 5] The '937 Reference states: "In a similar manner, the delay latch circuit 105 delays the outputs from the Y decoder 83 respectively by one cycle of the basic clock pulses $Ø_S$ to transmit the same to the transfer gate 95. Thus, selected are memory cells in the second memory cell array 65 forming an odd address plane by the outputs from the delay latch circuits 105 and 106. It is to be noted that odd address cycles are always delayed from the even address cycles respectively by one cycle of the basic clock pulses $Ø_S$. Thus, this embodiment is equivalent in operation to that shown in FIG. 3." ['937 Reference, Col. 7:53-63] The '495 Reference states: "The output of the block decoder 50 is supplied in common to the row decoders 20a and 20d and the column decoders 40a to 40d. " ['495 Reference, Col. 3:39-41] The '021 Reference states: "In FIG. 1, numeral 100 designates clock signals to be supplied to the interleave controller 20, the select controller 30 and the high-speed memory access controller 40, numerals 111, 112, 113, 114 designate

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	output data from the low-speed large-capacity memories 11, 12, 13, 14 respectively, numeral 120 designates an address signal to be supplied to the interleave controller 20, numerals 121, 122, 123, 124 designate address signals from the interleave controller 20 to the low-speed large-capacity memories 11, 12, 13, 14 respectively, ..." ['021 Reference, Col. 3:43-68] Each memory 11, 12, 13, and 14 would have a y-decoder. Further, the '1182 Reference could be combined with any of the '596 Reference or the '297 Reference or the '495 Reference to meet this limitation.
one Y-register for each Y-decoder;	This element is met by the '1182 Reference alone or in combination with the '196 Reference or the '937 Reference. Specifically, the '1182 Reference states: "Specifically, address signals that have been provided from an external terminal in accordance with operation mode signals that have been designated from specified external control signals are incorporated as the initial values; there is an address counter circuit that performs a stepping operation based on the pulse that has been provided from the external terminal; the address signals that have been formed by the above-mentioned address conter circuit in accordance with the above-mentioned operation mode signals are relayed to an address decoder via a multiplexer; and in accordance with the address signals formed by the above-mentioned address counter circuit, column selection operations for the other memory array where the word line is already in a state of selection is performed upon completion of the final selection of addresses for one of the memory arrays during column selection for the memory array that has been partitions into two." ['1182 Reference, Page 2, first and second column; *see also* Fig. 1; *see also* Claim 1]

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	To the extent AMD reads this limitation on the Samsung devices, this '1182 Reference meets this limitation. The '196 Reference states that: "The row and column location in the arrays 31, 33 at which data is accessed is controlled by the counters which, in one embodiment of the invention may be binary counters, or the like, which have an extended counting range that is double the number of address locations in the array to be accessed." ['196 Reference, Col. 4:49-55; See also, FIGS. 2A, 2B] The '937 Reference states: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42] Further, the '1182 Reference could be combined with any of the '596 Reference or the '297 Reference or the '495 Reference to meet this

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	limitation.
one Y-select circuit for each subarray, the Y-select circuit being responsive to the Y-decoder of the subarray to select all the columns that occupy a selected position in the groups of the subarray;	This limitation is met by the '1182 Reference alone or in combination with the '937 Reference. Specifically, the '1182 Reference states: "In addition, the center is a column decoder C-DCR, and here is one pair of common complementary data lines CD1 and CD2 that run in the vertical direction left and right. As a result, column switching circuits C-SW1 and C-SW2 that connect the complementary data lines connect the complementary data lines and the common data lines that correspond to the addresses." ['1182 Reference, Page 2, second column] "The main amplifiers MA 1, MA 2 are in an operative state in accordance with the timing signals Φ ma1 and Φ ma2, and they perform the operation of amplification of signals that have been read to the common complementary data lines CD1, CD2." ['1182 Reference, Page 3, second column] The '937 Reference states: "Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to a transfer gate 85.... In a similar manner, the transfer gate 95 transfers data read from the second memory cell array 94 to the sense amplifier 96 through an I/O line 103, while transferring data from the write circuit 98 received through the I/O line 103 to the second memory cell array 94." ['937 Reference, Col. 4:33-52] Further, the '1182 Reference could be combined with any of the '596 Reference or the '297 Reference or the '495 Reference to meet this

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	limitation.
a plurality of sense amplifier circuits for each subarray, each sense amplifier circuit for amplifying signals from a column selected by the Y-select circuit of the subarray;	This element is met in the '1182 Reference. Specfically, the '1182 Reference states: "During writing and reading, the sense amplifiers SA1, SA2 will be in an operative state selectively because of the dynamic signasl Φ pa1, Φ pa2 …." ['1182 Reference, Page 2, second column]
a memory output; and	This element is met in the '1182 Reference. Specifically, the '1182 Reference states that: "In response to that, if there is a reading operation where only the main amplifier operation timings signals Φma1 are at a high level, the main amplifier MA 1 will be in the operative state, and the write-enable signals [we bar] will be at a high level, and the memory information from the memory cell that has been selected as mentioned above will be transmitted to the external terminal D through the data output circuit of the data input-output circuit I/O." ['1182 Reference, Page 5, second colum]
a control circuit for selecting one of the sense amplifier circuits to provide data to the memory output;	This limitation is met by the '1182 Reference. Specifically, the '1182 Reference states: "In response to that, the operation timing signals Φ pa 1 and Φ pa 2 of the sense amplifiers SA 1 and SA 2, which are slower than the above-mentioned word line selection timing signals Φ x 1 and Φ x 2, are generated at the same time too. Next, in the event that the column address that serves as the above-

CLAIM	RESPONSE
	mentioned initial value was the final address 1023 that had been allocated to the memory array M-ARY 1 on the left side, only the data line selection timing signals Φ y1 will be made to be a high level, the column switching circuit C-SW 1 of the memory M-ARY 1 that is on the left side will be selected, and the data line that corresponds to the above-mentioned address will be linked to the common complementary data line CD 1. . . . " ['1182 Reference, Page 5, first column] Further, the '1182 Reference could be combined with any of the '596 Reference or the '297 Reference or the '495 Reference to meet this limitation.
wherein in a burst mode read operation, at least one X-register provides to its respective X-decoder signals identifying a row in one of the subarrays, and at least one Y-register provides to its respective Y-decoder signals identifying a position of columns in the groups of one of the subarrays.	This limitation is met by the '1182 Reference alone or in combination with any of the '196 Reference or the '937 Reference or the '754 Reference or the '494 Reference. Specifically, for the '1182 Reference, see the description of the operation of the circuit of Figure 1 from Page 4, second column to Page 6, second column. The '196 Reference states: "In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit lines in the other array are being precharged. Thus, as data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit lines in that array will already have been initialied." ['196 Reference, Col. 2:60-67] "In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and settling transient

CLAIM	RESPONSE
	signals) in preparation for the next access form such other array. Therefore, precharging times for one array overlap the time for performing read or write operation in the other array, and therefore do not limit operating speed." ['196 Reference, Col. 3:41-47] The '937 patent states that: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:33-42] The '754 Reference states: "Furthermore, this dynamic memory device has row and column address buffers 20 and 22 for respectively storing row and column address data supplied from an address signal generator (not shown); …." ['754 Reference, Page 4:44-51] "Output data from the row address buffer 20 excluding the most significant bit MSB is supplied to the row decoders 16-1 to 16-4, and the

CLAIM	RESPONSE
	output data from the column address buffer 22 is supplied to the columns decoders 14-1 and 14-2 through the gate circuits 30 and 32, respectively." ['754 Reference, Page 4:52-54] The '494 Reference states: In the example shown in FIG. 1 each memory block 14 and 15 has sixty four columns 35, each column being coupled to equate and precharge circuitry 36. The columns are arranged in groups, each group having eight pairs of bit lines so that when any column is addressed eight pairs of bit lines (one in each group) are simultaneously accessed, permitting transfer of eight bits or one word at a time. The bit lines are each connected to column multiplexing circuitry 37 for each columns and coupled to sense amplifier and write circuitry 38 for each column. Each sense amplifier and write circuit is connected through a bus driver circuit 39 to the data output 17. Each memory block 14 and 15 has 70 rows each having a word line 25. The word lines are connected to a row decoder 40. The row decoder is coupled to memory block 14 through a latch and word line driver 41 and to the memory block 15 through a latch and word line driver 42. The column multiplex circuitry 37 is controlled by a column counter 44. The row decoder 40 is controlled by a row counter 45. The latch and word line drivers 41 and 42 are controlled by pulse generators 46 and 47 respectively. Each of the drivers 41 and 42 is connected by two separate control lines 48 to the respective one of the pulse generators 46 and 47 so that each driver can be operated either to latch the output of the row decoder 40 or to drive all the word lines low. The selection of memory locations forming each cyclic pattern of addressing is controlled by the control until 13. The row counter 45 and columns counter 44 are connected so that unless instructed by the control 13 to do otherwise they

CLAIM	RESPONSE
	count through successive addresses along each row and then row by row." ['494 Reference, Col. 7:44-8:27] Further, the '1182 Reference could be combined with any of the '596 Reference or the '297 Reference or the '495 Reference to meet this limitation.
22. The memory of claim 20 wherein in the burst mode read operation while data from the sense amplifier circuits of one of the subarrays are provided to the memory output, the sense amplifier circuits of another one of the subarrays develop output signals corresponding to data in said other one of the subarrays.	This limitation is met by the '1182 Reference alone or in combination with the '196 Reference. Specifically, for the '1182 Reference, see the description of the operation of the circuit of Figure 1 from Page 4, second column to Page 6, second column. *See also* Figure 3. The '196 Reference states that: "In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit lines in the other array are being precharged. Thus, as data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit lines in that array will already have been initialied." ['196 Reference, Col. 2:60-67] "In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and settling transient signals) in preparation for the next access form such other array. Therefore, precharging times for one array overlap the time for performing read or write operation in the other array, and therefore do not limit operating speed." ['196 Reference, Col. 3:41-47]
23. The memory of claim 20 wherein in the burst mode	This limitation is met by the '1182 Reference alone or in combination

CLAIM	RESPONSE
read operation, the control circuit enables the sense amplifier circuit selected to provide data to the memory output and at the same time disables one or more sense amplifier circuits not selected to provide data to the memory output.	with any of the '754 Reference or the '788 Reference or the '937 Reference or the '003 Reference or the '178 Reference. Specifically, the '1182 Reference states: "In response to that, the operation timing signals Φ pa 1 and Φ pa 2 of the sense amplifiers SA 1 and SA 2, which are slower than the above-mentioned word line selection timing signals Φ x 1 and Φ x 2, are generated at the same time too. Next, in the event that the column address that serves as the above-mentioned initial value was the final address 1023 that had been allocated to the memory array M-ARY 1 on the left side, only the data line selection timing signals Φ y1 will be made to be a high level, the column switching circuit C-SW 1 of the memory M-ARY 1 that is on the left side will be selected, and the data line that corresponds to the above-mentioned address will be linked to the common complementary data line CD 1. . . . " ['1182 Reference, Page 5, first column] The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20]

CLAIM	RESPONSE
	"As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58] The '788 Reference states: "According to this arrangement, only one plane is selected in accordance with the content of the upper-order two bits of the row address. The selected plane is activated and exhibits the memory operation but the rest of the planes which are under the non-selection state are inoperative. Therefore, the decoders and the sense amplifiers are inoperative in these inoperative planes and the memory is not refreshed. Therefore, power is consumed in only the selected plane and unnecessary power consumption in the other plane can be saved. Thus, the requirement for low power consumption can be satisfied." ['788 Reference, Col. 5:57-68] The '937 Reference states: "The sense amplifier 86 is controlled by the signals SE_{EV} to amplify the read data thereby to supply the same to the data latch 87, which in turn temporarily stores the outputs from the sense amplifiers 86. When the signals SE_{EV} are at low levels, the data latch 87 is electrically cut off from the sense amplifier 86. Data from the data latch 87 are transferred to the output latch 89 when the signals OE_{EV} are at high levels. In a similar manner, the sense amplifier 96 is controlled by the signals SE_{OD} to amplify the read data thereby to supply the same to the data latch 97, which in turn temporarily stores the outputs from the sense amplifier 96. When the signals SE_{OD} are at low levels, the data latch 97 is electrically

CLAIM	RESPONSE
	cut off from the sense amplifier 96." ['937 Reference, Col. 4:52-66] The '003 Reference states: "The flash memory control 88 also selectively enables one of two sets of bi-directional data buffers 90 and 91 which respectively couple the bank data buses 82 and 83 to the processor section data bus 63. The bank data buses 81 and 83 can be coupled to the instruction bus 61 by the flash memory control 88 selectively enabling buffers 92 and 93, respectively." ['003 Reference, Col. 9:21-27] The '178 Reference states: "Referring now to FIG. 2, the circuit of FIG. 1 has been modified to utilize the fact that, when RA10=1, only one half of the ARRAY BANKs 20 are being utilized and that, when RA10=0, the other half of the ARRAY BANKs 20 are being utilized. In particular, the RA 10 address is used to cause only the half of the ARRAY BANKs 20 that are being utilized to draw power from the DRAM energy source during read/write operations, while at the same time permitting the periodic performance of the refresh cycle in the usual manner on all ARRAY BANKs." ['178 Reference, Col. 3:32-42]