EXHIBIT 1

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CLAIM	RESPONSE
out to said output in a shorter time than the first location to be read out.	The '587 Reference states: "The reduction in the memory access cycle time from a convention memory access operation, generally represented by the first prefetch with a three clock cycle span between event t1 and t2, is clearly evident when the times are compared to those of the consecutive prefetch operation extending for two clock cycles between corresponding time intervals t3 and t4. Time t2 and t4 identify the first clock interval suitable to initiate succeeding memory access operations." ['587 Reference, Col. 5:63-6:3] The '003 Reference states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41]

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	The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer. Typically, the access addresses of these 'extra' storage cells differ from the original access address by only one or two bits. However, subsequent accesses to these cells can be accomplished by simply executing additional access cycles without changing the access address. In the art, such memories are referred to as 'nibble mode'. In some other integrated circuit memories, a portion of the original address can be 'assumed' from one (or more) subsequent accesses, so that only the least significant portion of the address needs to be decoded, etc. Thus, once the original access had been completed, subsequent accesses to 'related' storage cells will be significantly quicker." ['199 Reference, Col. 1:13-28]
12. The memory of claim 8 wherein the sequence of locations L1, . . . , Ln is a sequence of increasing order of addresses.	This limitation is met by the '196 Reference. Specifically, the '196 Reference states: "Consecutive addresses are mapped sequentially be [sic] columns, so repeated reading or writing effectively marches along the row until the array boundary is reached." ['196 Reference, Col. 1:57-60]
13. The memory of claim 7 wherein in said operation any number of said locations addressed consecutively with wrap around can be read out to said output so that:	This element is met by the '196 Reference in combination with the '885 Reference or the '631 Reference. The '885 Reference states: "After the last memory address is reached, the access automatically rolls over to the first address." ['885 Reference, Col. 3:1-3] "A method as in claim 5 wherein the sequence of incremented addresses wraps around when the address of the Nth register is reached such that all N registers in the array are

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	read." ['885 Reference, Col. 7:45-48] The '631 Reference states that: "The above-described method is accomplished by utilizing two pieces of information, which are placed on the bus (23) by the GDP: the data word's offset and the number of words requested. The data word's offset in the cache line is derived from adress bits 2 and 3 (00=word 1, 01=word 2, 10=word 3, and 11=word 4). The number of words being requested is obtained from the size bits 0 and 1 (00=1word, 01=2 words, 10=3 words, and 11=4words). Using these two pieces of information, the following algorithm is executed: FIRST WORD ACCESSED = PROCESSOR WORD ADDRESS + SIZE +1 The 1 is added to the size in order to yield the correct offset. For example, if the GDP requests two words at offset 01 in a four-word line, it is convereted to a wraparound request of four words to memory starting at word four [offset (01) + word count (01) + 1 = 11]." ['631 Reference, Col. 3:46-65] See, '631 Reference, Table II:

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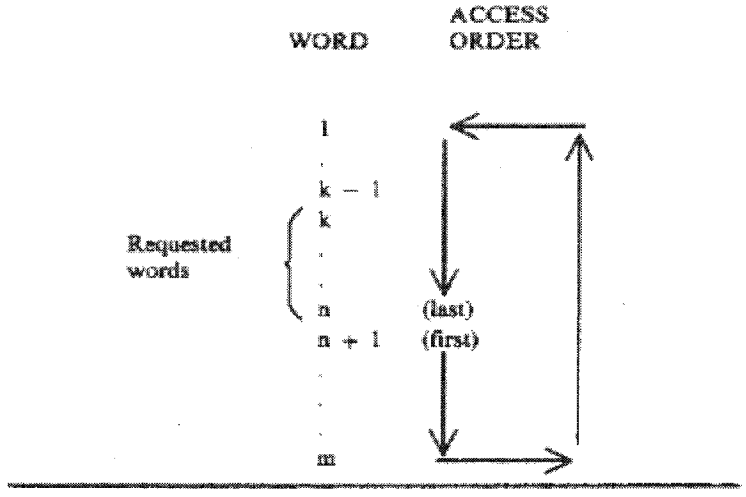
	TABLE II  See also, '631 Reference, Abstract, Table I, Fig. 3.
the first location to be read out in said operation is read out to said output after time tARA+tOE wherein: tARA is measured from the time that an address of said first location is made available to said memory to the time when said plurality of sense amplifier circuits	This element is met by the '196 Reference in combination with any of the '587 Reference or the '003 Reference or the '199 Reference. The '587 Reference states: "The reduction in the memory access cycle time from a convention memory access operation, generally represented by the first prefetch with a three clock cycle span between event t1 and t2, is clearly evident when the times are compared to those of the consecutive prefetch operation extending for two clock cycles between corresponding

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develops an output signal indicative of the contents of said first location; and tOE is the time to transfer the contents of any one of said locations from said plurality of sense amplifier circuits to said output of said memory; and	time intervals t3 and t4. Time t2 and t4 identify the first clock interval suitable to initiate succeeding memory access operations." ['587 Reference, Col. 5:63-6:3] The '003 Reference states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer. Typically, the access addresses of the 'extra' storage cells differ from the original access address by only one or two bits. However, subsequent accesses to these cells can be accomplished by simply executing additional access cycles without changing

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	the access address. In the art, such memories are referred to as 'nibble mode'. In some other integrated circuit memories, a portion of the original address can be 'assumed' for one (or more) subsequent accesses, so that only the least significant portion of the address needs to be decoded, etc. Thus, once the original access had been completed, subsequent accesses to 'related' storage cells will be significantly quicker." ['199 Reference, Col. 1:13-28]
every other location to be read out in said operation is read out to said output within time tOE.	This element is met by the '196 Reference in combination with any of the following: The '587 Reference states: "The reduction in the memory access cycle time from a convention memory access operation, generally represented by the first prefetch with a three clock cycle span between event t1 and t2, is clearly evident when the times are compared to those of the consecutive prefetch operation extending for two clock cycles between corresponding time intervals t3 and t4. Time t2 and t4 identify the first clock interval suitable to initiate succeeding memory access operations." ['587 Reference, Col. 5:63-6:3] The '003 Reference states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first

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	instruction." ['003 Reference, Col. 10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer. Typically, the access addresses of the 'extra' storage cells differ from the original access address by only one or two bits. However, subsequent accesses to these cells can be accomplished by simply executing additional access cycles without changing the access address. In the art, such memories are referred to as 'nibble mode'. In some other integrated circuit memories, a portion of the original address can be 'assumed' from one (or more) subsequent accesses, so that only the least significant portion of the address needs to be decoded, etc. Thus, once the original access had been completed, subsequent accesses to 'related' storage cells will be significantly quicker." ['199 Reference, Col. 1:13-28]
14. The memory of claim 8 wherein said memory is fabricated in an integrated circuit.	This element is met by the '196 Reference alone or in combination with any of the '754 Reference or the '199 Reference or the '312 Reference. It was well known in the art to fabricate memories as an integrated circuit and a person of ordinary skill would have know that the memory device shown in the '494 Reference could be fabricated in an integrated circuit.

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	The '754 Reference states: "The present invention relates to a semiconductor dynamic memory device. Mass-production of 64K bit dynamic type random access memory devices (DRAMs) has been enabled by the recent development of semiconductor memory devices of high packing density. Furthermore, a 256K bit DRAM has been developed." ['754 Reference, Page 2:3-6] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer." ['199 Reference, Col. 1:13-16] The '312 Reference states: "The individual circuit elements constructing the RAM of the present embodiment are formed on a semiconductor substrate such as a piece of single-crystalline silicon by the known technique for fabricating a CMOS (i.e., Complementary MOS) integreated circuit." ['312 Reference, Col. 2:34-38]
20. An integrated memory comprising:	
an array of memory locations, the array comprising a plurality of subarrays, each subarray comprising a predetermined number of groups of columns of the memory locations such that for any given column position in a group, the memory locations in any given row in the columns at said given position in the groups of the subarray have	This element is met in the '196 Reference. Specifically, the '196 Reference states that: "Consecutive addresses are mapped sequentially be [sic] columns, so repeated reading or writing effectively marches along the row until the array boundary is reached." ['196 Reference, Col. 1:57-60] "Referring now to FIGS. 2A and 2B, there is shown a block schematic diagram of a pair of RAM arrays 31, 33, each comprising a plurality of individual memory cells of

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consecutive addresses;	the type illustrated and described above with reference to FIGS. 1A and 1B." ['196 Reference, Col. 3:11-15]
one X-decoder for each subarray;	This elements is met by the '196 Reference alone or in combination with the '937 Reference or the '495 Reference or the '021 Reference. "Referring now to FIGS. 2A and 2B, there is shown a block schematic diagram of a pair of RAM arrays 31, 33, each comprising a plurality of individual memory cells of the type illustrated and described above with reference to FIGS. 1A and 1B. Each of these arrays may be configured to store data in a matrix of rows and columsn [sic] that is several columns long and several rows deep (e.g. 72 X1 28). The columns and rows of memory cells in each array are connected to decoders for writing and reading data into and out of selected memory cells in the arrays. Specifically, the write column decoders 35, 37 are connected to the dual arrays to address selected columns of memory cells, and the write row decoders and drivers 39, 41 are connected to the dual arrays to address selected rows of memory cells. Similarly, the read column decoders 45,47 are connected to the dual arrays to address selected columns of memory cells , and the read row decoders and drivers 49, 51 are connected to the dual arrays to address selected rows." ['196 Reference, Col. 3:11-29; See also FIGS 1A, 1B, 2A] "The row and column location in the arrays 31, 33 at which data is accessed is controlled by the counters which, in one embodiment of the invention may be binary counters, or the like, which have an extended counting range that is double the number of address locations in the array to be accessed." ['196 Reference, Col. 4:49-55; See also, FIGS. 2A, 2B] Further, the '937 Reference teaches the use of a plurality of decoders as well as the use of a single decoder for performing the same function. [Figs. 3 and 5] The '937

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	Reference states: "The latch (see FIG. 6) forming the delay latch circuit 106 fetches the outputs from the X decoder 82 on the leading edges of the clock pulses $Ø_L$, and hence the delay latch circuit 106 delays the outputs from the X decoder 82 respectively by one cycle of the basic clock pulses $Ø_S$ to transfer the same to the second memory cell array 94. . . . It is to be noted that odd address cycles are always delayed from the even address cycles respectively by one cycle of the basic clock pulses $Ø_S$. Thus, this embodiment is equivalent in operation to that shown in FIG. 3" ['937 Reference, Col. 7:44-63] The '495 Reference states: "The output of the block decoder 50 is supplied in common to the row decoders 20a and 20d and the column decoders 40a to 40d. As a result, one word line is selected in the memory cell array block 10a, for example." ['495 Reference, Col. 3:39-42] The '021 Reference states: "In FIG. 1, numeral 100 designates clock signals to be supplied to the interleave controller 20, the select controller 30 and the high-speed memory access controller 40, numerals 111, 112, 113, 114 designate output data from the low-speed large-capacity memories 11, 12, 13, 14 respectively, numeral 120 designates an address signal to be supplied to the interleave controller 20, numerals 121, 122, 123, 124 designate address signals from the interleave controller 20 to the low-speed large-capacity memories 11, 12, 13, 14 respectively, ..." ['021 Reference, Col. 3:43-68] Each memory 11, 12, 13, and 14 would have a decoder for receiving an address from interleave controller 20.
one X-register for each X-decoder;	This element is met by the '196 Reference alone or in combination with any of the '937 Reference or the '495 Reference or the '021 Reference.

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	The '196 Reference states that: "The row and column location in the arrays 31, 33 at which data is accessed is controlled by the counters which, in one embodiment of the invention may be binary counters, or the like, which have an extended counting range that is double the number of address locations in the array to be accessed." ['196 Reference, Col. 4:49-54; See also, FIGS. 2A, 2B] Further, one of ordinary skill in the art would know that the counters shown are, or can be, implemented through the use of a register. The '937 Reference states: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. Ina similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42] The '495 Reference states: "The register 70a, 70b, 70c or 70d selected by the block decoder 50 holds 8-bit address codes ARC0-ARC7 supplied in synchronism with the row selection signal RAS. Since the holding of the address codes ARC0-ARC7 will be maintained even after access is shifted to another cell array block, these registers 70a-70d store respectively the

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	address codes ARC0-ARC7 of the last access in the cell array blocks 10a-10d and supply them to the selectors 80a-80d which also receive the address codes ARC0-ARC7 supplied in synchronism with the row selection signal RAS and introduce them to the row decoders 20a-20d." ['495 Reference, Col. 4:25-37] The '021 Reference states: "Since the low-speed large-capacity memories 11, 12, 13, 14 performing the 4-way interleave operation are shifted in access timing usually by one cycle from each other, the memories 11 14 are provided respectively with registers 23 26 each for holding an address." ['021 Reference, Col. 4:5-9]
one Y-decoder for each subarray;	This elements is met by the '196 Reference alone or in combination with the '937 Reference or the '495 Reference or the '021 Reference. Specifically, the '196 Reference states: "Referring now to FIGS. 2A and 2B, there is shown a block schematic diagram of a pair of RAM arrays 31, 33, each comprising a plurality of individual memory cells of the type illustrated and described above with reference to FIGS. 1A and 1B. Each of these arrays may be configured to store data in a matrix of rows and columsn [sic] that is several columns long and several rows deep (e.g. 72X128). The columns and rows of memory cells in each array are connected to decoders for writing and reading data into and out of selected memory cells in the arrays. Specifically, the write column decoders 35, 37 are connected to the dual arrays to address selected columns of memory cells, and the write row decoders and drivers 39, 41 are connected to the dual arrays to address selected rows of memory cells. Similarly, the read column decoders 45,47 are connected to the dual arrays to address selected columns of memory cells , and the read row decoders and drivers 49, 51 are connected to the dual arrays to address selected rows." ['196 Reference, Col. 3:11-29; See also FIGS 1A, 1B, 2A]

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	"The row and column location in the arrays 31, 33 at which data is accessed is controlled by the counters which, in one embodiment of the invention may be binary counters, or the like, which have an extended counting range that is double the number of address locations in the array to be accessed." ['196 Reference, Col. 4:49-54; See also, FIGS. 2A, 2B] Further, the '937 Reference teaches the use of a plurality of decoders as well as the use of a single decoder for performing the same function. [Figs. 3 and 5] The '937 Reference states: "In a similar manner, the delay latch circuit 105 delays the outputs from the Y decoder 83 respectively by one cycle of the basic clock pulses $Ø_S$ to transmit the same to the transfer gate 95. Thus, selected are memory cells in the second memory cell array 65 forming an odd address plane by the outputs from the delay latch circuits 105 and 106. It is to be noted that odd address cycles are always delayed from the even address cycles respectively by one cycle of the basic clock pulses $Ø_S$. Thus, this embodiment is equivalent in operation to that shown in FIG. 3." ['937 Reference, Col. 7:53-63] The '495 Reference states: "The output of the block decoder 50 is supplied in common to the row decoders 20a and 20d and the column decoders 40a to 40d. " ['495 Reference, Col. 3:39-41] The '021 Reference states: "In FIG. 1, numeral 100 designates clock signals to be supplied to the interleave controller 20, the select controller 30 and the high-speed memory access controller 40, numerals 111, 112, 113, 114 designate output data from the low-speed large-capacity memories 11, 12, 13, 14 respectively, numeral 120 designates an address signal to be supplied to the interleave controller 20, numerals 121, 122, 123, 124 designate address

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	signals from the interleave controller 20 to the low-speed large-capacity memories 11, 12, 13, 14 respectively, ..." ['021 Reference, Col. 3:43-68] Each memory 11, 12, 13, and 14 would have a y-decoder.
one Y-register for each Y-decoder;	This element is met by the '196 Reference alone or in combination with the '937 Reference. The '196 Reference states that: "The row and column location in the arrays 31, 33 at which data is accessed is controlled by the counters which, in one embodiment of the invention may be binary counters, or the like, which have an extended counting range that is double the number of address locations in the array to be accessed." ['196 Reference, Col. 4:49-55; See also, FIGS. 2A, 2B] Further, one of ordinary skill in the art would know that the counters shown are, or can be, implemented through the use of a register. The '937 Reference states: "The address counter 81 receives the signals $\emptyset_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $\emptyset_{EV}$ (i.e., twice that of the basic clock pulses $\emptyset_S$). Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $\emptyset_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $\emptyset_{OD}$ (i.e., twice that of the basic clock pulses $\emptyset_S$). Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer

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	gate 95." ['937 Reference, Col. 4:29-42]
one Y-select circuit for each subarray, the Y-select circuit being responsive to the Y-decoder of the subarray to select all the columns that occupy a selected position in the groups of the subarray;	This element is met by the '196 Reference alone or in combination with the '937 Reference. The '196 Reference states that: "Similarly, the data which is to be read out from the RAM arrays 31, 33 is designated in selected 9-column segments by the column predecoders 61 which, in turn, is selected by the read pointer counters 63. The columns thus addressed may extend over both arrays, where each column is uniquely addressable, and the arrays alternate when the boundary of column addresses for a given array is reached, as previously described." ['196 Reference, Col. 4:5-12] The '937 Reference states: "Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to a transfer gate 85.... In a similar manner, the transfer gate 95 transfers data read from the second memory cell array 94 to the sense amplifier 96 through an I/O line 103, while transferring data from the write circuit 98 received through the I/O line 103 to the second memory cell array 94." ['937 Reference, Col. 4:33-52]
a plurality of sense amplifier circuits for each subarray, each sense amplifier circuit for amplifying signals from a column selected by the Y-select circuit of the	This element is met in the '196 Reference. Specifically, the '196 Reference states that: "Similarly, the data-out buffer 44 includes one byte of storage plus the additional parity or control bit, and is connected via sense amplifier 53 to receive the output of the read column decoders 45, 47." ['196 Reference, Col. 3:37-40]

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subarray;	See, FIG. 2A, which shows, at 53, "Sense Amps (9)", e.g., a collection of nine separate sense amplifiers for receiving 9 bits of information transmitted from the column decoders 45, 47.
a memory output; and	This element is met in the '196 Reference. Specifically, the '196 Reference states that: "Similarly, the data-out buffer 44 includes one byte of storage plus the additional parity or control bit, and is connected via sens amplifier 53 to receive the output of the read column decoders 45, 47." ['196 Reference, Col. 3:37-40] See, FIG. 2A and FIG. 2B which show the output of the sense amplifier leading to the data-out buffer.
a control circuit for selecting one of the sense amplifier circuits to provide data to the memory output;	It was well known in the art that information in the sense amplifiers could be read out one bit at a time. For example, the '754 Reference discloses this limitation. Specifically, the '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "A semiconductor dynamic memory device comprising: … a plurality of sense amplifying means (18-1 to 18-4; SA1 to SA8) responsive to a control signal input thereto, for selectively activating one sense amplifying means to sense and amplify

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	data on said selected data lines of one of said two column-selected memory blocks, and for selectively activating at least one other sense amplifying means to refresh data to said each memory cell along said selected word lines; ...." ['754 Reference, Page 6:53-7:5] Further, to the extent AMD contends that the accused Samsung devices practice this limitation, this limitation is met by the '196 Reference.
wherein in a burst mode read operation, at least one X-register provides to its respective X-decoder signals identifying a row in one of the subarrays, and at least one Y-register provides to its respective Y-decoder signals identifying a position of columns in the groups of one of the subarrays.	This element is met in the '196 Reference alone or in combination with the '937 Reference or the '754 Reference or the '494 Reference or admitted prior art disclosed in Figure 2 of the '990 patent. Specifically, the '196 Reference states that: "In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit lines in the other array are being precharged. Thus, as data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit lines in that array will already have been initialied." ['196 Reference, Col. 2:60-67] "In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and settling transient signals) in preparation for the next access form such other array. Therefore, precharging times for one array overlap the time for performing read or write operation in the other array, and therefore do not limit operating speed." ['196 Reference, Col. 3:41-47] The '937 patent states that: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder

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	82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:33-42] The '754 Reference states: "Furthermore, this dynamic memory device has row and column address buffers 20 and 22 for respectively storing row and column address data supplied from an address signal generator (not shown); …." ['754 Reference, Page 4:44-51] "Output data from the row address buffer 20 excluding the most significant bit MSB is supplied to the row decoders 16-1 to 16-4, and the output data from the column address buffer 22 is supplied to the columns decoders 14-1 and 14-2 through the gate circuits 30 and 32, respectively." ['754 Reference, Page 4:52-54] The '494 Reference states: In the example shown in FIG. 1 each memory block 14 and 15 has sixty four columns 35, each column being coupled to equate and precharge circuitry 36. The columns are arranged in groups, each group having eight pairs of bit lines so that when any column is addressed eight pairs of bit lines (one in each group) are simultaneously accessed, permitting transfer of eight bits or one word at a time. The bit lines are each connected to column multiplexing circuitry 37 for each columns and coupled to sense amplifier and write circuitry 38 for each column. Each sense amplifier and write circuit is connected through a bus driver circuit 39 to the data output 17. Each memory block 14

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	and 15 has 70 rows each having a word line 25. The word lines are connected to a row decoder 40. The row decoder is coupled to memory block 14 through a latch and word line driver 41 and to the memory block 15 through a latch and word line driver 42. The column multiplex circuitry 37 is controlled by a column counter 44. The row decoder 40 is controlled by a row counter 45. The latch and word line drivers 41 and 42 are controlled by pulse generators 46 and 47 respectively. Each of the drivers 41 and 42 is connected by two separate control lines 48 to the respective one of the pulse generators 46 and 47 so that each driver can be operated either to latch the output of the row decoder 40 or to drive all the word lines low. The selection of memory locations forming each cyclic pattern of addressing is controlled by the control until 13. The row counter 45 and columns counter 44 are connected so that unless instructed by the control 13 to do otherwise they count through successive addresses along each row and then row by row." ['494 Reference, Col. 7:44-8:27]
22. The memory of claim 20 wherein in the burst mode read operation while data from the sense amplifier circuits of one of the subarrays are provided to the memory output, the sense amplifier circuits of another one of the subarrays develop output signals corresponding to data in said other one of the subarrays.	This element is met in the '196 Reference. Specifically, the '196 Reference states that: "In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit lines in the other array are being precharged. Thus, as data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit lines in that array will already have been initialied." ['196 Reference, Col. 2:60-67] "In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and settling transient signals) in preparation for the next access form such other array. Therefore, precharging times for one array overlap the time for performing read or write operation in the other array, and therefore do not limit operating speed." ['196 Reference, Col. 3:41-47]
23. The memory of claim 20 wherein in the	This limitation is met by the '196 Reference in combination with any of the '754

CLAIM	RESPONSE
burst mode read operation, the control circuit enables the sense amplifier circuit selected to provide data to the memory output and at the same time disables one or more sense amplifier circuits not selected to provide data to the memory output.	Reference or the '788 Reference or the '937 Reference or the '003 Reference or the '178 Reference. The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58] The '788 Reference states: "According to this arrangement, only one plane is selected in accordance with the content of the upper-order two bits of the row address. The selected plane is activated and exhibits the memory operation but the rest of the planes which are under the non-selection state are inoperative. Therefore, the decoders and the sense amplifiers are inoperative in these inoperative planes and the memory is not refreshed. Therefore, power is consumed in only the selected plane and unnecessary power consumption in the other plane can be saved. Thus, the requirement for low power consumption can be satisfied." ['788 Reference, Col. 5:57-68] The '937 Reference states: