EXHIBIT 1

D9

Appendix D9
Defendants and Counterclaimants' Invalidity Contentions
Advanced Micro Devices, Inc., et al., v. Samsung Electronics Co., Ltd., et al., Case No. 3:08-CV-0986-SI

U.S. patent No. 5,559,990 Invalidity Chart: U.S. Patent No. 5,280,594 ("the '594 Reference")

All asserted claims are anticipated by the '594 Reference and/or are rendered obvious by it, either alone or in combination with other prior art described below and/or listed in Section I of Defendants' and Counterclaimants' Preliminary Invalidity Contentions and/or through modifications described below. Nothing in this invalidity chart should be construed as signifying or suggesting Defendants and Counterclaimants' adoption of or acquiescence in any claim scope and/or claim construction positions taken by Plaintiffs and Counterdefendants in this litigation.

CLAIM	RESPONSE
1. A memory comprising:	Although a preamble is normally not limiting, should this preamble be limiting, this element is met by U.S. Patent No. 5,280,594 ("the '594 Reference"). Specifically, the '594 Reference is titled "Architecture for High Speed Contiguous Sequential Access Memories."
a plurality of rows of memory locations;	This limitation is met by the '594 Reference. Specifically, the '594 Reference states: "The remaining address bits A3-A16 specifies row address." ['594 Reference, Col. 3:41-42] "memory array means having a plurality of memory cells for storing data and from which data may be retrieved, …" ['594 Reference, Col. 5:47-58]
a plurality of first registers, each first register for receiving a row address;	This limitation is met by the '594 Reference alone or in combination. Specifically, the '594 Reference states: "In this embodiment, the row address A3-A16 is latched into address counter 400." ['594 Reference, Col. 3:60-62]

	"A scheme removing even this limitation is provided in a copending application entitled 'Scheme for Eliminating Page Boundard,' by Elvan S. Young et al, Ser. No. 07,557,899,[1] now abandoned filed on the same day as the present invention, assigned to the same assignee as the present invention, and which is hereby incorporated by reference in its entirety." ['594 Reference, Col. 5:27-34] The '899 application states: "The organization of the memory array 503 is shown in Figure 6. As shown in Figure 6, the memory array 503 is divided into left and right halves. Word lines WLK+1 and WLK, corresponding to consecutive row addrsses are activated simultaneously when signal N+1 is asserted." ['899 Application, Page 7:16-20; *see also* Fig. 6] To the extent AMD reads this limitation on the Samsung devices, the '594 Reference discloses this limitation. Further, the '594 Reference could be combined with any of U.S. Patent No. 5,274,596 ("the '596 Reference") or U.S. Patent No. 4,811,297 ("the '297 Reference") or U.S. Patent No. 5,367,495 ("the '495 Reference") or U.S. Patent No. 4,680,738 ("the '738 Reference") or JP-02-282994-A ("the '994 Reference") or JP-62-1182-A ("the '1182 Reference") to meet this limitation.
a plurality of row decoders, each row decoder for activating a	This limitation is met by the '594 Reference alone or in

[1] The '899 application is the parent application for U.S. Patent No. 5,285,421 ("the '421 Reference") and the cites to the '899 reference should also be treated as cites to the same Figures and passages found in the '421 Reference.

portion of a row identified by signals from one of said first registers;	combination with U.S. Patent No. 4,849,937 ("the '937 Reference"). Specifically, the '594 Reference states: "A scheme removing even this limitation is provided in a copending application entitled 'Scheme for Eliminating Page Boundard,' by Elvan S. Young et al, Ser. No. 07,557,899, now abandoned filed on the same day as the present invention, assigned to the same assignee as the present invention, and which is hereby incorporated by reference in its entirety." ['594 Reference, Col. 5:27-34] The '899 application states: "The organization of the memory array 503 is shown in Figure 6. As shown in Figure 6, the memory array 503 is divided into left and right halves. Word lines WLK+1 and WLK, corresponding to consecutive row addrsses are activated simultaneously when signal N+1 is asserted." ['899 Application, Page 7:16-20; *see also* Fig. 6] Further, the '937 Reference teaches the use of a plurality of decoders as well as the use of a single decoder for performing the same function. [Figs. 3 and 5] The '937 Reference states: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$

	(i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42] "The latch (see FIG. 6) forming the delay latch circuit 106 fetches the outputs from the X decoder 82 on the leading edges of the clock pulses $Ø_L$, and hence the delay latch circuit 106 delays the outputs from the X decoder 82 respectively by one cycle of the basic clock pulses $Ø_S$ to transfer the same to the second memory cell array 94. . . . It is to be noted that odd address cycles are always delayed from the even address cycles respectively by one cycle of the basic clock pulses $Ø_S$. Thus, this embodiment is equivalent in operation to that shown in FIG. 3" ['937 Reference, Col. 7:44-63] Further, the '594 Reference could be combined with any of the '596 Reference or the '297 Reference or the '495 Reference or the '738 Reference or the '994 Reference or the '1182 Reference to meet this limitation.
one or more sense amplifiers for amplifying contents of said memory locations in the row portions; and	This limitation is met by the '594 Reference. Specifically, the '594 Reference states: "FIG. 4 shows a memory organization 40 in accordance with the present invention. For the purpose of comparison, it is assumed that the memory systems 30 and 40, shown respectively in FIGS. 3 and 4, have identical number of memory cells. However, instead of having the eight registers R0 through R7 load the output of sixty four bit lines simultaneously, as in memory system 30, the registers of memory system 40 are divided into two banks A and B, corresponding to registers R0-

	R3 and registers R4-R7 respectively." ['594 Reference, Col. 3:27-36; *see also* Figs. 1, 3, and 4] "A scheme removing even this limitation is provided in a copending application entitled 'Scheme for Eliminating Page Boundard,' by Elvan S. Young et al, Ser. No. 07,557,899, now abandoned filed on the same day as the present invention, assigned to the same assignee as the present invention, and which is hereby incorporated by reference in its entirety." ['594 Reference, Col. 5:27-34] The '899 application states: "During the initial access of memory system 50, rather than loading four bytes into register A, as in memory system 40 shown in Figure 4, eight bytes of data are loaded into registers A and B simultaneously from the initial access of memory system 50. As a result of the ability to activate word lines in the left and right halves independently, register banks A and B may be loaded simultaneously upon initial access with data from two different rows of memory cells, corresponding to two different word lines." ['594 Reference, Page 7:22-32; *see also* Figs. 1, 3, 4, 5 and 6]
an output for providing output signals from said sense amplifiers,	This limitation is met by the '594 Reference. Specifically, the '594 Reference states: "After the specified tOE period following the output enable signal [OE bar] is asserted (the output enable signal [OE bar] is asserted after the BURST signal), the intial access is completed by register ank A providing on output bus 40a the datum corresponding to the initial address. This data is provided by

	register R0, since the initial address is to be specified on a 4-byte boundary. Every tRCO thereafter, the next datum is sequentially provided in increasing address order." ['594 Reference, Col. 4:19-27]
wherein at least two locations L1 and L2 in different rows having different row addresses in said memory can be read out to said output in burst mode such that the memory receives an address of one of said locations and provides in response contents of a plurality of memory locations, including the locations L1 and L2, in the sequence of consecutive addresses, so that while one of said row decoders is activating a row portion comprising said location L1 and contents of said location L1 are being transferred from one or more of said sense amplifiers to said output, another one of said row decoders is activating a row portion comprising said location L2 and contents of said location L2 are being transferred from said location L2 to one or more of said sense amplifiers.	This limitation is met by the '594 Reference. Specifically, the '594 Reference states: "In accordance with the present invention, two output register banks are provided in a memory system. When enabled, the first register bank latches simultaneously from a first set of bit lines data corresponding to a first set of contiguous addresses. Likewise, when enabled, the second register bank independently latches from a second set of bit lines data corresponding to s second set of contiguous addresses following the first set of contiguous addresses. When the content of first register bank is sequentially output according to addresses of the data therein, the second register bank is being loaded with the data in the second set of bit lines corresponding to the next set of contiguous addresses. The first and second sets of contiguous addresses may involve the sme or different word lines." ['594 Reference, Col. 2:49-63; *see also* Figs. 1-5] The '899 application states: "The organization of the memory array 503 is shown in Figure 6. As shown in Figure 6, the memory array 503 is divided into left and right halves. Word lines WLK+1 and WLK, corresponding to consecutive row addrsses are activated simultaneously when signal N+1 is asserted. When signal N+1 is not asserted, activated word lines in both halves have the same row address. During the initial access of memory system 50,

	rather than loading four bytes into register A, as in memory system 40 shown in Figure 4, eight bytes of data are loaded into registers A and B simultaneously from the initial access of memory system 50. As a result of the ability to activate word lines in the left and right halves independently, register banks A and B may be loaded simultaneously upon initial access with data from two different rows of memory cells, corresponding to two different word lines." ['899 Application, Page 7:16-32; *see also* Fig. 6] Further, the '594 Reference could be combined with any of the '596 Reference or the '297 Reference or the '495 Reference or the '738 Reference or the '994 Reference or the '1182 Reference to meet this limitation.
2. The memory of claim 1, said memory having a random mode in which the memory receives an address and provides in response the contents of a unique memory location,	It was well-known in the art to retain a random mode while adding the functionality of a sequential read operation. The following are illustrative: EP 9 326 885 A2 ("the '885 Reference") states: "The circuit provides both random and sequential access functions and allows the memory to be used as a shift register of variable length." ['885 Reference, Page 1] U.S. Patent No. 5, 263,003 ("the '003 Reference") states: "In a first mode, the memory circuit responds to an initial request for access and an address signal by reading data from a storage location in one of the memory banks. Subsequent requests for access to continguous storage locations do no require an address signal, instead a control mechanism responds

	by generating an address to read data alternately from storage locations in the first and second memory banks. In a second mode, the memory circuit responds to every request for access to the memory circuit by enabling access to the first or second memory bank as indicated by an address which accompanied the request." ['003 Reference, Abstract]
wherein, both in burst mode and in random mode, while the contents of said location L1 are being transferred from one or more of said sense amplifiers to said output, the contents of said location L2 are being transferred from said location L2 to one or more of said sense amplifiers.	It would be obvious to a person of skill in the art that transferring the contents of a location L1 from one of the sens amplifiers to the output while the contents of a location L2 are transferred from the location L2 to one or more sense amplifiers could be used in either a burst mode or a random mode. *See* claim 1 above. Further, to the extent AMD reads this limitation on the Samsung devices, this limitation is met by numerous prior art references having both a random access mode and a burst mode.
3. The memory of claim 1 wherein when the locations L1 and L2 are read out in burst mode and when the contents of said location L1 are being transferred from one or more of said sense amplifiers to said output and the contents of said location L2 are being transferred from said location L2 to one or more of said sense amplifiers, the sense amplifiers from which the contents of said location L1 are being transferred are enabled and the sense amplifiers to which the contents of said location L2 are being transferred are disabled, but these latter sense amplifiers become enabled subsequently for amplifying the contents of said location L2.	This limitation is met by the '594 Reference alone or in combination with any of U.S. 4,937,788 ("the '788 Reference") or EP 0 087 754 B1 ("the '754 Reference") or the '937 Reference or the '003 Reference or U.S. Patent No. 5,251,178 ("the '178 Reference"). Specifically, the '594 Reference states: "A scheme removing even this limitation is provided in a copending application entitled 'Scheme for Eliminating Page Boundard,' by Elvan S. Young et al, Ser. No. 07,557,899, now abandoned filed on the same day as the present invention, assigned to the same assignee as the present invention, and which is hereby incorporated by reference in its entirety." ['594 Reference, Col. 5:27-34]

	The '899 application states: "Like memory system 40 shown in Figure 4, the output registers are divided into two banks A and B, receiving data from groups of bit lines, with each bit in each group addressable by the address bits A0-A2. [see inserts E2, E3 and R4] ['899 Application, Page 7:6-10; *see also* Figs. 4 and 5] The '421 Reference states: "Control signal busses 417 and 418 specify which of the four bytes in each of register banks A and B is to be output, and accordingly asserts an output enable signal to each register bank to enable its output buffer." ['421 Reference, Col. 4:43-47] The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58]

	The '788 Reference states: "According to this arrangement, only one plane is selected in accordance with the content of the upper-order two bits of the row address. The selected plane is activated and exhibits the memory operation but the rest of the planes which are under the non-selection state are inoperative. Therefore, the decoders and the sense amplifiers are inoperative in these inoperative planes and the memory is not refreshed. Therefore, power is consumed in only the selected plane and unnecessary power consumption in the other plane can be saved. Thus, the requirement for low power consumption can be satisfied." ['788 Reference, Col. 5:57-68] The '937 Reference states: "The sense amplifier 86 is controlled by the signals SE_{EV} to amplify the read data thereby to supply the same to the data latch 87, which in turn temporarily stores the outputs from the sense amplifiers 86. When the signals SE_{EV} are at low levels, the data latch 87 is electrically cut off from the sense amplifier 86. Data from the data latch 87 are transferred to the output latch 89 when the signals OE_{EV} are at high levels. In a similar manner, the sense amplifier 96 is controlled by the signals SE_{OD} to amplify the read data thereby to supply the same to the data latch 97, which in turn temporarily stores the outputs from the sense amplifier 96. When the signals SE_{OD} are at low levels, the data latch 97 is electrically cut off from the sense amplifier 96." ['937 Reference, Col. 4:52-66] The '003 Reference states:

	"The flash memory control 88 also selectively enables one of two sets of bi-directional data buffers 90 and 91 which respectively couple the bank data buses 82 and 83 to the processor section data bus 63. The bank data buses 82 and 83 can be coupled to the instruction bus 61 by the flash memory control 88 selectively enabling buffers 92 and 93, respectively." ['003 Reference, Col. 9:21-27] The '178 Reference states: "Referring now to FIG. 2, the circuit of FIG. 1 has been modified to utilize the fact that, when RA10=1, only one half of the ARRAY BANKs 20 are being utilized and that, when RA10=0, the other half of the ARRAY BANKs 20 are being utilized. In particular, the RA 10 address is used to cause only the half of the ARRAY BANKs 20 that are being utilized to draw power from the DRAM energy source during read/write operations, while at the same time permitting the periodic performance of the refresh cycle in the usual manner on all ARRAY BANKs." ['178 Reference, Col. 3:32-42]
4. The memory of claim 1 wherein:	
said memory comprises k pluralities S-1, . . . , S-k of locations wherein k is a number of said pluralities and is greater than or equal to two; for each plurality S-i, said sense amplifiers can receive simultaneously the contents of number m of locations from said plurality S-i, wherein m is a positive integer; and	This limitation is met by the '594 Reference. Specifically, the '594 Reference states: "A scheme removing even this limitation is provided in a copending application entitled 'Scheme for Eliminating Page Boundard,' by Elvan S. Young et al, Ser. No. 07,557,899, now abandoned filed on the same day as the present invention, assigned to the same assignee as the present invention, and which is hereby incorporated by reference in its entirety." ['594

	Reference, Col. 5:27-34] The '899 application states: "A word line in the left half memory array may be activated independently but simultaneously with a word line in the right half of the memory array." ['899 Reference, Page 4:9-11] "However, unlike the memory system 40 provided in Figure 4, the memory system 50 is organized into left and right halves, such that the word lines in each half of the memory system 50 are controlled independently of the word lines in the other half." ['899 Reference, Page 7:10-15]
time tARA does not exceed m * (k-1) * (tOE), wherein: tARA is measured from the time that an address of a location is made available to said memory to the time when one or more of said sense amplifiers develop an output signal indicative of the contents of said location; and tOE is the time to transfer an output of any one of said sense amplifiers to said output of said memory.	This limitation is met by the '594 Reference. Specifically, the '594 Reference states: "A scheme removing even this limitation is provided in a copending application entitled 'Scheme for Eliminating Page Boundard,' by Elvan S. Young et al, Ser. No. 07,557,899, now abandoned filed on the same day as the present invention, assigned to the same assignee as the present invention, and which is hereby incorporated by reference in its entirety." ['594 Reference, Col. 5:27-34] The '899 application shows this timing relationship in Figure 2. *See* timing description from Page 2:19-Page 3:8. "The operation of memory system 40 described in the aforementioned copending application shown in Figure 4 is feasible if each register bank satisfies the relation n x tRCO > tASA, where n is the nmber of registers in the register bank."

	['899 Reference, Page 5:8-12] "After the initial access, register banks A and B may be read and loaded in the same interleaving manner as described in the aforementioned copending application." [Insert E5] ['899 Reference, Page 8:20-22] *See also*, '421 Reference, Col. 5:26-53.
5. The memory of claim 1	
wherein, in burst mode, a time in which each location of said plurality except said one of said locations is read out to said output after a previous location has been read out to said output is shorter than a time in which said one of said locations is read out to said output after said address of said one of said locations has been received by said memory.	This limitation is met by the '594 Reference. Specifically, the '594 Reference states: "A scheme removing even this limitation is provided in a copending application entitled 'Scheme for Eliminating Page Boundard,' by Elvan S. Young et al, Ser. No. 07,557,899, now abandoned filed on the same day as the present invention, assigned to the same assignee as the present invention, and which is hereby incorporated by reference in its entirety." ['594 Reference, Col. 5:27-34] The '899 application shows this timing relationship in Figure 2. *See* timing description from Page 2:19-Page 3:8. "The operation of memory system 40 described in the aforementioned copending application shown in Figure 4 is feasible if each register bank satisfies the relation n x tRCO > tASA, where n is the number of registers in the register bank." ['899 Reference, Page 5:8-12] "After the initial access, register banks A and B may be read and loaded in the same interleaving manner as described in the

	aforementioned copending application." [Insert E5] ['899 Reference, Page 8:20-22] *See also*, '421 Reference, Col. 5:26-53.
6. The memory of claim 1 wherein said memory is fabricated in an integrated circuit.	This element is met by the '594 Reference alone or in combination with any of the '754 Reference or the '199 Reference, or U.S. Patent No. 4,899,312 ("the '312 Reference"). It was well known in the art to fabricate memories as an integrated circuit and a person of ordinary skill would have know that the memory device shown in the '196 Reference could be fabricated in an integrated circuit. The '754 Reference states: "The present invention relates to a semiconductor dynamic memory device. Mass-production of 64K bit dynamic type random access memory devices (DRAMs) has been enabled by the recent development of semiconductor memory devices of high packing density. Furthermore, a 256K bit DRAM has been developed." ['754 Reference, Page 2:1-4] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer." ['199 Reference, Col. 1:13-16] The '312 Reference states: "The individual circuit elements constructing the RAM of the

	present embodiment are formed on a semiconductor substrate such as a piece of single-crystalline silicon by the known technique for fabricating a CMOS (i.e., Complementary MOS) integreated circuit." ['312 Reference, Col. 2:34-38]
7. The memory of claim 1 further comprising:	
a plurality of second registers, each second register for receiving at least a portion of a column address; and	This limitation is met by the '594 Reference. Specifically, the '594 Reference states: "In this embodiment, the row address A3-A16 is latched into address counter 400." ['594 Reference, Col. 3:60-62] To the extent AMD reads this limitation on the Samsung devices, the '594 Reference discloses this limitation. Further, the '594 Reference could be combined with any of the '596 Reference or the '297 Reference or the '495 Reference or the '738 Reference or the '994 Reference or the '1182 Reference to meet this limitation.
a circuitry for each second register for selecting in response to signals from one of the second registers a plurality of columns to be read by the sense amplifiers.	This limitation is met by the '594 Reference. Specifically, the '594 Reference provides: "FIG. 1 shows a generalized organization of a memory system, comprising address input register 100, x-and y-decoders 101 and 102 (also known as row and columns decoders), a memory array 103, a sense amplifier circuit 104, a memory output register 105, and output buffers 106." ['594 Reference, Col. 1:13-18] "In accordance with the present invention, two output register banks are provided in a memory system. When enabled, the first register bank latches simultaneously from a first set of bit lines

	data corresponding to a first set of contiguous addresses. Likewise, when enabled, the second register bank independently latches from a second set of bit lines data corresponding to a second set of contiguous addresses following the first set of contiguous addrses." ['594 Reference, Col. 2:49-57] "A scheme removing even this limitation is provided in a copending application entitled 'Scheme for Eliminating Page Boundard,' by Elvan S. Young et al, Ser. No. 07,557,899, now abandoned filed on the same day as the present invention, assigned to the same assignee as the present invention, and which is hereby incorporated by reference in its entirety." ['594 Reference, Col. 5:27-34] The '899 application states: "The organization of the memory array 503 is shown in Figure 6. As shown in Figure 6, the memory array 503 is divided into left and right halves. Word lines WLK+1 and WLK, corresponding to consecutive row addrsses are activated simultaneously when signal N+1 is asserted." ['899 Application, Page 7:16-20; *see also* Fig. 6] Further, the '594 Reference could be combined with any of the '596 Reference or the '297 Reference or the '495 Reference or the '738 Reference or the '994 Reference or the '1182 Reference to meet this limitation.
8. A memory comprising:	Although a preamble is normally not limiting, should this preamble be limiting, this element is met by the '594 Reference. Specifically, the '594 Reference is titled "Architecture for High Speed Contiguous Sequential Access Memories."

a set of consecutively addressed memory locations L1, . . . Ln;	As found for the examiner, the '594 Reference discloses this element. Specifically the '594 References states that: "In accordance with the present invention, two output register banks are provided in a memory system. When enabled, the first register bank latches simultaneously from a first set of bit lines data corresponding to a first set of contiguous addresses. Likewise, when enabled, the second register bank independently latches from a second set of bit lines data corresponding to s second set of contiguous addresses following the first set of contiguous addresses. When the content of first register bank is sequentially output according to addresses of the data therein, the second register bank is being loaded with the data in the second set of bit lines corresponding to the next set of contiguous addresses. The first and second sets of contiguous addresses may involve the same or different word lines." ['594 Reference, Col. 2:49-63; *see also* Figs. 1-5]
a plurality of sense amplifier circuits for amplifying contents of said memory locations; and	As found for the examiner, the '594 Reference discloses this element. Specifically the '594 References states that: "FIG. 4 shows a memory organization 40 in accordance with the present invention. For the purpose of comparison, it is assumed that the memory systems 30 and 40, shown respectively in FIGS. 3 and 4, have identical number of memory cells. However, instead of having the eight registers R0 through R7 load the output of sixty four bit lines simultaneously, as in memory system 30, the registers of memory system 40 are divided into two banks A and B, corresponding to registers R0-R3 and registers R4-R7 respectively." ['594 Reference, Col. 3:27-36; *see also* Figs. 1, 3, and 4]

	"A scheme removing even this limitation is provided in a copending application entitled 'Scheme for Eliminating Page Boundard,' by Elvan S. Young et al, Ser. No. 07,557,899, now abandoned filed on the same day as the present invention, assigned to the same assignee as the present invention, and which is hereby incorporated by reference in its entirety." ['594 Reference, Col. 5:27-34] The '899 application states: "During the initial access of memory system 50, rather than loading four bytes into register A, as in memory system 40 shown in Figure 4, eight bytes of data are loaded into registers A and B simultaneously from the initial access of memory system 50. As a result of the ability to activate word lines in the left and right halves independently, register banks A and B may be loaded simultaneously upon initial access with data from two different rows of memory cells, corresponding to two different word lines." ['594 Reference, Page 7:22-32; *see also* Figs. 1, 3, 4, 5 and 6]
an output for providing output signals from said plurality of sense amplifier circuits,	As found for the examiner, the '594 Reference. Specifically the '594 References states that: "After the specified tOE period following the output enable signal [OE bar] is asserted (the output enable signal [OE bar] is asserted after the BURST signal), the intial access is completed by register bank A providing on output bus 40a the datum corresponding to the initial address. This data is provided by register R0, since the initial address is to be specified on a 4-byte boundary. Every tRCO thereafter, the next datum is sequentially provided in increasing address order." ['594 Reference, Col.

	4:19-27]
wherein said memory has a burst mode operation for receiving an address and reading out to said output, in response to said address, any given number of memory locations in the sequence of consecutive addresses with wrap around so that the next location, if any, to be read out after said location Ln is said location L1, such that during said operation while the contents of any location L to be read out other than the last location to be read out are being transferred from said plurality of sense amplifier circuits to said output, the contents of another location to be read out after said location L are being provided to said plurality of sense amplifier circuits for amplification and subsequent transfer to said output, and	This limitation is met by the '594 Reference alone or in combination with the U.S. Patent No. 4,912,631 ("the '631 Reference") or the '885 Reference. Specifically the '594 References states that: "In accordance with the present invention, two output register banks are provided in a memory system. When enabled, the first register bank latches simultaneously from a first set of bit lines data corresponding to a first set of contiguous addresses. Likewise, when enabled, the second register bank independently latches from a second set of bit lines data corresponding to s second set of contiguous addresses following the first set of contiguous addresses. When the content of first register bank is sequentially output according to addresses of the data therein, the second register bank is being loaded with the data in the second set of bit lines corresponding to the next set of contiguous addresses. The first and second sets of contiguous addresses may involve the same or different word lines." ['594 Reference, Col. 2:49-63; *see also* Figs. 1-5] "As a result, a continuous stream of data from contiguous addresses are made available every tRCO indefinitely for as long as burst mode is asserted. The limit on the number of data accessible from each initial access under burst mode is therefore removed." ['594 Reference, Col. 5:6-10] The '899 application states: "The present invention removes the restriction on the address of the first datum received in burst mode, thereby providing

	continuous sequential access every tRCO after the initial access, from any byte and regardless of whether row boundaries are crossed." ['899 Reference, Page 6:38-Page 7:4] "The organization of the memory array 503 is shown in Figure 6. As shown in Figure 6, the memory array 503 is divided into left and right halves. Word lines WLK+1 and WLK, corresponding to consecutive row addrsses are activated simultaneously when signal N+1 is asserted. When signal N+1 is not asserted, activated word lines in both halves have the same row address. During the initial access of memory system 50, rather than loading four bytes into register A, as in memory system 40 shown in Figure 4, eight bytes of data are loaded into registers A and B simultaneously from the initial access of memory system 50. As a result of the ability to activate word lines in the left and right halves independently, register banks A and B may be loaded simultaneously upon initial access with data from two different rows of memory cells, corresponding to two different word lines." ['899 Application, Page 7:16-32; *see also* Fig. 6] *See also*, '421 Reference, Col. 5:48-53. The '631 Reference states that: "The above-described method is accomplished by utilizing two pieces of information, which are placed on the bus (23) by the GDP: the data word's offset and the number of words requested. The data word's offset in the cache line is derived from adress bits 2 and 3 (00=word 1, 01=word 2, 10=word 3, and 11=word 4). The number of words being requested is obtained from the size bits 0 and 1 (00=1word, 01=2 words,

10=3 words, and 11=4words).

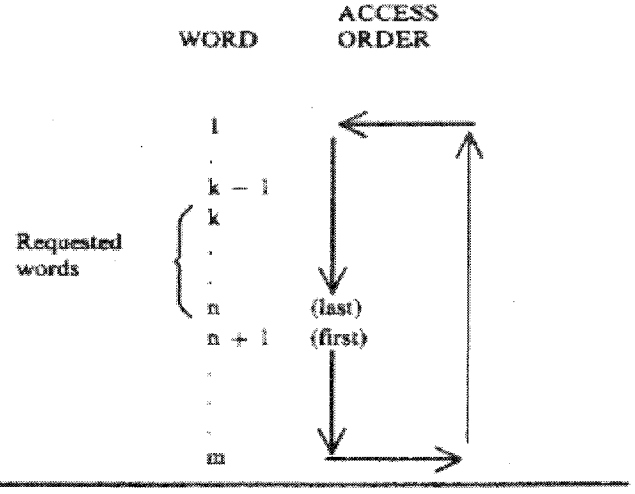
Using these two pieces of information, the following algorithm is executed:

FIRST WORD ACCESSED = PROCESSOR WORD ADDRESS + SIZE +1

The 1 is added to the size in order to yield the correct offset. For example, if the GDP requests two words at offset 01 in a four-word line, it is convereted to a wraparound request of four words to memory starting at word four [offset (01) + word count (01) + 1 = 11]." ['631 Reference, Col. 3:46-65]

See, '631 Reference, Table II:

TABLE II



	See also, '631 Reference, Abstract, Table I, Fig. 3. The '885 Reference states: "After the last memory address is reached, the access automatically rolls over to the first address." ['885 Reference, Col. 3:1-3] "A method as in claim 5 wherein the sequence of incremented addresses wraps around when the address of the Nth register is reached such that all N registers in the array are read." ['885 Reference, Col. 7:45-48] Further, the '594 Reference could be combined with any of the '596 Reference or the '297 Reference or the '495 Reference or the '738 Reference or the '994 Reference or the '1182 Reference to meet this limitation.
wherein said memory further comprises a control circuit for selectively enabling said sense amplifier circuits so that said control circuit enables a sense amplifier circuit whose output signals are being transferred to the output of said memory but said control circuit does not enable all said sense amplifier circuits at the same time.	This limitation is met by the '594 Reference alone or in combination with any of the '788 Reference or the '754 Reference or the '937 Reference or the '003 Reference or the '178 Reference. Specifically, the '594 Reference states: "A scheme removing even this limitation is provided in a copending application entitled 'Scheme for Eliminating Page Boundard,' by Elvan S. Young et al, Ser. No. 07,557,899, now abandoned filed on the same day as the present invention, assigned to the same assignee as the present invention, and which is hereby incorporated by reference in its entirety." ['594

	Reference, Col. 5:27-34] The '899 application states: "Like memory system 40 shown in Figure 4, the output registers are divided into two banks A and B, receiving data from groups of bit lines, with each bit in each group addressable by the address bits A0-A2. [see inserts E2, E3 and R4] ['899 Application, Page 7:6-10; *see also* Figs. 4 and 5] The '421 Reference states: "Control signal busses 417 and 418 specify which of the four bytes in each of register banks A and B is to be output, and accordingly asserts an output enable signal to each register bank to enable its output buffer." ['421 Reference, Col. 4:43-47] The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754

	Reference, Page 5:56-58] The '788 Reference states: "According to this arrangement, only one plane is selected in accordance with the content of the upper-order two bits of the row address. The selected plane is activated and exhibits the memory operation but the rest of the planes which are under the non-selection state are inoperative. Therefore, the decoders and the sense amplifiers are inoperative in these inoperative planes and the memory is not refreshed. Therefore, power is consumed in only the selected plane and unnecessary power consumption in the other plane can be saved. Thus, the requirement for low power consumption can be satisfied." ['788 Reference, Col. 5:57-68] The '937 Reference states: "The sense amplifier 86 is controlled by the signals SE_{EV} to amplify the read data thereby to supply the same to the data latch 87, which in turn temporarily stores the outputs from the sense amplifiers 86. When the signals SE_{EV} are at low levels, the data latch 87 is electrically cut off from the sense amplifier 86. Data from the data latch 87 are transferred to the output latch 89 when the signals OE_{EV} are at high levels. In a similar manner, the sense amplifier 96 is controlled by the signals SE_{OD} to amplify the read data thereby to supply the same to the data latch 97, which in turn temporarily stores the outputs from the sense amplifier 96. When the signals SE_{OD} are at low levels, the data latch 97 is electrically cut off from the sense amplifier 96." ['937 Reference, Col. 4:52-66]

	The '003 Reference states: "The flash memory control 88 also selectively enables one of two sets of bi-directional data buffers 90 and 91 which respectively couple the bank data buses 82 and 83 to the processor section data bus 63. The bank data buses 82 and 83 can be coupled to the instruction bus 61 by the flash memory control 88 selectively enabling buffers 92 and 93, respectively." ['003 Reference, Col. 9:21-27] The '178 Reference states: "Referring now to FIG. 2, the circuit of FIG. 1 has been modified to utilize the fact that, when RA10=1, only one half of the ARRAY BANKs 20 are being utilized and that, when RA10=0, the other half of the ARRAY BANKs 20 are being utilized. In particular, the RA 10 address is used to cause only the half of the ARRAY BANKs 20 that are being utilized to draw power from the DRAM energy source during read/write operations, while at the same time permitting the periodic performance of the refresh cycle in the usual manner on all ARRAY BANKs." ['178 Reference, Col. 3:32-42] Further, the '594 Reference could be combined with any of the '596 Reference or the '297 Reference or the '495 Reference or the '738 Reference or the '994 Reference or the '1182 Reference to meet this limitation.
9. The memory of claim 8 wherein, during said operation, said control circuit enables at the same time only:	
(1) the sense amplifier circuit whose output signals are being	This limitation is met by the '594 Reference alone or in

transferred to said output of said memory, and	combination with any of the '754 Reference. Specifically, the '594 Reference states: "A scheme removing even this limitation is provided in a copending application entitled 'Scheme for Eliminating Page Boundard,' by Elvan S. Young et al, Ser. No. 07,557,899, now abandoned filed on the same day as the present invention, assigned to the same assignee as the present invention, and which is hereby incorporated by reference in its entirety." ['594 Reference, Col. 5:27-34] The '899 application states: "Like memory system 40 shown in Figure 4, the output registers are divided into two banks A and B, receiving data from groups of bit lines, with each bit in each group addressable by the address bits A0-A2. [see inserts E2, E3 and R4] ['899 Application, Page 7:6-10; *see also* Figs. 4 and 5] The '421 Reference states: "Control signal busses 417 and 418 specify which of the four bytes in each of register banks A and B is to be output, and accordingly asserts an output enable signal to each register bank to enable its output buffer." ['421 Reference, Col. 4:43-47] The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow

	through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58] "A semiconductor dynamic memory device comprising: ... a plurality of sense amplifying means (18-1 to 18-4; SA1 to SA8) responsive to a control signal input thereto, for selectively activating one sense amplifying means to sense and amplify data on said selected data lines of one of said two column-selected memory blocks, and for selectively activating at least one other sense amplifying means to refresh data to said each memory cell along said selected word lines; ...." ['754 Reference, Page 6:53-7:5]
(2) a predetermined number of other sense amplifier circuits whose output signals will be transferred next to said output of said memory if said operation continues sufficiently long.	This limitation is met by the '594 Reference alone or in combination with any of the '754 Reference. Specifically, the '594 Reference states: "A scheme removing even this limitation is provided in a copending application entitled 'Scheme for Eliminating Page Boundard,' by Elvan S. Young et al, Ser. No. 07,557,899, now abandoned filed on the same day as the present invention, assigned to the same assignee as the present invention, and which is hereby incorporated by reference in its entirety." ['594

	Reference, Col. 5:27-34] The '899 application states: "Like memory system 40 shown in Figure 4, the output registers are divided into two banks A and B, receiving data from groups of bit lines, with each bit in each group addressable by the address bits A0-A2. [see inserts E2, E3 and R4] ['899 Application, Page 7:6-10; *see also* Figs. 4 and 5] The '421 Reference states: "Control signal busses 417 and 418 specify which of the four bytes in each of register banks A and B is to be output, and accordingly asserts an output enable signal to each register bank to enable its output buffer." ['421 Reference, Col. 4:43-47] The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754

	Reference, Page 5:56-58] "A semiconductor dynamic memory device comprising: … a plurality of sense amplifying means (18-1 to 18-4; SA1 to SA8) responsive to a control signal input thereto, for selectively activating one sense amplifying means to sense and amplify data on said selected data lines of one of said two column-selected memory blocks, and for selectively activating at least one other sense amplifying means to refresh data to said each memory cell along said selected word lines; …." ['754 Reference, Page 6:53-7:5]
10. The memory of claim 7 wherein:	
said set of locations comprises k subsets S-1, . . . , S-k wherein k is greater than or equal to two, such that, for a positive integer m and for any subset S-i, the contents of m consecutively addressed locations from said subset S-i can be transferred simultaneously to said plurality of sense amplifier circuits; and	This limitation is met by the '594 Reference. Specifically, the '594 Reference states: "A scheme removing even this limitation is provided in a copending application entitled 'Scheme for Eliminating Page Boundard,' by Elvan S. Young et al, Ser. No. 07,557,899, now abandoned filed on the same day as the present invention, assigned to the same assignee as the present invention, and which is hereby incorporated by reference in its entirety." ['594 Reference, Col. 5:27-34] The '899 application states: "A word line in the left half memory array may be activated independently but simultaneously with a word line in the right half of the memory array." ['899 Reference, Page 4:9-11] "However, unlike the memory system 40 provided in Figure 4, the memory system 50 is organized into left and right halves,

	such that the word lines in each half of the memory system 50 are controlled independently of the word lines in the other half." ['899 Reference, Page 7:10-15]
in said operation, time tARA does not exceed m * (k-1) * (tOE), wherein: tARA is measured from the time that an address of the first location to be read out in said operation is made available to said memory to the time when said plurality of sense amplifier circuits develops an output signal indicative of the contents of said first location; and tOE is the time to transfer the contents of any one of said locations from said plurality of sense amplifier circuits to said output.	This limitation is met by the '594 Reference. Specifically, the '594 Reference states: "A scheme removing even this limitation is provided in a copending application entitled 'Scheme for Eliminating Page Boundard,' by Elvan S. Young et al, Ser. No. 07,557,899, now abandoned filed on the same day as the present invention, assigned to the same assignee as the present invention, and which is hereby incorporated by reference in its entirety." ['594 Reference, Col. 5:27-34] The '899 application shows this timing relationship in Figure 2. *See* timing description from Page 2:19-Page 3:8. "The operation of memory system 40 described in the aforementioned copending application shown in Figure 4 is feasible if each register bank satisfies the relation n x tRCO > tASA, where n is the nmber of registers in the register bank." ['899 Reference, Page 5:8-12] "After the initial access, register banks A and B may be read and loaded in the same interleaving manner as described in the aforementioned copending application." [Insert E5] ['899 Reference, Page 8:20-22] *See also*, '421 Reference, Col. 5:26-53.
11. The memory of claim 8 wherein, in said operation, each location to be read out except the first location to be read out is	This limitation is met by the '594 Reference. Specifically, the

read out to said output in a shorter time than the first location to be read out.	'594 Reference states: "A scheme removing even this limitation is provided in a copending application entitled 'Scheme for Eliminating Page Boundard,' by Elvan S. Young et al, Ser. No. 07,557,899, now abandoned filed on the same day as the present invention, assigned to the same assignee as the present invention, and which is hereby incorporated by reference in its entirety." ['594 Reference, Col. 5:27-34] The '899 application shows this timing relationship in Figure 2. *See* timing description from Page 2:19-Page 3:8. "The operation of memory system 40 described in the aforementioned copending application shown in Figure 4 is feasible if each register bank satisfies the relation n x tRCO > tASA, where n is the nmber of registers in the register bank." ['899 Reference, Page 5:8-12] "After the initial access, register banks A and B may be read and loaded in the same interleaving manner as described in the aforementioned copending application." [Insert E5] ['899 Reference, Page 8:20-22] *See also*, '421 Reference, Col. 5:26-53.
12. The memory of claim 8 wherein the sequence of locations L1, . . . , Ln is a sequence of increasing order of addresses.	This limitation is met by the '594 Reference. Specifically, the '594 Reference states: "The memory system 40 multiplexes groups of thirty two bit lines to either register bank corresponding to four bytes of data having four contiguous addresses." ['594 Reference, Col. 3:36-

	39] The '899 application states: "The present invention removes the restriction on the address of the first datum received in burst mode, thereby providing continuous sequential access every tRCO after the initial access, from any byte and regardless of whether row boundaries are crossed." ['899 Reference, Page 6:38-Page 7:4] *See also*, '421 Reference, Col. 5:26-53.
13. The memory of claim 7 wherein in said operation any number of said locations addressed consecutively with wrap around can be read out to said output so that:	As found for the examiner, the '594 Reference discloses this element. Specifically the '594 References states that: "In accordance with the present invention, two output register banks are provided in a memory system. When enabled, the first register bank latches simultaneously from a first set of bit lines data corresponding to a first set of contiguous addresses. Likewise, when enabled, the second register bank independently latches from a second set of bit lines data corresponding to s second set of contiguous addresses following the first set of contiguous addresses. When the content of first register bank is sequentially output according to addresses of the data therein, the second register bank is being loaded with the data in the second set of bit lines corresponding to the next set of contiguous addresses. The first and second sets of contiguous addresses may involve the same or different word lines." ['594 Reference, Col. 2:49-63; *see also* Figs. 1-5] "As a result, a continuous stream of data from contiguous addresses are made available every tRCO indefinitely for as long as burst mode is asserted. The limit on the number of data

	accessivle from each initial access under burst mode is therefore removed." ['594 Reference, Col. 5:6-10] The '899 application states: "The present invention removes the restriction on the address of the first datum received in burst mode, thereby providing continuous sequential access every tRCO after the initial access, from any byte and regardless of whether row boundaries are crossed." ['899 Reference, Page 6:38-Page 7:4] "The organization of the memory array 503 is shown in Figure 6. As shown in Figure 6, the memory array 503 is divided into left and right halves. Word lines WLK+1 and WLK, corresponding to consecutive row addrsses are activated simultaneously when signal N+1 is asserted. When signal N+1 is not asserted, activated word lines in both halves have the same row address. During the initial access of memory system 50, rather than loading four bytes into register A, as in memory system 40 shown in Figure 4, eight bytes of data are loaded into registers A and B simultaneously from the initial access of memory system 50. As a result of the ability to activate word lines in the left and right halves independently, register banks A and B may be loaded simultaneously upon initial access with data from two different rows of memory cells, corresponding to two different word lines." ['899 Application, Page 7:16-32; *see also* Fig. 6] *See also*, '421 Reference, Col. 5:48-53.
the first location to be read out in said operation is read out to said output after time tARA+tOE wherein:	This limitation is met by the '594 Reference. Specifically, the '594 Reference states:

tARA is measured from the time that an address of said first location is made available to said memory to the time when said plurality of sense amplifier circuits develops an output signal indicative of the contents of said first location; and tOE is the time to transfer the contents of any one of said locations from said plurality of sense amplifier circuits to said output of said memory; and	This limitation is met by the '594 Reference. Specifically, the '594 Reference shows this timing relationship in Figure 2. *See* timing description from Col. 1:54-2:13] *See also* '899 Reference, Page 2:19-Page 3:8. "The operation of memory system 40 described in the aforementioned copending application shown in Figure 4 is feasible if each register bank satisfies the relation n x tRCO > tASA, where n is the nmber of registers in the register bank." ['899 Reference, Page 5:8-12] "After the initial access, register banks A and B may be read and loaded in the same interleaving manner as described in the aforementioned copending application." [Insert E5] ['899 Reference, Page 8:20-22] *See also*, '421 Reference, Col. 5:26-53.
every other location to be read out in said operation is read out to said output within time tOE.	This limitation is met by the '594 Reference. Specifically, the '594 Reference shows this timing relationship in Figure 2. *See* timing description from Col. 1:54-2:13] *See also* '899 Reference, Page 2:19-Page 3:8. "The operation of memory system 40 described in the aforementioned copending application shown in Figure 4 is feasible if each register bank satisfies the relation n x tRCO > tASA, where n is the number of registers in the register bank." ['899 Reference, Page 5:8-12] "After the initial access, register banks A and B may be read and loaded in the same interleaving manner as described in the aforementioned copending application." [Insert E5] ['899

	Reference, Page 8:20-22] *See also*, '421 Reference, Col. 5:26-53.
14. The memory of claim 8 wherein said memory is fabricated in an integrated circuit.	This element is met by the '594 Reference alone or in combination with any of the '754 Reference or the '199 Reference, or the '312 Reference. It was well known in the art to fabricate memories as an integrated circuit and a person of ordinary skill would have know that the memory device shown in the '196 Reference could be fabricated in an integrated circuit. The '754 Reference states: "The present invention relates to a semiconductor dynamic memory device. Mass-production of 64K bit dynamic type random access memory devices (DRAMs) has been enabled by the recent development of semiconductor memory devices of high packing density. Furthermore, a 256K bit DRAM has been developed." ['754 Reference, Page 2:1-4] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer." ['199 Reference, Col. 1:13-16] The '312 Reference states: "The individual circuit elements constructing the RAM of the present embodiment are formed on a semiconductor substrate

	such as a piece of single-crystalline silicon by the known technique for fabricating a CMOS (i.e., Complementary MOS) integreated circuit." ['312 Reference, Col. 2:34-38]
20. An integrated memory comprising:	Although a preamble is normally not limiting, should this preamble be limiting, this element is met by the '594 Reference. Specifically, the '594 Reference is titled "Architecture for High Speed Contiguous Sequential Access Memories."
an array of memory locations, the array comprising a plurality of subarrays, each subarray comprising a predetermined number of groups of columns of the memory locations such that for any given column position in a group, the memory locations in any given row in the columns at said given position in the groups of the subarray have consecutive addresses;	This limitation is met by the '594 Reference. Specifically, the '594 References states that: "In accordance with the present invention, two output register banks are provided in a memory system. When enabled, the first register bank latches simultaneously from a first set of bit lines data corresponding to a first set of contiguous addresses. Likewise, when enabled, the second register bank independently latches from a second set of bit lines data corresponding to s second set of contiguous addresses following the first set of contiguous addresses. When the content of first register bank is sequentially output according to addresses of the data therein, the second register bank is being loaded with the data in the second set of bit lines corresponding to the next set of contiguous addresses. The first and second sets of contiguous addresses may involve the same or different word lines." ['594 Reference, Col. 2:49-63; *see also* Figs. 1-5]
one X-decoder for each subarray;	This limitation is met by the '594 Reference alone or in combination with U.S. Patent No. 4,849,937 ("the '937 Reference"). Specifically, the '594 Reference states: "A scheme removing even this limitation is provided in a

	copending application entitled 'Scheme for Eliminating Page Boundard,' by Elvan S. Young et al, Ser. No. 07,557,899, now abandoned filed on the same day as the present invention, assigned to the same assignee as the present invention, and which is hereby incorporated by reference in its entirety." ['594 Reference, Col. 5:27-34] The '899 application states: "The organization of the memory array 503 is shown in Figure 6. As shown in Figure 6, the memory array 503 is divided into left and right halves. Word lines WLK+1 and WLK, corresponding to consecutive row addrsses are activated simultaneously when signal N+1 is asserted." ['899 Application, Page 7:16-20; *see also* Fig. 6] Further, the '937 Reference teaches the use of a plurality of decoders as well as the use of a single decoder for performing the same function. [Figs. 3 and 5] The '937 Reference states: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer

	gate 95." ['937 Reference, Col. 4:29-42] "The latch (see FIG. 6) forming the delay latch circuit 106 fetches the outputs from the X decoder 82 on the leading edges of the clock pulses $Ø_L$, and hence the delay latch circuit 106 delays the outputs from the X decoder 82 respectively by one cycle of the basic clock pulses $Ø_S$ to transfer the same to the second memory cell array 94. . . . It is to be noted that odd address cycles are always delayed from the even address cycles respectively by one cycle of the basic clock pulses $Ø_S$. Thus, this embodiment is equivalent in operation to that shown in FIG. 3" ['937 Reference, Col. 7:44-63] Further, the '594 Reference could be combined with any of the '596 Reference or the '297 Reference or the '495 Reference or the '738 Reference or the '994 Reference or the '1182 Reference or U.S. Patent No. 4,954,951 ("the '951 Reference") to meet this limitation.
one X-register for each X-decoder;	This limitation is met by the '594 Reference alone or in combination. Specifically, the '594 Reference states: "In this embodiment, the row address A3-A16 is latched into address counter 400." ['594 Reference, Col. 3:60-62] "A scheme removing even this limitation is provided in a copending application entitled 'Scheme for Eliminating Page Boundard,' by Elvan S. Young et al, Ser. No. 07,557,899,[2] now

[2] The '899 application is the parent application for U.S. Patent No. 5,285,421 ("the '421 Reference") and the cites to the '899 reference should also be treated as cites to the same Figures and passages found in the '421 Reference.

	abandoned filed on the same day as the present invention, assigned to the same assignee as the present invention, and which is hereby incorporated by reference in its entirety." ['594 Reference, Col. 5:27-34] The '899 application states: "The organization of the memory array 503 is shown in Figure 6. As shown in Figure 6, the memory array 503 is divided into left and right halves. Word lines WLK+1 and WLK, corresponding to consecutive row addrsses are activated simultaneously when signal N+1 is asserted." ['899 Application, Page 7:16-20; *see also* Fig. 6] To the extent AMD reads this limitation on the Samsung devices, the '594 Reference discloses this limitation. Further, the '594 Reference could be combined with any of the '596 Reference or the '297 Reference or the '495 Reference or the '738 Reference or the '994 Reference or the '1182 Reference or the '951 Reference to meet this limitation.
one Y-decoder for each subarray;	This limitation is met by the '594 Reference alone or in combination with U.S. Patent No. 4,849,937 ("the '937 Reference"). Specifically, the '594 Reference states: "FIG. 1 shows a generalized organization of a memory system, comprising address input register 100, x-and y-decoders 101 and 102 (also known as row and columns decoders), a memory array 103, a sense amplifier circuit 104, a memory output register 105, and output buffers 106." ['594 Reference, Col. 1:13-18] "A scheme removing even this limitation is provided in a

	copending application entitled 'Scheme for Eliminating Page Boundard,' by Elvan S. Young et al, Ser. No. 07,557,899, now abandoned filed on the same day as the present invention, assigned to the same assignee as the present invention, and which is hereby incorporated by reference in its entirety." ['594 Reference, Col. 5:27-34] The '899 application states: "The organization of the memory array 503 is shown in Figure 6. As shown in Figure 6, the memory array 503 is divided into left and right halves. Word lines WLK+1 and WLK, corresponding to consecutive row addrsses are activated simultaneously when signal N+1 is asserted." ['899 Application, Page 7:16-20; *see also* Fig. 6] A person of ordinary skill in the art would know to use one y-decoder for each subarray shown in Figure 6. Further, the '937 Reference teaches the use of a plurality of decoders as well as the use of a single decoder for performing the same function. [Figs. 3 and 5] The '937 Reference states: "The address counter 81 receives the signals $\emptyset_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $\emptyset_{EV}$ (i.e., twice that of the basic clock pulses $\emptyset_S$). Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $\emptyset_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $\emptyset_{OD}$ (i.e., twice that of the basic clock pulses $\emptyset_S$). Outputs from the X

	decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42] "The latch (see FIG. 6) forming the delay latch circuit 106 fetches the outputs from the X decoder 82 on the leading edges of the clock pulses $Ø_L$, and hence the delay latch circuit 106 delays the outputs from the X decoder 82 respectively by one cycle of the basic clock pulses $Ø_S$ to transfer the same to the second memory cell array 94. . . . It is to be noted that odd address cycles are always delayed from the even address cycles respectively by one cycle of the basic clock pulses $Ø_S$. Thus, this embodiment is equivalent in operation to that shown in FIG. 3" ['937 Reference, Col. 7:44-63] Further, the '594 Reference could be combined with any of the '596 Reference or the '297 Reference or the '495 Reference or the '738 Reference or the '994 Reference or the '1182 Reference or the '951 Reference to meet this limitation.
one Y-register for each Y-decoder;	This limitation is met by the '594 Reference. Specifically, the '594 Reference states: "In this embodiment, the row address A3-A16 is latched into address counter 400." ['594 Reference, Col. 3:60-62] To the extent AMD reads this limitation on the Samsung devices, the '594 Reference discloses this limitation. Further, the '594 Reference could be combined with any of the '596 Reference or the '297 Reference or the '495 Reference or the '738 Reference or the '994 Reference or the '1182 Reference

	or the '951 Reference to meet this limitation.
one Y-select circuit for each subarray, the Y-select circuit being responsive to the Y-decoder of the subarray to select all the columns that occupy a selected position in the groups of the subarray;	This limitation is met by the '594 Reference. Specifically, the '594 Reference provides: "In accordance with the present invention, two output register banks are provided in a memory system. When enabled, the first register bank latches simultaneously from a first set of bit lines data corresponding to a first set of contiguous addresses. Likewise, when enabled, the second register bank independently latches from a second set of bit lines data corresponding to a second set of contiguous addresses following the first set of contiguous addrses." ['594 Reference, Col. 2:49-57] Further, the '594 Reference could be combined with any of the '596 Reference or the '297 Reference or the '495 Reference or the '738 Reference or the '994 Reference or the '1182 Reference or the '951 Reference to meet this limitation.
a plurality of sense amplifier circuits for each subarray, each sense amplifier circuit for amplifying signals from a column selected by the Y-select circuit of the subarray;	This limitation is met by the '594 Reference. Specifically the '594 References states that: "FIG. 4 shows a memory organization 40 in accordance with the present invention. For the purpose of comparison, it is assumed that the memory systems 30 and 40, shown respectively in FIGS. 3 and 4, have identical number of memory cells. However, instead of having the eight registers R0 through R7 load the output of sixty four bit lines simultaneously, as in memory system 30, the registers of memory system 40 are divided into two banks A and B, corresponding to registers R0-R3 and registers R4-R7 respectively." ['594 Reference, Col. 3:27-36; *see also* Figs. 1, 3, and 4]

	"A scheme removing even this limitation is provided in a copending application entitled 'Scheme for Eliminating Page Boundard,' by Elvan S. Young et al, Ser. No. 07,557,899, now abandoned filed on the same day as the present invention, assigned to the same assignee as the present invention, and which is hereby incorporated by reference in its entirety." ['594 Reference, Col. 5:27-34] The '899 application states: "During the initial access of memory system 50, rather than loading four bytes into register A, as in memory system 40 shown in Figure 4, eight bytes of data are loaded into registers A and B simultaneously from the initial access of memory system 50. As a result of the ability to activate word lines in the left and right halves independently, register banks A and B may be loaded simultaneously upon initial access with data from two different rows of memory cells, corresponding to two different word lines." ['594 Reference, Page 7:22-32; *see also* Figs. 1, 3, 4, 5 and 6] Further, the '594 Reference could be combined with any of the '596 Reference or the '297 Reference or the '495 Reference or the '738 Reference or the '994 Reference or the '1182 Reference or the '951 Reference to meet this limitation.
a memory output; and	This limitation is met by the '594 Reference. Specifically the '594 References states that: "After the specified tOE period following the output enable signal [OE bar] is asserted (the output enable signal [OE bar] is asserted after the BURST signal), the intial access is completed

	by register bank A providing on output bus 40a the datum corresponding to the initial address. This data is provided by register R0, since the initial address is to be specified on a 4-byte boundary. Every tRCO thereafter, the next datum is sequentially provided in increasing address order." ['594 Reference, Col. 4:19-27] Further, the '594 Reference could be combined with any of the '596 Reference or the '297 Reference or the '495 Reference or the '738 Reference or the '994 Reference or the '1182 Reference or the '951 Reference to meet this limitation.
a control circuit for selecting one of the sense amplifier circuits to provide data to the memory output;	This limitation is met by the '594 Reference alone or in combination with the '754 Reference. Specifically, the '594 Reference states: "Each register bank is designed such that the total output time of each bank, i.e. the total time between the first byte of the output from the register bank is enabled to the time when the last byte output is available on the respective output bus 40a or 40b, exceeds the memory access tiem tASA." ['594 Reference, Col. 3:43-49] It was well known in the art that information in the sense amplifiers could be read out one bit at a time. For example, the '754 Reference discloses this limitation. Specifically, the '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active

	state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "A semiconductor dynamic memory device comprising: ... a plurality of sense amplifying means (18-1 to 18-4; SA1 to SA8) responsive to a control signal input thereto, for selectively activating one sense amplifying means to sense and amplify data on said selected data lines of one of said two column-selected memory blocks, and for selectively activating at least one other sense amplifying means to refresh data to said each memory cell along said selected word lines; ...." ['754 Reference, Page 6:53-7:5] To the extent AMD contends that the accused Samsung devices practice this limitation, this limitation is met by the '594 Reference.
wherein in a burst mode read operation, at least one X-register provides to its respective X-decoder signals identifying a row in one of the subarrays, and at least one Y-register provides to its respective Y-decoder signals identifying a position of columns in the groups of one of the subarrays.	This limitation is met by the '594 Reference. Specifically, the '594 Reference states: "In accordance with the present invention, two output register banks are provided in a memory system. When enabled, the first register bank latches simultaneously from a first set of bit lines data corresponding to a first set of contiguous addresses. Likewise, when enabled, the second register bank independently latches from a second set of bit lines data corresponding to s second set of contiguous addresses following the first set of contiguous addresses. When the content of first register bank is

	sequentially output according to addresses of the data therein, the second register bank is being loaded with the data in the second set of bit lines corresponding to the next set of contiguous addresses. The first and second sets of contiguous addresses may involve the sme or different word lines." ['594 Reference, Col. 2:49-63; *see also* Figs. 1-5] The '899 application states: "The organization of the memory array 503 is shown in Figure 6. As shown in Figure 6, the memory array 503 is divided into left and right halves. Word lines WLK+1 and WLK, corresponding to consecutive row addrsses are activated simultaneously when signal N+1 is asserted. When signal N+1 is not asserted, activated word lines in both halves have the same row address. During the initial access of memory system 50, rather than loading four bytes into register A, as in memory system 40 shown in Figure 4, eight bytes of data are loaded into registers A and B simultaneously from the initial access of memory system 50. As a result of the ability to activate word lines in the left and right halves independently, register banks A and B may be loaded simultaneously upon initial access with data from two different rows of memory cells, corresponding to two different word lines." ['899 Application, Page 7:16-32; *see also* Fig. 6] Further, the '594 Reference could be combined with any of the '596 Reference or the '297 Reference or the '495 Reference or the '738 Reference or the '994 Reference or the '1182 Reference or the '951 Reference to meet this limitation.
22. The memory of claim 20 wherein in the burst mode read	This limitation is met by the '594 Reference. Specifically, the

operation while data from the sense amplifier circuits of one of the subarrays are provided to the memory output, the sense amplifier circuits of another one of the subarrays develop output signals corresponding to data in said other one of the subarrays.	'594 Reference states: "In accordance with the present invention, two output register banks are provided in a memory system. When enabled, the first register bank latches simultaneously from a first set of bit lines data corresponding to a first set of contiguous addresses. Likewise, when enabled, the second register bank independently latches from a second set of bit lines data corresponding to s second set of contiguous addresses following the first set of contiguous addresses. When the content of first register bank is sequentially output according to addresses of the data therein, the second register bank is being loaded with the data in the second set of bit lines corresponding to the next set of contiguous addresses. The first and second sets of contiguous addresses may involve the sme or different word lines." ['594 Reference, Col. 2:49-63; *see also* Figs. 1-5] The '899 application states: "The organization of the memory array 503 is shown in Figure 6. As shown in Figure 6, the memory array 503 is divided into left and right halves. Word lines WLK+1 and WLK, corresponding to consecutive row addrsses are activated simultaneously when signal N+1 is asserted. When signal N+1 is not asserted, activated word lines in both halves have the same row address. During the initial access of memory system 50, rather than loading four bytes into register A, as in memory system 40 shown in Figure 4, eight bytes of data are loaded into registers A and B simultaneously from the initial access of memory system 50. As a result of the ability to activate word lines in the left and right halves independently, register banks A and B may be loaded simultaneously upon initial access with

	data from two different rows of memory cells, corresponding to two different word lines." ['899 Application, Page 7:16-32; *see also* Fig. 6] Further, the '594 Reference could be combined with any of the '596 Reference or the '297 Reference or the '495 Reference or the '738 Reference or the '994 Reference or the '1182 Reference to meet this limitation.
23. The memory of claim 20 wherein in the burst mode read operation, the control circuit enables the sense amplifier circuit selected to provide data to the memory output and at the same time disables one or more sense amplifier circuits not selected to provide data to the memory output.	This limitation is met by the '594 Reference alone or in combination with any of the '788 Reference or the '754 Reference or the '937 Reference or the '003 Reference or the '178 Reference. Specifically, the '594 Reference states: "A scheme removing even this limitation is provided in a copending application entitled 'Scheme for Eliminating Page Boundard,' by Elvan S. Young et al, Ser. No. 07,557,899, now abandoned filed on the same day as the present invention, assigned to the same assignee as the present invention, and which is hereby incorporated by reference in its entirety." ['594 Reference, Col. 5:27-34] The '899 application states: "Like memory system 40 shown in Figure 4, the output registers are divided into two banks A and B, receiving data from groups of bit lines, with each bit in each group addressable by the address bits A0-A2. [see inserts E2, E3 and R4] ['899 Application, Page 7:6-10; *see also* Figs. 4 and 5] The '421 Reference states: "Control signal busses 417 and 418 specify which of the four

	bytes in each of register banks A and B is to be output, and accordingly asserts an output enable signal to each register bank to enable its output buffer." ['421 Reference, Col. 4:43-47] The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58] The '788 Reference states: "According to this arrangement, only one plane is selected in accordance with the content of the upper-order two bits of the row address. The selected plane is activated and exhibits the memory operation but the rest of the planes which are under the non-selection state are inoperative. Therefore, the decoders and the sense amplifiers are inoperative in these inoperative planes and the memory is not refreshed. Therefore, power is consumed in only the selected plane and unnecessary power consumption in the other plane can be saved. Thus, the requirement for low

	power consumption can be satisfied." ['788 Reference, Col. 5:57-68] The '937 Reference states: "The sense amplifier 86 is controlled by the signals SE_{EV} to amplify the read data thereby to supply the same to the data latch 87, which in turn temporarily stores the outputs from the sense amplifiers 86. When the signals SE_{EV} are at low levels, the data latch 87 is electrically cut off from the sense amplifier 86. Data from the data latch 87 are transferred to the output latch 89 when the signals OE_{EV} are at high levels. In a similar manner, the sense amplifier 96 is controlled by the signals SE_{OD} to amplify the read data thereby to supply the same to the data latch 97, which in turn temporarily stores the outputs from the sense amplifier 96. When the signals SE_{OD} are at low levels, the data latch 97 is electrically cut off from the sense amplifier 96." ['937 Reference, Col. 4:52-66] The '003 Reference states: "The flash memory control 88 also selectively enables one of two sets of bi-directional data buffers 90 and 91 which respectively couple the bank data buses 82 and 83 to the processor section data bus 63. The bank data buses 82 and 83 can be coupled to the instruction bus 61 by the flash memory control 88 selectively enabling buffers 92 and 93, respectively." ['003 Reference, Col. 9:21-27] The '178 Reference states: "Referring now to FIG. 2, the circuit of FIG. 1 has been

	modified to utilize the fact that, when RA10=1, only one half of the ARRAY BANKs 20 are being utilized and that, when RA10=0, the other half of the ARRAY BANKs 20 are being utilized. In particular, the RA 10 address is used to cause only the half of the ARRAY BANKs 20 that are being utilized to draw power from the DRAM energy source during read/write operations, while at the same time permitting the periodic performance of the refresh cycle in the usual manner on all ARRAY BANKs." ['178 Reference, Col. 3:32-42]