EXHIBIT 1

D10 Pages 1-20

Appendix D10
Defendants and Counterclaimants' Invalidity Contentions
Advanced Micro Devices, Inc., et al., v. Samsung Electronics Co., Ltd., et al., Case No. 3:08-CV-0986-SI

U.S. patent No. 5,559,990 Invalidity Chart: U.S. Patent No. 5,263,003 ("the '003 Reference")

All asserted claims are anticipated by the '003 Reference and/or are rendered obvious by it, either alone or in combination with other prior art described below and/or listed in Section I of Defendants' and Counterclaimants' Preliminary Invalidity Contentions and/or through modifications described below. Nothing in this invalidity chart should be construed as signifying or suggesting Defendants and Counterclaimants' adoption of or acquiescence in any claim scope and/or claim construction positions taken by Plaintiffs and Counterdefendants in this litigation.

CLAIM	RESPONSE
1. A memory comprising:	Although a preamble is normally not limiting, should this preamble be limiting, this element is met by U.S. Patent No. 5,263,003 ("the '003 Reference"). Specifically, the '003 Reference is titled "Flash Memory Circuit and Method of Operation."
a plurality of rows of memory locations;	This element is met in the '003 Reference. Specifically, the '003 Reference states that: "The programmable read only memory in the processor section 31 is a flash-type memory 55 such as described in *Flash Memory Products Data Book*, published in 1989 by Advanced Micro Devices." ['003 Reference, Col. 7:41-44] "With reference to FIG. 3, the flash memory 55 has two banks 71 and 72, denoted by dashed lines, with each bank having four flash memory devices 73-76 and 77-80, respectively. For example, the flash memory devices are model 28F010 devices manufactured by Advanced Micro Devices. Each memory device is eight bits wide and four of them are connected in parallel to a common bank address bus 81 and internal bank internal data buses 82 and 83. Different bit lines of the data buses 82 and 83 connect to each memory device 73-76 and 77-80. Thus the combination of the four memory devices in a given bank enable a thirty-two bit wide word of data to be contained in each individually addressable storage location in the bank." ['003 Reference, Col. 8:1-14]

CLAIM	RESPONSE
a plurality of first registers, each first register for receiving a row address;	This element is met by the '003 Reference. Specifically, the '003 Reference states: "The programmable read only memory in the processor section 31 is a flash-type memory 55 such as described in *Flash Memory Products Data Book*, published in 1989 by Advanced Micro Devices." ['003 Reference, Col. 7:41-44] "With reference to FIG. 3, the flash memory 55 has two banks 71 and 72, denoted by dashed lines, with each bank having four flash memory devices 73-76 and 77-80, respectively. For example, the flash memory devices are model 28F010 devices manufactured by Advanced Micro Devices. Each memory device is eight bits wide and four of them are connected in parallel to a common bank address bus 81 and internal bank internal data buses 82 and 83. Different bit lines of the data buses 82 and 83 connect to each memory device 73-76 and 77-80. Thus the combination of the four memory devices in a given bank enable a thirty-two bit wide word of data to be contained in each individually addressable storage location in the bank." ['003 Reference, Col. 8:1-14] A person of ordinary skill in the art would know that each memory device would have a plurality of registers for receiving a row address. "The result of that operation is passed on to the bank address generator 86 where it is used as the first address for accessing the flash memory banks 71 and 72." ['003 Reference, Col. 10:34-37] "While this is occurring, the bank address generator 86 increments the least significant address bits that are applied to the lower bus 81L" for the second flash memory bank 72. This action prepares the second bank 72 to supply the next instruction when a subsequent access request is received by the flash memory 55." ['003 Reference, Col. 11:27-32] Bank address generator 86 has a plurality of registers for receiving a row address.

CLAIM	RESPONSE
	See also Figs. 3, 4a and 4b; Col. 8:57-9:12 and Col. 10:16-42.
a plurality of row decoders, each row decoder for activating a portion of a row identified by signals from one of said first registers;	This elements is met by the '003 Reference. Specifically, the '003 Reference states: "The programmable read only memory in the processor section 31 is a flash-type memory 55 such as described in *Flash Memory Products Data Book*, published in 1989 by Advanced Micro Devices." ['003 Reference, Col. 7:41-44] "With reference to FIG. 3, the flash memory 55 has two banks 71 and 72, denoted by dashed lines, with each bank having four flash memory devices 73-76 and 77-80, respectively. For example, the flash memory devices are model 28F010 devices manufactured by Advanced Micro Devices. Each memory device is eight bits wide and four of them are connected in parallel to a common bank address bus 81 and internal bank internal data buses 82 and 83. Different bit lines of the data buses 82 and 83 connect to each memory device 73-76 and 77-80. Thus the combination of the four memory devices in a given bank enable a thirty-two bit wide word of data to be contained in each individually addressable storage location in the bank." ['003 Reference, Col. 8:1-14] A person of ordinary skill in the art would know that each memory device would have a row decoder. *See also* Figs. 3, 4a and 4b; Col. 8:57-9:12 and Col. 10:16-42.
one or more sense amplifiers for amplifying contents of said memory locations in the row portions; and	This element is met in the '003 Reference. Specifically, the '003 Reference states that: "The programmable read only memory in the processor section 31 is a flash-type memory 55 such as described in *Flash Memory Products Data Book*, published in 1989 by Advanced Micro Devices." ['003 Reference, Col. 7:41-44]

CLAIM	RESPONSE
	"With reference to FIG. 3, the flash memory 55 has two banks 71 and 72, denoted by dashed lines, with each bank having four flash memory devices 73-76 and 77-80, respectively. For example, the flash memory devices are model 28F010 devices manufactured by Advanced Micro Devices. Each memory device is eight bits wide and four of them are connected in parallel to a common bank address bus 81 and internal bank internal data buses 82 and 83. Different bit lines of the data buses 82 and 83 connect to each memory device 73-76 and 77-80. Thus the combination of the four memory devices in a given bank enable a thirty-two bit wide word of data to be contained in each individually addressable storage location in the bank." ['003 Reference, Col. 8:1-14] A person of ordinary skill in the art would know that each memory device would have a sense amplifiers. *See also* Figs. 3, 4a and 4b; Col. 8:57-9:12 and Col. 10:16-42.
an output for providing output signals from said sense amplifiers,	This element is met in the '003 Reference. Specifically, the '003 Reference states that: "The programmable read only memory in the processor section 31 is a flash-type memory 55 such as described in *Flash Memory Products Data Book*, published in 1989 by Advanced Micro Devices." ['003 Reference, Col. 7:41-44] "With reference to FIG. 3, the flash memory 55 has two banks 71 and 72, denoted by dashed lines, with each bank having four flash memory devices 73-76 and 77-80, respectively. For example, the flash memory devices are model 28F010 devices manufactured by Advanced Micro Devices. Each memory device is eight bits wide and four of them are connected in parallel to a common bank address bus 81 and internal bank internal data buses 82 and 83. Different bit lines of the data buses 82 and 83 connect to eah memory device 73-76 and 77-80. Thus the combination of the four memory devices in a given bank enable a thirty-two bit wide word of data to be contained in each individually addressable storage location in the bank." ['003

CLAIM	RESPONSE
	Reference, Col. 8:1-14] A person of ordinary skill in the art would know that each memory device would have output for providing output signals from the sense amplifiers. *See also* Figs. 3, 4a and 4b; Col. 8:57-9:12 and Col. 10:16-42.
wherein at least two locations L1 and L2 in different rows having different row addresses in said memory can be read out to said output in burst mode such that the memory receives an address of one of said locations and provides in response contents of a plurality of memory locations, including the locations L1 and L2, in the sequence of consecutive addresses, so that while one of said row decoders is activating a row portion comprising said location L1 and contents of said location L1 are being transferred from one or more of said sense amplifiers to said output, another one of said row decoders is activating a row portion comprising said location L2 and contents of said location L2 are being transferred from said location L2 to one or more of said sense amplifiers.	This element is met in the '003 Reference. Specifically, the '003 Reference states that: "Standard memories are commonly configured as interleaved banks of devices to obtain improved performance and faster access time. In this technique, two or more banks of identical memory devices are arranged in such a way that the requests for data from each one overlap, i.e. when one bank is delivering data, the other bank is preparing to deliver the next sequential item of data." ['003 Reference, Col. 1:22-29] "In the first mode, the control mechanism responds to an initial request for access and an address signal by reading data from a storage location in one of the memory banks. Subsequent requests for access to the next adjacent storage location do not require that an address be sent with the request. The control mechanism responds to such subsequent requests by generating addresses to read data alternately from storage locations in the first and second memory banks." ['003 Reference, Col. 2:48-52] "These particular devices are configured to operate in the burst addresing mode performed by the second microprocessor 54. In this addressing mode, the second microprocessor 54 sends an initial address of a section of memory which it wishes to access. For example, the address may be the storage location for the first of a series of program instructions which are to be consecutively read from the memory and applied to the microprocessor. The flash memory 55 receives the initial address and upon the receipt of control signals for each subsequent read/write cycle, the memory address generator increments steps to the next consecutive storage location." ['003 Reference,

CLAIM	RESPONSE
.	Col. 7:44-56] *See also* '003 Reference, Col. 8:14-45, Col. 8:66-9:39, Col. 9:49-11:41.
2. The memory of claim 1, said memory having a random mode in which the memory receives an address and provides in response the contents of a unique memory location,	The '003 Reference meets this limitation. Specifically, the '003 Reference states: "In a first mode, the memory circuit responds to an initial request for access and an address signal by reading data from a storage location in one of the memory banks. Subsequent requests for access to continguous storage locations do not require an address signal, instead a control mechanism responds by generating an address to read data alternately from storage locations in the first and second memory banks. In a second mode, the memory circuit responds to every request for access to the memory circuit by enabling access to the first or second memory bank as indicated by an address which accompanied the request." ['003 Reference, Abstract]
wherein, both in burst mode and in random mode, while the contents of said location L1 are being transferred from one or more of said sense amplifiers to said output, the contents of said location L2 are being transferred from said location L2 to one or more of said sense amplifiers.	It would be obvious to a person of skill in the art that transferring the contents of a location L1 from one of the sens amplifiers to the output while the contents of a location L2 are transferred from the location L2 to one or more sense amplifiers could be used in either a burst mode or a random mode. *See* claim 1 above. Further, to the extent AMD reads this limitation on the Samsung devices, this limitation is met by numerous prior art references having both a random access mode and a burst mode.
3. The memory of claim 1 wherein when the locations L1 and L2 are read out in burst mode and when the contents of said location L1 are being transferred from one or more of said sense amplifiers to said output and the contents of said location L2 are being	This limitation is met by the '003 Reference alone or in combination with any of U.S. 4,937,788 or EP 0 087 754 B1 ("the '754 Reference") or the '937 Reference or U.S. Patent No. 5,251,178 ("the '178 Reference"): The '003 Reference states: "The flash memory control 88 also selectively enables one of two sets of bi-directional

CLAIM	RESPONSE
transferred from said location L2 to one or more of said sense amplifiers, the sense amplifiers from which the contents of said location L1 are being transferred are enabled and the sense amplifiers to which the contents of said location L2 are being transferred are disabled, but these latter sense amplifiers become enabled subsequently for amplifying the contents of said location L2.	data buffers 90 and 91 which respectively couple the bank data buses 82 and 83 to the processor section data bus 63. The bank data buses 82 and 83 can be coupled to the instruction bus 61 by the flash memory control 88 selectively enabling buffers 92 and 93, respectively." ['003 Reference, Col. 9:21-27] "In the interleaved access mode both banks 71 and 72 are simultaneously activated by address and control signals from the second microprocessor 54, but only one bank at a time is connected by buffers 90-93 to the instruction and data buses 61 and 63." ['003 Reference, Col. 9:52-57] The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58] The '788 Reference states: "According to this arrangement, only one plane is selected in accordance with the content of the upper-order two bits of the row address. The selected plane is activated and exhibits the memory operation but the rest of the planes which are under the non-

CLAIM	RESPONSE
	selection state are inoperative. Therefore, the decoders and the sense amplifiers are inoperative in these inoperative planes and the memory is not refreshed. Therefore, power is consumed in only the selected plane and unnecessary power consumption in the other plane can be saved. Thus, the requirement for low power consumption can be satisfied." ['788 Reference, Col. 5:57-68] The '937 Reference states: "The sense amplifier 86 is controlled by the signals SE_{EV} to amplify the read data thereby to supply the same to the data latch 87, which in turn temporarily stores the outputs from the sense amplifiers 86. When the signals SE_{EV} are at low levels, the data latch 87 is electrically cut off from the sense amplifier 86. Data from the data latch 87 are transferred to the output latch 89 when the signals OE_{EV} are at high levels. In a similar manner, the sense amplifier 96 is controlled by the signals SE_{OD} to amplify the read data thereby to supply the same to the data latch 97, which in turn temporarily stores the outputs from the sense amplifier 96. When the signals SE_{OD} are at low levels, the data latch 97 is electrically cut off from the sense amplifier 96." ['937 Reference, Col. 4:52-66] The '178 Reference states: "Referring now to FIG. 2, the circuit of FIG. 1 has been modified to utilize the fact that, when RA10=1, only one half of the ARRAY BANKs 20 are being utilized and that, when RA10=0, the other half of the ARRAY BANKs 20 are being utilized. In particular, the RA 10 address is used to cause only the half of the ARRAY BANKs 20 that are being utilized to draw power from the DRAM energy source during read/write operations, while at the same time permitting the periodic performance of the refresh cycle in the usual manner on all ARRAY BANKs." ['178 Reference, Col. 3:32-42]

CLAIM	RESPONSE
4. The memory of claim 1 wherein:	
said memory comprises k pluralities S-1, . . . , S-k of locations wherein k is a number of said pluralities and is greater than or equal to two; for each plurality S-i, said sense amplifiers can receive simultaneously the contents of number m of locations from said plurality S-i, wherein m is a positive integer; and	This limitation is met by the '003. Specifically, the '003 Reference states: "The memory has first and second memory banks each having a series of storage locations and being coupled to the means for exchanging data. In the preferred embodiment, each memory bank is formed by a plurality of integrated circuit memory devices connected in parallel with each device storing a different group of bits of a word of digital data. An address bus is connected to the first and second memory banks to carry an address signal that indicates a storage location to be accessed." ['003 Reference, Col. 2:37-46] "The flash memory 55 can be configured to sequentially access only the storage locations in one of the memory banks 71 or 72, or to access both memory banks in an interleaved manner." ['003 Reference, Col. 9:49-52]
time tARA does not exceed m * (k-1) * (tOE), wherein: tARA is measured from the time that an address of a location is made available to said memory to the time when one or more of said sense amplifiers develop an output signal indicative of the contents of said location; and tOE is the time to transfer an output of any one of said sense amplifiers to said output of said memory.	A person of skill in the art would know that this timing relationship would be used when designing the memory disclosed in claim 1.

CLAIM	RESPONSE
5. The memory of claim 1	
wherein, in burst mode, a time in which each location of said plurality except said one of said locations is read out to said output after a previous location has been read out to said output is shorter than a time in which said one of said locations is read out to said output after said address of said one of said locations has been received by said memory.	This element is met for the '003 Reference. Specifically, the '003 Reference states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41]
6. The memory of claim 1 wherein said memory is fabricated in an integrated circuit.	This element is met by the '003 Reference in combination with any of the '754 Reference or the '199 Reference, or U.S. Patent No. 4,899,312 ("the '312 Reference"). The '754 Reference states: "The present invention relates to a semiconductor dynamic memory device. Mass-production of 64K bit dynamic type random access memory devices (DRAMs) has been enabled by the recent development of semiconductor memory devices of high

CLAIM	RESPONSE
	packing density. Furthermore, a 256K bit DRAM has been developed." ['754 Reference, Page 2:1-4] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer." ['199 Reference, Col. 1:13-16] The '312 Reference states: "The individual circuit elements constructing the RAM of the present embodiment are formed on a semiconductor substrate such as a piece of single-crystalline silicon by the known technique for fabricating a CMOS (i.e., Complementary MOS) integreated circuit." ['312 Reference, Col. 2:34-38]
7. The memory of claim 1 further comprising:	
a plurality of second registers, each second register for receiving at least a portion of a column address; and	This element is met by the '003 Reference. Specifically, the '003 Reference states: "The programmable read only memory in the processor section 31 is a flash-type memory 55 such as described in *Flash Memory Products Data Book*, published in 1989 by Advanced Micro Devices." ['003 Reference, Col. 7:41-44] "With reference to FIG. 3, the flash memory 55 has two banks 71 and 72, denoted by dashed lines, with each bank having four flash memory devices 73-76 and 77-80, respectively. For example, the flash memory devices are model 28F010 devices manufactured by Advanced Micro Devices. Each memory device is eight bits wide and four of them are connected in parallel to a common bank address bus 81 and internal bank internal data buses 82 and 83. Different bit lines of the data buses 82 and

CLAIM	RESPONSE
	83 connect to each memory device 73-76 and 77-80. Thus the combination of the four memory devices in a given bank enable a thirty-two bit wide word of data to be contained in each individually addressable storage location in the bank." ['003 Reference, Col. 8:1-14] A person of ordinary skill in the art would know that each memory device would have a plurality of registers for receiving a column address. "The result of that operation is passed on to the bank address generator 86 where it is used as the first address for accessing the flash memory banks 71 and 72." ['003 Reference, Col. 10:34-37] "While this is occurring, the bank address generator 86 increments the least significant address bits that are applied to the lower bus 81L" for the second flash memory bank 72. This action prepares the second bank 72 to supply the next instruction when a subsequent access request is received by the flash memory 55." ['003 Reference, Col. 11:27-32] Bank address generator 86 has a plurality of registers for receiving a column address. *See also* Figs. 3, 4a and 4b; Col. 8:57-9:12 and Col. 10:16-42.
a circuitry for each second register for selecting in response to signals from one of the second registers a plurality of columns to be read by the sense amplifiers.	This element is met in the '003 Reference. Specifically, the '003 Reference states that: "The programmable read only memory in the processor section 31 is a flash-type memory 55 such as described in *Flash Memory Products Data Book*, published in 1989 by Advanced Micro Devices." ['003 Reference, Col. 7:41-44] "With reference to FIG. 3, the flash memory 55 has two banks 71 and 72, denoted by dashed lines, with each bank having four flash memory devices 73-76 and 77-80, respectively. For example, the flash memory devices are model 28F010 devices manufactured by Advanced Micro Devices. Each memory device is eight bits wide

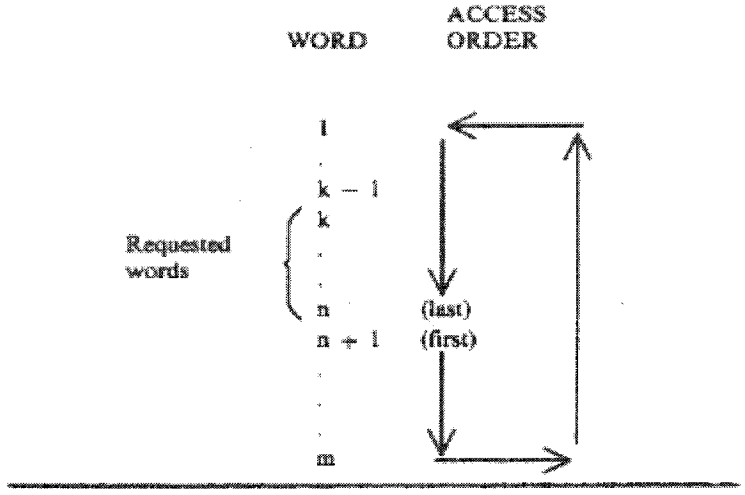
CLAIM	RESPONSE
	and four of them are connected in parallel to a common bank address bus 81 and internal bank internal data buses 82 and 83. Different bit lines of the data buses 82 and 83 connect to eah memory device 73-76 and 77-80. Thus the combination of the four memory devices in a given bank enable a thirty-two bit wide word of data to be contained in each individually addressable storage location in the bank." ['003 Reference, Col. 8:1-14] A person of ordinary skill in the art would know that each memory device would have circuitry for selecting columns in response to signals from the column registers. *See also* Figs. 3, 4a and 4b; Col. 8:57-9:12 and Col. 10:16-42.
8. A memory comprising:	Although a preamble is normally not limiting, should this preamble be limiting, this element is met in the '003 Reference. Specifically, the '003 Reference is titled "Flash Memory Circuit and Method of Operation."
a set of consecutively addressed memory locations L1, . . . Ln;	This element is met in the '003 Reference. Specifically, the '003 Reference states that: "In a first mode, the memory circuit responds to an initial request for access and an address signal by reading data from a storage location in one of the memory banks. Subsequent requests for access to continguous storage locations do not require an address signal, instead a control mechanism responds by generating an address to read data alternately from storage locations in the first and second memory banks. In a second mode, the memory circuit responds to every request for access to the memory circuit by enabling access to the first or second memory bank as indicated by an address which accompanied the request." ['003 Reference, Abstract] "These particular devices are configured to operate in the burst addressing mode performed by the second microprocessor 54. In this addressing mode, the second microprocessor 54 sends an initial address of a section of memory which it wishes to

CLAIM	RESPONSE
	access. For example, the address may be the storage location for the first of a series of program instructions which are to be consecutively read from the memory and applied to the microprocessor. The flash memory 55 receives the initial address and upon the receipt of control signals for each subsequent read/write cycle, the memory address generator increments steps to the next consecutive storage location." ['003 Reference, Col. 7:44-56]
a plurality of sense amplifier circuits for amplifying contents of said memory locations; and	This element is met in the '003 Reference. Specifically, the '003 Reference states that: "The programmable read only memory in the processor section 31 is a flash-type memory 55 such as described in *Flash Memory Products Data Book*, published in 1989 by Advanced Micro Devices." ['003 Reference, Col. 7:41-44] "With reference to FIG. 3, the flash memory 55 has two banks 71 and 72, denoted by dashed lines, with each bank having four flash memory devices 73-76 and 77-80, respectively. For example, the flash memory devices are model 28F010 devices manufactured by Advanced Micro Devices. Each memory device is eight bits wide and four of them are connected in parallel to a common bank address bus 81 and internal bank internal data buses 82 and 83. Different bit lines of the data buses 82 and 83 connect to each memory device 73-76 and 77-80. Thus the combination of the four memory devices in a given bank enable a thirty-two bit wide word of data to be contained in each individually addressable storage location in the bank." ['003 Reference, Col. 8:1-14] A person of ordinary skill in the art would know that each memory device would have sense amplifiers. *See also* Figs. 3, 4a and 4b; Col. 8:57-9:12 and Col. 10:16-42.
an output for providing output signals from	This element is met in the '003 Reference. Specifically, the '003 Reference states that:

CLAIM	RESPONSE
said plurality of sense amplifier circuits,	"The programmable read only memory in the processor section 31 is a flash-type memory 55 such as described in *Flash Memory Products Data Book*, published in 1989 by Advanced Micro Devices." ['003 Reference, Col. 7:41-44] "With reference to FIG. 3, the flash memory 55 has two banks 71 and 72, denoted by dashed lines, with each bank having four flash memory devices 73-76 and 77-80, respectively. For example, the flash memory devices are model 28F010 devices manufactured by Advanced Micro Devices. Each memory device is eight bits wide and four of them are connected in parallel to a common bank address bus 81 and internal bank internal data buses 82 and 83. Different bit lines of the data buses 82 and 83 connect to each memory device 73-76 and 77-80. Thus the combination of the four memory devices in a given bank enable a thirty-two bit wide word of data to be contained in each individually addressable storage location in the bank." ['003 Reference, Col. 8:1-14] A person of ordinary skill in the art would know that each memory device would have output for providing output signals from the sense amplifiers. *See also* Figs. 3, 4a and 4b; Col. 8:57-9:12 and Col. 10:16-42.
wherein said memory has a burst mode operation for receiving an address and reading out to said output, in response to said address, any given number of memory locations in the sequence of consecutive addresses with wrap around so that the next location, if any, to be read out after said location Ln is said location L1, such that during said operation while the contents of any location L to be read out other than the	This element is met in the '003 Reference in combination with EP 0 326 885 ("the '885 Reference") or U.S. Patent No. 4,912,631 ("the '631 Reference"). Specifically, the '003 Reference states that: "Standard memories are commonly configured as interleaved banks of devices to obtain improved performance and faster access time. In this technique, two or more banks of identical memory devices are arranged in such a way that the requests for data from each one overlap, i.e. when one bank is delivering data, the other bank is preparing to deliver the next sequential item of data." ['003 Reference, Col. 1:22-29]

CLAIM	RESPONSE
last location to be read out are being transferred from said plurality of sense amplifier circuits to said output, the contents of another location to be read out after said location L are being provided to said plurality of sense amplifier circuits for amplification and subsequent transfer to said output, and	"In the first mode, the control mechanism responds to an initial request for access and an address signal by reading data from a storage location in one of the memory banks. Subsequent requests for access to the next adjacent storage location do not require that an address be sent with the request. The control mechanism responds to such subsequent requests by generating addresses to read data alternately from storage locations in the first and second memory banks." ['003 Reference, Col. 2:48-52] "These particular devices are configured to operate in the burst addressing mode performed by the second microprocessor 54. In this addressing mode, the second microprocessor 54 sends an initial address of a section of memory which it wishes to access. For example, the address may be the storage location for the first of a series of program instructions which are to be consecutively read from the memory and applied to the microprocessor. The flash memory 55 receives the initial address and upon the receipt of control signals for each subsequent read/write cycle, the memory address generator increments steps to the next consecutive storage location." ['003 Reference, Col. 7:44-56] *See also* '003 Reference, Col. 8:14-45, Col. 8:66-9:39, Col. 9:49-11:41. The '885 Reference states: "After the last memory address is reached, the access automatically rolls over to the first address." ['885 Reference, Col. 3:1-3] "A method as in claim 5 wherein the sequence of incremented addresses wraps around when the address of the Nth register is reached such that all N registers in the array are read." ['885 Reference, Col. 7:45-48] The '631 Reference states that:

CLAIM	RESPONSE
	"The above-described method is accomplished by utilizing two pieces of information, which are placed on the bus (23) by the GDP: the data word's offset and the number of words requested. The data word's offset in the cache line is derived from adress bits 2 and 3 (00=word 1, 01=word 2, 10=word 3, and 11=word 4). The number of words being requested is obtained from the size bits 0 and 1 (00=1word, 01=2 words, 10=3 words, and 11=4words). Using these two pieces of information, the following algorithm is executed: FIRST WORD ACCESSED = PROCESSOR WORD ADDRESS + SIZE +1 The 1 is added to the size in order to yield the correct offset. For example, if the GDP requests two words at offset 01 in a four-word line, it is convereted to a wraparound request of four words to memory starting at word four [offset (01) + word count (01) + 1 = 11]." ['631 Reference, Col. 3:46-65] See, '631 Reference, Table II:

CLAIM	RESPONSE
	TABLE II  See also, '631 Reference, Abstract, Table I, Fig. 3.
wherein said memory further comprises a control circuit for selectively enabling said sense amplifier circuits so that said control circuit enables a sense amplifier circuit whose output signals are being transferred to the output of said memory but said control circuit does not enable all said sense amplifier circuits at the same time.	This limitation is met by the '003 Reference alone or in combination with any of the '754 Reference or the '937 Reference or the '178 Reference. The '003 Reference states: "The flash memory control 88 also selectively enables one of two sets of bi-directional data buffers 90 and 91 which respectively couple the bank data buses 82 and 83 to the processor section data bus 63. The bank data buses 82 and 83 can be coupled to the instruction bus 61 by the flash memory control 88 selectively enabling buffers 92 and

CLAIM	RESPONSE
	93, respectively." ['003 Reference, Col. 9:21-27] "In the interleaved access mode both banks 71 and 72 are simultaneously activated by address and control signals from the second microprocessor 54, but only one bank at a time is connected by buffers 90-93 to the instruction and data buses 61 and 63." ['003 Reference, Col. 9:52-57] The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58] The '788 Reference states: "According to this arrangement, only one plane is selected in accordance with the content of the upper-order two bits of the row address. The selected plane is activated and exhibits the memory operation but the rest of the planes which are under the non-selection state are inoperative. Therefore, the decoders and the sense amplifiers are inoperative in these inoperative planes and the memory is not refreshed. Therefore, power is consumed in only the selected plane and unnecessary power consumption in

CLAIM	RESPONSE
	the other plane can be saved. Thus, the requirement for low power consumption can be satisfied." ['788 Reference, Col. 5:57-68] The '937 Reference states: "The sense amplifier 86 is controlled by the signals SE_{EV} to amplify the read data thereby to supply the same to the data latch 87, which in turn temporarily stores the outputs from the sense amplifiers 86. When the signals SE_{EV} are at low levels, the data latch 87 is electrically cut off from the sense amplifier 86. Data from the data latch 87 are transferred to the output latch 89 when the signals OE_{EV} are at high levels. In a similar manner, the sense amplifier 96 is controlled by the signals SE_{OD} to amplify the read data thereby to supply the same to the data latch 97, which in turn temporarily stores the outputs from the sense amplifier 96. When the signals SE_{OD} are at low levels, the data latch 97 is electrically cut off from the sense amplifier 96." ['937 Reference, Col. 4:52-66] The '178 Reference states: "Referring now to FIG. 2, the circuit of FIG. 1 has been modified to utilize the fact that, when RA10=1, only one half of the ARRAY BANKs 20 are being utilized and that, when RA10=0, the other half of the ARRAY BANKs 20 are being utilized. In particular, the RA 10 address is used to cause only the half of the ARRAY BANKs 20 that are being utilized to draw power from the DRAM energy source during read/write operations, while at the same time permitting the periodic performance of the refresh cycle in the usual manner on all ARRAY BANKs." ['178 Reference, Col. 3:32-42]
9. The memory of claim 8 wherein, during said operation, said control circuit enables at the same time only:	