EXHIBIT 1

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CLAIM	RESPONSE
(1) the sense amplifier circuit whose output signals are being transferred to said output of said memory, and	This limitation is met by the '003 Reference alone or in combination with the '754 Reference. Specifically, the '003 Reference states: "The flash memory control 88 also selectively enables one of two sets of bi-directional data buffers 90 and 91 which respectively couple the bank data buses 82 and 83 to the processor section dtat bus 63. The bank data buses 82 and 83 can be coupled to the instruction bus 61 by the flash memory control 88 selectively enabling buffers 92 and 93, respectively." ['003 Reference, Col. 9:21-27] "In the interleaved access mode both banks 71 and 72 are simultaneously activated by address and control signals from the second microprocessor 54, but only one bank at a time is connected by buffers 90-93 to the instruction and data buses 61 an 63." ['003 Reference, Col. 9:52-57] *See also*, '003 Reference, Col. 10:16-66. The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754

CLAIM	RESPONSE
	Reference, Page 5:56-58] "A semiconductor dynamic memory device comprising: … a plurality of sense amplifying means (18-1 to 18-4; SA1 to SA8) responsive to a control signal input thereto, for selectively activating one sense amplifying means to sense and amplify data on said selected data lines of one of said two column-selected memory blocks, and for selectively activating at least one other sense amplifying means to refresh data to said each memory cell along said selected word lines; …." ['754 Reference, Page 6:53-7:5]
(2) a predetermined number of other sense amplifier circuits whose output signals will be transferred next to said output of said memory if said operation continues sufficiently long.	This limitation is met by the '003 Reference alone or in combination with the '754 Reference. Specifically, the '003 Reference states: "The flash memory control 88 also selectively enables one of two sets of bi-directional data buffers 90 and 91 which respectively couple the bank data buses 82 and 83 to the processor section dtat bus 63. The bank data buses 82 and 83 can be coupled to the instruction bus 61 by the flash memory control 88 selectively enabling buffers 92 and 93, respectively." ['003 Reference, Col. 9:21-27] "In the interleaved access mode both banks 71 and 72 are simultaneously activated by address and control signals from the second microprocessor 54, but only one bank at a time is connected by buffers 90-93 to the instruction and data buses 61 an 63." ['003 Reference, Col. 9:52-57] *See also*, '003 Reference, Col. 10:16-66. The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state.

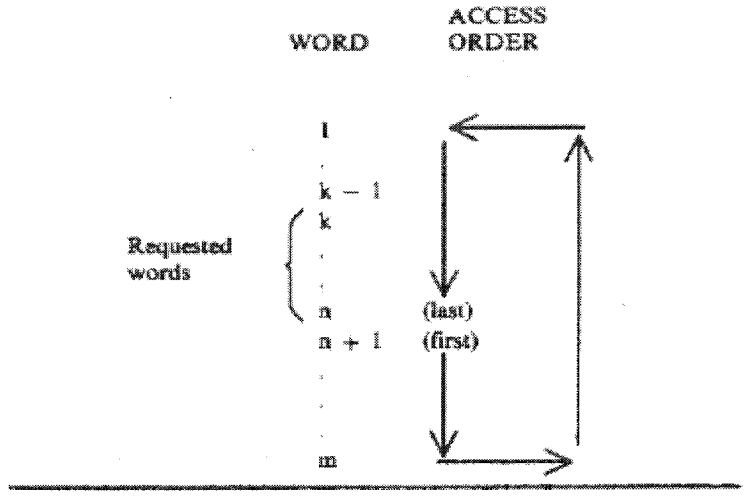
CLAIM	RESPONSE
	Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58] "A semiconductor dynamic memory device comprising: ... a plurality of sense amplifying means (18-1 to 18-4; SA1 to SA8) responsive to a control signal input thereto, for selectively activating one sense amplifying means to sense and amplify data on said selected data lines of one of said two column-selected memory blocks, and for selectively activating at least one other sense amplifying means to refresh data to said each memory cell along said selected word lines; ...." ['754 Reference, Page 6:53-7:5]
10. The memory of claim 7 wherein:	
said set of locations comprises k subsets S-1, . . . , S-k wherein k is greater than or equal to two, such that, for a positive integer m and for any subset S-i, the contents of m consecutively addressed locations from said subset S-i can be transferred simultaneously to said plurality of sense amplifier circuits; and	This limitation is met by the '003. Specifically, the '003 Reference states: "The memory has first and second memory banks each having a series of storage locations and being coupled to the means for exchanging data. In the preferred embodiment, each memory bank is formed by a plurality of integrated circuit memory devices connected in parallel with each device storing a different group of bits of a word of digital data. An address bus is connected to the first and second memory banks to carry an address signal that indicates a storage location to be accessed." ['003 Reference, Col. 2:37-46] "The flash memory 55 can be configured to sequentially access only the storage

CLAIM	RESPONSE
	locations in one of the memory banks 71 or 72, or to access both memory banks in an interleaved manner." ['003 Reference, Col. 9:49-52]
in said operation, time tARA does not exceed m * (k-1) * (tOE), wherein: tARA is measured from the time that an address of the first location to be read out in said operation is made available to said memory to the time when said plurality of sense amplifier circuits develops an output signal indicative of the contents of said first location; and tOE is the time to transfer the contents of any one of said locations from said plurality of sense amplifier circuits to said output.	A person of skill in the art would know that this timing relationship would be used when designing the memory disclosed in claim 1.
11. The memory of claim 8 wherein, in said operation, each location to be read out except the first location to be read out is read out to said output in a shorter time than the first location to be read out.	This element is met for the '003 Reference. Specifically, the '003 Reference states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13]

CLAIM	RESPONSE
	"In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41]
12. The memory of claim 8 wherein the sequence of locations L1, . . . , Ln is a sequence of increasing order of addresses.	This limitation is met by the '003 Reference. Specifically, the '003 Reference states: "In a first mode, the memory circuit responds to an initial request for access and an address signal by reading data from a storage location in one of the memory banks. Subsequent requests for access to continguous storage locations do no require an address signal, instead a control mechanism responds by generating an address to read data alternately from storage locations in the first and second memory banks. In a second mode, the memory circuit responds to every request for access to the memory circuit by enabling access to the first or second memory bank as indicated by an address which accompanied the request." ['003 Reference, Abstract] "These particular devices are configured to operate in the burst addressing mode performed by the second microprocessor 54. In this addressing mode, the second microprocessor 54 sends an initial address of a section of memory which it wishes to access. For example, the address may be the storage location for the first of a series of program instructions which are to be consecutively read from the memory and applied to the microprocessor. The flash memory 55 receives the initial address and upon the receipt of control signals for each subsequent read/write cycle, the memory address generator increments steps to the next consecutive storage location." ['003 Reference, Col. 7:44-56]
13. The memory of claim 7 wherein in said	This element is met by the '003 Reference in combination with the '885 or the '631.

CLAIM	RESPONSE
operation any number of said locations addressed consecutively with wrap around can be read out to said output so that:	Specifically, the '003 Reference states: "Standard memories are commonly configured as interleaved banks of devices to obtain improved performance and faster access time. In this technique, two or more banks of identical memory devices are arranged in such a way that the requests for data from each one overlap, i.e. when one bank is delivering data, the other bank is preparing to deliver the next sequential item of data." ['003 Reference, Col. 1:22-29] "In the first mode, the control mechanism responds to an initial request for access and an address signal by reading data from a storage location in one of the memory banks. Subsequent requests for access to the next adjacent storage location do not require that an address be sent with the request.. The control mechanism responds to such subsequent requests by generating addresses to read data alternately from storage locations in the first and second memory banks." ['003 Reference, Col. 2:48-52] "These particular devices are configured to operate in the burst addressing mode performed by the second microprocessor 54. In this addressing mode, the second microprocessor 54 sends an initial address of a section of memory which it wishes to access. For example, the address may be the storage location for the first of a series of program instructions which are to be consecutively read from the memory and applied to the microprocessor. The flash memory 55 receives the initial address and upon the receipt of control signals for each subsequent read/write cycle, the memory address generator increments steps to the next consecutive storage location." ['003 Reference, Col. 7:44-56] *See also* '003 Reference, Col. 8:14-45, Col. 8:66-9:39, Col. 9:49-11:41. The '885 Reference states:

CLAIM	RESPONSE
	"After the last memory address is reached, the access automatically rolls over to the first address." ['885 Reference, Col. 3:1-3] "A method as in claim 5 wherein the sequence of incremented addresses wraps around when the address of the Nth register is reached such that all N registers in the array are read." ['885 Reference, Col. 7:45-48] The '631 Reference states that: "The above-described method is accomplished by utilizing two pieces of information, which are placed on the bus (23) by the GDP: the data word's offset and the number of words requested. The data word's offset in the cache line is derived from adress bits 2 and 3 (00=word 1, 01=word 2, 10=word 3, and 11=word 4). The number of words being requested is obtained from the size bits 0 and 1 (00=1word, 01=2 words, 10=3 words, and 11=4words). Using these two pieces of information, the following algorithm is executed: FIRST WORD ACCESSED = PROCESSOR WORD ADDRESS + SIZE +1 The 1 is added to the size in order to yield the correct offset. For example, if the GDP requests two words at offset 01 in a four-word line, it is convereted to a wraparound request of four words to memory starting at word four [offset (01) + word count (01) + 1 = 11]." ['631 Reference, Col. 3:46-65] See, '631 Reference, Table II:

CLAIM	RESPONSE
	TABLE II  See also, '631 Reference, Abstract, Table I, Fig. 3.
the first location to be read out in said operation is read out to said output after time tARA+tOE wherein: tARA is measured from the time that an address of said first location is made available to said memory to the time when said plurality of sense amplifier circuits	This element is met by the '003 Reference. Specifically, the '003 Reference states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address

CLAIM	RESPONSE
develops an output signal indicative of the contents of said first location; and tOE is the time to transfer the contents of any one of said locations from said plurality of sense amplifier circuits to said output of said memory; and	in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41]
every other location to be read out in said operation is read out to said output within time tOE.	This element is met by the '003 Reference. Specifically, the '003 Reference states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with

CLAIM	RESPONSE
	each access request." ['003 Reference, Col. 11:33-41]
14. The memory of claim 8 wherein said memory is fabricated in an integrated circuit.	This element is met by the '003 Reference in combination with any of the '754 Reference or the '199 Reference or the '312 Reference. The '754 Reference states: "The present invention relates to a semiconductor dynamic memory device. Mass-production of 64K bit dynamic type random access memory devices (DRAMs) has been enabled by the recent development of semiconductor memory devices of high packing density. Furthermore, a 256K bit DRAM has been developed." ['754 Reference, Page 2:3-6] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer." ['199 Reference, Col. 1:13-16] The '312 Reference states: "The individual circuit elements constructing the RAM of the present embodiment are formed on a semiconductor substrate such as a piece of single-crystalline silicon by the known technique for fabricating a CMOS (i.e., Complementary MOS) integreated circuit." ['312 Reference, Col. 2:34-38]
20. An integrated memory comprising:	Although a preamble is normally not limiting, should this preamble be limiting, this element is met in the '003 Reference. Specifically, the '003 Reference is titled "Flash Memory Circuit and Method of Operation."
an array of memory locations, the array	This element is met in the '003 Reference. Specifically, the '003 Reference states that:

CLAIM	RESPONSE
comprising a plurality of subarrays, each subarray comprising a predetermined number of groups of columns of the memory locations such that for any given column position in a group, the memory locations in any given row in the columns at said given position in the groups of the subarray have consecutive addresses;	"In a first mode, the memory circuit responds to an initial request for access and an address signal by reading data from a storage location in one of the memory banks. Subsequent requests for access to continguous storage locations do not require an address signal, instead a control mechanism responds by generating an address to read data alternately from storage locations in the first and second memory banks. In a second mode, the memory circuit responds to every request for access to the memory circuit by enabling access to the first or second memory bank as indicated by an address which accompanied the request." ['003 Reference, Abstract] "These particular devices are configured to operate in the burst addressing mode performed by the second microprocessor 54. In this addressing mode, the second microprocessor 54 sends an initial address of a section of memory which it wishes to access. For example, the address may be the storage location for the first of a series of program instructions which are to be consecutively read from the memory and applied to the microprocessor. The flash memory 55 receives the initial address and upon the receipt of control signals for each subsequent read/write cycle, the memory address generator increments steps to the next consecutive storage location." ['003 Reference, Col. 7:44-56]
one X-decoder for each subarray;	This element is met by the '003 Reference. Specifically, the '003 Reference states: "The programmable read only memory in the processor section 31 is a flash-type memory 55 such as described in *Flash Memory Products Data Book*, published in 1989 by Advanced Micro Devices." ['033 Reference, Col. 7:41-44] "With reference to FIG. 3, the flash memory 55 has two banks 71 and 72, denoted by dashed lines, with each bank having four flash memory devices 73-76 and 77-80, respectively. For example, the flash memory devices are model 28F010 devices

CLAIM	RESPONSE
	manufactured by Advanced Micro Devices. Each memory device is eight bits wide and four of them are connected in parallel to a common bank address bus 81 and internal bank internal data buses 82 and 83. Different bit lines of the data buses 82 and 83 connect to eah memory device 73-76 and 77-80. Thus the combination of the four memory devices in a given bank enable a thirty-two bit wide word of data to be contained in each individually addressable storage location in the bank." ['003 Reference, Col. 8:1-14] A person of ordinary skill in the art would know that each memory device would have an X-decoder. *See also* Figs. 3, 4a and 4b; Col. 8:57-9:12 and Col. 10:16-42.
one X-register for each X-decoder;	This element is met by the '003 Reference. Specifically, the '003 Reference states: "The programmable read only memory in the processor section 31 is a flash-type memory 55 such as described in *Flash Memory Products Data Book*, published in 1989 by Advanced Micro Devices." ['003 Reference, Col. 7:41-44] "With reference to FIG. 3, the flash memory 55 has two banks 71 and 72, denoted by dashed lines, with each bank having four flash memory devices 73-76 and 77-80, respectively. For example, the flash memory devices are model 28F010 devices manufactured by Advanced Micro Devices. Each memory device is eight bits wide and four of them are connected in parallel to a common bank address bus 81 and internal bank internal data buses 82 and 83. Different bit lines of the data buses 82 and 83 connect to each memory device 73-76 and 77-80. Thus the combination of the four memory devices in a given bank enable a thirty-two bit wide word of data to be contained in each individually addressable storage location in the bank." ['003 Reference, Col. 8:1-14] A person of ordinary skill in the art would know that each memory device would have an X register for each X-decoder.

CLAIM	RESPONSE
	"The result of that operation is passed on to the bank address generator 86 where it is used as the first address for accessing the flash memory banks 71 and 72." ['003 Reference, Col. 10:34-37] "While this is occurring, the bank address generator 86 increments the least significant address bits that are applied to the lower bus 81L" for the second flash memory bank 72. This action prepares the second bank 72 to supply the next instruction when a subsequent access request is received by the flash memory 55." ['003 Reference, Col. 11:27-32] Bank address generator 86 has a plurality of X-registers. *See also* Figs. 3, 4a and 4b; Col. 8:57-9:12 and Col. 10:16-42.
one Y-decoder for each subarray;	This element is met by the '003 Reference. Specifically, the '003 Reference states: "The programmable read only memory in the processor section 31 is a flash-type memory 55 such as described in *Flash Memory Products Data Book*, published in 1989 by Advanced Micro Devices." ['003 Reference, Col. 7:41-44] "With reference to FIG. 3, the flash memory 55 has two banks 71 and 72, denoted by dashed lines, with each bank having four flash memory devices 73-76 and 77-80, respectively. For example, the flash memory devices are model 28F010 devices manufactured by Advanced Micro Devices. Each memory device is eight bits wide and four of them are connected in parallel to a common bank address bus 81 and internal bank internal data buses 82 and 83. Different bit lines of the data buses 82 and 83 connect to each memory device 73-76 and 77-80. Thus the combination of the four memory devices in a given bank enable a thirty-two bit wide word of data to be contained in each individually addressable storage location in the bank." ['003 Reference, Col. 8:1-14] A person of ordinary skill in the art would know that each memory device would have a Y decoder for receiving a row address.

CLAIM	RESPONSE
	See also Figs. 3, 4a and 4b; Col. 8:57-9:12 and Col. 10:16-42.
one Y-register for each Y-decoder;	This element is met by the '003 Reference. Specifically, the '003 Reference states: "The programmable read only memory in the processor section 31 is a flash-type memory 55 such as described in *Flash Memory Products Data Book*, published in 1989 by Advanced Micro Devices." ['003 Reference, Col. 7:41-44] "With reference to FIG. 3, the flash memory 55 has two banks 71 and 72, denoted by dashed lines, with each bank having four flash memory devices 73-76 and 77-80, respectively. For example, the flash memory devices are model 28F010 devices manufactured by Advanced Micro Devices. Each memory device is eight bits wide and four of them are connected in parallel to a common bank address bus 81 and internal bank internal data buses 82 and 83. Different bit lines of the data buses 82 and 83 connect to each memory device 73-76 and 77-80. Thus the combination of the four memory devices in a given bank enable a thirty-two bit wide word of data to be contained in each individually addressable storage location in the bank." ['003 Reference, Col. 8:1-14] A person of ordinary skill in the art would know that each memory device would have a Y register for receiving a row address. "The result of that operation is passed on to the bank address generator 86 where it is used as the first address for accessing the flash memory banks 71 and 72." ['003 Reference, Col. 10:34-37] "While this is occurring, the bank address generator 86 increments the least significant address bits that are applied to the lower bus 81L" for the second flash memory bank 72. This action prepares the second bank 72 to supply the next instruction when a subsequent access request is received by the flash memory 55." ['003 Reference, Col.

CLAIM	RESPONSE
	11:27-32] Bank address generator 86 has a plurality of Y-registers. *See also* Figs. 3, 4a and 4b; Col. 8:57-9:12 and Col. 10:16-42.
one Y-select circuit for each subarray, the Y-select circuit being responsive to the Y-decoder of the subarray to select all the columns that occupy a selected position in the groups of the subarray;	This element is met by the '003 Reference. Specifically, the '003 Reference states: "The programmable read only memory in the processor section 31 is a flash-type memory 55 such as described in *Flash Memory Products Data Book*, published in 1989 by Advanced Micro Devices." ['003 Reference, Col. 7:41-44] "With reference to FIG. 3, the flash memory 55 has two banks 71 and 72, denoted by dashed lines, with each bank having four flash memory devices 73-76 and 77-80, respectively. For example, the flash memory devices are model 28F010 devices manufactured by Advanced Micro Devices. Each memory device is eight bits wide and four of them are connected in parallel to a common bank address bus 81 and internal bank internal data buses 82 and 83. Different bit lines of the data buses 82 and 83 connect to each memory device 73-76 and 77-80. Thus the combination of the four memory devices in a given bank enable a thirty-two bit wide word of data to be contained in each individually addressable storage location in the bank." ['003 Reference, Col. 8:1-14] A person of ordinary skill in the art would know that each memory device would have a Y-select circuit. *See also* Figs. 3, 4a and 4b; Col. 8:57-9:12 and Col. 10:16-42.
a plurality of sense amplifier circuits for each subarray, each sense amplifier circuit for amplifying signals from a column selected by the Y-select circuit of the	This element is met by the '003 Reference. Specifically, the '003 Reference states: "The programmable read only memory in the processor section 31 is a flash-type memory 55 such as described in *Flash Memory Products Data Book*, published in

CLAIM	RESPONSE
subarray;	1989 by Advanced Micro Devices." ['003 Reference, Col. 7:41-44] "With reference to FIG. 3, the flash memory 55 has two banks 71 and 72, denoted by dashed lines, with each bank having four flash memory devices 73-76 and 77-80, respectively. For example, the flash memory devices are model 28F010 devices manufactured by Advanced Micro Devices. Each memory device is eight bits wide and four of them are connected in parallel to a common bank address bus 81 and internal bank internal data buses 82 and 83. Different bit lines of the data buses 82 and 83 connect to each memory device 73-76 and 77-80. Thus the combination of the four memory devices in a given bank enable a thirty-two bit wide word of data to be contained in each individually addressable storage location in the bank." ['003 Reference, Col. 8:1-14] A person of ordinary skill in the art would know that each memory device would have sense amplifiers. *See also* Figs. 3, 4a and 4b; Col. 8:57-9:12 and Col. 10:16-42.
a memory output; and	This element is met by the '003 Reference. Specifically, the '003 Reference states: "The programmable read only memory in the processor section 31 is a flash-type memory 55 such as described in *Flash Memory Products Data Book*, published in 1989 by Advanced Micro Devices." ['003 Reference, Col. 7:41-44] "With reference to FIG. 3, the flash memory 55 has two banks 71 and 72, denoted by dashed lines, with each bank having four flash memory devices 73-76 and 77-80, respectively. For example, the flash memory devices are model 28F010 devices manufactured by Advanced Micro Devices. Each memory device is eight bits wide and four of them are connected in parallel to a common bank address bus 81 and internal bank internal data buses 82 and 83. Different bit lines of the data buses 82 and 83 connect to each memory device 73-76 and 77-80. Thus the combination of the four

CLAIM	RESPONSE
	memory devices in a given bank enable a thirty-two bit wide word of data to be contained in each individually addressable storage location in the bank." ['003 Reference, Col. 8:1-14] A person of ordinary skill in the art would know that each memory device would have an output. "In the interleaved access mode both banks 71 and 72 are simultaneously activated by address and control signals from the second microprocessor 54, but only one bank at a time is connected by buffers 90-93 to the instruction and data buses 61 and 63." ['003 Reference, Col. 9:52-57]
a control circuit for selecting one of the sense amplifier circuits to provide data to the memory output;	It was well known in the art that information in the sense amplifiers could be read out one bit at a time and a person of skill in the art would understand this limitation to be met by the '003 Reference alone or in combination with the '754 Reference. The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "A semiconductor dynamic memory device comprising: … a plurality of sense amplifying means (18-1 to 18-4; SA1 to SA8) responsive to a control signal input thereto, for selectively activating one sense amplifying means to sense and amplify data on said selected data lines of one of said two column-selected memory blocks, and for selectively activating at least one other sense amplifying means to refresh data to

CLAIM	RESPONSE
	said each memory cell along said selected word lines; ...." ['754 Reference, Page 6:53-7:5]
wherein in a burst mode read operation, at least one X-register provides to its respective X-decoder signals identifying a row in one of the subarrays, and at least one Y-register provides to its respective Y-decoder signals identifying a position of columns in the groups of one of the subarrays.	This element is met in the '003 Reference alone or in combination with the '937 Reference or the '754 Reference or U.S. Patent No. 4,875,196 ("the '196 Reference") or U.S. Patent No. 5,036,494 ("the '494 Reference") or admitted prior art disclosed in Figure 2 of the '990 patent.. This element is met by the '003 Reference. Specifically, the '003 Reference states: "The programmable read only memory in the processor section 31 is a flash-type memory 55 such as described in *Flash Memory Products Data Book*, published in 1989 by Advanced Micro Devices." ['003 Reference, Col. 7:41-44] "With reference to FIG. 3, the flash memory 55 has two banks 71 and 72, denoted by dashed lines, with each bank having four flash memory devices 73-76 and 77-80, respectively. For example, the flash memory devices are model 28F010 devices manufactured by Advanced Micro Devices. Each memory device is eight bits wide and four of them are connected in parallel to a common bank address bus 81 and internal bank internal data buses 82 and 83. Different bit lines of the data buses 82 and 83 connect to each memory device 73-76 and 77-80. Thus the combination of the four memory devices in a given bank enable a thirty-two bit wide word of data to be contained in each individually addressable storage location in the bank." ['003 Reference, Col. 8:1-14] A person of ordinary skill in the art would know that each memory device operates in the manner claimed. *See also* Figs. 3, 4a and 4b; Col. 8:15-32, Col. 9:49-10:66. The '937 patent states that:

CLAIM	RESPONSE
	"The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:33-42] The '754 Reference states: "Furthermore, this dynamic memory device has row and column address buffers 20 and 22 for respectively storing row and column address data supplied from an address signal generator (not shown); …." ['754 Reference, Page 4:44-51] "Output data from the row address buffer 20 excluding the most significant bit MSB is supplied to the row decoders 16-1 to 16-4, and the output data from the column address buffer 22 is supplied to the columns decoders 14-1 and 14-2 through the gate circuits 30 and 32, respectively." ['754 Reference, Page 4:52-54] The '196 Reference states: "In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit lines in the other array are being precharged. Thus, as data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit

CLAIM	RESPONSE
	lines in that array will already have been initialied." ['196 Reference, Col. 2:60-67] "In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and settling transient signals) in preparation for the next access form such other array. Therefore, precharging times for one array overlap the time for performing read or write operation in the other array, and therefore do not limit operating speed." ['196 Reference, Col. 3:41-47] The '494 Reference states: In the example shown in FIG. 1 each memory block 14 and 15 has sixty four columns 35, each column being coupled to equate and precharge circuitry 36. The columns are arranged in groups, each group having eight pairs of bit lines so that when any column is addressed eight pairs of bit lines (one in each group) are simultaneously accessed, permitting transfer of eight bits or one word at a time. The bit lines are each connected to column multiplexing circuitry 37 for each columns and coupled to sense amplifier and write circuitry 38 for each column. Each sense amplifier and write circuit is connected through a bus driver circuit 39 to the data output 17. Each memory block 14 and 15 has 70 rows each having a word line 25. The word lines are connected to a row decoder 40. The row decoder is coupled to memory block 14 through a latch and word line driver 41 and to the memory block 15 through a latch and word line driver 42. The column multiplex circuitry 37 is controlled by a column counter 44. The row decoder 40 is controlled by a row counter 45. The latch and word line drivers 41 and 42 are controlled by pulse generators 46 and 47 respectively. Each of the drivers 41 and 42 is connected by two separate control lines 48 to the respective one of the pulse generators 46 and 47 so that each driver can be operated either to latch the output of the row decoder 40 or to drive all the word lines low. The selection of memory locations forming each cyclic pattern of addressing is controlled by the control until 13. The row counter 45 and columns counter 44 are connected so that unless

CLAIM	RESPONSE
	instructed by the control 13 to do otherwise they count through successive addresses along each row and then row by row." ['494 Reference, Col. 7:44-8:27]
22. The memory of claim 20 wherein in the burst mode read operation while data from the sense amplifier circuits of one of the subarrays are provided to the memory output, the sense amplifier circuits of another one of the subarrays develop output signals corresponding to data in said other one of the subarrays.	This element is met in the '003 Reference. Specifically, the '003 Reference states that: "Standard memories are commonly configured as interleaved banks of devices to obtain improved performance and faster access time. In this technique, two or more banks of identical memory devices are arranged in such a way that the requests for data from each one overlap, i.e. when one bank is delivering data, the other bank is preparing to deliver the next sequential item of data." ['003 Reference, Col. 1:22-29] "In the first mode, the control mechanism responds to an initial request for access and an address signal by reading data from a storage location in one of the memory banks. Subsequent requests for access to the next adjacent storage location do not require that an address be sent with the request.. The control mechanism responds to such subsequent requests by generating addresses to read data alternately from storage locations in the first and second memory banks." ['003 Reference, Col. 2:48-52] "These particular devices are configured to operate in the burst addressing mode performed by the second microprocessor 54. In this addressing mode, the second microprocessor 54 sends an initial address of a section of memory which it wishes to access. For example, the address may be the storage location for the first of a series of program instructions which are to be consecutively read from the memory and applied to the microprocessor. The flash memory 55 receives the initial address and upon the receipt of control signals for each subsequent read/write cycle, the memory address generator increments steps to the next consecutive storage location." ['003 Reference, Col. 7:44-56] *See also* '003 Reference, Col. 8:14-45, Col. 8:66-9:39, Col. 9:49-11:41.

CLAIM	RESPONSE
23. The memory of claim 20 wherein in the burst mode read operation, the control circuit enables the sense amplifier circuit selected to provide data to the memory output and at the same time disables one or more sense amplifier circuits not selected to provide data to the memory output.	This limitation is met by the '003 Reference alone or in combination with any of the '754 Reference or the '788 Refernce or the '937 Reference or the '178 Reference. The '003 Reference states: "The flash memory control 88 also selectively enables one of two sets of bi-directional data buffers 90 and 91 which respectively couple the bank data buses 82 and 83 to the processor section data bus 63. The bank data buses 82 and 83 can be coupled to the instruction bus 61 by the flash memory control 88 selectively enabling buffers 92 and 93, respectively." ['003 Reference, Col. 9:21-27] "In the interleaved access mode both banks 71 and 72 are simultaneously activated by address and control signals from the second microprocessor 54, but only one bank at a time is connected by buffers 90-93 to the instruction and data buses 61 and 63." ['003 Reference, Col. 9:52-57] The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754

CLAIM	RESPONSE
	Reference, Page 5:56-58] The '788 Reference states: "According to this arrangement, only one plane is selected in accordance with the content of the upper-order two bits of the row address. The selected plane is activated and exhibits the memory operation but the rest of the planes which are under the non-selection state are inoperative. Therefore, the decoders and the sense amplifiers are inoperative in these inoperative planes and the memory is not refreshed. Therefore, power is consumed in only the selected plane and unnecessary power consumption in the other plane can be saved. Thus, the requirement for low power consumption can be satisfied." ['788 Reference, Col. 5:57-68] The '937 Reference states: "The sense amplifier 86 is controlled by the signals SE_{EV} to amplify the read data thereby to supply the same to the data latch 87, which in turn temporarily stores the outputs from the sense amplifiers 86. When the signals SE_{EV} are at low levels, the data latch 87 is electrically cut off from the sense amplifier 86. Data from the data latch 87 are transferred to the output latch 89 when the signals OE_{EV} are at high levels. In a similar manner, the sense amplifier 96 is controlled by the signals SE_{OD} to amplify the read data thereby to supply the same to the data latch 97, which in turn temporarily stores the outputs from the sense amplifier 96. When the signals SE_{OD} are at low levels, the data latch 97 is electrically cut off from the sense amplifier 96." ['937 Reference, Col. 4:52-66] The '178 Reference states: "Referring now to FIG. 2, the circuit of FIG. 1 has been modified to utilize the fact

CLAIM	RESPONSE
	that, when RA10=1, only one half of the ARRAY BANKs 20 are being utilized and that, when RA10=0, the other half of the ARRAY BANKs 20 are being utilized. In particular, the RA 10 address is used to cause only the half of the ARRAY BANKs 20 that are being utilized to draw power from the DRAM energy source during read/write operations, while at the same time permitting the periodic performance of the refresh cycle in the usual manner on all ARRAY BANKs." ['178 Reference, Col. 3:32-42]