EXHIBIT 1

D11

Appendix D11
Defendants and Counterclaimants' Invalidity Contentions
Advanced Micro Devices, Inc., et al., v. Samsung Electronics Co., Ltd., et al., Case No. 3:08-CV-0986-SI

U.S. patent No. 5,559,990 Invalidity Chart: EP 0 326 885 ("'885 Reference")

All asserted claims are anticipated by the '885 Reference and/or are rendered obvious by it, either alone or in combination with other prior art described below and/or listed in Section I of Defendants' and Counterclaimants' Preliminary Invalidity Contentions and/or through modifications described below. Nothing in this invalidity chart should be construed as signifying or suggesting Defendants and Counterclaimants' adoption of or acquiescence in any claim scope and/or claim construction positions taken by Plaintiffs and Counterdefendants in this litigation.

CLAIM	RESPONSE
1. A memory comprising:	Although a preamble is normally not limiting, should this preamble be limiting, this element is met by EP 0 326 885 ("the '885 Reference"). Specifically, the '885 Reference is titled "Sequential read access of serial memories with user defined starting address."
a plurality of rows of memory locations;	This element is met by EP 0 326 885 A2 ("the '885 Reference"). Specifically, the '885 Reference states: "Fig. 1 shows the basic elements of an electrically erasable programmable read only memory (EEPROM) device. The device includes an EEPROM array 2 which is divided into 256 storage registers of 16 bits each." ['885 Reference, Col. 3:44-48; *see also* Figs. 1 and 2]
a plurality of first registers, each first register for receiving a row address;	This element is met by '885 Reference in combination with any of U.S. Patent No. 4,849,937 ("the '937 Reference") or U.S. Patent No. 5,367,495 ("the '495 Reference") or U.S. Patent No. 4,759,021 ("the '021 Reference") or U.S. Patent No. 5,036,494 ("the '494 Reference").

	"A READ instruction loads the address of the memory register to be read from the instruction register 4 into an 8-bit address register 7. The data from the accessed storage register is then transferred in parallel to data shift register 5 via the sense amplifiers 6 and then clocked out serially to the Data-Out pin DO." ['885 Reference, Col. 4:16-22; *see also*, Figs. 1 and 2] To the extent AMD reads this limitation on the Samsung devices, this limitation is met by the '885 patent. The '937 Reference states: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42] The '495 Reference states: "The register 70a, 70b, 70c or 70d selected by the block decoder 50 holds 8-bit address codes ARC0-ARC7 supplied in synchronism with the row selection signal RAS. Since the holding of the address codes ARC0-ARC7 will be maintained even after access is shifted to another cell array block, these registers 70a-70d store respectively the address codes ARC0-

	ARC7 of the last access in the cell array blocks 10a-10d and supply them to the selectors 80a-80d which also receive the address codes ARC0-ARC7 supplied in synchronism with the row selection signal RAS and introduce them to the row decoders 20a-20d." ['495 Reference, Col. 4:25-37] The '021 Reference states: "Since the low-speed large-capacity memories 11, 12, 13, 14 performing the 4-way interleave operation are shifted in access timing usually by one cycle from each other, the memories 11 14 are provided respectively with registers 23 26 each for holding an address." ['021 Reference, Col. 4:5-9]. The '494 Reference states: "The row decoder 40 is controlled by a row counter 45. The latch and word line drivers 41 and 42 are controlled by pulse generators 46 and 47 respectively." ['494 Reference, Col. 8:14-17]
a plurality of row decoders, each row decoder for activating a portion of a row identified by signals from one of said first registers;	This elements is met by the '885 Reference in combination with any of the '937 Reference or the '495 Reference or the '021 Reference or the '494 Reference. The '937 Reference teaches the use of a plurality of decoders as well as the use of a single decoder for performing the same function. [Figs. 3 and 5] The '937 Reference states: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 82

	are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42] "The latch (see FIG. 6) forming the delay latch circuit 106 fetches the outputs from the X decoder 82 on the leading edges of the clock pulses $Ø_L$, and hence the delay latch circuit 106 delays the outputs from the X decoder 82 respectively by one cycle of the basic clock pulses $Ø_S$ to transfer the same to the second memory cell array 94. . . . It is to be noted that odd address cycles are always delayed from the even address cycles respectively by one cycle of the basic clock pulses $Ø_S$. Thus, this embodiment is equivalent in operation to that shown in FIG. 3" ['937 Reference, Col. 7:44-63] The '495 Reference states: "The output of the block decoder 50 is supplied in common to the row decoders 20a and 20d and the column decoders 40a and 40d. As a result, one word line is selected in the memory cell array block 10a, for example." ['495 Reference, Col. 3:39-42] The '021 Reference states: "In FIG. 1, numeral 100 designates clock signals to be supplied to the interleave controller 20, the select controller 30 and the high-speed memory access controller 40, numerals 111, 112,

	113, 114 designate output data from the low-speed large-capacity memories 11, 12, 13, 14 respectively, numeral 120 designates an address signal to be supplied to the interleave controller 20, numerals 121, 122, 123, 124 designate address signals from the interleave controller 20 to the low-speed large-capacity memories 11, 12, 13, 14 respectively, …." ['021 Reference, Col. 3:43-68] Each memory 11, 12, 13, and 14 would have a decoder for receiving an address from interleave controller 20. The '494 Reference states: "The row decoder 40 is controlled by a row counter 45. The latch and word line drivers 41 and 42 are controlled by pulse generators 46 and 47 respectively." ['494 Reference, Col. 8:14-17] "The row address that is being used by an active array is stored in the latch 41 and 42 and the address on the output 51 of the row counter 45 is the address of the next row that will be used." ['494 Reference, Col. 9:37-40] "It will be appreciated that by use of the latches 41 and 42, the row decoder 40 may hold an address which is latched for both memory blocks 14 and 15 but when data transfers have been effected by selective addressing within array 0 the swap array condition will enable row decoder 40 to advance to the next required row address array 0 while latches 42 hold the existing row address for the addressing which will now occur in array 1 in the same row as just used for addressing in array 0." ['494 Reference, Col. 12:56-65]

one or more sense amplifiers for amplifying contents of said memory locations in the row portions; and	This element is met by the '885 Reference. Specifically, the '885 Reference states: "A READ instruction loads the address of the memory register to be read from the instruction register 4 into an 8-bit address register 7. The data from the accessed storage register is then transferred in parallel to data shift register 5 via the sense amplifiers 6 and then clocked out serially to the Data-Out pin DO." ['885 Reference, Col. 4:16-22; *see also*, Figs. 1 and 2]
an output for providing output signals from said sense amplifiers,	This element is met by the '885 Reference. Specifically, the '885 Reference states: "A READ instruction loads the address of the memory register to be read from the instruction register 4 into an 8-bit address register 7. The data from the accessed storage register is then transferred in parallel to data shift register 5 via the sense amplifiers 6 and then clocked out serially to the Data-Out pin DO." ['885 Reference, Col. 4:16-22; *see also*, Figs. 1 and 2]
wherein at least two locations L1 and L2 in different rows having different row addresses in said memory can be read out to said output in burst mode such that the memory receives an address of one of said locations and provides in response contents of a plurality of memory locations, including the locations L1 and L2, in the sequence of consecutive addresses, so that while one of said row decoders is activating a row portion comprising said location L1 and contents of said location L1 are being transferred from one or more of said sense amplifiers to said output, another one of said row decoders is activating a row portion comprising said location L2 and contents of said location L2 are being transferred from said	This element is met by the '885 Reference in combination with the '494 Reference or U.S. Patent No. 4,875,196 ("the '196 Reference"). Specifically, the '885 Reference states: "After the last memory address is reached, the access automatically rolls over to the first address." ['885 Reference, Col. 3:1-3] "A method as in claim 5 wherein the sequence of incremented addresses wraps around when the address of the Nth register is reached such that all N registers in the array are read." ['885

location L2 to one or more of said sense amplifiers.	Reference, Col. 7:45-48] Further, the feature of transferring the contents of location L from a plurality of sense amplifier circuits to the output while the contents of another location to be read out after the location L are provided to the plurality of sense amplifiers circuits for amplification was well known in the art. The following are illustrative: The '494 Reference states: "The selection of memory locations forming each cyclic pattern of addressing is controlled by the control unit 13. The row counter 45 and column counter 44 are connected so that unless instructed by the control 13 to do otherwise they count through successive addresses along each row and then row by row." ['494 Reference, Col. 8:22-27] "Consequently after reaching address 0 the column and row counters cycle sequentially along each row for the two memory blocks in turn (starting at column zero of row 0 in array 0) using all memory locations in each row and then moving to the next row and repeating the operation." ['494 Reference, Col. 11:26-31] "addressing sequentially more than one memory location in said first memory block and effecting a data transfer for each memory location addressed, and at the same time effecting an equate operation on bit lines in said second memory block; and after addressing memory locations in said first memory block, switching said addressing and equate operation so as to address sequentially more than one memory location in said second memory block and effecting a data transfer for each memory

	location addressed and at the same time equating bit lines in said first memory block." ['494 Reference, Col. 13:36-48] The '196 Reference states that: "In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit lines in the other array are being precharged. Thus, as data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit lines in that array will already have been initialied." ['196 Reference, 2:60-67] "In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and settling transient signals) in preparation for the next access form such other array. Therefore, precharging items for one array overlap the time for performing read or write operation in the other array, and therefore do not limit operating speed." ['196 Reference, Col. 3:41-47]
2. The memory of claim 1, said memory having a random mode in which the memory receives an address and provides in response the contents of a unique memory location,	This element is met by the '885 Reference. Specifically, the '885 patent states: "The circuit provides both random and sequential access functions and allows the memory to be used as a shift register of variable length." ['885 Reference, Page 1]
wherein, both in burst mode and in random mode, while the contents of said location L1 are being transferred from one or more of said sense amplifiers to said output, the contents of said location L2 are being transferred from said location L2 to one or more of	It would be obvious to a person of skill in the art that transferring the contents of a location L1 from one of the sense amplifiers to the output while the contents of a location L2 are transferred from the location L2 to one or more sense amplifiers

said sense amplifiers.	could be used in either a burst mode or a random mode. *See* claim 1 above. Further, to the extent AMD reads this limitation on the Samsung devices, this limitation is met by numerous prior art references having both a random access mode and a burst mode.
3. The memory of claim 1 wherein when the locations L1 and L2 are read out in burst mode and when the contents of said location L1 are being transferred from one or more of said sense amplifiers to said output and the contents of said location L2 are being transferred from said location L2 to one or more of said sense amplifiers, the sense amplifiers from which the contents of said location L1 are being transferred are enabled and the sense amplifiers to which the contents of said location L2 are being transferred are disabled, but these latter sense amplifiers become enabled subsequently for amplifying the contents of said location L2.	This element is met in the '885 Reference in combination with any of EP 0 087 754 B1 ("the '754 Reference") or U.S. Patent No. 4,937,788 ("the '788 Reference") or the '937 Reference or U.S. Patent No. 5,263,003 ("the '003 Reference") or U.S. Patent No. 5,251,178 ("the '178 Reference"). The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58] The '788 Reference states:

	"According to this arrangement, only one plane is selected in accordance with the content of the upper-order two bits of the row address. The selected plane is activated and exhibits the memory operation but the rest of the planes which are under the non-selection state are inoperative. Therefore, the decoders and the sense amplifiers are inoperative in these inoperative planes and the memory is not refreshed. Therefore, power is consumed in only the selected plane and unnecessary power consumption in the other plane can be saved. Thus, the requirement for low power consumption can be satisfied." ['788 Reference, Col. 5:57-68] The '937 Reference states: "The sense amplifier 86 is controlled by the signals SE_{EV} to amplify the read data thereby to supply the same to the data latch 87, which in turn temporarily stores the outputs from the sense amplifiers 86. When the signals SE_{EV} are at low levels, the data latch 87 is electrically cut off from the sense amplifier 86. Data from the data latch 87 are transferred to the output latch 89 when the signals OE_{EV} are at high levels. In a similar manner, the sense amplifier 96 is controlled by the signals SE_{OD} to amplify the read data thereby to supply the same to the data latch 97, which in turn temporarily stores the outputs from the sense amplifier 96. When the signals SE_{OD} are at low levels, the data latch 97 is electrically cut off from the sense amplifier 96." ['937 Reference, Col. 4:52-66] The '003 Reference states: "The flash memory control 88 also selectively enables one of

	two sets of bi-directional data buffers 90 and 91 which respectively couple the bank data buses 82 and 83 to the processor section data bus 63. The bank data buses 82 and 83 can be coupled to the instruction bus 61 by the flash memory control 88 selectively enabling buffers 92 and 93, respectively." ['003 Reference, Col. 9:21-27] The '178 Reference states: "Referring now to FIG. 2, the circuit of FIG. 1 has been modified to utilize the fact that, when RA10=1, only one half of the ARRAY BANKs 20 are being utilized and that, when RA10=0, the other half of the ARRAY BANKs 20 are being utilized. In particular, the RA 10 address is used to cause only the half of the ARRAY BANKs 20 that are being utilized to draw power from the DRAM energy source during read/write operations, while at the same time permitting the periodic performance of the refresh cycle in the usual manner on all ARRAY BANKs." ['178 Reference, Col. 3:32-42]
4. The memory of claim 1 wherein:	
said memory comprises k pluralities S-1, . . . , S-k of locations wherein k is a number of said pluralities and is greater than or equal to two; for each plurality S-i, said sense amplifiers can receive simultaneously the contents of number m of locations from said plurality S-i, wherein m is a positive integer; and	This limitation is met by the '885 Reference in combination with the '754 Reference or the '494 Reference. The '738 Reference states: "In accordance with the above objects, there are provided a first and a second set of memory cells, a column decoder, a row decoder, a pair of column shift registers for addressing the column address lines, a pair of row shift registers for addressing the row address lines, a multiplexer having a first and a second

	input coupled to the data output lines of the first and second sets, respectively, a data register and means for shifting the shift registers and switching the multiplexer between its first and second inputs." ['738 Reference, Col. 1:43-52; *see also* Fig. 1] The '754 Reference states: "4x2(n-1) (n: a positive integer) memory blocks, each of which includes a plurality of cells substantially arranged in a matrix form, and a plurality of word lines and data lines coupled to said memory cells; … a plurality of sense amplifying means responsive to a control signal input thereto, for selectively activating one sense amplifying means to sense and amplify data on said selected data lines of one of said two column-selected memory blocks, and for selectively activating at least one other sense amplifying means to refresh data of said each memory cell along said selected word lines …." ['754 Reference, Page 4:1-10] The '494 Reference states: "The bit lines are each connected to column multiplexing circuitry 37 for each column and coupled to sense amplifier and coupled to sense amplifier and write circuitry 38 for each column. Each sense amplifier and write circuit is connected through a bus driver circuit 39 to the data output 17. Each memory block 14 and 15 has 70 rows each having a word line 25. The word lines are connected to a row decoder 40. The row decoder is coupled to memory block 14 through a latch and word line driver 41 and to the memory block 15 through a latch and word line driver 42. The column multiplex circuitry 37 is controlled by a column counter 44. The row decoder 40 is

	controlled by a row counter 45. The latch and word line drivers 41 and 42 are controlled by pulse generators 46 and 47 respectively." ['494 Reference, Col. 8:3-17]
time tARA does not exceed m * (k-1) * (tOE), wherein: tARA is measured from the time that an address of a location is made available to said memory to the time when one or more of said sense amplifiers develop an output signal indicative of the contents of said location; and tOE is the time to transfer an output of any one of said sense amplifiers to said output of said memory.	A person of skill in the art would know that this timing relationship would be used when designing the memory disclosed in claim 1.
5. The memory of claim 1	
wherein, in burst mode, a time in which each location of said plurality except said one of said locations is read out to said output after a previous location has been read out to said output is shorter than a time in which said one of said locations is read out to said output after said address of said one of said locations has been received by said memory.	This element is met for the '885 Reference alone or in combination with JP-02-282994-A ("the '994 Reference") or U.S. Patent No. 4,918,587 ("the '587 Reference") or the '003 Reference or U.S. Patent No. 4,799,199 ("the '199 Reference"). The '885 Reference states: "Circuitry for serial read memory access utilizing a random starting address. Fast read access is provided without upsetting the original data pattern stored in the memory core if the sequential read is terminated in midstream." ['885 Reference, Page 1] The '994 Reference states: "For that reason, even if the address moves serially to the next row and changes, the data itself will be read at high speed t_0. As is evident from the explanation above, as long as serial access

	continues, the internal data can continue to be read at high speed." ['994 Reference, Page 4, Column 1] "In the specifications, the address access time t_1 is estimated at 150 ns, and t_0 is estimated at the level of 30 ns for simple determination at the number of steps of the gates. In a hypothesis of the worst-case scenario for the current jump command +1 instruction, the jump command would be 3 bytes for the operand +2 data, 1 instruction would be 1 byte. Therefore, the average access time is {150 ns x 1 + 30 ns x 3}/4 = 60 ns. In contrast, the access time is 150 ns when the invention is not used." ['994 Reference, Page 4, Column 2] The '587 Reference states: "The reduction in the memory access cycle time from a convention memory access operation, generally represented by the first prefetch with a three clock cycle span between event t1 and t2, is clearly evident when the times are compared to those of the consecutive prefetch operation extending for two clock cycles between corresponding time intervals t3 and t4. Time t2 and t4 identify the first clock interval suitable to initiate succeeding memory access operations." ['587 Reference, Col. 5:63-6:3] The '003 Reference states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus

	buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer. Typically, the access addresses of these 'extra' storage cells differ from the original access address by only one or two bits. However, subsequent accesses to these cells can be accomplished by simply executing additional access cycles without changing the access address. In the art, such memories are referred to as 'nibble mode'. In some other integrated circuit memories, a portion of the original address can be 'assumed' for one (or more) subsequent accesses, so that only the least significant portion of the address needs to be decoded, etc. Thus, once the original access had been

	completed, subsequent accesses to 'related' storage cells will be significantly quicker." ['199 Reference, Col. 1:13-28]
6. The memory of claim 1 wherein said memory is fabricated in an integrated circuit.	This element is met by the '885 Reference alone or in combination with any of the '754 Reference or the '199 Reference, or U.S. Patent No. 4,899,312 ("the '312 Reference"). The '885 Reference states: "The present invention relates to integrated circuits and, in particular, to circuitry which provides fast read access in serial memories utilizing random starting address." ['885 Reference, Col. 1:6-9] The '754 Reference states: "The present invention relates to a semiconductor dynamic memory device. Mass-production of 64K bit dynamic type random access memory devices (DRAMs) has been enabled by the recent development of semiconductor memory devices of high packing density. Furthermore, a 256K bit DRAM has been developed." ['754 Reference, Page 2:3-6] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer." ['199 Reference, Col. 1:13-16] The '312 Reference states: "The individual circuit elements constructing the RAM of the

	present embodiment are formed on a semiconductor substrate such as a piece of single-crystalline silicon by the known technique for fabricating a CMOS (i.e., Complementary MOS) integrated circuit." ['312 Reference, Col. 2:34-38]
7. The memory of claim 1 further comprising:	
a plurality of second registers, each second register for receiving at least a portion of a column address; and	This element is met by the '885 Reference in combination with the '937 Reference. The '937 Reference states that: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e. twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. Ina similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e. twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42]
a circuitry for each second register for selecting in response to signals from one of the second registers a plurality of columns to be read by the sense amplifiers.	This element is met in the '937 Reference. Specifically, the '937 Reference states: "Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied

	to a transfer gate 85.... In a similar manner, the transfer gate 95 transfers data read from the second memory cell array 94 to the sense amplifier 96 through an I/O line 103, while transferring data from the write circuit 98 received through the I/O line 103 to the second memory cell array 94." ['937 Reference, Col. 4:33-52]
8. A memory comprising:	Although a preamble is normally not limiting, should this preamble be limiting, this element is met by the '885 Reference. Specifically, the '885 Reference is titled "Sequential read access of serial memories with user defined starting address."
a set of consecutively addressed memory locations L1, . . . Ln;	This element is met by the '885 Reference. Specifically, the '885 Reference states: "An embodiment of circuitry for sequential read access of a serial memory array in accordance with the present invention comprises an address latch which stores an address used to access the memory array to read data from a corresponding data register in the array. The address latch includes a counter which increments the stored address upon receipt of an address increment signal." ['885 Reference, Col. 3:7-14; *see also* Fig. 3]
a plurality of sense amplifier circuits for amplifying contents of said memory locations; and	This element is met by the '885 Reference. Specifically, the '885 Reference states: "A READ instruction loads the address of the memory register to be read from the instruction register 4 into an 8-bit address register 7. The data from the accessed storage register is then transferred in parallel to data shift register 5 via the sense amplifiers 6 and then clocked out serially to the Data-Out pin

	DO." ['885 Reference, Col. 4:16-22; *see also*, Figs. 1 and 2]
an output for providing output signals from said plurality of sense amplifier circuits,	This element is met by the '885 Reference. Specifically, the '885 Reference states: "A READ instruction loads the address of the memory register to be read from the instruction register 4 into an 8-bit address register 7. The data from the accessed storage register is then transferred in parallel to data shift register 5 via the sense amplifiers 6 and then clocked out serially to the Data-Out pin DO." ['885 Reference, Col. 4:16-22; *see also*, Figs. 1 and 2]
wherein said memory has a burst mode operation for receiving an address and reading out to said output, in response to said address, any given number of memory locations in the sequence of consecutive addresses with wrap around so that the next location, if any, to be read out after said location Ln is said location L1, such that during said operation while the contents of any location L to be read out other than the last location to be read out are being transferred from said plurality of sense amplifier circuits to said output, the contents of another location to be read out after said location L are being provided to said plurality of sense amplifier circuits for amplification and subsequent transfer to said output, and	This element is met by the '885 Reference in combination with the '494 Reference or the '196 Reference. Specifically, the '885 Reference states: "After the last memory address is reached, the access automatically rolls over to the first address." ['885 Reference, Col. 3:1-3] "A method as in claim 5 wherein the sequence of incremented addresses wraps around when the address of the Nth register is reached such that all N registers in the array are read." ['885 Reference, Col. 7:45-48] The '494 Reference states: "The selection of memory locations forming each cyclic pattern of addressing is controlled by the control unit 13. The row counter 45 and column counter 44 are connected so that unless instructed by the control 13 to do otherwise they count through successive addresses along each row and then row by row."

	['494 Reference, Col. 8:22-27] "Consequently after reaching address 0 the column and row counters cycle sequentially along each row for the two memory blocks in turn (starting at column zero of row 0 in array 0) using all memory locations in each row and then moving to the next row and repeating the operation." ['494 Reference, Col. 11:26-31] "addressing sequentially more than one memory location in said first memory block and effecting a data transfer for each memory location addressed, and at the same time effecting an equate operation on bit lines in said second memory block; and after addressing memory locations in said first memory block, switching said addressing and equate operation so as to address sequentially more than one memory location in said second memory block and effecting a data transfer for each memory location addressed and at the same time equating bit lines in said first memory block." ['494 Reference, Col. 13:36-48] The '196 Reference states that: "In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit lines in the other array are being precharged. Thus, as data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit lines in that array will already have been initialied." ['196 Reference, Col. 2:60-67] "In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and

	settling transient signals) in preparation for the next access form such other array. Therefore, precharging times for one array overlap the time for performing read or write operation in the other array, and therefore do not limit operating speed." ['196 Reference, 3:41-47]
wherein said memory further comprises a control circuit for selectively enabling said sense amplifier circuits so that said control circuit enables a sense amplifier circuit whose output signals are being transferred to the output of said memory but said control circuit does not enable all said sense amplifier circuits at the same time.	This element is met in the '885 Reference in combination with any of the '754 Reference or the '788 Reference or the '937 Reference or the '003 Reference or the '178 Reference. The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58] The '788 Reference states: "According to this arrangement, only one plane is selected in accordance with the content of the upper-order two bits of the

	row address. The selected plane is activated and exhibits the memory operation but the rest of the planes which are under the non-selection state are inoperative. Therefore, the decoders and the sense amplifiers are inoperative in these inoperative planes and the memory is not refreshed. Therefore, power is consumed in only the selected plane and unnecessary power consumption in the other plane can be saved. Thus, the requirement for low power consumption can be satisfied." ['788 Reference, Col. 5:57-68] The '937 Reference states: "The sense amplifier 86 is controlled by the signals SE_{EV} to amplify the read data thereby to supply the same to the data latch 87, which in turn temporarily stores the outputs from the sense amplifiers 86. When the signals SE_{EV} are at low levels, the data latch 87 is electrically cut off from the sense amplifier 86. Data from the data latch 87 are transferred to the output latch 89 when the signals OE_{EV} are at high levels. In a similar manner, the sense amplifier 96 is controlled by the signals SE_{OD} to amplify the read data thereby to supply the same to the data latch 97, which in turn temporarily stores the outputs from the sense amplifier 96. When the signals SE_{OD} are at low levels, the data latch 97 is electrically cut off from the sense amplifier 96." ['937 Reference, Col. 4:52-66] The '003 Reference states: "The flash memory control 88 also selectively enables one of two sets of bi-directional data buffers 90 and 91 which respectively couple the bank data buses 82 and 83 to the processor section data bus 63. The bank data buses 82 and 83

	can be coupled to the instruction bus 61 by the flash memory control 88 selectively enabling buffers 92 and 93, respectively." ['003 Reference, Col. 9:21-27] The '178 Reference states: "Referring now to FIG. 2, the circuit of FIG. 1 has been modified to utilize the fact that, when RA10=1, only one half of the ARRAY BANKs 20 are being utilized and that, when RA10=0, the other half of the ARRAY BANKs 20 are being utilized. In particular, the RA 10 address is used to cause only the half of the ARRAY BANKs 20 that are being utilized to draw power from the DRAM energy source during read/write operations, while at the same time permitting the periodic performance of the refresh cycle in the usual manner on all ARRAY BANKs." ['178 Reference, Col. 3:32-42]
9. The memory of claim 8 wherein, during said operation, said control circuit enables at the same time only:	
(1) the sense amplifier circuit whose output signals are being transferred to said output of said memory, and	This limitation is met by the '885 Reference in combination with the '754 Reference. The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption

	and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58] "A semiconductor dynamic memory device comprising: … a plurality of sense amplifying means (18-1 to 18-4; SA1 to SA8) responsive to a control signal input thereto, for selectively activating one sense amplifying means to sense and amplify data on said selected data lines of one of said two column-selected memory blocks, and for selectively activating at least one other sense amplifying means to refresh data to said each memory cell along said selected word lines; …." ['754 Reference, Page 6:53-7:5]
(2) a predetermined number of other sense amplifier circuits whose output signals will be transferred next to said output of said memory if said operation continues sufficiently long.	This limitation is met by the '885 Reference in combination with the '754 Reference. The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly

	reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58] "A semiconductor dynamic memory device comprising: … a plurality of sense amplifying means (18-1 to 18-4; SA1 to SA8) responsive to a control signal input thereto, for selectively activating one sense amplifying means to sense and amplify data on said selected data lines of one of said two column-selected memory blocks, and for selectively activating at least one other sense amplifying means to refresh data to said each memory cell along said selected word lines; …." ['754 Reference, Page 6:53-7:5]
10. The memory of claim 7 wherein:	
said set of locations comprises k subsets S-1, . . . , S-k wherein k is greater than or equal to two, such that, for a positive integer m and for any subset S-i, the contents of m consecutively addressed locations from said subset S-i can be transferred simultaneously to said plurality of sense amplifier circuits; and	This limitation is met by the '885 Reference in combination with the '754 Reference or the '494 Reference. The '754 Reference states: "4x2(n-1) (n: a positive integer) memory blocks, each of which includes a plurality of cells substantially arranged in a matrix form, and a plurality of word lines and data lines coupled to said memory cells; … a plurality of sense amplifying means responsive to a control signal input thereto, for selectively activating one sense amplifying means to sense and amplify data on said selected data lines of one of said two column-selected memory blocks, and for selectively activating at least one other

	sense amplifying means to refresh data of said each memory cell along said selected word lines ...." ['754 Reference, Page 4:1-10] The '494 Reference states: "The bit lines are each connected to column multiplexing circuitry 37 for each column and coupled to sense amplifier and coupled to sense amplifier and write circuitry 38 for each column. Each sense amplifier and write circuit is connected through a bus driver circuit 39 to the data output 17. Each memory block 14 and 15 has 70 rows each having a word line 25. The word lines are connected to a row decoder 40. The row decoder is coupled to memory block 14 through a latch and word line driver 41 and to the memory block 15 through a latch and word line driver 42. The column multiplex circuitry 37 is controlled by a column counter 44. The row decoder 40 is controlled by a row counter 45. The latch and word line drivers 41 and 42 are controlled by pulse generators 46 and 47 respectively." ['494 Reference, Col. 8:3-17]
in said operation, time tARA does not exceed m * (k-1) * (tOE), wherein: tARA is measured from the time that an address of the first location to be read out in said operation is made available to said memory to the time when said plurality of sense amplifier circuits develops an output signal indicative of the contents of said first location; and tOE is the time to transfer the contents of any one of said locations from said plurality of sense amplifier circuits to said output.	A person of skill in the art would know that this timing relationship would be used when designing the memory disclosed in claim 1.

11. The memory of claim 8 wherein, in said operation, each location to be read out except the first location to be read out is read out to said output in a shorter time than the first location to be read out.	This element is met for the '885 Reference alone or in combination with the '994 Reference or the '587 Reference or the '003 Reference or the '199 Reference. The '885 Reference states: "Circuitry for serial read memory access utilizing a random starting address. Fast read access is provided without upsetting the original data pattern stored in the memory core if the sequential read is terminated in midstream." ['885 Reference, Page 1] The '994 Reference states: "For that reason, even if the address moves serially to the next row and changes, the data itself will be read at high speed t_0. As is evident from the explanation above, as long as serial access continues, the internal data can continue to be read at high speed." ['994 Reference, Page 4, Column 1] "In the specifications, the address access time t_1 is estimated at 150 ns, and t_0 is estimated at the level of 30 ns for simple determination at the number of steps of the gates. In a hypothesis of the worst-case scenario for the current jump command +1 instruction, the jump command would be 3 bytes for the operand +2 data, 1 instruction would be 1 byte. Therefore, the average access time is {150 ns x 1 + 30 ns x 3}/4 = 60 ns. In contrast, the access time is 150 ns when the invention is not used." ['994 Reference, Page 4, Column 2] The '587 Reference states: "The reduction in the memory access cycle time from a

	convention memory access operation, generally represented by the first prefetch with a three clock cycle span between event t1 and t2, is clearly evident when the times are compared to those of the consecutive prefetch operation extending for two clock cycles between corresponding time intervals t3 and t4. Time t2 and t4 identify the first clock interval suitable to initiate succeeding memory access operations." ['587 Reference, Col. 5:63-6:3] The '003 Reference states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the

	second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer. Typically, the access addresses of these 'extra' storage cells differ from the original access address by only one or two bits. However, subsequent accesses to these cells can be accomplished by simply executing additional access cycles without changing the access address. In the art, such memories are referred to as 'nibble mode'. In some other integrated circuit memories, a portion of the original address can be 'assumed' for one (or more) subsequent accesses, so that only the least significant portion of the address needs to be decoded, etc. Thus, once the original access had been completed, subsequent accesses to 'related' storage cells will be significantly quicker." ['199 Reference, Col. 1:13-28]
12. The memory of claim 8 wherein the sequence of locations L1, . . . , Ln is a sequence of increasing order of addresses.	This limitation is met by the '885 Reference. Specifically, the '885 Reference states: "An embodiment of circuitry for sequential read access of a serial memory array in accordance with the present invention comprises an address latch which stores an address used to access the memory array to read data from a corresponding data register in the array. The address latch includes a counter which increments the stored address upon receipt of an address increment signal." ['885 Reference, Col. 3:7-14; *see also* Fig. 3]
13. The memory of claim 7 wherein in said operation any number	This element is met by the '885 Reference. Specifically, the

of said locations addressed consecutively with wrap around can be read out to said output so that:	'885 Reference states: "After the last memory address is reached, the access automatically rolls over to the first address." ['885 Reference, Col. 3:1-3] "A method as in claim 5 wherein the sequence of incremented addresses wraps around when the address of the Nth register is reached such that all N registers in the array are read." ['885 Reference, Col. 7:45-48] "An embodiment of circuitry for sequential read access of a serial memory array in accordance with the present invention comprises an address latch which stores an address used to access the memory array to read data from a corresponding data register in the array. The address latch includes a counter which increments the stored address upon receipt of an address increment signal." ['885 Reference, Col. 3:7-14]
the first location to be read out in said operation is read out to said output after time tARA+tOE wherein: tARA is measured from the time that an address of said first location is made available to said memory to the time when said plurality of sense amplifier circuits develops an output signal indicative of the contents of said first location; and tOE is the time to transfer the contents of any one of said locations from said plurality of sense amplifier circuits to said output of said memory; and	This element is met by the '885 Reference alone or in combination with any of the '994 Reference or the '587 Reference or the '003 Reference or the '199 Reference. The '885 Reference states: "An embodiment of circuitry for sequential read access of a serial memory array in accordance with the present invention comprises an address latch which stores an address used to access the memory array to read data from a corresponding data register in the array. The address latch includes a counter which increments the stored address upon receipt of an address increment signal." ['885 Reference, Col. 3:7-14]

	The '994 Reference states: "For that reason, even if the address moves serially to the next row and changes, the data itself will be read at high speed t_0. As is evident from the explanation above, as long as serial access continues, the internal data can continue to be read at high speed." ['994 Reference, Page 4, Column 1] "In the specifications, the address access time t_1 is estimated at 150 ns, and t_0 is estimated at the level of 30 ns for simple determination at the number of steps of the gates. In a hypothesis of the worst-case scenario for the current jump command +1 instruction, the jump command would be 3 bytes for the operand +2 data, 1 instruction would be 1 byte. Therefore, the average access time is {150 ns x 1 + 30 ns x 3}/4 = 60 ns. In contrast, the access time is 150 ns when the invention is not used." ['994 Reference, Page 4, Column 2] The '587 Reference states: "The reduction in the memory access cycle time from a convention memory access operation, generally represented by the first prefetch with a three clock cycle span between event t1 and t2, is clearly evident when the times are compared to those of the consecutive prefetch operation extending for two clock cycles between corresponding time intervals t3 and t4. Time t2 and t4 identify the first clock interval suitable to initiate succeeding memory access operations." ['587 Reference, Col. 5:63-6:3] The '003 Reference states: "The consecutive program instructions are read alternately from

	the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer. Typically, the access addresses of these 'extra' storage cells differ from the original access address by only one or two bits. However, subsequent accesses to these cells can be accomplished by simply executing additional access cycles without changing the access address. In

	the art, such memories are referred to as 'nibble mode'. In some other integrated circuit memories, a portion of the original address can be 'assumed' for one (or more) subsequent accesses, so that only the least significant portion of the address needs to be decoded, etc. Thus, once the original access had been completed, subsequent accesses to 'related' storage cells will be significantly quicker." ['199 Reference, Col. 1:13-28]
every other location to be read out in said operation is read out to said output within time tOE.	This element is met by the '885 Reference alone or in combination with any of the '994 Reference or the '587 Reference or the '003 Reference or the '199 Reference. The '885 Reference states: "An embodiment of circuitry for sequential read access of a serial memory array in accordance with the present invention comprises an address latch which stores an address used to access the memory array to read data from a corresponding data register in the array. The address latch includes a counter which increments the stored address upon receipt of an address increment signal." ['885 Reference, Col. 3:7-14] The '994 Reference states: "For that reason, even if the address moves serially to the next row and changes, the data itself will be read at high speed t_0. As is evident from the explanation above, as long as serial access continues, the internal data can continue to be read at high speed." ['994 Reference, Page 4, Column 1] "In the specifications, the address access time t_1 is estimated at 150 ns, and t_0 is estimated at the level of 30 ns for simple determination at the number of steps of the gates. In a

	hypothesis of the worst-case scenario for the current jump command +1 instruction, the jump command would be 3 bytes for the operand +2 data, 1 instruction would be 1 byte. Therefore, the average access time is {150 ns x 1 + 30 ns x 3}/4 = 60 ns. In contrast, the access time is 150 ns when the invention is not used." ['994 Reference, Page 4, column 2] The '587 Reference states: "The reduction in the memory access cycle time from a conventional memory access operation, generally represented by the first prefetch with a three clock cycle span between event t1 and t2, is clearly evident when the times are compared to those of the consecutive prefetch operation extending for two clock cycles between corresponding time intervals t3 and t4. Time t2 and t4 identify the first clock interval suitable to initiate succeeding memory access operations." ['587 Reference, Col. 5:63-6:3] The '003 Reference states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to

	obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer. Typically, the access addresses of these 'extra' storage cells differ from the original access address by only one or two bits. However, subsequent accesses to these cells can be accomplished by simply executing additional access cycles without changing the access address. In the art, such memories are referred to as 'nibble mode'. In some other integrated circuit memories, a portion of the original address can be 'assumed' for one (or more) subsequent accesses, so that only the least significant portion of the address needs to be decoded, etc. Thus, once the original access had been completed, subsequent accesses to 'related' storage cells will be significantly quicker." ['199 Reference, Col. 1:13-28]
14. The memory of claim 8 wherein said memory is fabricated in an integrated circuit.	This element is met by the '885 Reference alone or in combination with any of the '754 Reference or the '199

	Reference or the '312 Reference. The '885 Reference states: "The present invention relates to integrated circuits and, in particular, to circuitry which provides fast read access in serial memories utilizing random starting address." ['885 Reference, Col. 1:6-9] The '754 Reference states: "The present invention relates to a semiconductor dynamic memory device. Mass-production of 64K bit dynamic type random access memory devices (DRAMs) has been enabled by the recent development of semiconductor memory devices of high packing density. Furthermore, a 256K bit DRAM has been developed." ['754 Reference, Page 2:3-6] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer." ['199 Reference, Col. 1:13-16] The '312 Reference states: "The individual circuit elements constructing the RAM of the present embodiment are formed on a semiconductor substrate such as a piece of single-crystalline silicon by the known technique for fabricating a CMOS (i.e., Complementary MOS) integreated circuit." ['312 Reference, Col. 2:34-38]