EXHIBIT 1

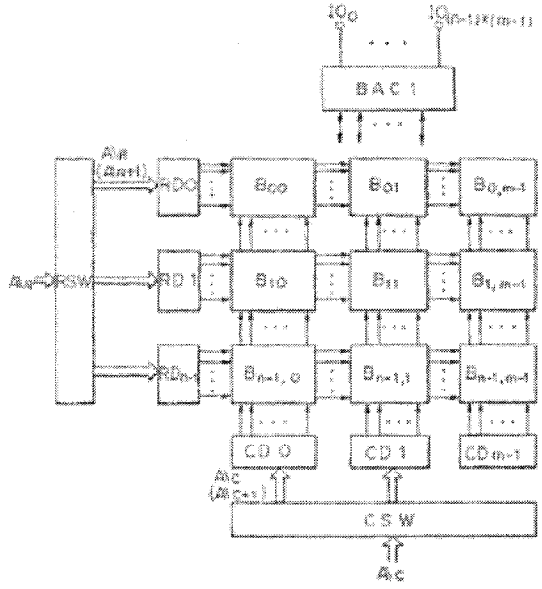
D12 Pages 1-31

Appendix D12
Defendants and Counterclaimants' Invalidity Contentions
Advanced Micro Devices, Inc., et al., v. Samsung Electronics Co., Ltd., et al., Case No. 3:08-CV-0986-SI

U.S. Patent No. 5,559,990 Invalidity Chart: U.S. Patent No. 4,811,297 ("the '297 Reference")

All asserted claims are anticipated by the '297 Reference and/or are rendered obvious by it, either alone or in combination with other prior art described below and/or listed in Section I of Defendants' and Counterclaimants' Preliminary Invalidity Contentions and/or through modifications described below. Nothing in this invalidity chart should be construed as signifying or suggesting Defendants and Counterclaimants' adoption of or acquiescence in any claim scope and/or claim construction positions taken by Plaintiffs and Counterdefendants in this litigation.

CLAIM	RESPONSE
1. A memory comprising:	Although a preamble is normally not limiting, should this preamble be limiting, this element is met in U.S. Patent No. 4,811,297 ("the '297 Reference"). Specifically, the '297 Reference is titled "Boundary-Free Semiconductor Memory Device."
a plurality of rows of memory locations;	This element is met in the '297 Reference. Specifically, the '297 Reference states that: "An entire chip is divided into N blocks (N = n x m) in accordance with a desired rectangular group of bits (n x m bits). The same row decoder is provided for every m blocks, and a row address $\bar{A}_r$ or a row address $\bar{A}_{r+1}$ adjacent thereto is given to the row decoders. * * * N bits of memory cells are accessed from the blocks, and the accessed memory cells are rearranged, thereby obtaining a desired rectangular group of bits." ['297 Reference, Abstract]. See, e.g., Figs. 6, 7, 21, 22.

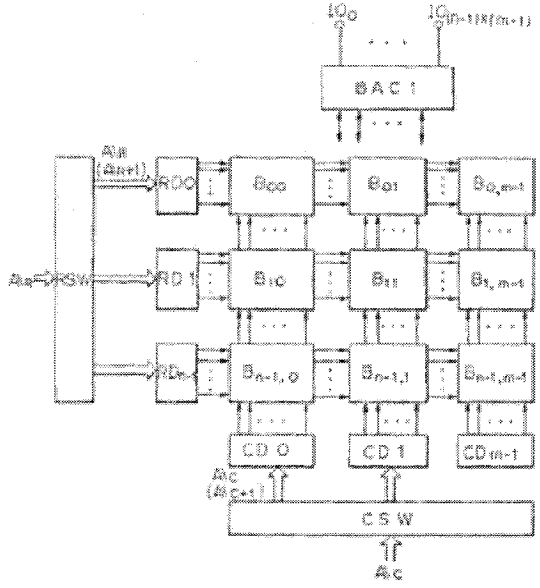
CLAIM	RESPONSE
	Fig. 6 
a plurality of first registers, each first register for receiving a row address;	This element is met in the '297 Reference alone or in combination with any of U.S. Patent No. 4,849,937 ("the '937 Reference") or U.S. Patent No. 5,367,495 ("the '495 Reference") or U.S. Patent No. 4,759,021 ("the '021 Reference"). Specifically, one of ordinary skill in the art would know that registers would be used to receive a row address to perform the operation described in the '297 Reference. Further, the use of a plurality of registers was well known in the art. The following are

CLAIM	RESPONSE
	illustrative: The '937 Reference states: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42] The '495 Reference states: "The register 70a, 70b, 70c or 70d selected by the block decoder 50 holds 8-bit address codes ARC0-ARC7 supplied in synchronism with the row selection signal RAS. Since the holding of the address codes ARC0-ARC7 will be maintained even after access is shifted to another cell array block, these registers 70a-70d store respectively the address codes ARC0-ARC7 of the last access in the cell array blocks 10a-10d and supply them to the selectors 80a-80d which also receive the address codes ARC0-ARC7 supplied in synchronism with the row selection signal RAS and introduce them to the row decoders 20a-20d." ['495 Reference, Col. 4:25-37] The '021 Reference states: "Since the low-speed large-capacity memories 11, 12, 13, 14 performing the 4-way interleave operation are shifted in access timing usually by one cycle from each other, the memories 11 14 are provided respectively with registers 23 26 each for holding an

CLAIM	RESPONSE
	address." ['021 Reference, Col. 4:5-9]
a plurality of row decoders, each row decoder for activating a portion of a row identified by signals from one of said first registers;	This element is met in the '297 Reference alone or in combination with any of the '937 Reference or the '495 Reference or the '021 Reference. The '297 Reference states: "In FIG. 6, which illustrates a first embodiment of the boundary-free semiconductor memory device, memory cells are divided into n rows x m columns of memory cell blocks B_{00}, B_{01}, . . ., B_{0n-1},; B_{10}, B_{11}, . . ., $B_{1,m-1}$; $B_{n-1,0}$, $B_{n-1,1}$, . . . , $B_{n-1,m-1}$. n number of same row selecting circuits RD0, RD1, . . ., and RD_{n-1} are provided commonly for each row of memory cell blocks, . . ." ['297 Reference, 7:8-15]. See, FIG. 6:

CLAIM	RESPONSE

Fig. 6



Further, the use of a plurality of decoders is well known in the prior art. The following are illustrative:

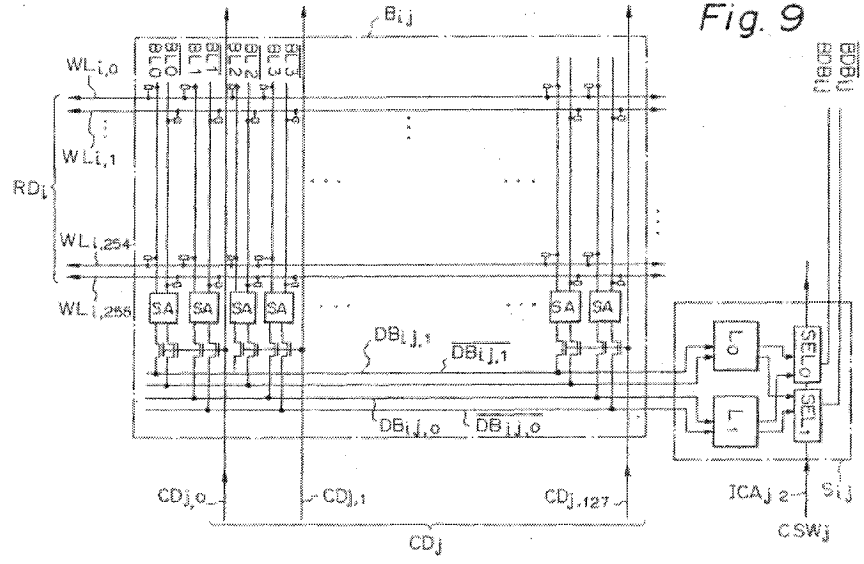
The '937 Reference teaches the use of a plurality of decoders as well as the use of a single decoder for performing the same function. [Figs. 3 and 5] The '937 Reference states:

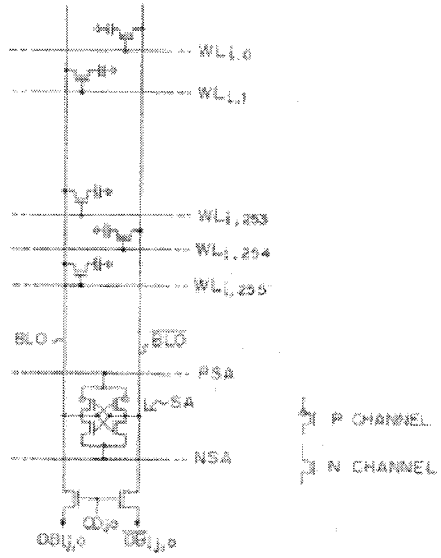
"The address counter 81 receives the signals $\emptyset_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $\emptyset_{EV}$ (i.e., twice that of the basic clock pulses $\emptyset_S$). Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the

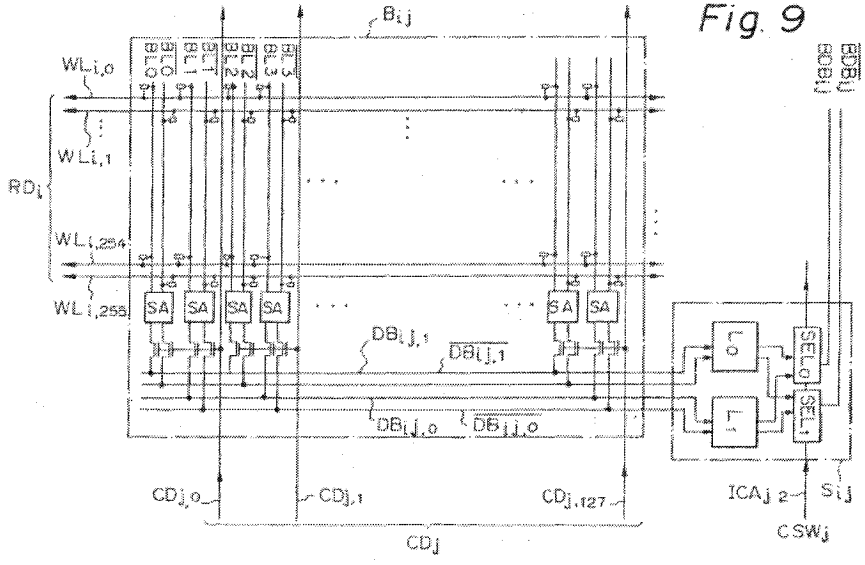
CLAIM	RESPONSE
	transfer gate 85. In a similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42] "The latch (see FIG. 6) forming the delay latch circuit 106 fetches the outputs from the X decoder 82 on the leading edges of the clock pulses $Ø_L$, and hence the delay latch circuit 106 delays the outputs from the X decoder 82 respectively by one cycle of the basic clock pulses $Ø_S$ to transfer the same to the second memory cell array 94. . . . It is to be noted that odd address cycles are always delayed from the even address cycles respectively by one cycle of the basic clock pulses $Ø_S$. Thus, this embodiment is equivalent in operation to that shown in FIG. 3" ['937 Reference, Col. 7:44-63] The '495 Reference states: "The output of the block decoder 50 is supplied in common to the row decoders 20a and 20d and the column decoders 40a and 40d. As a result, one word line is selected in the memory cell array block 10a, for example." ['495 Reference, Col. 3:39-42] The '021 Reference states: "In FIG. 1, numeral 100 designates clock signals to be supplied to the interleave controller 20, the select controller 30 and the high-speed memory access controller 40, numerals 111, 112, 113, 114 designate output data from the low-speed large-capacity memories 11, 12, 13, 14 respectively, numeral 120 designates an address signal to be supplied to the interleave controller 20, numerals 121, 122, 123, 124 designate address signals from the interleave controller 20 to the low-speed large-capacity memories 11, 12, 13, 14 respectively, ..." ['021 Reference, Col. 3:43-68] Each memory 11, 12, 13, and 14 would have a decoder for receiving an address from interleave controller 20.

CLAIM	RESPONSE
one or more sense amplifiers for amplifying contents of said memory locations in the row portions; and	This element is met in the '297 Reference. Specifically, the '297 Reference states that: ". . . as illustrated in FIG. 10, memory cells are provided at every other intersection of a pair of bit lines and word lines on one side of each sense amplifier SA. Note that the sense amplifier SA of FIG. 10 is comprised of p-channel transistors between a line PSA and bit lines BL0 and $\overline{\text{BLO}}$, and N-channel transistors between a line NSA and bit lines BL0 and $\overline{\text{BLO}}$, and when the lines PSA and NSA are made high and low, respectively, the sense amplifier SA is operated." ['297 Reference, 8:26-35]. See, FIGs. 9 and 10:

CLAIM	RESPONSE



CLAIM	RESPONSE
	Fig. 10  See also, FIG. 23., '297 Reference.
an output for providing output signals from said sense amplifiers,	This element is met in the '297 Reference. "The switch S_{ij} is comprised of two data bus latches L0 and L1 and two selectors SEL0 and SEL1. As illustrated in FIG. 11, each of the selectors is comprised of an inverter I, AND circuits G1 and G2, and an OR circuit G3. That is, in accordance with a bit CSW_j of a column address, one of the data bus latches L0 and L1 is connected to the block data buses BDB_{ij} and $\overline{BDB_{ij}}$." ['297 Reference, 8:46-52.]

CLAIM	RESPONSE
	FIG. 9 shows output lines and an output buffer (a data bus latch) connected to the sense amplifiers:  Moreover, it is inherent in the '297 Reference that there is an output for providing output signals from the sense amplifiers.
wherein at least two locations L1 and L2 in different rows having different row addresses in said memory can be read out to said output in burst mode such that	This element is met in the '297 Reference alone or in combination with the U.S. Patent No. 5,036,494 ("the '494 Reference") or U.S. Patent No. 4,875,196 ("the '196 Reference"). Specifically, the '297 Reference states that:

CLAIM	RESPONSE
the memory receives an address of one of said locations and provides in response contents of a plurality of memory locations, including the locations L1 and L2, in the sequence of consecutive addresses, so that while one of said row decoders is activating a row portion comprising said location L1 and contents of said location L1 are being transferred from one or more of said sense amplifiers to said output, another one of said row decoders is activating a row portion comprising said location L2 and contents of said location L2 are being transferred from said location L2 to one or more of said sense amplifiers.	"That is, in a serial access mode, n rows such as four rows adjacent to a voluntary proposition of the logic bit map plane, are accessed in the sequence of the adjacent row data by the arranging means." ['297 Reference, 2:47-51] "Another object of the present invention is to provide a boundary-free semiconductor memory device in which a voluntary adjacent n-row bit group can be accessed in a serial access mode." ['297 Reference, 1:67-2:2] See also, '297 Reference, 13:1-47 and FIGs. 6, 7, 21 and 22. The '494 Reference states: "The selection of memory locations forming each cyclic pattern of addressing is controlled by the control unit 13. The row counter 45 and column counter 44 are connected so that unless instructed by the control 13 to do otherwise they count through successive addresses along each row and then row by row." ['494 Reference, Col. 8:22-27] "Consequently after reaching address 0 the column and row counters cycle sequentially along each row for the two memory blocks in turn (starting at column zero of row 0 in array 0) using all memory locations in each row and then moving to the next row and repeating the operation." ['494 Reference, Col. 11:26-31] "addressing sequentially more than one memory location in said first memory block and effecting a data transfer for each memory location addressed, and at the same time effecting an equate operation on bit lines in said second memory block; and after addressing memory locations in said first memory block, switching said addressing and equate operation so as to address sequentially more than one memory location in said second memory block and effecting a data transfer for each memory location addressed and at the same time equating bit lines in said first memory block." ['494 Reference, Col.

CLAIM	RESPONSE
	13:36-48] The '196 Reference states that: "In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit lines in the other array are being precharged. Thus, as data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit lines in that array will already have been initialied." ['196 Reference, Col. 2:60-67] "In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and settling transient signals) in preparation for the next access form such other array. Therefore, precharging items for one array overlap the time for performing read or write operation in the other array, and therefore do not limit operating speed." ['196 Reference, Col. 3:41-47]
2. The memory of claim 1, said memory having a random mode in which the memory receives an address and provides in response the contents of a unique memory location,	It was well-known in the art to retain a random mode while adding the functionality of a sequential read operation. The following are illustrative: EP 9 326 885 A2 ("the '885 Reference") states: "The circuit provides both random and sequential access functions and allows the memory to be used as a shift register of variable length." ['885 Reference, Page 1] U.S. Patent No. 5, 263,003 ("the '003 Reference") states: "In a first mode, the memory circuit responds to an initial request for access and an address signal by reading data from a storage location in one of the memory banks. Subsequent requests for access to continguous storage locations do not require an address signal,

CLAIM	RESPONSE
	instead a control mechanism responds by generating an address to read data alternately from storage locations in the first and second memory banks. In a second mode, the memory circuit responds to every request for access to the memory circuit by enabling access to the first or second memory bank as indicated by an address which accompanied the request." ['003 Reference, Abstract]
wherein, both in burst mode and in random mode, while the contents of said location L1 are being transferred from one or more of said sense amplifiers to said output, the contents of said location L2 are being transferred from said location L2 to one or more of said sense amplifiers.	It would be obvious to a person of skill in the art that transferring the contents of a location L1 from one of the sens amplifiers to the output while the contents of a location L2 are transferred from the location L2 to one or more sense amplifiers could be used in either a burst mode or a random mode. *See* claim 1 above. Further, to the extent AMD reads this limitation on the Samsung devices, this limitation is met by prior art references having both a random access mode and a burst mode.
3. The memory of claim 1 wherein when the locations L1 and L2 are read out in burst mode and when the contents of said location L1 are being transferred from one or more of said sense amplifiers to said output and the contents of said location L2 are being transferred from said location L2 to one or more of said sense amplifiers, the sense amplifiers from which the contents of said location L1 are being transferred are enabled and the sense amplifiers to which the contents of said location L2 are being transferred are disabled, but	This element is met in the '297 Reference alone or in combination with any of U.S. Patent No. 4,937,788 ("the '788 Reference") or the '937 Reference or the '003 Reference or U.S. Patent No. 5,251,178 ("the '178 Reference") or EP 0 087 754 B1 ("the '754 Reference"). Specifically, the '297 Reference states that: ". . . as illustrated in FIG. 10, memory cells are provided at every other intersection of a pair of bit lines and word lines on one side of each sense amplifier SA. Note that the sense amplifier SA of FIG. 10 is comprised of p-channel transistors between a line PSA and bit lines BL0 and $\overline{BL0}$, and N-channel transistors between a line NSA and bit lines BL0 and BL0, and when the lines PSA and NSA are made high and low, respectively, the sense amplifier SA is operated. Also, in FIG. 9, the row decoder RD_i selects one word line from 256 word lines $WL_{i,0}$, $WL_{i,1}$, . . . , and $WL_{i,225}$, while the column decoder CD_j selects two pairs of bit lines such as BL0 and $\overline{BL0}$; and BL1 and $\overline{BL1}$ by the column selection

CLAIM	RESPONSE
these latter sense amplifiers become enabled subsequently for amplifying the contents of said location L2.	signals $CD_{j,0}$, $CD_{j,1}$, . . . , and $CD_{j,127}$ thereof, and connects them to data buses $DB_{ij,0}$ and $\overline{DB}_{ij,0}$; $DB_{ij,1}$ and $\overline{DB}_{ij,1}$ within the block, and further, one pair of the two paires of the data buses $DB_{ij,0}$ and $\overline{DB}_{ij,0}$; $DB_{ij,1}$ and $\overline{DB}_{ij,1}$ within the block is selected by a switch S_{ij} and is connected to block data buses BDB_{ij} and $\overline{BDB}_{ij}$." ['297 Reference, 8:26-45]. See also, '297 Reference, 13:48-14:14, 14:59-15:7, FIGs. 9, 10, 23. Further, this element was well-known in the art. The following are illustrative: The '788 Reference states: "According to this arrangement, only one plane is selected in accordance with the content of the upper-order two bits of the row address. The selected plane is activated and exhibits the memory operation but the rest of the planes which are under the non-selection state are inoperative. Therefore, the decoders and the sense amplifiers are inoperative in these inoperative planes and the memory is not refreshed. Therefore, power is consumed in only the selected plane and unnecessary power consumption in the other plane can be saved. Thus, the requirement for low power consumption can be satisfied." ['788 Reference, Col. 5:57-68] The '937 Reference states: "The sense amplifier 86 is controlled by the signals SEEV to amplify the read data thereby to supply the same to the data latch 87, which in turn temporarily stores the outputs from the sense amplifiers 86. When the signals SE_{EV} are at low levels, the data latch 87 is electrically cut off from the sense amplifier 86. Data from the data latch 87 are transferred to the output latch 89 when the signals OE_{EV} are at high levels. In a similar manner, the

CLAIM	RESPONSE
	sense amplifier 96 is controlled by the signals SE_{OD} to amplify the read data thereby to supply the same to the data latch 97, which in turn temporarily stores the outputs from the sense amplifier 96. When the signals SE_{OD} are at low levels, the data latch 97 is electrically cut off from the sense amplifier 96." ['937 Reference, Col. 4:52-66] The '003 Reference states: "The flash memory control 88 also selectively enables one of two sets of bi-directional data buffers 90 and 91 which respectively couple the bank data buses 82 and 83 to the processor section data bus 63. The bank data buses 82 and 83 can be coupled to the instruction bus 61 by the flash memory control 88 selectively enabling buffers 92 and 93, respectively." ['003 Reference, Col. 9:21-27] The '178 Reference states: "Referring now to FIG. 2, the circuit of FIG. 1 has been modified to utilize the fact that, when RA10=1, only one half of the ARRAY BANKs 20 are being utilized and that, when RA10=0, the other half of the ARRAY BANKs 20 are being utilized. In particular, the RA 10 address is used to cause only the half of the ARRAY BANKs 20 that are being utilized to draw power from the DRAM energy source during read/write operations, while at the same time permitting the periodic performance of the refresh cycle in the usual manner on all ARRAY BANKs." ['178 Reference, Col. 3:32-42] The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense

CLAIM	RESPONSE
	amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58]
4. The memory of claim 1 wherein:	
said memory comprises k pluralities S-1, . . . , S-k of locations wherein k is a number of said pluralities and is greater than or equal to two; for each plurality S-i, said sense amplifiers can receive simultaneously the contents of number m of locations from said plurality S-i, wherein m is a positive integer; and	This limitation is met by the '297 Reference. Specifically, the '297 Reference states: "An entire chip is divided into N blocks (N = n x m) in accordance with a desired rectangular group of bits (n x m bits). The same row decoder is provided for every m blocks, and a row address $\bar{A}_r$ or a row address $\bar{A}_{r+1}$ adjacent thereto is given to the row decoders. * * * N bits of memory cells are accessed from the blocks, and the accessed memory cells are rearranged, thereby obtaining a desired rectangular group of bits." ['297 Reference, Abstract]. See, e.g., Figs. 6, 7, 9, 10, 21, 22 and 23. ". . . as illustrated in FIG. 10, memory cells are provided at every other intersection of a pair of bit lines and word lines on one side of each sense amplifier SA. Note that the sense amplifier SA of FIG. 10 is comprised of p-channel transistors between a line PSA and bit lines BL0 and $\overline{BLO}$, and N-channel transistors between a line NSA and bit lines BL0 and $\overline{BLO}$, and when the lines PSA and NSA are made high and low, respectively, the sense amplifier SA is operated." ['297 Reference, 8:26-35].

CLAIM	RESPONSE
time tARA does not exceed m * (k-1) * (tOE), wherein: tARA is measured from the time that an address of a location is made available to said memory to the time when one or more of said sense amplifiers develop an output signal indicative of the contents of said location; and tOE is the time to transfer an output of any one of said sense amplifiers to said output of said memory.	A person of skill in the art would know that this timing relationship would be used when designing the memory disclosed in claim 1.
5. The memory of claim 1 wherein, in burst mode, a time in which each location of said plurality except said one of said locations is read out to said output after a previous location has been read out to said output is shorter than a time in which said one of said locations is read out to said output after said address of said one of said locations has been received by said memory.	This element is met for the '297 Reference alone or in combination with U.S. Patent No. 4,918,587 ("the '587 Reference") or the '003 Reference or U.S. Patent No. 4,799,199 ("the '199 Reference"). The '297 Reference states: "The second embodiment of FIG. 21 will be explained in more detail with reference to FIG. 22. In FIG. 22, elements for a serial access mode are added to the elements of FIG. 7. That is, a shift register SR_{ij} is arranged along the row direction of each of the cell blocks B_{ij} (i=0~3, j=0~3), and the output SRO_{ij} is connected to multiplexers MPX0 to MPX3. Further, the sequence of serial data buses SRD_0 to SRD_3 of the multiplexer MPX0 to MPX3 is changed by a bus arranging circuit BAC2, and is connected to input/output terminals SIO_0 to SIO_3 for a serial access mode. Also, in a serial access mode, the row-

CLAIM	RESPONSE
	side switches RSW0 to RSW3 are operated in the same way as in a random access mode, and as a result, the voluntary four rows Y_0, Y_0+1, Y_0+2, and Y_0+3 (Y_0 is the row address of the pointing bit PB) are selected. Then, the rows are simultaneously transmitted in parallel via transfer gates to the shift registers of 1024 bits x 4 rows. Note that the 1024 bit x one row shift register is comprised of shift registers SR_{i0}, SR_{i1}, SR_{i2}, and SR_{i3} provided in parallel to the four cell blocks. Subsequently, data is read out of the 1024 bits x 4 rows shift registers at a high speed clock rate such as about 20 to 30 MHz without addresses at an asynchronous mode of a random access and a serial access." ['297 Reference, 13:23-47] See, FIGs. 21, 22 of the '297 Reference. The '587 Reference states: "The reduction in the memory access cycle time from a conventional memory access operation, generally represented by the first prefetch with a three clock cycle span between event t1 and t2, is clearly evident when the times are compared to those of the consecutive prefetch operation extending for two clock cycles between corresponding time intervals t3 and t4. Time t2 and t4 identify the first clock interval suitable to initiate succeeding memory access operations." ['587 Reference, Col. 5:63-6:3] The '003 Reference states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from

CLAIM	RESPONSE
	the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer. Typically, the access addresses of these 'extra' storage cells differ from the original access address by only one or two bits. However, subsequent accesses to these cells can be accomplished by simply executing additional access cycles without changing the access address. In the art, such memories are referred to as 'nibble mode'. In some other integrated circuit memories, a portion of the original address can be 'assumed' from one (or more) subsequent accesses, so that only the least significant portion of the address needs to be decoded, etc. Thus, once the original access had been completed, subsequent accesses to 'related' storage cells will be significantly quicker." ['199 Reference, Col. 1:13-28]
6. The memory of claim 1 wherein said memory is fabricated in an integrated circuit.	This element is met by the '297 Reference alone or in combination with any of the '754 Reference or the '199 Reference or U.S. Patent No. 4,899,312 ("the '312 Reference"). The '297 Reference is entitled "Boundary-Free Semiconductor Memory Device." Moreover, the '297 Reference Abstract begins by saying "An entire chip is divided into . .

CLAIM	RESPONSE
	." Further, it was well known in the art to fabricate memories as an integrated circuit and a person of ordinary skill would have know that the memory device shown in the '297 Reference could be fabricated in an integrated circuit. The '754 Reference states: "The present invention relates to a semiconductor dynamic memory device. Mass-production of 64K bit dynamic type random access memory devices (DRAMs) has been enabled by the recent development of semiconductor memory devices of high packing density. Furthermore, a 256K bit DRAM has been developed." ['754 Reference, Page 2:3-6] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer." ['199 Reference, Col. 1:13-16] The '312 Reference states: "The individual circuit elements constructing the RAM of the present embodiment are formed on a semiconductor substrate such as a piece of single-crystalline silicon by the known technique for fabricating a CMOS (i.e., Complementary MOS) integreated circuit." ['312 Reference, Col. 2:34-38]
7. The memory of claim 1 further comprising:	
a plurality of second registers, each	This element is met by the '297 Reference, alone or in combination with the '196

CLAIM	RESPONSE
second register for receiving at least a portion of a column address; and	Reference or the '937 Reference. The '297 Reference states: "An entire chip is divided into N blocks (N = n x m) in accordance with a desired rectangular group of bits (n x x bits). The same row decoder is provided for every m blocks, and a row address $\bar{A}_r$ or a row address $\bar{A}_{r+1}$ adjacent thereto is given to the row decoders. Similarly, the same colum decoder is provided for every m blocks, and a column address $\bar{A}_c$ or a column address $\bar{A}_c+1$ adjacent thereto is given to the column decoders. N bits of memory cells are accessed from the blocks, and the accessed memory cells are rearranged, thereby obtaining a desired rectangular group of bits." ['297 Reference, Abstract]. "In FIG. 6, which illustrates a first embodiment of the boundary-free semiconductor memory device, memory cells are divided into n rows x m columns of memory cell blocks B_{00}, B_{01}, . . ., B_{0n-1},; B_{10}, B_{11}, . . ., $B_{1,m-1}$; $B_{n-1,0}$, $B_{n-1,1}$, . . . , $B_{n-1,m-1}$. n number of same row selecting circuits RD0, RD1, . . ., and RD_{n-1} are provided commonly for each row of memory cell blocks, and m number of same column selecting means CD_0, CD_1, . . . and CD_{m-1} are provided commonly for each column of the memory cell blocks." ['297 Reference, 7:8-15]. "According to the configuration of the cell block B_{ij} as shown in FIG. 6, since each of the column decoders CD_j has a 128-bit configuration, ... Also, each of the column decoder CD_j is constructed to be able to directly select one bit line pair from 256 pairs of bit lines. In this case, all the 8 bit addresses from the column-side switches CSW0 to CSW3 are supplied to all the respective column decoders CD_j, and the switch S_{ij} is deleted." ['297 Reference, 8:53-66] The '196 Reference states that:

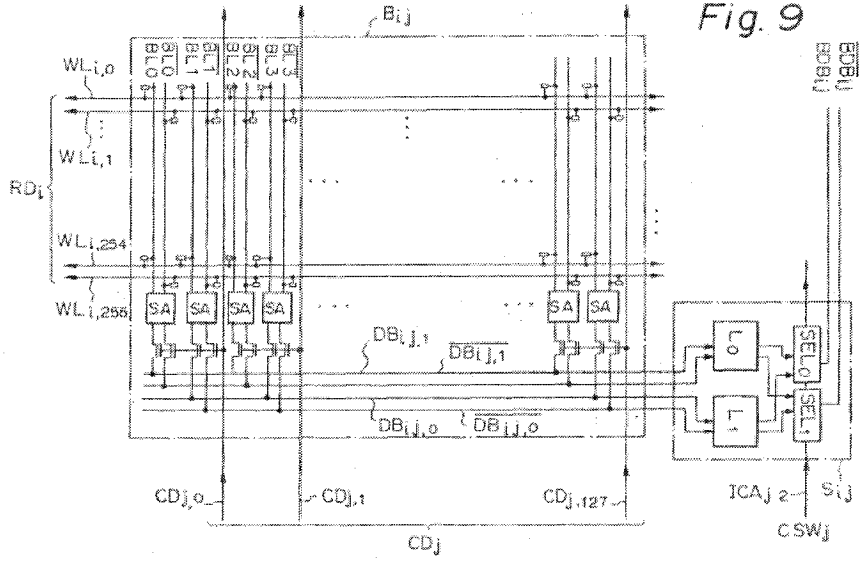
CLAIM	RESPONSE
	"The row and column location in the arrays 31, 33 at which data is accessed is controlled by the counters which, in one embodiment of the invention may be binary counters, or the like, which have an extended counting range that is double the number of address locations in the array to be accessed." ['196 Reference, Col. 4:49-55; See also, FIGS. 2A, 2B] Further, one of ordinary skill in the art would know that the counters shown are, or can be, implemented through the use of a register. The '937 Reference states that: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e. twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. Ina similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e. twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42]
a circuitry for each second register for selecting in response to signals from one of the second registers a plurality of columns to be read by the sense amplifiers.	This element is met in the '297 Reference in combination with the '196 Reference or the '937 Reference. The '297 Reference states: "An entire chip is divided into N blocks (N = n x m) in accordance with a desired rectangular group of bits (n x x bits). The same row decoder is provided for every m blocks, and a row address $\bar{A}_r$ or a row address $\bar{A}_{r+1}$ adjacent thereto is given to the row

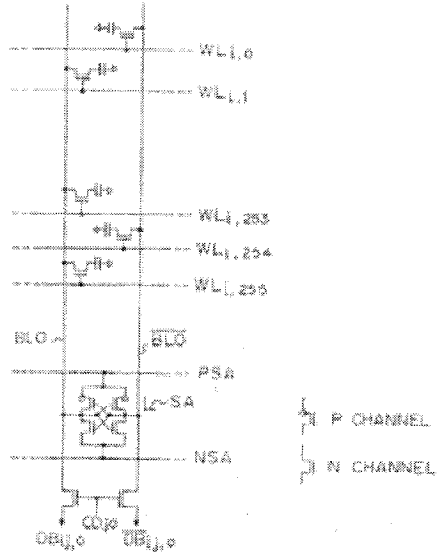
CLAIM	RESPONSE
	decoders. Similarly, the same colum decoder is provided for every m blocks, and a column address $\bar{A}_c$ or a column address $\bar{A}_c+1$ adjacent thereto is given to the column decoders. N bits of memory cells are accessed from the blocks, and the accessed memory cells are rearranged, thereby obtaining a desired rectangular group of bits." ['297 Reference, Abstract]. "In FIG. 6, which illustrates a first embodiment of the boundary-free semiconductor memory device, memory cells are divided into n rows x m columns of memory cell blocks B_{00}, B_{01}, . . ., B_{0n-1}; B_{10}, B_{11}, . . ., $B_{1,m-1}$; $B_{n-1,0}$, $B_{n-1,1}$, . . . , $B_{n-1,m-1}$. n number of same row selecting circuits RD0, RD1, . . ., and RD_{n-1} are provided commonly for each row of memory cell blocks, and m number of same column selecting means CD_0, CD_1, . . . and CD_{m-1} are provided commonly for each column of the memory cell blocks." ['297 Reference, 7:8-15]. "According to the configuration of the cell block B_{ij} as shown in FIG. 6, sinch each of the column decoders CD_j has a 128-bit configuration, ... Also, each of the column decoder CD_j is constructed to be able to directly select one bit line pair from 256 pairs of bit lines. In this case, all the 8 bit addresses from the column-side switches CSW0 to CSW3 are supplied to all the respective column decoders CD_j, and the switch S_{ij} is deleted." ['297 Reference, 8:53-66] The '196 Reference states that: "Referring now to FIGS. 2A and 2B, there is shown a block schematic diagram of a pair of RAM arrays 31, 33, each comprising a plurality of individual memory cells of the type illustrated and described above with reference to FIGS. 1A and 1B. Each of these arrays may be configured to store data in a matrix of rows and columsn [sic] that is several columns long and several rows deep (e.g. 72X128). The columns and rows of memory cells in each array are connected to decoders for writing and reading data into and out of

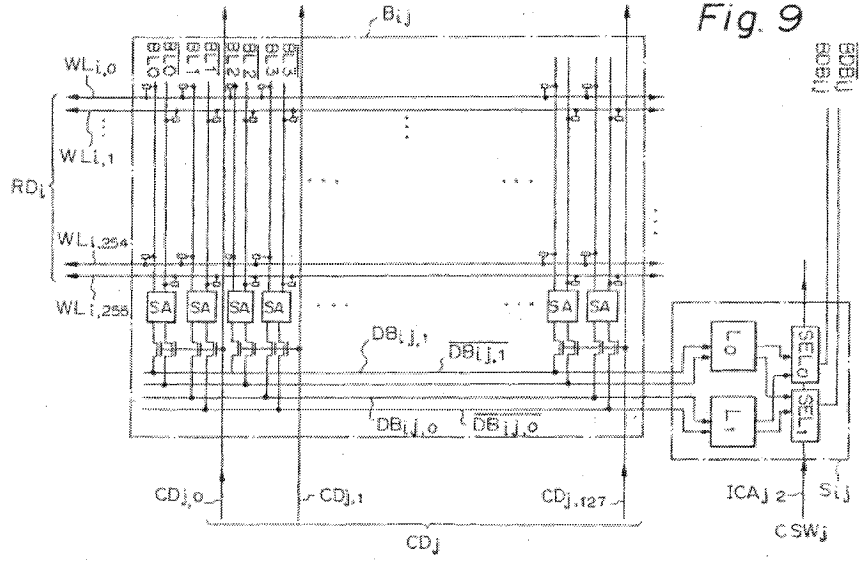
CLAIM	RESPONSE
	selected memory cells in the arrays. Specifically, the write column decoders 35, 37 are connected to the dual arrays to address selected columns of memory cells, and the write row decoders and drivers 39, 41 are connected to the dual arrays to address selected rows of memory cells. Similarly, the read column decoders 45,47 are connected to the dual arrays to address selected columns of memory cells , and the read row decoders and drivers 49, 51 are connected to the dual arrays to address selected rows." ['196 Reference, Col. 3:11-29; See also FIGS 1A, 1B, 2A] "Similarly, the data which is to be read out from the RAM arrays 31, 33 is designated in selected 9-column segments by the column predecoders 61 which, in turn, is selected by the read pointer counters 63. The columns thus addressed may extend over both arrays, where each column is uniquely addressable, and the arrays alternate when the boundary of column addresses for a given array is reached, as previously described." ['196 Reference, Col. 4:5-12] The '937 Reference states: "Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to a transfer gate 85.... In a similar manner, the transfer gate 95 transfers data read from the second memory cell array 94 to the sense amplifier 96 through an I/O line 103, while transferring data from the write circuit 98 received through the I/O line 103 to the second memory cell array 94." ['937 Reference, Col. 4:33-52]
8. A memory comprising:	Although a preamble is normally not limiting, should this preamble be limiting, this element is met by the '297 Reference. Specifically, the '297 Reference is entitled "Boundary-Free Semiconductor Memory Device."
a set of consecutively addressed memory	This element is met in the '297 Reference. Specifically, the '297 Reference states that:

CLAIM	RESPONSE
locations L1, . . . Ln;	"Thus, in a serial access mode, n rows such as four rows adjacent to a voluntary position of the logic bit map plane are accessed, and the rows are accessed in the sequence of the adjacent row by the arranging circuit by BAC2. Therefore, it is possible to access a desired n-rows bit group as well as a desired rectangular bit group." ['297 Reference, 13:16-22]
a plurality of sense amplifier circuits for amplifying contents of said memory locations; and	This element is met in the '297 Reference. Specifically, the '297 Reference states that: ". . . as illustrated in FIG. 10, memory cells are provided at every other intersection of a pair of bit lines and word lines on one side of each sense amplifier SA. Note that the sense amplifier SA of FIG. 10 is comprised of p-channel transistors between a line PSA and bit lines BL0 and $\overline{BL0}$, and N-channel transistors between a line NSA and bit lines BL0 and BL0, and when the lines PSA and NSA are made high and low, respectively, the sense amplifier SA is operated." ['297 Reference, 8:26-35]. See, FIGs. 9 and 10:

CLAIM	RESPONSE

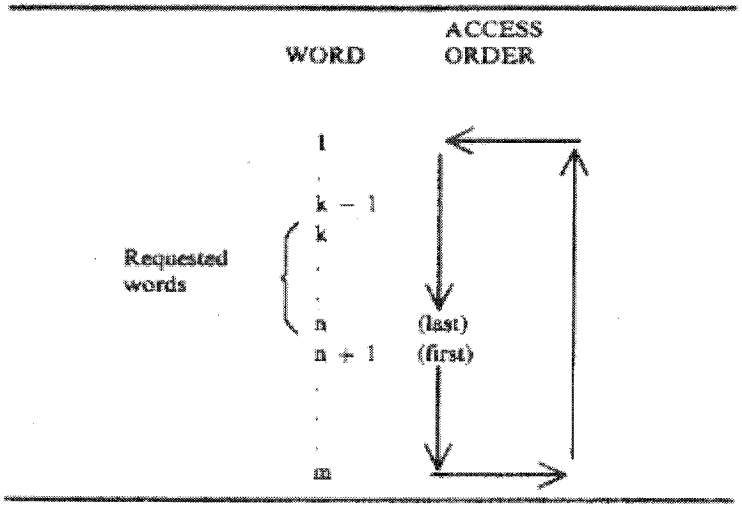


CLAIM	RESPONSE
	Fig. 10  See also, FIG. 23, '297 Reference.
an output for providing output signals from said plurality of sense amplifier circuits,	This element is met in the '297 Reference. "The switch S_{ij} is comprised of two data bus latches L0 and L1 and two selectors SEL0 and SEL1. As illustrated in FIG. 11, each of the selectors is comprised of an inverter I, AND circuits G1 and G2, and an OR circuit G3. That is, in accordance with a bit CSW_j of a column address, one of the data bus latches L0 and L1 is connected to the block data buses BDB_{ij} and $\overline{BDB}_{ij}$." ['297 Reference, 8:46-52.]

CLAIM	RESPONSE
	FIG. 9 shows output lines and an output buffer (a data bus latch) connected to the sense amplifiers: 
wherein said memory has a burst mode operation for receiving an address and reading out to said output, in response to said address, any given number of memory locations in the sequence of	Moreover, it is inherent in the '297 Reference that there is an output for providing output signals from the sense amplifiers. This element is met in the '297 Reference alone or in combination with the '196 Reference or the '885 Reference or the '631 Reference. Specifically, the '297 Reference states that: "That is, in a serial access mode, n rows such as four rows adjacent to a voluntary proposition of the logic bit map plane, are accessed in the sequence of the adjacent row

CLAIM	RESPONSE
consecutive addresses with wrap around so that the next location, if any, to be read out after said location Ln is said location L1, such that during said operation while the contents of any location L to be read out other than the last location to be read out are being transferred from said plurality of sense amplifier circuits to said output, the contents of another location to be read out after said location L are being provided to said plurality of sense amplifier circuits for amplification and subsequent transfer to said output, and	data by the arranging means." ['297 Reference, 2:47-51] "Another object of the present invention is to provide a boundary-free semiconductor memory device in which a voluntary adjacent n-row bit group can be accessed in a serial access mode." ['297 Reference, 1:67-2:2] See also, '297 Reference, 13:1-47 and FIGs. 6, 7, 21 and 22. The '196 Reference states that: "In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit lines in the other array are being precharged. Thus, as data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit lines in that array will already have been initialized." ['196 Reference, Col. 2:60-67] "In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and settling transient signals) in preparation for the next access form such other array. Therefore, precharging times for one array overlap the time for performing read or write operation in the other array, and therefore do not limit operating speed." ['196 Reference, 3:41-47] The '885 Reference states: "After the last memory address is reached, the access automatically rolls over to the first address." ['885 Reference, page 1; Col. 3:1-3] "A method as in claim 5 wherein the sequence of incremented addresses wraps around when the address of the Nth register is reached such that all N registers in the array are

CLAIM	RESPONSE
	read." ['885 Reference, Col. 7:45-48] The '631 Reference states that: "The above-described method is accomplished by utilizing two pieces of information, which are placed on the bus (23) by the GDP: the data word's offset and the number of words requested. The data word's offset in the cache line is derived from adress bits 2 and 3 (00=word 1, 01=word 2, 10=word 3, and 11=word 4). The number of words being requested is obtained from the size bits 0 and 1 (00=1word, 01=2 words, 10=3 words, and 11=4words). Using these two pieces of information, the following algorithm is executed: FIRST WORD ACCESSED = PROCESSOR WORD ADDRESS + SIZE +1 The 1 is added to the size in order to yield the correct offset. For example, if the GDP requests two words at offset 01 in a four-word line, it is convereted to a wraparound request of four words to memory starting at word four [offset (01) + word count (01) + 1 = 11]." ['631 Reference, Col. 3:46-65] See, '631 Reference, Table II:

CLAIM	RESPONSE
	TABLE II  See also, '631 Reference, Abstract, Table I, Fig. 3.
wherein said memory further comprises a control circuit for selectively enabling said sense amplifier circuits so that said control circuit enables a sense amplifier circuit whose output signals are being transferred to the output of said memory but said control circuit does not enable all said sense amplifier circuits at the same time.	This element is met in the '297 Reference alone or in combination with any of the '788 Reference or the '937 Reference or the '003 Reference or the '178 Reference or the '754 Reference. Specifically, the '297 Reference states that: ". . . as illustrated in FIG. 10, memory cells are provided at every other intersection of a pair of bit lines and word lines on one side of each sense amplifier SA. Note that the sense amplifier SA of FIG. 10 is comprised of p-channel transistors between a line PSA and bit lines BL0 and $\overline{\text{BL0}}$, and N-channel transistors between a line NSA and bit lines BL0 and