EXHIBIT 1

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CLAIM	RESPONSE
	$\overline{BL0}$, and when the lines PSA and NSA are made high and low, respectively, the sense amplifier SA is operated. Also, in FIG. 9, the row decoder RD_i selects one word line from 256 word lines $WL_{i,0}$, $WL_{i,1}$, . . . , and $WL_{i,225}$, while the column decoder CD_j selects two pairs of bit lines such as BL0 and $\overline{BL0}$; and BL1 and $\overline{BL1}$ by the column selection signals $CD_{j,0}$, $CD_{j,1}$, . . . , and $CD_{j,127}$ thereof, and connects them to data buses $DB_{ij,0}$ and $\overline{DB}_{ij,0}$; $DB_{ij,1}$ and $\overline{DB}_{ij,1}$ within the block, and further, one pair of the two paires of the data buses $DB_{ij,0}$ and $\overline{DB}_{ij,0}$; $DB_{ij,1}$ and $\overline{DB}_{ij,1}$ within the block is selected by a switch S_{ij} and is connected to block data buses BDB_{ij} and $\overline{BDB}_{ij}$." ['297 Reference, 8:26-45]. "Also, the control circuit CONT receives external signals such as a chip enable signal $\overline{CE}$, a batch transfer signal $\overline{TR}$ for a serial access mode, a read/write signal R/W, and a serial clock signal SCLK and generates various internal signals such as the batch transfer signal TR, the shift clock signals P1 and P2, and the serial clock signal SC. For example, the external shift clock signal SCLK is buffered to generate an internal shift clock signal SC which is four-divided to generate the shift clock signals P1 and P2. Further, the internal batch transfer signal TR is generated from the chip enable signal $\overline{CE}$ and the external transfer signal $\overline{TR}$." ('297 Reference, 13:51-14:3.) See also, '297 Reference, 14:4-14:14, 14:59-15:7, FIGs. 9, 10, 23. Further, this element was well-known in the art. The following are illustrative: The '788 Reference states:

CLAIM	RESPONSE
	"According to this arrangement, only one plane is selected in accordance with the content of the upper-order two bits of the row address. The selected plane is activated and exhibits the memory operation but the rest of the planes which are under the non-selection state are inoperative. Therefore, the decoders and the sense amplifiers are inoperative in these inoperative planes and the memory is not refreshed. Therefore, power is consumed in only the selected plane and unnecessary power consumption in the other plane can be saved. Thus, the requirement for low power consumption can be satisfied." ['788 Reference, Col. 5:57-68] The '937 Reference states: "The sense amplifier 86 is controlled by the signals SE_{EV} to simplify the read data thereby to supply the same to the data latch 87, which in turn temporarily stores the outputs from the sense amplifiers 86. When the signals SE_{EV} are at low levels, the data latch 87 is electrically cut off from the sense amplifier 86. Data from the data latch 87 are transferred to the output latch 89 when the signals OE_{EV} are at high levels. In a similar manner, the sense amplifier 96 is controlled by the signals SE_{OD} to amplify the read data thereby to supply the same to the data latch 97, which in turn temporarily stores the outputs from the sense amplifier 96. When the signals SE_{OD} are at low levels, the data latch 97 is electrically cut off from the sense amplifier 96." ['937 Reference, Col. 4:52-66] The '003 Reference states: "The flash memory control 88 also selectively enables one of two sets of bi-directional data buffers 90 and 91 which respectively couple the bank data buses 82 and 83 to the processor section data bus 63. The bank data buses 82 and 83 can be coupled to the instruction bus 61 by the flash memory control 88 selectively enabling buffers 92 and 93, respectively." ['003 Reference, Col. 9:21-27]

CLAIM	RESPONSE
	The '178 Reference states: "Referring now to FIG. 2, the circuit of FIG. 1 has been modified to utilize the fact that, when RA10=1, only one half of the ARRAY BANKs 20 are being utilized and that, when RA10=0, the other half of the ARRAY BANKs 20 are being utilized. In particular, the RA 10 address is used to cause only the half of the ARRAY BANKs 20 that are being utilized to draw power from the DRAM energy source during read/write operations, while at the same time permitting the periodic performance of the refresh cycle in the usual manner on all ARRAY BANKs." ['178 Reference, Col. 3:32-42] The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58]
9. The memory of claim 8 wherein, during said operation, said control circuit enables at the same time only: (1) the sense amplifier circuit whose	This limitation is met by the '297 Reference alone or in combination with the '754

CLAIM	RESPONSE
output signals are being transferred to said output of said memory, and	Reference. Specifically, the '297 Reference states that: ". . . as illustrated in FIG. 10, memory cells are provided at every other intersection of a pair of bit lines and word lines on one side of each sense amplifier SA. Note that the sense amplifier SA of FIG. 10 is comprised of p-channel transistors between a line PSA and bit lines BL0 and $\overline{BL0}$, and N-channel transistors between a line NSA and bit lines BL0 and $\overline{BL0}$, and when the lines PSA and NSA are made high and low, respectively, the sense amplifier SA is operated. Also, in FIG. 9, the row decoder RD_i selects one word line from 256 word lines $WL_{i,0}$, $WL_{i,1}$, . . . , and $WL_{i,225}$, while the column decoder CD_j selects two pairs of bit lines such as BL0 and $\overline{BL0}$; and BL1 and $\overline{BL1}$ by the column selection signals $CD_{j,0}$, $CD_{j,1}$, . . . , and $CD_{j,127}$ thereof, and connects them to data buses $DB_{ij,0}$ and $\overline{DB}_{ij,0}$; $DB_{ij,1}$ and $\overline{DB}_{ij,1}$ within the block, and further, one pair of the two pairs of the data buses $DB_{ij,0}$ and $\overline{DB}_{ij,0}$; $DB_{ij,1}$ and $\overline{DB}_{ij,1}$ within the block is selected by a switch S_{ij} and is connected to block data buses BDB_{ij} and $\overline{BDB}_{ij}$." ['297 Reference, 8:26-45]. "For this purpose, the multiplexers MPX0 to MPX3 carry out a parallel/serial transformation from 4 bits to 1 bits. Therefore, the shift registers SR_{00} to SR_{33} are operated by shift clock signals P_1 and P_2 having four times the period of a serial clock signal SC of the multiplexers MPX0 to MPX3. Then, four serial data buses SRD_0 to SRD_3 are rearranged and connected ot the four serial input/output terminals SIO_0 to SIO_3. Also, the control circuit CONT receives external signals such as a chip enable signal $\overline{CE}$, a batch transfer signal $\overline{TR}$ for a serial access mode, a read/write signal R/W, and a serial

CLAIM	RESPONSE
	clock signal SCLK and generates various internal signals such as the batch transfer signal TR, the shift clock signals P1 and P2, and the serial clock signal SC. For example, the external shift clock signal SCLK is buffered to generate an internal shift clock signal SC which is four-divided to generate the shift clock signals P1 and P2. Further, the internal batch transfer signal TR is generated from the chip enable signal $\overline{CE}$ and the external transfer signal $\overline{TR}$." ('297 Reference, 13:51-14:3.) See also, '297 Reference, 14:4-14:14, 14:59-15:7, FIGs. 9, 10, 23. The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58] "A semiconductor dynamic memory device comprising: ... a plurality of sense amplifying means (18-1 to 18-4; SA1 to SA8) responsive to a control signal input thereto, for selectively activating one sense amplifying means to sense and amplify data on said selected data lines of one of said two column-selected memory blocks, and for selectively

CLAIM	RESPONSE
	activating at least one other sense amplifying means to refresh data to said each memory cell along said selected word lines; ...." ['754 Reference, Page 6:53-7:5] This limitation is met by the '297 Reference in combination with the '754 Reference.
(2) a predetermined number of other sense amplifier circuits whose output signals will be transferred next to said output of said memory if said operation continues sufficiently long.	The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58] "A semiconductor dynamic memory device comprising: ... a plurality of sense amplifying means (18-1 to 18-4; SA1 to SA8) responsive to a control signal input thereto, for selectively activating one sense amplifying means to sense and amplify data on said selected data lines of one of said two column-selected memory blocks, and for selectively activating at least one other sense amplifying means to refresh data to said each memory cell along said selected word lines; ...." ['754 Reference, Page 6:53-7:5]
10. The memory of claim 7 wherein:	
said set of locations comprises k subsets S-1, . . . , S-k wherein k is greater than or equal to two, such that, for a positive	This limitation is met by the '297 Reference. Specifically, the '297 Reference states: "An entire chip is divided into N blocks (N = n x m) in accordance with a desired

CLAIM	RESPONSE
integer m and for any subset S-i, the contents of m consecutively addressed locations from said subset S-i can be transferred simultaneously to said plurality of sense amplifier circuits; and	rectangular group of bits (n x m bits). The same row decoder is provided for every m blocks, and a row address $\bar{A}_r$ or a row address $\bar{A}_{r+1}$ adjacent thereto is given to the row decoders. * * * N bits of memory cells are accessed from the blocks, and the accessed memory cells are rearranged, thereby obtaining a desired rectangular group of bits." ['297 Reference, Abstract]. See, e.g., Figs. 6, 7, 9, 10, 21, 22 and 23.
in said operation, time tARA does not exceed m * (k-1) * (tOE), wherein: tARA is measured from the time that an address of the first location to be read out in said operation is made available to said memory to the time when said plurality of sense amplifier circuits develops an output signal indicative of the contents of said first location; and tOE is the time to transfer the contents of any one of said locations from said plurality of sense amplifier circuits to said output.	A person of skill in the art would know that this timing relationship would be used when designing the memory disclosed in claim 1.
11. The memory of claim 8 wherein, in said operation, each location to be read out except the first location to be read out is read out to said output in a shorter time than the first location to be read out.	This element is met for the '297 Reference alone or in combination with the '587 Reference or the '003 Reference or the '199 Reference. The '297 Reference states: "The second embodiment of FIG. 21 will be explained in more detail with reference to FIG. 22. In FIG. 22, elements for a serial access mode are added to the elements of FIG. 7.

CLAIM	RESPONSE
	That is, a shift register SR_{ij} is arranged along the row direction of each of the cell blocks B_{ij} (i=0~3, j=0~3), and the output SRO_{ij} is connected to multiplexers MPX0 to MPX3. Further, the sequence of serial data buses SRD_0 to SRD_3 of the multiplexer MPX0 to MPX3 is changed by a bus arranging circuit BAC2, and is connected to input/output terminals SIO_0 to SIO_3 for a serial access mode. Also, in a serial access mode, the row-side switches RSW0 to RSW3 are operated in the same way as in a random access mode, and as a result, the voluntary four rows Y_0, Y_0+1, Y_0+2, and Y_0+3 (Y_0 is the row address of the pointing bit PB) are selected. Then, the rows are simultaneously transmitted in parallel via transfer gates to the shift registers of 1024 bits x 4 rows. Note that the 1024 bit x one row shift register is comprised of shift registers SR_{i0}, SR_{i1}, SR_{i2}, and SR_{i3} provided in parallel to the four cell blocks. Subsequently, data is read out of the 1024 bits x 4 rows shift registers at a high speed clock rate such as about 20 to 30 MHz without addresses at an asynchronous mode of a random access and a serial access." ['297 Reference, 13:23-47] See, FIGs. 21, 22 of '297 Reference. The '587 Reference states: "The reduction in the memory access cycle time from a convention memory access operation, generally represented by the first prefetch with a three clock cycle span between event t1 and t2, is clearly evident when the times are compared to those of the consecutive prefetch operation extending for two clock cycles between corresponding time intervals t3 and t4. Time t2 and t4 identify the first clock interval suitable to initiate succeeding memory access operations." ['587 Reference, Col. 5:63-6:3] The '003 Reference states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the

CLAIM	RESPONSE
	second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer. Typically, the access addresses of these 'extra' storage cells differ from the original access address by only one or two bits. However, subsequent accesses to these cells can be accomplished by simply executing additional access cycles without changing the access address. In the art, such memories are referred to as 'nibble mode'. In some other integrated circuit memories, a portion of the original address can be 'assumed' for one (or more) subsequent accesses, so that only the least significant portion of the address needs to be decoded, etc. Thus, once the original access had been completed, subsequent accesses to 'related' storage cells will be significantly quicker." ['199 Reference, Col. 1:13-28]
12. The memory of claim 8 wherein the	This element is met in the '297 Reference. Specifically, the '297 Reference states that:

CLAIM	RESPONSE
sequence of locations L1, . . . , Ln is a sequence of increasing order of addresses.	"Thus, in a serial access mode, n rows such as four rows adjacent to a voluntary position of the logic bit map plane are accessed, and the rows are accessed in the sequence of the adjacent row by the arranging circuit by BAC2. Therefore, it is possible to access a desired n-rows bit group as well as a desired rectangular bit group." ['297 Reference, 13:16-22]
13. The memory of claim 7 wherein in said operation any number of said locations addressed consecutively with wrap around can be read out to said output so that:	This element is met by the '297 Reference alone or in combination with any of the '587 Reference or the '003 Reference or the '199 Reference. The '297 Reference states that: "That is, in a serial access mode, n rows such as four rows adjacent to a voluntary proposition of the logic bit map plane, are accessed in the sequence of the adjacent row data by the arranging means." ['297 Reference, 2:47-51] "Another object of the present invention is to provide a boundary-free semiconductor memory device in which a voluntary adjacent n-row bit group can be accessed in a serial access mode." ['297 Reference, 1:67-2:2] See also, '297 Reference, 13:1-47 and FIGs. 6, 7, 21 and 22. The '587 Reference states: "The reduction in the memory access cycle time from a convention memory access operation, generally represented by the first prefetch with a three clock cycle span between event t1 and t2, is clearly evident when the times are compared to those of the consecutive prefetch operation extending for two clock cycles between corresponding time intervals t3 and t4. Time t2 and t4 identify the first clock interval suitable to initiate succeeding

CLAIM	RESPONSE
	memory access operations." ['587 Reference, Col. 5:63-6:3] The '003 Reference states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer. Typically, the access addresses of these 'extra' storage cells differ from the original access address by only one or two bits. However, subsequent accesses to these cells can be accomplished by simply executing additional access cycles without changing the access address. In the art, such memories are referred to as 'nibble mode'. In some other

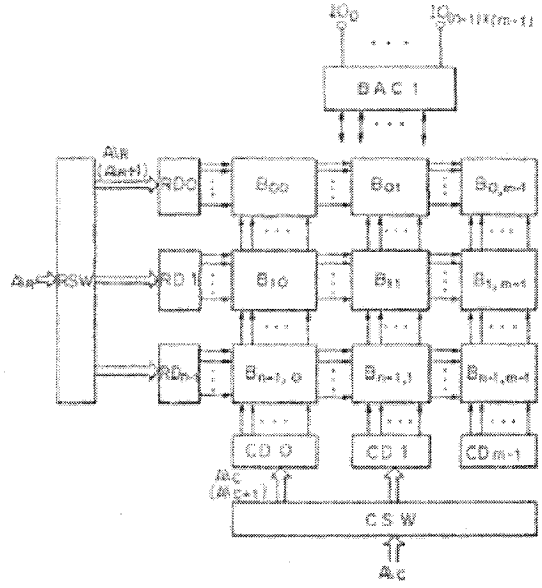
CLAIM	RESPONSE
	integrated circuit memories, a portion of the original address can be 'assumed' for one (or more) subsequent accesses, so that only the least significant portion of the address needs to be decoded, etc. Thus, once the original access had been completed, subsequent accesses to 'related' storage cells will be significantly quicker." ['199 Reference, Col. 1:13-28]
the first location to be read out in said operation is read out to said output after time tARA+tOE wherein: tARA is measured from the time that an address of said first location is made available to said memory to the time when said plurality of sense amplifier circuits develops an output signal indicative of the contents of said first location; and tOE is the time to transfer the contents of any one of said locations from said plurality of sense amplifier circuits to said output of said memory; and	This element is met by the '297 Reference in combination with any of the '587 Reference or the '003 Reference or the '199 Reference. The '587 Reference states: "The reduction in the memory access cycle time from a convention memory access operation, generally represented by the first prefetch with a three clock cycle span between event t1 and t2, is clearly evident when the times are compared to those of the consecutive prefetch operation extending for two clock cycles between corresponding time intervals t3 and t4. Time t2 and t4 identify the first clock interval suitable to initiate succeeding memory access operations." ['587 Reference, Col. 5:63-6:3] The '003 Reference states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13]

CLAIM	RESPONSE
	"In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer. Typically, the access addresses of these 'extra' storage cells differ from the original access address by only one or two bits. However, subsequent accesses to these cells can be accomplished by simply executing additional access cycles without changing the access address. In the art, such memories are referred to as 'nibble mode'. In some other integrated circuit memories, a portion of the original address can be 'assumed' for one (or more) subsequent accesses, so that only the least significant portion of the address needs to be decoded, etc. Thus, once the original access had been completed, subsequent accesses to 'related' storage cells will be significantly quicker." ['199 Reference, Col. 1:13-28]
every other location to be read out in said operation is read out to said output within time tOE.	This element is met by the '297 Reference in combination with any of the '587 Reference or the '003 Reference or the '199 Reference. The '587 Reference states: "The reduction in the memory access cycle time from a convention memory access operation, generally represented by the first prefetch with a three clock cycle span between event t1 and t2, is clearly evident when the times are compared to those of the consecutive prefetch operation extending for two clock cycles between corresponding time intervals t3 and t4. Time t2 and t4 identify the first clock interval suitable to initiate succeeding

CLAIM	RESPONSE
	memory access operations." ['587 Reference, Col. 5:63-6:3] The '003 Reference states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer. Typically, the access addresses of these 'extra' storage cells differ from the original access address by only one or two bits. However, subsequent accesses to these cells can be accomplished by simply executing additional access cycles without changing the access address. In the art, such memories are referred to as 'nibble mode'. In some other

CLAIM	RESPONSE
	integrated circuit memories, a portion of the original address can be 'assumed' for one (or more) subsequent accesses, so that only the least significant portion of the address needs to be decoded, etc. Thus, once the original access had been completed, subsequent accesses to 'related' storage cells will be significantly quicker." ['199 Reference, Col. 1:13-28]
14. The memory of claim 8 wherein said memory is fabricated in an integrated circuit.	This element is met by the '297 Reference alone or in combination with any of the '754 Reference, the '199 Reference, or the '312 Reference. The '297 Reference is entitled "Boundary-Free Semiconductor Memory Device." Moreover, the '297 Reference Abstract begins by saying "An entire chip is divided into . . ." Further, it was well known in the art to fabricate memories as an integrated circuit and a person of ordinary skill would have know that the memory device shown in the '297 Reference could be fabricated in an integrated circuit. The '754 Reference states: "The present invention relates to a semiconductor dynamic memory device. Mass-production of 64K bit dynamic type random access memory devices (DRAMs) has been enabled by the recent development of semiconductor memory devices of high packing density. Furthermore, a 256K bit DRAM has been developed." ['754 Reference, Page 2:1-4] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer." ['199 Reference, Col. 1:13-16] The '312 Reference states:

CLAIM	RESPONSE
	"The individual circuit elements constructing the RAM of the present embodiment are formed on a semiconductor substrate such as a piece of single-crystalline silicon by the known technique for fabricating a CMOS (i.e., Complementary MOS) integreated circuit." ['312 Reference, Col. 2:34-38]
20. An integrated memory comprising:	
an array of memory locations, the array comprising a plurality of subarrays, each subarray comprising a predetermined number of groups of columns of the memory locations such that for any given column position in a group, the memory locations in any given row in the columns at said given position in the groups of the subarray have consecutive addresses;	This limitation is met by the '297 Reference. Specifically, the Abstract and FIGs. 6, 7, 21 and 22 show this limitation. "An entire chip is divided into N blocks (N = n x m) in accordance with a desired rectangular group of bits (n x x bits). The same row decoder is provided for every m blocks, and a row address $\bar{A}_r$ or a row address $\bar{A}_{r+1}$ adjacent thereto is given to the row decoders. * * * "N bits of memory cells are accessed from the blocks, and the accessed memory cells are rearranged, thereby obtaining a desired rectangular group of bits." ['297 Reference, Abstract]. See, e.g., FIG. 6:

CLAIM	RESPONSE
	Fig. 6 
one X-decoder for each subarray;	The '297 Reference meets this limitation. Specifically, the '297 Reference states: "An entire chip is divided into N blocks (N = n x m) in accordance with a desired rectangular group of bits (n x m bits). The same row decoder is provided for every m blocks, and a row address $\bar{A}_r$ or a row address $\bar{A}_{r+1}$ adjacent thereto is given to the row decoders. * * * N bits of memory cells are accessed from the blocks, and the accessed memory cells are rearranged, thereby obtaining a desired rectangular group of bits." ['297 Reference, Abstract].

CLAIM	RESPONSE
	See, e.g., Figs. 6, 7, 21, 22.
one X-register for each X-decoder;	This element is met by the '297 Reference alone or in combination with any of the '196 Reference or the '937 Reference or the '495 Reference or the '021 Reference. To the extent that AMD reads this limitation on the Samsung devices, the '297 Reference meets this limitation. The '196 Reference states that: "The row and column location in the arrays 31, 33 at which data is accessed is controlled by the counters which, in one embodiment of the invention may be binary counters, or the like, which have an extended counting range that is double the number of address locations in the array to be accessed." '196 Reference, 4:49-54; See also, FIGS. 2A, 2B. The '495 Reference states: "The register 70a, 70b, 70c or 70d selected by the block decoder 50 holds 8-bit address codes ARC0-ARC7 supplied in synchronism with the row selection signal RAS. Since the holding of the address codes ARC0-ARC7 will be maintained even after access is shifted to another cell array block, these registers 70a-70d store respectively the address codes ARC0-ARC7 of the last access in the cell array blocks 10a-10d and supply them to the selectors 80a and 80d which also receive the address codes ARC0-ARC7 supplied in synchronism with the row selection signal RAS and introduce them to the row decoders 20a to 20d." ['495 Reference, Col. 4:25-37] The '937 Reference states:

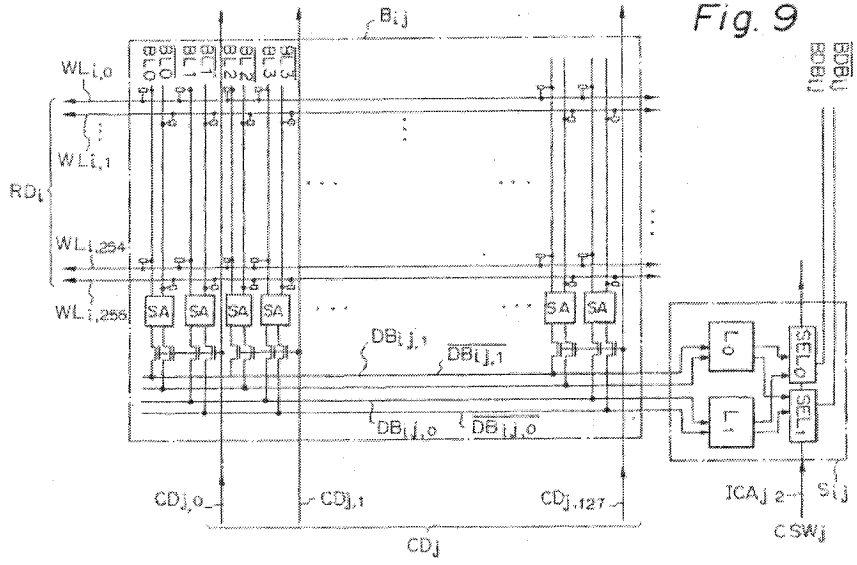
CLAIM	RESPONSE
	"The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e. twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e. twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42] The '021 Reference states: "Since the low-speed large-capacity memories 11, 12, 13, 14 performing the 4-way interleave operation are shifted in access timing usually by one cycle from each other, the memories 11 14 are provided respectively with registers 23 26 each for holding an address." ['021 Reference, Col. 4:5-9]
one Y-decoder for each subarray;	This element is met by the '297 Reference alone or in combination with any of the '937 Reference and '196 Reference or the '495 Reference or the '021 Reference. Specifically, the '297 Reference states that: ". . . as illustrated in FIG. 10, memory cells are provided at every other intersection of a pair of bit lines and word lines on one side of each sense amplifier SA. Note that the sense amplifier SA of FIG. 10 is comprised of p-channel transistors between a line PSA and bit lines BL0 and BL0, and N-channel transistors between a line NSA and bit lines BL0 and $\overline{BL0}$, and when the lines PSA and NSA are made high and low, respectively, the sense

CLAIM	RESPONSE
	amplifier SA is operated. Also, in FIG. 9, the row decoder RD_i selects one word line from 256 word lines $WL_{i,0}$, $WL_{i,1}$, . . . , and $WL_{i,225}$, while the column decoder CD_j selects two pairs of bit lines such as BL0 and BL0; and BL1 and $\overline{BL1}$ by the column selection signals $CD_{j,0}$, $CD_{j,1}$, . . . , and $CD_{j,127}$ thereof, and connects them to data buses $DB_{ij,0}$ and $\overline{DB}_{ij,0}$; $DB_{ij,1}$ and $\overline{DB}_{ij,1}$ within the block, and further, one pair of the two paires of the data buses $DB_{ij,0}$ and $\overline{DB}_{ij,0}$; $DB_{ij,1}$ and $\overline{DB}_{ij,1}$ within the block is selected by a switch S_{ij} and is connected to block data buses BDB_{ij} and $\overline{BDB}_{ij}$." ['297 Reference, 8:26-45]. See also, '297 Reference, 13:48-14:14, 14:59-15:7, FIGs. 9, 10, 23. The '937 Reference states: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e., twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e., twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42] The '196 Reference states: "Referring now to FIGS. 2A and 2B, there is shown a block schematic diagram of a pair of RAM arrays 31, 33, each comprising a plurality of individual memory cells of the type

CLAIM	RESPONSE
	illustrated and described above with reference to FIGS. 1A and 1B. Each of these arrays may be configured to store data in a matrix of rows and columsn [sic] that is several columns long and several rows deep (e.g. 72 X128). The columns and rows of memory cells in each array are connected to decoders for writing and reading data into and out of selected memory cells in the arrays. Specifically, the write column decoders 35, 37 are connected to the dual arrays to address selected columns of memory cells, and the write row decoders and drivers 39, 41 are connected to the dual arrays to address selected rows of memory cells. Similarly, the read column decoders 45, 47 are connected to the dual arrays to address selected columns of memory cells , and the read row decoders and drivers 49, 51 are connected to the dual arrays to address selected rows." ['196 Reference, Col. 3:11-29; See also FIGS 1A, 1B, 2A.] "The row and column location in the arrays 31, 33 at which data is accessed is controlled by the counters which, in one embodiment of the invention may be binary counters, or the like, which have an extended counting range that is double the number of address locations in the array to be accessed." ['196 Reference, Col. 4:49-54; See also, FIGS. 2A, 2B.] The '495 Reference states: "The output of the block decoder 50 is supplied in common to the row decoders 20a and 20d and the column decoders 40a to 40d. As a result, one word line is selected in the memory cell array block 10a, for example." ['495 Reference, Col. 3:39-42] The '937 Reference states: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e., twice that of the basic clock pulses $Ø_{S}$). Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $Ø_{OD}$ to

CLAIM	RESPONSE
	supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e., twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." '937 Reference, Col. 4:29-42 The '021 Reference states: "In FIG. 1, numeral 100 designates clock signals to be supplied to the interleave controller 20, the select controller 30 and the high-speed memory access controller 40, numerals 111, 112, 113, 114 designate output data from the low-speed large-capacity memories 11, 12, 13, 14 respectively, numeral 120 designates an address signal to be supplied to the interleave controller 20, numerals 121, 122, 123, 124 designate address signals from the interleave controller 20 to the low-speed large-capacity memories 11, 12, 13, 14 respectively, ..." ['021 Reference, Col. 3:43-68] Each memory 11, 12, 13, and 14 would have a y-decoder.
one Y-register for each Y-decoder;	The '297 Reference meets this limitation in combination with any of the '937 Reference, . To the extent AMD claims that the accused Samsung devices practice this limitation, this limitation is disclosed in the '297 Reference. The '937 Reference states that: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e., twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and Y add address signals to a Y decoder

CLAIM	RESPONSE
	93 in the cycle of the signals $Ø_{OD}$ (i.e. twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42]
one Y-select circuit for each subarray, the Y-select circuit being responsive to the Y-decoder of the subarray to select all the columns that occupy a selected position in the groups of the subarray;	This limitation is met by the '297 Reference. Specifically, See FIGs. 6, 7, 21, 22.
a plurality of sense amplifier circuits for each subarray, each sense amplifier circuit for amplifying signals from a column selected by the Y-select circuit of the subarray;	This element is met by the '297 Reference. Specifically, the '297 Reference states: ". . . as illustrated in FIG. 10, memory cells are provided at every other intersection of a pair of bit lines and word lines on one side of each sense amplifier SA. Note that the sense amplifier SA of FIG. 10 is comprised of p-channel transistors between a line PSA and bit lines BL0 and $\overline{BLO}$, and N-channel transistors between a line NSA and bit lines BL0 and $\overline{BLO}$, and when the lines PSA and NSA are made high and low, respectively, the sense amplifier SA is operated." ['297 Reference, 8:26-35].
a memory output; and	This element is met by the '297 Reference. FIG. 9 of the '297 Reference shows output lines and an output buffer (a data bus latch) connected to the sense amplifiers:

CLAIM	RESPONSE
	
	Moreover, it is inherent in the '297 Reference that there is an output for providing output signals from the sense amplifiers.
a control circuit for selecting one of the sense amplifier circuits to provide data to the memory output;	This limitation is met by the '297 Reference, alone or in combination with the '788 Reference or the '937 Reference or the '003 Reference or the '178 Reference or the '754 Reference. Specifically, the '297 Reference states: "Also, the control circuit CONT receives external signals such as a chip enable signal $\overline{CE}$, a batch transfer signal $\overline{TR}$ for a serial access mode, a read/write signal R/W, and a serial clock signal SCLK and generates various internal signals such as the batch transfer signal

CLAIM	RESPONSE
	TR, the shift clock signals P1 and P2, and the serial clock signal SC. For example, the external shift clock signal SCLK is buffered to generate an internal shift clock signal SC which is four-divided to generate the shift clock signals P1 and P2. Further, the internal batch transfer signal TR is generated from the chip enable signal $\overline{CE}$ and the external transfer signal $\overline{TR}$." ('297 Reference, 13:51-14:3.) See also, '297 Reference, 14:4-14:14, 14:59-15:7, FIGs. 9, 10, 23. Further, this element was well-known in the art. The following are illustrative: The '788 Reference states: "According to this arrangement, only one plane is selected in accordance with the content of the upper-order two bits of the row address. The selected plane is activated and exhibits the memory operation but the rest of the planes which are under the non-selection state are inoperative. Therefore, the decoders and the sense amplifiers are inoperative in these inoperative planes and the memory is not refreshed. Therefore, power is consumed in only the selected plane and unnecessary power consumption in the other plane can be saved. Thus, the requirement for low power consumption can be satisfied." ['788 Reference, Col. 5:57-68] The '937 Reference states: "The sense amplifier 86 is controlled by the signals SE_{EV} to simplify the read data thereby to supply the same to the data latch 87, which in turn temporarily stores the outputs from the sense amplifiers 86. When the signals SE_{EV} are at low levels, the data latch 87 is electrically cut off from the sense amplifier 86. Data from the data latch 87 are transferred to the output latch 89 when the signals OE_{EV} are at high levels. In a similar manner, the

CLAIM	RESPONSE
	sense amplifier 96 is controlled by the signals SE_{OD} to amplify the read data thereby to supply the same to the data latch 97, which in turn temporarily stores the outputs from the sense amplifier 96. When the signals SE_{OD} are at low levels, the data latch 97 is electrically cut off from the sense amplifier 96." ['937 Reference, Col. 4:52-66] The '003 Reference states: "The flash memory control 88 also selectively enables one of two sets of bi-directional data buffers 90 and 91 which respectively couple the bank data buses 82 and 83 to the processor section data bus 63. The bank data buses 82 and 83 can be coupled to the instruction bus 61 by the flash memory control 88 selectively enabling buffers 92 and 93, respectively." ['003 Reference, Col. 9:21-27] The '178 Reference states: "Referring now to FIG. 2, the circuit of FIG. 1 has been modified to utilize the fact that, when RA10=1, only one half of the ARRAY BANKs 20 are being utilized and that, when RA10=0, the other half of the ARRAY BANKs 20 are being utilized. In particular, the RA 10 address is used to cause only the half of the ARRAY BANKs 20 that are being utilized to draw power from the DRAM energy source during read/write operations, while at the same time permitting the periodic performance of the refresh cycle in the usual manner on all ARRAY BANKs." ['178 Reference, Col. 3:32-42] The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense

CLAIM	RESPONSE
	amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58]
wherein in a burst mode read operation, at least one X-register provides to its respective X-decoder signals identifying a row in one of the subarrays, and at least one Y-register provides to its respective Y-decoder signals identifying a position of columns in the groups of one of the subarrays.	This limitation is met by the '297 Reference alone or in combination with any of the '937 Reference or the '196 Reference or U.S. Patent No. 5,036,494 ("the '494 Reference") or admitted prior art disclosed in Figure 2 of the '990 patent. The '297 Reference states: "Another object of the present invention is to provide a boundary-free semiconductor memory device in which a voluntary adjacent n-row bit group can be accessed in a serial access mode." ['297 Reference, 1:67-2:2] See also, '297 Reference, 13:1-47 and FIGs. 6, 7, 21 and 22. The '937 patent states that: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e., twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder

CLAIM	RESPONSE
	93 in the cycle of the signals $Ø_{OD}$ (i.e., twice that of the basic clock pulses $Ø_{S}$). Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42] The '196 Reference states that: "In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit lines in the other array are being precharged. Thus, as data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit lines in that array will already have been initialied." '196 Reference, Col. 2:60-67 "In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and settling transient signals) in preparation for the next access form such other array. Therefore, precharging times for one array overlap the time for performing read or write operation in the other array, and therefore do not limit operating speed." ['196 Reference, Col. 3:41-47] The '494 Reference states: In the example shown in FIG. 1 each memory block 14 and 15 has sixty four columns 35, each column being coupled to equate and precharge circuitry 36. The columns are arranged in groups, each group having eight pairs of bit lines so that when any column is addressed eight pairs of bit lines (one in each group) are simultaneously accessed, permitting transfer of eight bits or one word at a time. The bit lines are each connected to column multiplexing circuitry 37 for each column and coupled to sense amplifier and write circuitry 38 for each column. Each sense amplifier and write circuit is connected through a bus driver circuit 39 to the data output 17. Each memory block 14 and 15 has 70 rows each having a word line 25. The word lines are connected to a row decoder 40. The row

CLAIM	RESPONSE
	decoder is coupled to memory block 14 through a latch and word line driver 41 and to the memory block 15 through a latch and word line driver 42. The column multiplex circuitry 37 is controlled by a column counter 44. The row decoder 40 is controlled by a row counter 45. The latch and word line drivers 41 and 42 are controlled by pulse generators 46 and 47 respectively. Each of the drivers 41 and 42 is connected by two separate control lines 48 to the respective one of the pulse generators 46 and 47 so that each driver can be operated either to latch the output of the row decoder 40 or to drive all the word lines low. The selection of memory locations forming each cyclic pattern of addressing is controlled by the control until 13. The row counter 45 and columns counter 44 are connected so that unless instructed by the control 13 to do otherwise they count through successive addresses along each row and then row by row." ['494 Reference, Col. 7:44-8:27] Further, the '990 patent discloses prior art Figure 2 showing an embodiment with a burst mode operation. A person of skill in the art would know to implement a burst mode operation with the circuitry of the '937 Reference to provide faster memory access. ['990 Reference, Col. 1:36-44]
22. The memory of claim 20 wherein in the burst mode read operation while data from the sense amplifier circuits of one of the subarrays are provided to the memory output, the sense amplifier circuits of another one of the subarrays develop output signals corresponding to data in said other one of the subarrays.	This element is met by the '494 Reference in combination with the '196 Reference or the '494 Reference. The '196 Reference states that: "In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit lines in the other array are being precharged. Thus, as data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit lines in that array will already have been initialied." ['196 Reference, Col. 2:60-67]

CLAIM	RESPONSE
	"In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and settling transient signals) in preparation for the next access form such other array. Therefore, precharging times for one array overlap the time for performing read or write operation in the other array, and therefore do not limit operating speed." ['196 Reference, Col. 3:41-51] The '494 Reference states: "The selection of memory locations forming each cyclic pattern of addressing is controlled by the control unit 13. The row counter 45 and column counter 44 are connected so that unless instructed by the control 13 to do otherwise they count through successive addresses along each row and then row by row." ['494 Reference, Col. 8:22-27] "Consequently after reaching address 0 the column and row counters cycle sequentially along each row for the two memory blocks in turn (starting at column zero of row 0 in array 0) using all memory locations in each row and then moving to the next row and repeating the operation." ['494 Reference, Col. 11:26-31] "addressing sequentially more than one memory location in said first memory block and effecting a data transfer for each memory location addressed, and at the same time effecting an equate operation on bit lines in said second memory block; and after addressing memory locations in said first memory block, switching said addressing and equate operation so as to address sequentially more than one memory location in said second memory block and effecting a data transfer for each memory location addressed and at the same time equating bit lines in said first memory block." ['494 Reference, Col. 13:36-48]
23. The memory of claim 20 wherein in the burst mode read operation, the control circuit enables the sense	This limitation is met by the '297 Reference. Specifically, the '297 Reference states: ""Another object of the present invention is to provide a boundary-free semiconductor

CLAIM	RESPONSE
amplifier circuit selected to provide data to the memory output and at the same time disables one or more sense amplifier circuits not selected to provide data to the memory output.	memory device in which a voluntary adjacent n-row bit group can be accessed in a serial access mode." ['297 Reference, 1:67-2:2] "Also, the control circuit CONT receives external signals such as a chip enable signal $\overline{CE}$, a batch transfer signal $\overline{TR}$ for a serial access mode, a read/write signal R/W, and a serial clock signal SCLK and generates various internal signals such as the batch transfer signal TR, the shift clock signals P1 and P2, and the serial clock signal SC. For example, the external shift clock signal SCLK is buffered to generate an internal shift clock signal SC which is four-divided to generate the shift clock signals P1 and P2. Further, the internal batch transfer signal TR is generated from the chip enable signal $\overline{CE}$ and the external transfer signal $\overline{TR}$." ('297 Reference, 13:51-14:3.) See also, '297 Reference, 13:1-47 and FIGs. 6, 7, 21 and 22.