Goodard v. Google, Inc.
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EXHIBIT 1

C1-C5

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Appendix C1

Defendants and Counterclaimants' Invalidity Contentions

Advanced Micro Devices, Inc. et al. v. Samsung Electronics Co., Ltd. et al., Case No. CV-08-0986-SI

U.S. Patent No. 5,248,893 Invalidity Chart: K. Sunouchi, et. al., *Double LDD Concave (DLC) Structure for Sub-Half Micron MOSFET*, IEDM 88, pp. 226-29 ("Sunouchi")

All asserted claims are anticipated by the Sunouchi and/or are rendered obvious by it, either alone or in combination with other prior art described below and/or listed in Section I of Defendants' and Counterclaimants' Preliminary Invalidity Contentions and/or through modifications described below. Nothing in this invalidity chart should be construed as signifying or suggesting Defendants and Counterclaimants' adoption of or acquiescence in any claim scope and/or claim construction positions taken by Plaintiffs and Counterdefendants in this litigation.

To the extent a feature of the claims may not be disclosed or suggested by Sunouchi alone, one of skill in the art would know to consider Natori, et. al., *An Analysis of the Concave MOSFET*, IEEE Transactions on Electron. Devices, Vol. ED-25, No. 4, April 1978 ("Natori"), especially since Sunouchi and Natori both discuss the same subject matter, *viz.*, concave transistors.

U.S. Patent No. 5,248,893	
Claim 1	
Claim limitation	**Sunouchi**
1 An insulated gate field effect device comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, Sunouchi discloses this limitation. *See, e.g.*, Sunouchi at 226 ("A new concave structure MOSFET ... was developed....").
a first conductivity type semiconductor substrate having a main surface;	*See, e.g., id.* at Fig. 1.
said semiconductor substrate having a concave surface formed on said main surface extending to a prespecified depth below the main surface;	*See, e.g., id.* at Figs. 1-2; *see, e.g., id.* at 226 ("The silicon substrate is etched to 0.5 um depth, using the oxide mask.").
an insulating film formed on said concave surface;	*See, e.g., id.* at Figs. 1-2; *see, e.g., id.* at 226 ("After gate oxidation (20nm), the gate poly silicon is patterned, and the n^+ source and drain region is fabricated by arsenic (As^+) implantation (Fig. 2(C)).").
a conductive gate electrode formed above said insulating film, overlying	*See, e.g., id.* at Figs. 1-2; *see, e.g., id.* at 226 ("After gate oxidation (20nm), the gate poly silicon is patterned,

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the concave surface;	and the n^+ source and drain region is fabricated by arsenic (As^+) implantation (Fig. 2(C)).") .
first and second impurity regions of a second conductivity type respectively formed in the substrate, in the vicinity of said main surfaces, self-aligned to and positioned at one side and the other side of said gate electrode respectively; and	*See*, *e.g.*, *id.* at Figs. 1-2; *see*, *e.g.*, *id.* at 226 ("After gate oxidation (20nm), the gate poly silicon is patterned, and the n^+ source and drain region is fabricated by arsenic (As^+) implantation (Fig. 2(C)).") .
a first conductivity type region located in said semiconductor substrate between said first and second impurity regions for defining a channel region and a channel-free region extending conformably under and along said concave surface;	*See*, *e.g.*, *id.* at Figs. 1-2; *see*, *e.g.*, *id.* at 226 ("Then, boron (B^+) is implanted to the bottom of the groove as channel implantation (Fig. 2(B)). After gate oxidation (20nm), the gate poly silicon is patterned, and the n^+ source and drain region is fabricated by arsenic (As^+) implantation (Fig. 2(C)).") .
wherein the depth of said concave surface is set to a value which ranges between one and two times the depth of said first and second impurity regions, and	*See*, *e.g.*, *id.* at Figs. 1-2.
wherein the concave surface is continuously curved in the vicinity of at least one of the first and second impurity regions to produce smooth merger of a conforming first depletion region formed around the at least one impurity region and a conforming second depletion region	*See*, *e.g.*, *id.* at Figs. 1-2, 4, 6, and 8; *see*, *e.g.*, *id.* at 227 ("The short channel effects of DLC as a function of channel length, compared with planar MOSFETs, are shown in Fig. 4."); *see*, *e.g.*, *id.* ("Figure 6 shows Id-Vd characteristics, compared with conventional MOSFETs with the same geometrical channel length."); *see*, *e.g.*, *id.* ("The DLC is an ideal structure for reducing the electric field at the drain. … For the DLC structure, degradation in drain current Ids as a function of stress time is shown in Fig.8, compared with conventional concave MOSFETs and planar MOSFETs. … It is found that drain current degradation dIds/Idso in DLC is smaller than that in the planar MOSFET and conventional concave structure. This result indicates that the

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formed in the vicinity of the gate electrode so that excessive field concentration will not develop in the vicinity where the first and second depletion regions meet.	carrier injection into gate-oxide is reduced in DLC, because of reduced electric field at the drain.").
Claim 2	
Claim limitation	**Sunouchi**
2. An insulated gate field effect device according to claim 1, wherein one of said first and second impurity regions constitutes a drain region of said insulated gate field effect device, the other of said first and second impurity regions constitutes a source region and wherein the concave surface is continuously curved at least in the vicinity of the drain region, where the channel-free region develops during an off state of the device, to produce smooth merger of the conforming first depletion region which develops in the vicinity of the channel-free region and the drain region and the conforming second depletion region formed in the vicinity of the gate electrode so that excessive field concentration will not develop in the vicinity of the	*See, e.g., id.* at Figs. 1-2, 4, 6, and 8; *see, e.g., id.* at 226 ("Then, boron (B^+) is implanted to the bottom of the groove as channel implantation (Fig. 2(B)). After gate oxidation (20nm), the gate poly silicon is patterned, and the n^+ source and drain region is fabricated by arsenic (As^+) implantation (Fig. 2(C))."); *see, e.g., id.* at 227 ("The short channel effects of DLC as a function of channel length, compared with planar MOSFETs, are shown in Fig. 4."); *see, e.g., id.* ("Figure 6 shows Id-Vd characteristics, compared with conventional MOSFETs with the same geometrical channel length."); *see, e.g., id.* ("The DLC is an ideal structure for reducing the electric field at the drain. … For the DLC structure, degradation in drain current Ids as a function of stress time is shown in Fig.8, compared with conventional concave MOSFETs and planar MOSFETs. … It is found that drain current degradation dIds/Idso in DLC is smaller than that in the planar MOSFET and conventional concave structure. This result indicates that the carrier injection into gate-oxide is reduced in DLC, because of reduced electric field at the drain.").

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channel-free region.	
Claim 3	
Claim limitation	**Sunouchi**
3. An insulated gate field effect device according to claim 1, which comprises a metal oxide semiconductor (MOS) transistor, and wherein said insulating film comprises an oxide film.	*See, e.g., id.* at 226 ("A new concave structure MOSFET … was developed…."); *see, e.g., id.* ("After gate oxidation (20nm), the gate poly silicon is patterned, and the n+ source and drain region is fabricated by arsenic (As+) implantation (Fig. 2(C))."); *see, e.g., id.* at Figs. 1-2.
Claim 4	
Claim limitation	**Sunouchi**
4. An insulated-gate field effect transistor comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, Sunouchi discloses this limitation. *See, e.g.,* Sunouchi at 226 ("A new concave structure MOSFET … was developed….").
a substrate having a substantially planar main surface and a concave surface portion extending continuously from the main surface to a predetermined depth below the main surface;	*See, e.g., id.* at Figs. 1-2; *see, e.g., id.* at 226 ("The silicon substrate is etched to 0.5 um depth, using the oxide mask.").
an insulating layer conformably disposed on the main surface and the concave surface portion;	*See, e.g., id.* at Figs. 1-2; *see, e.g., id.* at 226 ("After gate oxidation (20nm), the gate poly silicon is patterned, and the n^+ source and drain region is fabricated by arsenic (As^+) implantation (Fig. 2(C)).").
a gate conformably disposed on the insulating layer, overlying the concave surface portion, the gate	*See, e.g., id.* at Figs. 1-2; *see, e.g., id.* at 226 ("After gate oxidation (20nm), the gate poly silicon is patterned, and the n^+ source and drain region is fabricated by arsenic (As^+) implantation (Fig. 2(C)).").

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having opposed first and second sides;	
implanted source and drain regions disposed within the substrate and self-aligned to the respective first and second opposed sides of the gate; and	*See, e.g., id.* at Figs. 1-2; *see, e.g., id.* at 226 ("After gate oxidation (20nm), the gate poly silicon is patterned, and the n^+ source and drain region is fabricated by arsenic (As^+) implantation (Fig. 2(C)).").
a channel-region formed between the source and drain regions, for defining a channel that conducts current between the source and drain regions when the transistor is in a turned-on state;	*See, e.g., id.* at Figs. 1-2; *see, e.g., id.* at 226 ("Then, boron (B^+) is implanted to the bottom of the groove as channel implantation (Fig. 2(B)). After gate oxidation (20nm), the gate poly silicon is patterned, and the n^+ source and drain region is fabricated by arsenic (As^+) implantation (Fig. 2(C)).").
wherein a channel-free zone develops in the substrate, under the gate and between the source and drain regions, when the transistor is in a turned-off state; and	*See, e.g., id.* at Figs. 1-2, 4, 6, and 8; *see, e.g., id.* at 226 ("Then, boron (B^+) is implanted to the bottom of the groove as channel implantation (Fig. 2(B)). After gate oxidation (20nm), the gate poly silicon is patterned, and the n^+ source and drain region is fabricated by arsenic (As^+) implantation (Fig. 2(C)).").
wherein the gate and concave surface portion are curved at least in the vicinity of the channel-free zone such that a smoothly curved depletion zone boundary will develop in the vicinity of the channel-free zone when the transistor is in the turned-off state.	*See, e.g., id.* at Figs. 1-2, 4, 6, and 8; *see, e.g., id.* at 227 ("The short channel effects of DLC as a function of channel length, compared with planar MOSFETs, are shown in Fig. 4."); *see, e.g., id.* ("Figure 6 shows Id-Vd characteristics, compared with conventional MOSFETs with the same geometrical channel length."); *see, e.g., id.* ("The DLC is an ideal structure for reducing the electric field at the drain. … For the DLC structure, degradation in drain current Ids as a function of stress time is shown in Fig.8, compared with conventional concave MOSFETs and planar MOSFETs. … It is found that drain current degradation dIds/Idso in DLC is smaller than that in the planar MOSFET and conventional concave structure. This result indicates that the carrier injection into gate-oxide is reduced in DLC, because of reduced electric field at the drain.").
Claim 5	

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Claim limitation	Sunouchi
5. An insulated-gate field effect transistor according to claim 4 wherein the concave surface portion is curved in a transverse cross-sectional plane extending through the transistor between but not intersecting the first and second sides of the gate so as to provide an effective channel width greater than a width of the channel as projected onto the plane of the main substrate surface.	*See, e.g., id.* at Figs. 1-2, 4; *see, e.g., id.* at 227 ("The short channel effects of DLC as a function of channel length, compared with planar MOSFETs, are shown in Fig. 4."); *see, e.g., id.* ("Figure 6 shows Id-Vd characteristics, compared with conventional MOSFETs with the same geometrical channel length."); *see, e.g., id.* ("The DLC is an ideal structure for reducing the electric field at the drain. … For the DLC structure, degradation in drain current Ids as a function of stress time is shown in Fig.8, compared with conventional concave MOSFETs and planar MOSFETs. … It is found that drain current degradation dIds/Idso in DLC is smaller than that in the planar MOSFET and conventional concave structure. This result indicates that the carrier injection into gate-oxide is reduced in DLC, because of reduced electric field at the drain.").

Claim 6

Claim limitation	Sunouchi
6. An insulated-gate field effect transistor according to claim 5 wherein the concave surface portion is curved both in the transverse cross-sectional plane and in a non-transverse cross-sectional plane, extending between and joining the first and second sides of the gate, so as to provide an effective channel surface area greater than an area of the channel as projected onto the plane of the main substrate surface.	*See, e.g., id.* at Figs. 1-2, 4; *see, e.g., id.* at 227 ("The short channel effects of DLC as a function of channel length, compared with planar MOSFETs, are shown in Fig. 4."); *see, e.g., id.* ("Figure 6 shows Id-Vd characteristics, compared with conventional MOSFETs with the same geometrical channel length."); *see, e.g., id.* ("The DLC is an ideal structure for reducing the electric field at the drain. … For the DLC structure, degradation in drain current Ids as a function of stress time is shown in Fig.8, compared with conventional concave MOSFETs and planar MOSFETs. … It is found that drain current degradation dIds/Idso in DLC is smaller than that in the planar MOSFET and conventional concave structure. This result indicates that the carrier injection into gate-oxide is reduced in DLC, because of reduced electric field at the drain."). *See also* Natori at 454 (discussing isotropic and anisotropic etching).

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Claim 7

Claim limitation	Sunouchi
7. An insulated-gate field effect transistor according to claim 6 wherein the concave surface portion is equally curved both in the transverse cross-sectional plane and in the non-transverse cross-sectional plane, so as to provide a sheet-like depletion region having a uniform thickness and a smooth bottom boundary underlying the channel region and the source and drain regions, when the transistor is in a turned-off state.	*See, e.g., id.* at Figs. 1, 4, and 6. One of skill in the art would understand that a standard etch technique would result in an equally curved concavity in the transverse and non-transverse planes. *See also* Natori at 454 (discussing isotropic etching).

Claim 11

Claim limitation	Sunouchi
11. An insulated-gate field effect transistor according to claim 4 wherein the depth of the concave surface portion is set to a value which ranges between one and two times the depth of the source and drain regions.	*See, e.g., id.* at Figs. 1-2, 4, 6, and 8; *see, e.g., id.* at 227 ("The short channel effects of DLC as a function of channel length, compared with planar MOSFETs, are shown in Fig. 4."); *see, e.g., id.* ("Figure 6 shows Id-Vd characteristics, compared with conventional MOSFETs with the same geometrical channel length."); *see, e.g., id.* ("The DLC is an ideal structure for reducing the electric field at the drain. … For the DLC structure, degradation in drain current Ids as a function of stress time is shown in Fig.8, compared with conventional concave MOSFETs and planar MOSFETs. … It is found that drain current degradation dIds/Idso in DLC is smaller than that in the planar MOSFET and conventional concave structure. This result indicates that the carrier injection into gate-oxide is reduced in DLC, because of reduced electric field at the drain.").

Appendix C2

Defendants and Counterclaimants' Invalidity Contentions

Advanced Micro Devices, Inc. et al. v. Samsung Electronics Co., Ltd. et al., Case No. CV-08-0986-SI

U.S. Patent No. 5,248,893 Invalidity Chart: Japanese Patent Application No. 52-115664 ("JPA '664")

All asserted claims are anticipated by the JPA '664 and/or are rendered obvious by it, either alone or in combination with other prior art described below and/or listed in Section I of Defendants' and Counterclaimants' Preliminary Invalidity Contentions and/or through modifications described below. Nothing in this invalidity chart should be construed as signifying or suggesting Defendants and Counterclaimants' adoption of or acquiescence in any claim scope and/or claim construction positions taken by Plaintiffs and Counterdefendants in this litigation.

U.S. Patent No. 5,248,893	
Claim 1	
Claim limitation	**JPA '664**
1 An insulated gate field effect device comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, JPA '664 discloses an insulated gate field effect device. *See, e.g.*, JPA '664 at Fig. 2; *see, e.g.*, JPA '664 translation at 1 ("This invention relates to semiconductor devices, in particular MOS transistor devices....").
a first conductivity type semiconductor substrate having a main surface;	*See, e.g.*, JPA '664 at Figs. 2-4; *see, e.g.*, JPA '664 translation at 2 ("Specifically, a p^- substrate with a concentration of impurities of approximately $10^{15}/cm^3$ is prepared as in step (a).").
said semiconductor substrate having a concave surface formed on said main surface extending to a prespecified depth below the main surface;	*See, e.g.*, JPA '664 at Figs 2-4; *see, e.g.*, JPA '664 translation at 2 ("A recessed groove (6) with depth a depth of d is formed on the surface of a P-type substrate (5)...."); *see, e.g.*, *id.* ("Of course, the depth (d) of the groove must be deep enough that this value is not negative.").
an insulating film formed on said concave surface;	*See, e.g.*, JPA '664 at Figs 2-4; *see, e.g.*, JPA '664 translation at 2 ("The resists (17) are removed and an SiO2 membrane (18) with a thickness of approximately 0.1μ is provided in step (e)....").
a conductive gate electrode formed above said insulating film, overlying the concave surface;	*See, e.g.*, JPA '664 at Figs 2-4; *see, e.g.*, JPA '664 translation at 2 ("The resists (17) are removed and an SiO2 membrane (18) with a thickness of approximately 0.1μ is provided in step (e) and in step (f), a polysilicon gate electrode with a length of 35μ is formed above it....").
first and second impurity regions of	*See, e.g.*, JPA '664 at Figs 2-4; *see, e.g.*, JPA '664 translation at 2 ("Additionally, an n-type impurity is

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a second conductivity type respectively formed in the substrate, in the vicinity of said main surfaces, self-aligned to and positioned at one side and the other side of said gate electrode respectively; and	dispersed within a source region (7) with a depth of x_{sj} and a drain region (8) with a depth of x_{dj} to the right and left of this channel, on top of which the source and drain electrodes respectively are formed. At this point, they are formed so that the drain region has a depth of $x_{sj} = d - \sqrt{\frac{2\varepsilon}{qN}} \left(\sqrt{\lvert V_{sub} \rvert + V_B} - \sqrt{\lvert V_{sub} \rvert + 2\phi_F} \right)$. Of course, the depth (d) of the groove must be deep enough that this value is not negative. The source and the drain can be formed through dispersion, ion injection or another means and selective epitaxy can be carried out instead of creation of a channel."); *see, e.g., id.* ("The resists (17) are removed and an SiO2 membrane (18) with a thickness of approximately 0.1µ is provided in step (e) and in step (f), a polysilicon gate electrode with a length of 35µ is formed above it, and the N-type impurities are dispersed from the areas from which the oxidized layer was removed to create a source region (20') and drain region (20) with a impurity concentrations of approximately $10^{19}/cm^3$ and depths of dispersion from the surface of approximately 1.0µ.").
a first conductivity type region located in said semiconductor substrate between said first and second impurity regions for defining a channel region and a channel-free region extending conformably under and along said concave surface;	*See, e.g.*, JPA '664 at Figs 2-4; *see, e.g.*, JPA '664 translation at 2 ("An overview of the equipotential lines of a MOS transistor with this structure during operation is shown in Figure 4. As can be seen, the equipotential lines that run from the channel area directly below the groove to the area directly below the source are parallel to the surface when the dispersion depth of the source region is adjusted to the value given above. When the dispersion of the source region is deeper, the equipotential lines close to the source are forced downwards by the tendency shown in Figure 1 (b) and there is a protruding curve in the channel near the source and the threshold voltage that must be applied to the gate is further reduced due to the fact that an inversion layer is formed in this area, leading to the short-channel effect. On the other hand, when the dispersion of the source region is deeper [sic], the distribution of the equipotential lines is as shown in Figure 5 and the equipotential lines in the source region are pulled upwards instead. Because of this, the curve protrudes downward in the area of the channel near the source (21) and the threshold voltage in this area is higher than that in the other parts of the channel, making formation of an inversion layer difficult. Because the formation of an inversion layer at the beginning of the channel plays a decisive role in controlling the current from the source region to the drain region and carrying out switching, the efficacy in eliminating variation in the threshold voltage that causes the equipotential lines in source region to bend and obtaining short-channel elements that have threshold voltages that are as stable as those of long-channel transistors is clear. Furthermore, this structure can prevent the easy occurrence of breakdown between the source and drain accompanying reduction of the channel length.").

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wherein the depth of said concave surface is set to a value which ranges between one and two times the depth of said first and second impurity regions, and	*See, e.g.*, JPA '664 at Figs 2-4; *see, e.g.*, JPA '664 translation at 2 ("Additionally, an n-type impurity is dispersed within a source region (7) with a depth of x_{sj} and a drain region (8) with a depth of x_{dj} to the right and left of this channel, on top of which the source and drain electrodes respectively are formed. At this point, they are formed so that the drain region has a depth of $x_{sj} = d - \sqrt{\frac{2\varepsilon}{qN}} \left(\sqrt{\lvert V_{sub} \rvert + V_B} - \sqrt{\lvert V_{sub} \rvert + 2\phi_F} \right)$ Of course, the depth (d) of the groove must be deep enough that this value is not negative. The source and the drain can be formed through dispersion, ion injection or another means and selective epitaxy can be carried out instead of creation of a channel."); *see, e.g., id.* ("The resists (17) are removed and an SiO2 membrane (18) with a thickness of approximately 0.1μ is provided in step (e) and in step (f), a polysilicon gate electrode with a length of 35μ is formed above it, and the N-type impurities are dispersed from the areas from which the oxidized layer was removed to create a source region (20') and drain region (20) with a impurity concentrations of approximately $10^{19}/cm^3$ and depths of dispersion from the surface of approximately 1.0μ.").
wherein the concave surface is continuously curved in the vicinity of at least one of the first and second impurity regions to produce smooth merger of a conforming first depletion region formed around the at least one impurity region and a conforming second depletion region formed in the vicinity of the gate electrode so that excessive field concentration will not develop in the vicinity where the first and second depletion regions meet.	*See, e.g.*, JPA '664 at Figs 2-4; *see, e.g.*, JPA '664 translation at 2 ("An overview of the equipotential lines of a MOS transistor with this structure during operation is shown in Figure 4. As can be seen, the equipotential lines that run from the channel area directly below the groove to the area directly below the source are parallel to the surface when the dispersion depth of the source region is adjusted to the value given above. When the dispersion of the source region is deeper, the equipotential lines close to the source are forced downwards by the tendency shown in Figure 1 (b) and there is a protruding curve in the channel near the source and the threshold voltage that must be applied to the gate is further reduced due to the fact that an inversion layer is formed in this area, leading to the short-channel effect. On the other hand, when the dispersion of the source region is deeper [sic], the distribution of the equipotential lines is as shown in Figure 5 and the equipotential lines in the source region are pulled upwards instead. Because of this, the curve protrudes downward in the area of the channel near the source (21) and the threshold voltage in this area is higher than that in the other parts of the channel, making formation of an inversion layer difficult. Because the formation of an inversion layer at the beginning of the channel plays a decisive role in controlling the current from the source region to the drain region and carrying out switching, the efficacy in eliminating variation in the threshold voltage that causes the equipotential lines in source region to bend and obtaining short-channel elements that have threshold voltages that are as stable as those of long-channel transistors is clear. Furthermore, this structure can prevent the easy occurrence of breakdown between the source and drain accompanying reduction of the

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	channel length.").
Claim 2	
Claim limitation	**JPA '664**
2. An insulated gate field effect device according to claim 1, wherein one of said first and second impurity regions constitutes a drain region of said insulated gate field effect device, the other of said first and second impurity regions constitutes a source region and wherein the concave surface is continuously curved at least in the vicinity of the drain region, where the channel-free region develops during an off state of the device, to produce smooth merger of the conforming first depletion region which develops in the vicinity of the channel-free region and the drain region and the conforming second depletion region formed in the vicinity of the gate electrode so that excessive field concentration will not develop in the vicinity of the channel-free region.	*See, e.g.*, JPA '664 at Figs 2-4; *see, e.g.*, JPA '664 translation at 2 ("Additionally, an n-type impurity is dispersed within a source region (7) with a depth of x_{sj} and a drain region (8) with a depth of x_{dj} to the right and left of this channel, on top of which the source and drain electrodes respectively are formed. At this point, they are formed so that the drain region has a depth of $x_{sj} = d - \sqrt{\frac{2\varepsilon}{qN}}\left(\sqrt{\lvert V_{SUB}\rvert + V_B} - \sqrt{\lvert V_{SUB}\rvert + 2\phi_F}\right)$. Of course, the depth (d) of the groove must be deep enough that this value is not negative. The source and the drain can be formed through dispersion, ion injection or another means and selective epitaxy can be carried out instead of creation of a channel."); *see, e.g.*, *id.* ("The resists (17) are removed and an SiO2 membrane (18) with a thickness of approximately 0.1μ is provided in step (e) and in step (f), a polysilicon gate electrode with a length of 35μ is formed above it, and the N-type impurities are dispersed from the areas from which the oxidized layer was removed to create a source region (20') and drain region (20) with a impurity concentrations of approximately $10^{19}/cm^3$ and depths of dispersion from the surface of approximately 1.0μ."); *see, e.g.*, *id.* ("An overview of the equipotential lines of a MOS transistor with this structure during operation is shown in Figure 4. As can be seen, the equipotential lines that run from the channel area directly below the groove to the area directly below the source are parallel to the surface when the dispersion depth of the source region is adjusted to the value given above. When the dispersion of the source region is deeper, the equipotential lines close to the source are forced downwards by the tendency shown in Figure 1 (b) and there is a protruding curve in the channel near the source and the threshold voltage that must be applied to the gate is further reduced due to the fact that an inversion layer is formed in this area, leading to the short-channel effect. On the other hand, when the dispersion of the source region is deeper [sic], the distribution of the equipotential lines is as shown in Figure 5 and the equipotential lines in the source region are pulled upwards instead. Because of this, the curve protrudes downward in the area of the channel near the source (21) and the threshold voltage in this area is higher than that in the other parts of the channel, making formation of an inversion layer difficult. Because the formation of an inversion layer at the beginning of the channel plays a decisive role in controlling the current from the source region to the drain region and carrying out switching, the efficacy in eliminating

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	variation in the threshold voltage that causes the equipotential lines in source region to bend and obtaining short-channel elements that have threshold voltages that are as stable as those of long-channel transistors is clear. Furthermore, this structure can prevent the easy occurrence of breakdown between the source and drain accompanying reduction of the channel length.").
Claim 3	
Claim limitation	**JPA '664**
3. An insulated gate field effect device according to claim 1, which comprises a metal oxide semiconductor (MOS) transistor, and wherein said insulating film comprises an oxide film.	*See, e.g.*, JPA '664 at Figs 1-4; *see, e.g.*, JPA '664 translation at 2 ("The purpose of this invention is to provide a MOS transistor design ...."); *see, e.g.*, *id.* ("The resists (17) are removed and an SiO2 membrane (18) with a thickness of approximately 0.1μ is provided in step (e) and in step (f), a polysilicon gate electrode with a length of 35μ is formed above it....").
Claim 4	
Claim limitation	**JPA '664**
4. An insulated-gate field effect transistor comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, JPA '664 discloses an insulated gate field effect transistor. *See, e.g.*, JPA '664 at Fig. 2; *see, e.g.*, JPA '664 translation at 1 ("This invention relates to semiconductor devices, in particular MOS transistor devices....").
a substrate having a substantially planar main surface and a concave surface portion extending continuously from the main surface to a predetermined depth below the main surface;	*See, e.g.*, JPA '664 at Figs 2-4; *see, e.g.*, JPA '664 translation at 2 ("A recessed groove (6) with depth a depth of d is formed on the surface of a P-type substrate (5)...."); *see, e.g.*, *id.* ("Of course, the depth (d) of the groove must be deep enough that this value is not negative.").
an insulating layer conformably disposed on the main surface and	*See, e.g.*, JPA '664 at Figs 2-4; *see, e.g.*, JPA '664 translation at 2 ("The resists (17) are removed and an SiO2 membrane (18) with a thickness of approximately 0.1μ is provided in step (e)....").

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the concave surface portion;	
a gate conformably disposed on the insulating layer, overlying the concave surface portion, the gate having opposed first and second sides;	*See, e.g.*, JPA '664 at Figs 2-4; *see, e.g.*, JPA '664 translation at 2 ("The resists (17) are removed and an SiO2 membrane (18) with a thickness of approximately 0.1μ is provided in step (e) and in step (f), a polysilicon gate electrode with a length of 35μ is formed above it.....").
implanted source and drain regions disposed within the substrate and self-aligned to the respective first and second opposed sides of the gate; and	*See, e.g.*, JPA '664 at Figs 2-4; *see, e.g.*, JPA '664 translation at 2 ("Additionally, an n-type impurity is dispersed within a source region (7) with a depth of x_{sj} and a drain region (8) with a depth of x_{dj} to the right and left of this channel, on top of which the source and drain electrodes respectively are formed. At this point, they are formed so that the drain region has a depth of $$x_{sj} = d - \sqrt{\frac{2\varepsilon}{qN}} \left(\sqrt{\lvert V_{SUB} \rvert + V_B} - \sqrt{\lvert V_{SUB} \rvert + 2\phi_F} \right)$$ Of course, the depth (d) of the groove must be deep enough that this value is not negative. The source and the drain can be formed through dispersion, ion injection or another means and selective epitaxy can be carried out instead of creation of a channel."); *see, e.g.*, *id.* ("The resists (17) are removed and an SiO2 membrane (18) with a thickness of approximately 0.1μ is provided in step (e) and in step (f), a polysilicon gate electrode with a length of 35μ is formed above it, and the N-type impurities are dispersed from the areas from which the oxidized layer was removed to create a source region (20') and drain region (20) with a impurity concentrations of approximately $10^{19}/cm^3$ and depths of dispersion from the surface of approximately 1.0μ.").
a channel-region formed between the source and drain regions, for defining a channel that conducts current between the source and drain regions when the transistor is in a turned-on state;	*See, e.g.*, JPA '664 at Figs 2-4; *see, e.g.*, JPA '664 translation at 2 ("An overview of the equipotential lines of a MOS transistor with this structure during operation is shown in Figure 4. As can be seen, the equipotential lines that run from the channel area directly below the groove to the area directly below the source are parallel to the surface when the dispersion depth of the source region is adjusted to the value given above. When the dispersion of the source region is deeper, the equipotential lines close to the source are forced downwards by the tendency shown in Figure 1 (b) and there is a protruding curve in the channel near the source and the threshold voltage that must be applied to the gate is further reduced due to the fact that an inversion layer is formed in this area, leading to the short-channel effect. On the other hand, when the dispersion of the source region is deeper [sic], the distribution of the equipotential lines is as shown in Figure 5 and the equipotential lines in the source region are pulled upwards instead. Because of this, the curve protrudes downward in the

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	area of the channel near the source (21) and the threshold voltage in this area is higher than that in the other parts of the channel, making formation of an inversion layer difficult. Because the formation of an inversion layer at the beginning of the channel plays a decisive role in controlling the current from the source region to the drain region and carrying out switching, the efficacy in eliminating variation in the threshold voltage that causes the equipotential lines in source region to bend and obtaining short-channel elements that have threshold voltages that are as stable as those of long-channel transistors is clear. Furthermore, this structure can prevent the easy occurrence of breakdown between the source and drain accompanying reduction of the channel length.").
wherein a channel-free zone develops in the substrate, under the gate and between the source and drain regions, when the transistor is in a turned-off state; and	*See, e.g.*, JPA '664 at Figs 2-4; *see, e.g.*, JPA '664 translation at 2 ("An overview of the equipotential lines of a MOS transistor with this structure during operation is shown in Figure 4. As can be seen, the equipotential lines that run from the channel area directly below the groove to the area directly below the source are parallel to the surface when the dispersion depth of the source region is adjusted to the value given above. When the dispersion of the source region is deeper, the equipotential lines close to the source are forced downwards by the tendency shown in Figure 1 (b) and there is a protruding curve in the channel near the source and the threshold voltage that must be applied to the gate is further reduced due to the fact that an inversion layer is formed in this area, leading to the short-channel effect. On the other hand, when the dispersion of the source region is deeper [sic], the distribution of the equipotential lines is as shown in Figure 5 and the equipotential lines in the source region are pulled upwards instead. Because of this, the curve protrudes downward in the area of the channel near the source (21) and the threshold voltage in this area is higher than that in the other parts of the channel, making formation of an inversion layer difficult. Because the formation of an inversion layer at the beginning of the channel plays a decisive role in controlling the current from the source region to the drain region and carrying out switching, the efficacy in eliminating variation in the threshold voltage that causes the equipotential lines in source region to bend and obtaining short-channel elements that have threshold voltages that are as stable as those of long-channel transistors is clear. Furthermore, this structure can prevent the easy occurrence of breakdown between the source and drain accompanying reduction of the channel length.").
wherein the gate and concave surface portion are curved at least in the vicinity of the channel-free zone such that a smoothly curved	*See, e.g.*, JPA '664 at Figs 2-4; *see, e.g.*, JPA '664 translation at 2 ("An overview of the equipotential lines of a MOS transistor with this structure during operation is shown in Figure 4. As can be seen, the equipotential lines that run from the channel area directly below the groove to the area directly below the source are parallel to the surface when the dispersion depth of the source region is adjusted to the value given above. When the

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depletion zone boundary will develop in the vicinity of the channel-free zone when the transistor is in the turned-off state.	dispersion of the source region is deeper, the equipotential lines close to the source are forced downwards by the tendency shown in Figure 1 (b) and there is a protruding curve in the channel near the source and the threshold voltage that must be applied to the gate is further reduced due to the fact that an inversion layer is formed in this area, leading to the short-channel effect. On the other hand, when the dispersion of the source region is deeper [sic], the distribution of the equipotential lines is as shown in Figure 5 and the equipotential lines in the source region are pulled upwards instead. Because of this, the curve protrudes downward in the area of the channel near the source (21) and the threshold voltage in this area is higher than that in the other parts of the channel, making formation of an inversion layer difficult. Because the formation of an inversion layer at the beginning of the channel plays a decisive role in controlling the current from the source region to the drain region and carrying out switching, the efficacy in eliminating variation in the threshold voltage that causes the equipotential lines in source region to bend and obtaining short-channel elements that have threshold voltages that are as stable as those of long-channel transistors is clear. Furthermore, this structure can prevent the easy occurrence of breakdown between the source and drain accompanying reduction of the channel length.").
Claim 5	
Claim limitation	**JPA '664**
5. An insulated-gate field effect transistor according to claim 4 wherein the concave surface portion is curved in a transverse cross-sectional plane extending through the transistor between but not intersecting the first and second sides of the gate so as to provide an effective channel width greater than a width of the channel as projected onto the plane of the main substrate surface.	*See, e.g.*, JPA '664 at Figs 2-4; *see, e.g.*, JPA '664 translation at 2 ("The purpose of this invention is to provide a MOS transistor design that avoids problems resulting from issues such as the short-channel effect that is mentioned above when they are caused by the structure of the source."); *see, e.g.*, *id.* ("A recessed groove (6) with depth a depth of d is formed on the surface of a P-type substrate (5)...."); *see, e.g.*, *id.* ("Of course, the depth (d) of the groove must be deep enough that this value is not negative.").

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Claim 6

Claim limitation	**JPA '664**
6. An insulated-gate field effect transistor according to claim 5 wherein the concave surface portion is curved both in the transverse cross-sectional plane and in a non-transverse cross-sectional plane, extending between and joining the first and second sides of the gate, so as to provide an effective channel surface area greater than an area of the channel as projected onto the plane of the main substrate surface.	*See, e.g.*, JPA '664 at Figs 2-4; *see, e.g.*, JPA '664 translation at 2 ("The purpose of this invention is to provide a MOS transistor design that avoids problems resulting from issues such as the short-channel effect that is mentioned above when they are caused by the structure of the source."); *see, e.g.*, *id.* ("A recessed groove (6) with depth a depth of d is formed on the surface of a P-type substrate (5)...."); *see, e.g.*, *id.* ("Of course, the depth (d) of the groove must be deep enough that this value is not negative."); *see, e.g.*, *id.* ("An overview of the equipotential lines of a MOS transistor with this structure during operation is shown in Figure 4. As can be seen, the equipotential lines that run from the channel area directly below the groove to the area directly below the source are parallel to the surface when the dispersion depth of the source region is adjusted to the value given above. When the dispersion of the source region is deeper, the equipotential lines close to the source are forced downwards by the tendency shown in Figure 1 (b) and there is a protruding curve in the channel near the source and the threshold voltage that must be applied to the gate is further reduced due to the fact that an inversion layer is formed in this area, leading to the short-channel effect. On the other hand, when the dispersion of the source region is deeper [sic], the distribution of the equipotential lines is as shown in Figure 5 and the equipotential lines in the source region are pulled upwards instead. Because of this, the curve protrudes downward in the area of the channel near the source (21) and the threshold voltage in this area is higher than that in the other parts of the channel, making formation of an inversion layer difficult. Because the formation of an inversion layer at the beginning of the channel plays a decisive role in controlling the current from the source region to the drain region and carrying out switching, the efficacy in eliminating variation in the threshold voltage that causes the equipotential lines in source region to bend and obtaining short-channel elements that have threshold voltages that are as stable as those of long-channel transistors is clear. Furthermore, this structure can prevent the easy occurrence of breakdown between the source and drain accompanying reduction of the channel length.").

Claim 7

Claim limitation	**JPA '664**
7. An insulated-gate field effect transistor according to claim 6 wherein the concave surface portion	*See, e.g.*, JPA '664 at Figs 2-4; *see, e.g.*, JPA '664 translation at 2 ("The purpose of this invention is to provide a MOS transistor design that avoids problems resulting from issues such as the short-channel effect that is mentioned above when they are caused by the structure of the source."); *see, e.g.*, *id.* ("A recessed groove (6)

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is equally curved both in the transverse cross-sectional plane and in the non-transverse cross-sectional plane, so as to provide a sheet-like depletion region having a uniform thickness and a smooth bottom boundary underlying the channel region and the source and drain regions, when the transistor is in a turned-off state.	with depth a depth of d is formed on the surface of a P-type substrate (5)...."); *see, e.g., id.* ("Of course, the depth (d) of the groove must be deep enough that this value is not negative."); *see, e.g., id.* ("An overview of the equipotential lines of a MOS transistor with this structure during operation is shown in Figure 4. As can be seen, the equipotential lines that run from the channel area directly below the groove to the area directly below the source are parallel to the surface when the dispersion depth of the source region is adjusted to the value given above. When the dispersion of the source region is deeper, the equipotential lines close to the source are forced downwards by the tendency shown in Figure 1 (b) and there is a protruding curve in the channel near the source and the threshold voltage that must be applied to the gate is further reduced due to the fact that an inversion layer is formed in this area, leading to the short-channel effect. On the other hand, when the dispersion of the source region is deeper [sic], the distribution of the equipotential lines is as shown in Figure 5 and the equipotential lines in the source region are pulled upwards instead. Because of this, the curve protrudes downward in the area of the channel near the source (21) and the threshold voltage in this area is higher than that in the other parts of the channel, making formation of an inversion layer difficult. Because the formation of an inversion layer at the beginning of the channel plays a decisive role in controlling the current from the source region to the drain region and carrying out switching, the efficacy in eliminating variation in the threshold voltage that causes the equipotential lines in source region to bend and obtaining short-channel elements that have threshold voltages that are as stable as those of long-channel transistors is clear. Furthermore, this structure can prevent the easy occurrence of breakdown between the source and drain accompanying reduction of the channel length.").

Claim 11

Claim limitation	JPA '664
11. An insulated-gate field effect transistor according to claim 4 wherein the depth of the concave surface portion is set to a value which ranges between one and two times the depth of the source and drain regions.	*See, e.g.*, JPA '664 at Figs 2-4; *see, e.g.*, JPA '664 translation at 2 ("Additionally, an n-type impurity is dispersed within a source region (7) with a depth of x_{sj} and a drain region (8) with a depth of x_{dj} to the right and left of this channel, on top of which the source and drain electrodes respectively are formed. At this point, they are formed so that the drain region has a depth of $x_{sj} = d - \sqrt{\frac{2\varepsilon}{qN}} \left(\sqrt{\lvert V_{SUB} \rvert + V_B} - \sqrt{\lvert V_{SUB} \rvert + 2\phi_F} \right)$. Of course, the depth (d) of the groove must be deep enough that this value is not negative. The source and the drain can be formed through dispersion, ion injection or another means and selective epitaxy can be carried out

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	instead of creation of a channel."); *see, e.g., id.* ("The resists (17) are removed and an SiO2 membrane (18) with a thickness of approximately 0.1μ is provided in step (e) and in step (f), a polysilicon gate electrode with a length of 35μ is formed above it, and the N-type impurities are dispersed from the areas from which the oxidized layer was removed to create a source region (20') and drain region (20) with a impurity concentrations of approximately $10^{19}/cm^3$ and depths of dispersion from the surface of approximately 1.0μ.").

Appendix C3

Defendants and Counterclaimants' Invalidity Contentions

Advanced Micro Devices, Inc. et al. v. Samsung Electronics Co., Ltd. et al., Case No. CV-08-0986-SI

U.S. Patent No. 5,248,893 Invalidity Chart: Japanese Patent Application No. 53-74394 ("JPA '394")

All asserted claims are anticipated by the JPA '394 and/or are rendered obvious by it, either alone or in combination with other prior art described below and/or listed in Section I of Defendants' and Counterclaimants' Preliminary Invalidity Contentions and/or through modifications described below. Nothing in this invalidity chart should be construed as signifying or suggesting Defendants and Counterclaimants' adoption of or acquiescence in any claim scope and/or claim construction positions taken by Plaintiffs and Counterdefendants in this litigation.

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Claim 1	
Claim limitation	**JPA '394**
1 An insulated gate field effect device comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, JPA '394 discloses an insulated gate field effect device. *See, e.g.*, JPA '394 at Fig. 1; *see, e.g.*, JPA '394 translation at 1 ("This invention relates to a MOSFET…..").
a first conductivity type semiconductor substrate having a main surface;	*See, e.g.*, JPA '394 at Figs. 1-4; *see, e.g.*, JPA '394 translation at 2 ("First, as in (a) the (100) face of a P-type silicone substrate is prepared having an impurity concentration of approximately $10^{15}/cm^3$.").
said semiconductor substrate having a concave surface formed on said main surface extending to a prespecified depth below the main surface;	*See, e.g.*, JPA '394 at Figs 1-4; *see, e.g.*, JPA '394 translation at 1-2 ("[T]he MOSFET channel region is formed at the bottom of a grove [sic, groove] provided in the surface of the semiconductor and the source and drain diffusion areas are formed higher than the channel region…"); *see, e.g.*, *id.* at 2 ("As shown in FIG. 1, a MOSFET channel area is formed at the bottom of a groove having a depth d, which is formed in the surface of the [substrate]. Then, the MOSFET is fabricated so that, when the depths of the source and drain diffusion areas are X_{sJ} and X_{dJ}, respectively, X_{sJ} and X_{dJ} substantially satisfy: $d \geq X_{sJ} \geq d - \sqrt{\frac{2\epsilon}{gN}}\left(\sqrt{\lvert V_{avB}\rvert + V_B} - \sqrt{\lvert V_{avB}\rvert + 2\phi_F}\right)$ $d \geq X_{dJ} \geq d - \sqrt{\frac{2\epsilon}{gN}}\left(\sqrt{\lvert V_{avB}\rvert + V_D + V_B} - \sqrt{\lvert V_{avB}\rvert + 2\phi_F}\right)$."); *see, e.g.*, *id.* ("A resist is applied and etching is performed so as to form a recessed groove (13) having a width of approximately 3 μ and a depth of

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	approximately 1.5 μ in the MOS transistor channel formation region.").
an insulating film formed on said concave surface;	*See, e.g.*, JPA '394 at Figs 1-4; *see, e.g.*, JPA '394 translation at 2 ("The resist is removed and the silicon surface is thermally oxidized so as to form a gate silicon oxide film (14) of approximately 1000 Å, and thereon a polycrystalline silicone gate electrode (15) is formed.").
a conductive gate electrode formed above said insulating film, overlying the concave surface;	*See, e.g.*, JPA '394 at Figs 1-4; *see, e.g.*, JPA '394 translation at 2 ("The resist is removed and the silicon surface is thermally oxidized so as to form a gate silicon oxide film (14) of approximately 1000 Å, and thereon a polycrystalline silicone gate electrode (15) is formed").
first and second impurity regions of a second conductivity type respectively formed in the substrate, in the vicinity of said main surfaces, self-aligned to and positioned at one side and the other side of said gate electrode respectively; and	*See, e.g.*, JPA '394 at Figs 1-4; *see, e.g.*, JPA '394 translation at 2 ("The resist is removed and the silicon surface is thermally oxidized so as to form a gate silicon oxide film (14) of approximately 1000 Å, and thereon a polycrystalline silicone gate electrode (15) is formed (d). So as to achieve self alignment with the polycrystalline silicone the gate electrode, first an N-type impurity is diffused in the source region (e) and then likewise diffused in the drain region, so as to form a source diffusion region (16) having an impurity level of approximately $10^{19}/cm^3$ and a depth of 1.4 μ, and a drain diffusion region (17) having substantially the same concentration and a depth of approximately 0 .7 μ.").
a first conductivity type region located in said semiconductor substrate between said first and second impurity regions for defining a channel region and a channel-free region extending conformably under and along said concave surface;	*See, e.g.*, JPA '394 at Figs 1-4; *see, e.g.*, JPA '394 translation at 2 ("The equipotential line distribution of an MOS transistor according to this invention, when operating, is schematically illustrated in FIG. 3. As shown in the drawing, the spread of the depletion layer resulting from the built-in voltage in the source region and the spread of the depletion layer resulting from the built-in voltage plus, [sic] the drain voltage is substantially absorbed by the part between the channel surface and the source and drain junction surfaces so that the equipotential lines in the vicinity of the channel surface are nearly parallel lines. Because upward protrusion and downward protrusion curvature of the equipotential lines is suppressed, the lowering of the threshold voltage that usually results from the short channel effect and the raising of the threshold voltage, which is the opposite phenomena, are effectively prevented. Furthermore, by virtue of this constitution, the depletion layer is prevented from extending from the source or the drain by the recessed groove structure, whereby the breakdown voltage between the source and the drain can be increased.").
wherein the depth of said concave surface is set to a value which	*See, e.g.*, JPA '394 at Figs 1-4; *see, e.g.*, JPA '394 translation at 2 ("The resist is removed and the silicon surface is thermally oxidized so as to form a gate silicon oxide film (14) of approximately 1000 Å, and thereon

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ranges between one and two times the depth of said first and second impurity regions, and	a polycrystalline silicone gate electrode (15) is formed (d). So as to achieve self alignment with the polycrystalline silicone the gate electrode, first an N-type impurity is diffused in the source region (e) and then likewise diffused in the drain region, so as to form a source diffusion region (16) having an impurity level of approximately $10^{19}/cm^3$ and a depth of 1.4 μ, and a drain diffusion region (17) having substantially the same concentration and a depth of approximately 0.7 μ."); *see, e.g., id.* ("A resist is applied and etching is performed so as to form a recessed groove (13) having a width of approximately 3 μ and a depth of approximately 1.5 μ in the MOS transistor channel formation region.").
wherein the concave surface is continuously curved in the vicinity of at least one of the first and second impurity regions to produce smooth merger of a conforming first depletion region formed around the at least one impurity region and a conforming second depletion region formed in the vicinity of the gate electrode so that excessive field concentration will not develop in the vicinity where the first and second depletion regions meet.	*See, e.g.*, JPA '394 at Figs 1-4; *see, e.g.*, JPA '394 translation at 2 ("The equipotential line distribution of an MOS transistor according to this invention, when operating, is schematically illustrated in FIG. 3. As shown in the drawing, the spread of the depletion layer resulting from the built-in voltage in the source region and the spread of the depletion layer resulting from the built-in voltage plus, [sic] the drain voltage is substantially absorbed by the part between the channel surface and the source and drain junction surfaces so that the equipotential lines in the vicinity of the channel surface are nearly parallel lines. Because upward protrusion and downward protrusion curvature of the equipotential lines is suppressed, the lowering of the threshold voltage that usually results from the short channel effect and the raising of the threshold voltage, which is the opposite phenomena, are effectively prevented. Furthermore, by virtue of this constitution, the depletion layer is prevented from extending from the source or the drain by the recessed groove structure, whereby the breakdown voltage between the source and the drain can be increased.").
Claim 2	
Claim limitation	**JPA '394**
2. An insulated gate field effect device according to claim 1, wherein one of said first and second impurity regions constitutes a drain region of said insulated gate field effect device, the other of said first and second impurity regions	*See, e.g.*, JPA '394 at Figs 1-4; *see, e.g.*, JPA '394 translation at 2 ("The resist is removed and the silicon surface is thermally oxidized so as to form a gate silicon oxide film (14) of approximately 1000 Å, and thereon a polycrystalline silicone gate electrode (15) is formed (d). So as to achieve self alignment with the polycrystalline silicone the gate electrode, first an N-type impurity is diffused in the source region (e) and then likewise diffused in the drain region, so as to form a source diffusion region (16) having an impurity level of approximately $10^{19}/cm^3$ and a depth of 1.4 μ, and a drain diffusion region (17) having substantially the same concentration and a depth of approximately 0 .7 μ."); *see, e.g., id.* ("The equipotential line distribution of an

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constitutes a source region and wherein the concave surface is continuously curved at least in the vicinity of the drain region, where the channel-free region develops during an off state of the device, to produce smooth merger of the conforming first depletion region which develops in the vicinity of the channel-free region and the drain region and the conforming second depletion region formed in the vicinity of the gate electrode so that excessive field concentration will not develop in the vicinity of the channel-free region.	MOS transistor according to this invention, when operating, is schematically illustrated in FIG. 3. As shown in the drawing, the spread of the depletion layer resulting from the built-in voltage in the source region and the spread of the depletion layer resulting from the built-in voltage plus, [sic] the drain voltage is substantially absorbed by the part between the channel surface and the source and drain junction surfaces so that the equipotential lines in the vicinity of the channel surface are nearly parallel lines. Because upward protrusion and downward protrusion curvature of the equipotential lines is suppressed, the lowering of the threshold voltage that usually results from the short channel effect and the raising of the threshold voltage, which is the opposite phenomena, are effectively prevented. Furthermore, by virtue of this constitution, the depletion layer is prevented from extending from the source or the drain by the recessed groove structure, whereby the breakdown voltage between the source and the drain can be increased.").
Claim 3	
Claim limitation	**JPA '394**
3. An insulated gate field effect device according to claim 1, which comprises a metal oxide semiconductor (MOS) transistor, and wherein said insulating film comprises an oxide film.	*See*, *e.g.*, JPA '394 at Figs 1-4; *see*, *e.g.*, JPA '394 translation at 1 ("This invention relates to a MOSFET…."); *see*, *e.g.*, *id.* at 2 ("The resist is removed and the silicon surface is thermally oxidized so as to form a gate silicon oxide film (14) of approximately 1000 Å, and thereon a polycrystalline silicone gate electrode (15) is formed.").
Claim 4	
Claim limitation	**JPA '394**
4. An insulated-gate field effect	Assuming for present purposes (without admitting) that the preamble is a claim limitation, JPA '394 discloses an insulated gate field effect transistor. *See*, *e.g.*, JPA '394 at Fig. 1; *see*, *e.g.*, JPA '394 translation at 1 ("This

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transistor comprising:	invention relates to a MOSFET.....").
a substrate having a substantially planar main surface and a concave surface portion extending continuously from the main surface to a predetermined depth below the main surface;	*See*, *e.g.*, JPA '394 at Figs 1-4; *see*, *e.g.*, JPA '394 translation at 1-2 ("[T]he MOSFET channel region is formed at the bottom of a grove [sic, groove] provided in the surface of the semiconductor and the source and drain diffusion areas are formed higher than the channel region..."); *see*, *e.g.*, *id.* at 2 ("As shown in FIG. 1, a MOSFET channel area is formed at the bottom of a groove having a depth d, which is formed in the surface of the [substrate]. Then, the MOSFET is fabricated so that, when the depths of the source and drain diffusion areas are X_{sJ} and X_{dJ}, respectively, X_{sJ} and X_{dJ} substantially satisfy: $d \geq X_{sJ} \geq d - \sqrt{\frac{2\varepsilon}{qN}}\left(\sqrt{\lvert V_{sub}\rvert + V_B} - \sqrt{\lvert V_{sub}\rvert + 2\phi_F}\right)$ $d \geq X_{dJ} \geq d - \sqrt{\frac{2\varepsilon}{qN}}\left(\sqrt{\lvert V_{sub}\rvert + V_D + V_B} - \sqrt{\lvert V_{sub}\rvert + 2\phi_F}\right)$."); *see*, *e.g.*, *id.* ("A resist is applied and etching is performed so as to form a recessed groove (13) having a width of approximately 3 μ and a depth of approximately 1.5 μ in the MOS transistor channel formation region.").
an insulating layer conformably disposed on the main surface and the concave surface portion;	*See*, *e.g.*, JPA '394 at Figs 1-4; *see*, *e.g.*, JPA '394 translation at 2 ("The resist is removed and the silicon surface is thermally oxidized so as to form a gate silicon oxide film (14) of approximately 1000 Å, and thereon a polycrystalline silicone gate electrode (15) is formed.").
a gate conformably disposed on the insulating layer, overlying the concave surface portion, the gate having opposed first and second sides;	*See*, *e.g.*, JPA '394 at Figs 1-4; *see*, *e.g.*, JPA '394 translation at 2 ("The resist is removed and the silicon surface is thermally oxidized so as to form a gate silicon oxide film (14) of approximately 1000 Å, and thereon a polycrystalline silicone gate electrode (15) is formed").
implanted source and drain regions disposed within the substrate and self-aligned to the respective first and second opposed sides of the gate; and	*See*, *e.g.*, JPA '394 at Figs 1-4; *see*, *e.g.*, JPA '394 translation at 2 ("The resist is removed and the silicon surface is thermally oxidized so as to form a gate silicon oxide film (14) of approximately 1000 Å, and thereon a polycrystalline silicone gate electrode (15) is formed (d). So as to achieve self alignment with the polycrystalline silicone the gate electrode, first an N-type impurity is diffused in the source region (e) and then likewise diffused in the drain region, so as to form a source diffusion region (16) having an impurity level of approximately $10^{19}/cm^3$ and a depth of 1.4 μ, and a drain diffusion region (17) having substantially the same

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	concentration and a depth of approximately 0 .7 μ.").
a channel-region formed between the source and drain regions, for defining a channel that conducts current between the source and drain regions when the transistor is in a turned-on state;	*See, e.g.*, JPA '394 at Figs 1-4; *see, e.g.*, JPA '394 translation at 2 ("The equipotential line distribution of an MOS transistor according to this invention, when operating, is schematically illustrated in FIG. 3. As shown in the drawing, the spread of the depletion layer resulting from the built-in voltage in the source region and the spread of the depletion layer resulting from the built-in voltage plus, [sic] the drain voltage is substantially absorbed by the part between the channel surface and the source and drain junction surfaces so that the equipotential lines in the vicinity of the channel surface are nearly parallel lines. Because upward protrusion and downward protrusion curvature of the equipotential lines is suppressed, the lowering of the threshold voltage that usually results from the short channel effect and the raising of the threshold voltage, which is the opposite phenomena, are effectively prevented. Furthermore, by virtue of this constitution, the depletion layer is prevented from extending from the source or the drain by the recessed groove structure, whereby the breakdown voltage between the source and the drain can be increased.").
wherein a channel-free zone develops in the substrate, under the gate and between the source and drain regions, when the transistor is in a turned-off state; and	*See, e.g.*, JPA '394 at Figs 1-4; *see, e.g.*, JPA '394 translation at 2 ("The equipotential line distribution of an MOS transistor according to this invention, when operating, is schematically illustrated in FIG. 3. As shown in the drawing, the spread of the depletion layer resulting from the built-in voltage in the source region and the spread of the depletion layer resulting from the built-in voltage plus, [sic] the drain voltage is substantially absorbed by the part between the channel surface and the source and drain junction surfaces so that the equipotential lines in the vicinity of the channel surface are nearly parallel lines. Because upward protrusion and downward protrusion curvature of the equipotential lines is suppressed, the lowering of the threshold voltage that usually results from the short channel effect and the raising of the threshold voltage, which is the opposite phenomena, are effectively prevented. Furthermore, by virtue of this constitution, the depletion layer is prevented from extending from the source or the drain by the recessed groove structure, whereby the breakdown voltage between the source and the drain can be increased.").
wherein the gate and concave surface portion are curved at least in the vicinity of the channel-free zone such that a smoothly curved depletion zone boundary will develop in the vicinity of the	*See, e.g.*, JPA '394 at Figs 1-4; *see, e.g.*, JPA '394 translation at 2 ("The equipotential line distribution of an MOS transistor according to this invention, when operating, is schematically illustrated in FIG. 3. As shown in the drawing, the spread of the depletion layer resulting from the built-in voltage in the source region and the spread of the depletion layer resulting from the built-in voltage plus, [sic] the drain voltage is substantially absorbed by the part between the channel surface and the source and drain junction surfaces so that the equipotential lines in the vicinity of the channel surface are nearly parallel lines. Because upward protrusion

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channel-free zone when the transistor is in the turned-off state.	and downward protrusion curvature of the equipotential lines is suppressed, the lowering of the threshold voltage that usually results from the short channel effect and the raising of the threshold voltage, which is the opposite phenomena, are effectively prevented. Furthermore, by virtue of this constitution, the depletion layer is prevented from extending from the source or the drain by the recessed groove structure, whereby the breakdown voltage between the source and the drain can be increased.").
Claim 5	
Claim limitation	**JPA '394**
5. An insulated-gate field effect transistor according to claim 4 wherein the concave surface portion is curved in a transverse cross-sectional plane extending through the transistor between but not intersecting the first and second sides of the gate so as to provide an effective channel width greater than a width of the channel as projected onto the plane of the main substrate surface.	*See, e.g.*, JPA '394 at Figs 1-4; *see, e.g.*, JPA '394 translation at 1 ("This invention relates to a MOSFET having improved characteristics as a results of alleviating or eliminating the lowering of the threshold voltage that results from the short channel effect, as well as preventing increases in the threshold voltage (reverse short channel effect), which are possible in MOSFETs having grooved structures."); *see, e.g.*, *id.* at 1-2 ("[T]he MOSFET channel region is formed at the bottom of a grove [sic, groove] provided in the surface of the semiconductor and the source and drain diffusion areas are formed higher than the channel region…"); *see, e.g.*, *id.* at 2 ("As shown in FIG. 1, a MOSFET channel area is formed at the bottom of a groove having a depth d, which is formed in the surface of the [substrate]. Then, the MOSFET is fabricated so that, when the depths of the source and drain diffusion areas are X_{sJ} and X_{dJ}, respectively, X_{sJ} and X_{dJ} substantially satisfy: $d \geq X_{sJ} \geq d - \sqrt{\frac{2\epsilon}{qN}}\left(\sqrt{\lvert V_{sub} \rvert + V_B} - \sqrt{\lvert V_{sub} \rvert + 2\phi_F}\right)$ $d \geq X_{dJ} \geq d - \sqrt{\frac{2\epsilon}{qN}}\left(\sqrt{\lvert V_{sub} \rvert + V_D + V_B} - \sqrt{\lvert V_{sub} \rvert + 2\phi_F}\right)$."); *see, e.g.*, *id.* ("A resist is applied and etching is performed so as to form a recessed groove (13) having a width of approximately 3 μ and a depth of approximately 1.5 μ in the MOS transistor channel formation region.").
Claim 6	
Claim limitation	**JPA '394**
6. An insulated-gate field effect transistor according to claim 5	*See, e.g.*, JPA '394 at Figs 1-4; *see, e.g.*, JPA '394 translation at 1 ("This invention relates to a MOSFET having improved characteristics as a results of alleviating or eliminating the lowering of the threshold voltage that

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wherein the concave surface portion is curved both in the transverse cross-sectional plane and in a non-transverse cross-sectional plane, extending between and joining the first and second sides of the gate, so as to provide an effective channel surface area greater than an area of the channel as projected onto the plane of the main substrate surface.	results from the short channel effect, as well as preventing increases in the threshold voltage (reverse short channel effect), which are possible in MOSFETs having grooved structures."); *see, e.g., id.* at 1-2 ("[T]he MOSFET channel region is formed at the bottom of a grove [sic, groove] provided in the surface of the semiconductor and the source and drain diffusion areas are formed higher than the channel region…"); *see, e.g., id.* at 2 ("As shown in FIG. 1, a MOSFET channel area is formed at the bottom of a groove having a depth d, which is formed in the surface of the [substrate]. Then, the MOSFET is fabricated so that, when the depths of the source and drain diffusion areas are X_{sJ} and X_{dJ}, respectively, X_{sJ} and X_{dJ} substantially satisfy: $d \geq X_{sJ} \geq d - \sqrt{\frac{2\epsilon}{qN}}\left(\sqrt{\lvert V_{evB}\rvert + V_B} - \sqrt{\lvert V_{evB}\rvert + 2\phi_F}\right)$ $d \geq X_{dJ} \geq d - \sqrt{\frac{2\epsilon}{qN}}\left(\sqrt{\lvert V_{evB}\rvert + V_D + V_B} - \sqrt{\lvert V_{evB}\rvert + 2\phi_F}\right)$."); *see, e.g., id.* ("A resist is applied and etching is performed so as to form a recessed groove (13) having a width of approximately 3 μ and a depth of approximately 1.5 μ in the MOS transistor channel formation region."); *see, e.g., id.* ("[A] semicircular or V-shaped groove or any other shaped groove may be used to achieve substantially the same effect.").

Claim 7

Claim limitation	JPA '394
7. An insulated-gate field effect transistor according to claim 6 wherein the concave surface portion is equally curved both in the transverse cross-sectional plane and in the non-transverse cross-sectional plane, so as to provide a sheet-like depletion region having a uniform thickness and a smooth bottom boundary underlying the channel region and the source and drain regions, when the transistor is in a	*See, e.g.*, JPA '394 at Figs 1-4; *see, e.g.*, JPA '394 translation at 1 ("This invention relates to a MOSFET having improved characteristics as a results of alleviating or eliminating the lowering of the threshold voltage that results from the short channel effect, as well as preventing increases in the threshold voltage (reverse short channel effect), which are possible in MOSFETs having grooved structures."); *see, e.g., id.* at 1-2 ("[T]he MOSFET channel region is formed at the bottom of a grove [sic, groove] provided in the surface of the semiconductor and the source and drain diffusion areas are formed higher than the channel region…"); *see, e.g., id.* at 2 ("As shown in FIG. 1, a MOSFET channel area is formed at the bottom of a groove having a depth d, which is formed in the surface of the [substrate]. Then, the MOSFET is fabricated so that, when the depths of the source and drain diffusion areas are X_{sJ} and X_{dJ}, respectively, X_{sJ} and X_{dJ} substantially satisfy:

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turned-off state.	$d \geq X_{dJ} \geq d - \sqrt{\frac{2\epsilon}{qN}} (\sqrt{\lvert V_{BVB} \rvert + V_B} - \sqrt{\lvert V_{BVB} \rvert + 2\phi_F})$ $d \geq X_{dJ} \geq d - \sqrt{\frac{2\epsilon}{qN}} (\sqrt{\lvert V_{BVB} \rvert + V_D + V_B} - \sqrt{\lvert V_{BVB} \rvert + 2\phi_F})$."); *see, e.g.*, *id.* ("A resist is applied and etching is performed so as to form a recessed groove (13) having a width of approximately 3 μ and a depth of approximately 1.5 μ in the MOS transistor channel formation region."); *see, e.g.*, *id.* ("[A] semicircular or V-shaped groove or any other shaped groove may be used to achieve substantially the same effect.").
Claim 11	
Claim limitation	**JPA '394**
11. An insulated-gate field effect transistor according to claim 4 wherein the depth of the concave surface portion is set to a value which ranges between one and two times the depth of the source and drain regions.	*See, e.g.*, JPA '394 at Figs 1-4; *see, e.g.*, JPA '394 translation at 2 ("The resist is removed and the silicon surface is thermally oxidized so as to form a gate silicon oxide film (14) of approximately 1000 Å, and thereon a polycrystalline silicone gate electrode (15) is formed (d). So as to achieve self alignment with the polycrystalline silicone the gate electrode, first an N-type impurity is diffused in the source region (e) and then likewise diffused in the drain region, so as to form a source diffusion region (16) having an impurity level of approximately $10^{19}/cm^3$ and a depth of 1.4 μ, and a drain diffusion region (17) having substantially the same concentration and a depth of approximately 0.7 μ."); *see, e.g.*, *id.* ("A resist is applied and etching is performed so as to form a recessed groove (13) having a width of approximately 3 μ and a depth of approximately 1.5 μ in the MOS transistor channel formation region.").

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All asserted claims are anticipated by the Natori and/or are rendered obvious by it, either alone or in combination with other prior art described below and/or listed in Section I of Defendants' and Counterclaimants' Preliminary Invalidity Contentions and/or through modifications described below. Nothing in this invalidity chart should be construed as signifying or suggesting Defendants and Counterclaimants' adoption of or acquiescence in any claim scope and/or claim construction positions taken by Plaintiffs and Counterdefendants in this litigation.

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Claim 1	
Claim limitation	**Natori**
1 An insulated gate field effect device comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, Natori discloses an insulated gate field effect device. *See, e.g.*, Natori at Fig. 4.
a first conductivity type semiconductor substrate having a main surface;	*See, e.g.*, Natori at Fig. 4.
said semiconductor substrate having a concave surface formed on said main surface extending to a prespecified depth below the main surface;	*See, e.g.*, Natori at Fig. 4, 9, 13, 14; *see, e.g.*, *id.* at 448-49 (List of Symbols); *see, e.g.*, *id.* at 450 ("This paper shows … the concave MOS structure…. The source and drain junction depth is shallower than the channel region. This means that a negative x_J can be realized in the MOSFET."); *see, e.g.*, *id.* at 455 ("As for the optimum structure of the concave MOSFET, two possibilities are pointed out. One of them is the adjustment of the junction depth x_J so that neither the threshold voltage increase nor the lowering takes place. And the other is the adjustment of the corner structure in the channel region of the MOSFET. The two limitting [sic] cases along this line are the V-MOSFET and the cylindrical MOSFET. The value of R in the corner is desired to satisfy the condition $R >> t_{ox}$, or else the decrease of the capacitance of the gate oxide is brought about and the decrease of the conductance of the MOSFET results.").
an insulating film formed on said concave surface;	*See, e.g.*, Natori at Fig. 4; *see, e.g.*, *id.* at 454 ("Then the thick field oxide layer is placed, the transistor region is defined, a polysilicon gate is formed on the gate oxide with t_{ox} = 1000 Å, and the source and the drain regions are diffused.").

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a conductive gate electrode formed above said insulating film, overlying the concave surface;	*See, e.g.*, Natori at Fig. 4; *see, e.g.*, *id.* at 454 ("Then the thick field oxide layer is placed, the transistor region is defined, a polysilicon gate is formed on the gate oxide with t_{ox} = 1000 Å, and the source and the drain regions are diffused.").
first and second impurity regions of a second conductivity type respectively formed in the substrate, in the vicinity of said main surfaces, self-aligned to and positioned at one side and the other side of said gate electrode respectively; and	*See, e.g.*, Natori at Fig. 4; *see, e.g.*, *id.* at 454 ("Then the thick field oxide layer is placed, the transistor region is defined, a polysilicon gate is formed on the gate oxide with t_{ox} = 1000 Å, and the source and the drain regions are diffused.").
a first conductivity type region located in said semiconductor substrate between said first and second impurity regions for defining a channel region and a channel-free region extending conformably under and along said concave surface;	*See, e.g.*, Natori at Figs. 4, 5, 6, 9, 13; *see, e.g.*, *id.* at 448-49 (List of Symbols); *see, e.g.*, *id.* at 450 ("The profile of the depletion region and the equipotential lines in this situation is illustrated in Fig. 5(a). This condition will be realized by (1) and (2) in the one-sided step junction approximation $x_{sJ} = P - (x_{dS} - x_{dG})$, at source (1) $x_{dJ} = P - (x_{dD} - x_{dG})$, at drain. (2) When x_{sJ} and x_{dJ} are larger than $\{P - (x_{dS} - x_{dG})\}$ and $\{P - (x_{dD} - x_{dG})\}$, respectively, Fig. 5(b) schematically shows the profile of the depletion charge and the equipotential lines. Since the profile of equipotential line distribution is similar to that of Fig. 3, the threshold voltage lowering is brought about. On the other hand, if x_{sJ} and x_{dJ} are smaller than $\{P - (x_{dS} - x_{dG})\}$ and $\{P - (x_{dD} - x_{dG})\}$, respectively, the equipotential lines bend in the opposite direction as shown in Fig. 5(c)."); *see, e.g.*, *id.* ("Fig. 6 shows the cross-sectional view of the gate controlled diode region included in the MOSFET structure and the depletion charge profile near there. The depletion charge width near the gate oxide is broader in the concave structure than in the normal one. This suggests that the electric field in the concave MOSFET is less than in the standard MOSFET structure. Since the surface induced avalanche breakdown is initiated at these high-field regions, the breakdown voltage of the concave MOSFET is higher than that of the normal shallow diffusion MOSFET."); *see, e.g.*, *id.* at 452 ("Fig. 9 shows an example of the equipotential line distribution in the triode region of a concave MOSFET. The width of the gate oxide is not correctly illustrated in the figure. The profile of the equipotential line distribution is similar to Fig. 5(c) and the increase of the threshold voltage is seen in this

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	example. The threshold voltage of the concave MOSFET in Fig. 4 is controlled by the high threshold voltage value of the corner MOSFET's in the equivalent circuit model of Fig. 7."); *see, e.g., id.* at 453 ("Fig. 13(a) shows that the pinchoff point is located near the corner on the drain side. The electrostatic potential distribution near the corner on the source side is not so much affected by the drain voltage and the normal device action is not disturbed by the punch-through breakdown of the MOSFET. According to Fig. 13(b), on the other hand, the electrostatic potential distribution near the source of the normal MOSFET is much affected by the drain voltage. The fact that one of the equipotential lines in the figure does not approach the semiconductor surface indicates that the potential barrier between the source and the drain is lowered by the effect of the drain voltage. This figure as well as other calculated data suggest the presence of the punch-through breakdown of the MOSFET. Thus it is concluded that the concave MOSFET structure has the advantage of the higher punch-through breakdown voltage than in the normal MOSFET structure.").
wherein the depth of said concave surface is set to a value which ranges between one and two times the depth of said first and second impurity regions, and	*See, e.g.*, Natori at Figs. 4, 5, 9, 13; *see, e.g., id.* at 448-49 (List of Symbols); *see, e.g., id.* at 450 ("The cross-sectional view of an ideal concave MOSFET is shown in Fig. 4. The source and drain junction depth is shallower than the channel region."); *see, e.g., id.* ("The profile of the depletion region and the equipotential lines in this situation is illustrated in Fig. 5(a). This condition will be realized by (1) and (2) in the one-sided step junction approximation $x_{sJ} = P - (x_{dS} - x_{dG})$, at source (1) $x_{dJ} = P - (x_{dD} - x_{dG})$, at drain. (2) When x_{sJ} and x_{dJ} are larger than $\{P - (x_{dS} - x_{dG})\}$ and $\{P - (x_{dD} - x_{dG})\}$, respectively, Fig. 5(b) schematically shows the profile of the depletion charge and the equipotential lines. Since the profile of equipotential line distribution is similar to that of Fig. 3, the threshold voltage lowering is brought about. On the other hand, if x_{sJ} and x_{dJ} are smaller than $\{P - (x_{dS} - x_{dG})\}$ and $\{P - (x_{dD} - x_{dG})\}$, respectively, the equipotential lines bend in the opposite direction as shown in Fig. 5(c)."); *see, e.g., id.* at 455 ("As for the optimum structure of the concave MOSFET, two possibilities are pointed out. One of them is the adjustment of the junction depth x_J so that neither the threshold voltage increase nor the lowering takes place."); *see, e.g., id.* at 454 ("The source and the drain diffused with phosphorus has the fixed junction depth of 1.5 µm.... The depth of the groove has a fixed value of 1.5 µm in all cases.").

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wherein the concave surface is continuously curved in the vicinity of at least one of the first and second impurity regions to produce smooth merger of a conforming first depletion region formed around the at least one impurity region and a conforming second depletion region formed in the vicinity of the gate electrode so that excessive field concentration will not develop in the vicinity where the first and second depletion regions meet.	*See, e.g.*, Natori at Figs. 4, 5, 6, 9, 13; *see, e.g.*, *id.* at 448-49 (List of Symbols); *see, e.g.*, *id.* at 450 ("The profile of the depletion region and the equipotential lines in this situation is illustrated in Fig. 5(a). This condition will be realized by (1) and (2) in the one-sided step junction approximation $x_{sJ} = P - (x_{dS} - x_{dG})$, at source (1) $x_{dJ} = P - (x_{dD} - x_{dG})$, at drain. (2) When x_{sJ} and x_{dJ} are larger than $\{P - (x_{dS} - x_{dG})\}$ and $\{P - (x_{dD} - x_{dG})\}$, respectively, Fig. 5(b) schematically shows the profile of the depletion charge and the equipotential lines. Since the profile of equipotential line distribution is similar to that of Fig. 3, the threshold voltage lowering is brought about. On the other hand, if x_{sJ} and x_{dJ} are smaller than $\{P - (x_{dS} - x_{dG})\}$ and $\{P - (x_{dD} - x_{dG})\}$, respectively, the equipotential lines bend in the opposite direction as shown in Fig. 5(c)."); *see, e.g.*, *id.* ("Fig. 6 shows the cross-sectional view of the gate controlled diode region included in the MOSFET structure and the depletion charge profile near there. The depletion charge width near the gate oxide is broader in the concave structure than in the normal one. This suggests that the electric field in the concave MOSFET is less than in the standard MOSFET structure. Since the surface induced avalanche breakdown is initiated at these high-field regions, the breakdown voltage of the concave MOSFET is higher than that of the normal shallow diffusion MOSFET."); *see, e.g.*, *id.* at 452 ("Fig. 9 shows an example of the equipotential line distribution in the triode region of a concave MOSFET. The width of the gate oxide is not correctly illustrated in the figure. The profile of the equipotential line distribution is similar to Fig. 5(c) and the increase of the threshold voltage is seen in this example. The threshold voltage of the concave MOSFET in Fig. 4 is controlled by the high threshold voltage value of the corner MOSFET's in the equivalent circuit model of Fig. 7."); *see, e.g.*, *id.* at 453 ("Fig. 13(a) shows that the pinchoff point is located near the corner on the drain side. The electrostatic potential distribution near the corner on the source side is not so much affected by the drain voltage and the normal device action is not disturbed by the punch-through breakdown of the MOSFET. According to Fig. 13(b), on the other hand, the electrostatic potential distribution near the source of the normal MOSFET is much affected by the drain voltage. The fact that one of the equipotential lines in the figure does not approach the semiconductor surface indicates that the potential barrier between the source and the drain is lowered by the effect of the drain voltage. This figure as well as other calculated data suggest the presence of the punch-through breakdown of the MOSFET. Thus it is concluded that the concave MOSFET structure has the advantage of the higher punch-through breakdown voltage than in the normal MOSFET structure.").

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Claim 2

Claim limitation	Natori
2. An insulated gate field effect device according to claim 1, wherein one of said first and second impurity regions constitutes a drain region of said insulated gate field effect device, the other of said first and second impurity regions constitutes a source region and wherein the concave surface is continuously curved at least in the vicinity of the drain region, where the channel-free region develops during an off state of the device, to produce smooth merger of the conforming first depletion region which develops in the vicinity of the channel-free region and the drain region and the conforming second depletion region formed in the vicinity of the gate electrode so that excessive field concentration will not develop in the vicinity of the channel-free region.	*See, e.g.*, Natori at Figs. 4, 5, 6, 9, 13; *see, e.g.*, *id.* at 448-49 (List of Symbols); *see, e.g.*, *id.* at 450 ("The profile of the depletion region and the equipotential lines in this situation is illustrated in Fig. 5(a). This condition will be realized by (1) and (2) in the one-sided step junction approximation $x_{sJ} = P - (x_{dS} - x_{dG})$, at source (1) $x_{dJ} = P - (x_{dD} - x_{dG})$, at drain. (2) When x_{sJ} and x_{dJ} are larger than $\{P - (x_{dS} - x_{dG})\}$ and $\{P - (x_{dD} - x_{dG})\}$, respectively, Fig. 5(b) schematically shows the profile of the depletion charge and the equipotential lines. Since the profile of equipotential line distribution is similar to that of Fig. 3, the threshold voltage lowering is brought about. On the other hand, if x_{sJ} and x_{dJ} are smaller than $\{P - (x_{dS} - x_{dG})\}$ and $\{P - (x_{dD} - x_{dG})\}$, respectively, the equipotential lines bend in the opposite direction as shown in Fig. 5(c)."); *see, e.g.*, *id.* ("Fig. 6 shows the cross-sectional view of the gate controlled diode region included in the MOSFET structure and the depletion charge profile near there. The depletion charge width near the gate oxide is broader in the concave structure than in the normal one. This suggests that the electric field in the concave MOSFET is less than in the standard MOSFET structure. Since the surface induced avalanche breakdown is initiated at these high-field regions, the breakdown voltage of the concave MOSFET is higher than that of the normal shallow diffusion MOSFET."); *see, e.g.*, *id.* at 452 ("Fig. 9 shows an example of the equipotential line distribution in the triode region of a concave MOSFET. The width of the gate oxide is not correctly illustrated in the figure. The profile of the equipotential line distribution is similar to Fig. 5(c) and the increase of the threshold voltage is seen in this example. The threshold voltage of the concave MOSFET in Fig. 4 is controlled by the high threshold voltage value of the corner MOSFET's in the equivalent circuit model of Fig. 7."); *see, e.g.*, *id.* at 453 ("Fig. 13(a) shows that the pinchoff point is located near the corner on the drain side. The electrostatic potential distribution near the corner on the source side is not so much affected by the drain voltage and the normal device action is not disturbed by the punch-through breakdown of the MOSFET. According to Fig. 13(b), on the other hand, the electrostatic potential distribution near the source of the normal MOSFET is much affected by the drain voltage. The fact that one of the equipotential lines in the figure does not approach the semiconductor surface indicates that the potential barrier between the source and the drain is lowered by the effect of the drain

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	voltage. This figure as well as other calculated data suggest the presence of the punch-through breakdown of the MOSFET. Thus it is concluded that the concave MOSFET structure has the advantage of the higher punch-through breakdown voltage than in the normal MOSFET structure."); *see, e.g., id.* at 454 ("Then the thick field oxide layer is placed, the transistor region is defined, a polysilicon gate is formed on the gate oxide with t_{ox} = 1000 Å, and the source and the drain regions are diffused.").
Claim 3	
Claim limitation	**Natori**
3. An insulated gate field effect device according to claim 1, which comprises a metal oxide semiconductor (MOS) transistor, and wherein said insulating film comprises an oxide film.	*See, e.g.*, Natori at Fig. 4; *see, e.g., id.* at 450 ("The cross-sectional view of an ideal concave MOSFET is shown in Fig. 4."); *see, e.g., id.* at 454 ("Then the thick field oxide layer is placed, the transistor region is defined, a polysilicon gate is formed on the gate oxide with t_{ox} = 1000 Å, and the source and the drain regions are diffused.").
Claim 4	
Claim limitation	**Natori**
4. An insulated-gate field effect transistor comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, Natori discloses an insulated-gate field effect transistor. *See, e.g.*, Natori at Fig. 4.
a substrate having a substantially planar main surface and a concave surface portion extending continuously from the main surface to a predetermined depth below the main surface;	*See, e.g.*, Natori at Fig. 4, 9, 13, 14; *see, e.g., id.* at 448-49 (List of Symbols); *see, e.g., id.* at 450 ("This paper shows … the concave MOS structure…. The source and drain junction depth is shallower than the channel region. This means that a negative x_J can be realized in the MOSFET."); *see, e.g., id.* at 455 ("As for the optimum structure of the concave MOSFET, two possibilities are pointed out. One of them is the adjustment of the junction depth x_J so that neither the threshold voltage increase nor the lowering takes place. And the other is the adjustment of the corner structure in the channel region of the MOSFET. The two limitting [sic] cases along this line are the V-MOSFET and the cylindrical MOSFET. The value of R in the corner is desired to satisfy the condition $R >> t_{ox}$, or else the decrease of the capacitance of the gate oxide is brought about and the decrease of the conductance of the MOSFET results.").

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an insulating layer conformably disposed on the main surface and the concave surface portion;	*See, e.g.*, Natori at Fig. 4; *see, e.g.*, *id.* at 454 ("Then the thick field oxide layer is placed, the transistor region is defined, a polysilicon gate is formed on the gate oxide with t_{ox} = 1000 Å, and the source and the drain regions are diffused.").
a gate conformably disposed on the insulating layer, overlying the concave surface portion, the gate having opposed first and second sides;	*See, e.g.*, Natori at Fig. 4; *see, e.g.*, *id.* at 454 ("Then the thick field oxide layer is placed, the transistor region is defined, a polysilicon gate is formed on the gate oxide with t_{ox} = 1000 Å, and the source and the drain regions are diffused.").
implanted source and drain regions disposed within the substrate and self-aligned to the respective first and second opposed sides of the gate; and	*See, e.g.*, Natori at Fig. 4; *see, e.g.*, *id.* at 454 ("Then the thick field oxide layer is placed, the transistor region is defined, a polysilicon gate is formed on the gate oxide with t_{ox} = 1000 Å, and the source and the drain regions are diffused.").
a channel-region formed between the source and drain regions, for defining a channel that conducts current between the source and drain regions when the transistor is in a turned-on state;	*See, e.g.*, Natori at Figs. 4, 5, 6, 9, 13; *see, e.g.*, *id.* at 448-49 (List of Symbols); *see, e.g.*, *id.* at 450 ("The profile of the depletion region and the equipotential lines in this situation is illustrated in Fig. 5(a). This condition will be realized by (1) and (2) in the one-sided step junction approximation $x_{sJ} = P - (x_{dS} - x_{dG})$, at source (1) $x_{dJ} = P - (x_{dD} - x_{dG})$, at drain. (2) When x_{sJ} and x_{dJ} are larger than $\{P - (x_{dS} - x_{dG})\}$ and $\{P - (x_{dD} - x_{dG})\}$, respectively, Fig. 5(b) schematically shows the profile of the depletion charge and the equipotential lines. Since the profile of equipotential line distribution is similar to that of Fig. 3, the threshold voltage lowering is brought about. On the other hand, if x_{sJ} and x_{dJ} are smaller than $\{P - (x_{dS} - x_{dG})\}$ and $\{P - (x_{dD} - x_{dG})\}$, respectively, the equipotential lines bend in the opposite direction as shown in Fig. 5(c)."); *see, e.g.*, *id.* ("Fig. 6 shows the cross-sectional view of the gate controlled diode region included in the MOSFET structure and the depletion charge profile near there. The depletion charge width near the gate oxide is broader in the concave structure than in the normal one. This suggests that the electric field in the concave MOSFET is less than in the standard MOSFET structure. Since the surface induced avalanche breakdown is initiated at these high-field regions, the

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	breakdown voltage of the concave MOSFET is higher than that of the normal shallow diffusion MOSFET."); *see, e.g., id.* at 452 ("Fig. 9 shows an example of the equipotential line distribution in the triode region of a concave MOSFET. The width of the gate oxide is not correctly illustrated in the figure. The profile of the equipotential line distribution is similar to Fig. 5(c) and the increase of the threshold voltage is seen in this example. The threshold voltage of the concave MOSFET in Fig. 4 is controlled by the high threshold voltage value of the corner MOSFET's in the equivalent circuit model of Fig. 7."); *see, e.g., id.* at 453 ("Fig. 13(a) shows that the pinchoff point is located near the corner on the drain side. The electrostatic potential distribution near the corner on the source side is not so much affected by the drain voltage and the normal device action is not disturbed by the punch-through breakdown of the MOSFET. According to Fig. 13(b), on the other hand, the electrostatic potential distribution near the source of the normal MOSFET is much affected by the drain voltage. The fact that one of the equipotential lines in the figure does not approach the semiconductor surface indicates that the potential barrier between the source and the drain is lowered by the effect of the drain voltage. This figure as well as other calculated data suggest the presence of the punch-through breakdown of the MOSFET. Thus it is concluded that the concave MOSFET structure has the advantage of the higher punch-through breakdown voltage than in the normal MOSFET structure.").
wherein a channel-free zone develops in the substrate, under the gate and between the source and drain regions, when the transistor is in a turned-off state; and	*See, e.g.*, Natori at Figs. 4, 5, 6, 9, 13; *see, e.g., id.* at 448-49 (List of Symbols); *see, e.g., id.* at 450 ("The profile of the depletion region and the equipotential lines in this situation is illustrated in Fig. 5(a). This condition will be realized by (1) and (2) in the one-sided step junction approximation $x_{sJ} = P - (x_{dS} - x_{dG})$, at source (1) $x_{dJ} = P - (x_{dD} - x_{dG})$, at drain. (2) When x_{sJ} and x_{dJ} are larger than $\{P - (x_{dS} - x_{dG})\}$ and $\{P - (x_{dD} - x_{dG})\}$, respectively, Fig. 5(b) schematically shows the profile of the depletion charge and the equipotential lines. Since the profile of equipotential line distribution is similar to that of Fig. 3, the threshold voltage lowering is brought about. On the other hand, if x_{sJ} and x_{dJ} are smaller than $\{P - (x_{dS} - x_{dG})\}$ and $\{P - (x_{dD} - x_{dG})\}$, respectively, the equipotential lines bend in the opposite direction as shown in Fig. 5(c)."); *see, e.g., id.* ("Fig. 6 shows the cross-sectional view of the gate controlled diode region included in the MOSFET structure and the depletion charge profile near there. The depletion charge width near the gate oxide is broader in the concave structure than in the normal one. This suggests that the electric field in the concave MOSFET is less than in the standard

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	MOSFET structure. Since the surface induced avalanche breakdown is initiated at these high-field regions, the breakdown voltage of the concave MOSFET is higher than that of the normal shallow diffusion MOSFET."); *see, e.g., id.* at 452 ("Fig. 9 shows an example of the equipotential line distribution in the triode region of a concave MOSFET. The width of the gate oxide is not correctly illustrated in the figure. The profile of the equipotential line distribution is similar to Fig. 5(c) and the increase of the threshold voltage is seen in this example. The threshold voltage of the concave MOSFET in Fig. 4 is controlled by the high threshold voltage value of the corner MOSFET's in the equivalent circuit model of Fig. 7."); *see, e.g., id.* at 453 ("Fig. 13(a) shows that the pinchoff point is located near the corner on the drain side. The electrostatic potential distribution near the corner on the source side is not so much affected by the drain voltage and the normal device action is not disturbed by the punch-through breakdown of the MOSFET. According to Fig. 13(b), on the other hand, the electrostatic potential distribution near the source of the normal MOSFET is much affected by the drain voltage. The fact that one of the equipotential lines in the figure does not approach the semiconductor surface indicates that the potential barrier between the source and the drain is lowered by the effect of the drain voltage. This figure as well as other calculated data suggest the presence of the punch-through breakdown of the MOSFET. Thus it is concluded that the concave MOSFET structure has the advantage of the higher punch-through breakdown voltage than in the normal MOSFET structure.").
wherein the gate and concave surface portion are curved at least in the vicinity of the channel-free zone such that a smoothly curved depletion zone boundary will develop in the vicinity of the channel-free zone when the transistor is in the turned-off state.	*See, e.g.*, Natori at Figs. 4, 5, 6, 9, 13; *see, e.g., id.* at 448-49 (List of Symbols); *see, e.g., id.* at 450 ("The profile of the depletion region and the equipotential lines in this situation is illustrated in Fig. 5(a). This condition will be realized by (1) and (2) in the one-sided step junction approximation $x_{sJ} = P - (x_{dS} - x_{dG})$, at source (1) $x_{dJ} = P - (x_{dD} - x_{dG})$, at drain. (2) When x_{sJ} and x_{dJ} are larger than $\{P - (x_{dS} - x_{dG})\}$ and $\{P - (x_{dD} - x_{dG})\}$, respectively, Fig. 5(b) schematically shows the profile of the depletion charge and the equipotential lines. Since the profile of equipotential line distribution is similar to that of Fig. 3, the threshold voltage lowering is brought about. On the other hand, if x_{sJ} and x_{dJ} are smaller than $\{P - (x_{dS} - x_{dG})\}$ and $\{P - (x_{dD} - x_{dG})\}$, respectively, the equipotential lines bend in the opposite direction as shown in Fig. 5(c)."); *see, e.g., id.* ("Fig. 6 shows the cross-sectional view of the gate controlled diode region included in the MOSFET structure and the depletion charge profile near there. The depletion charge width near the gate oxide is broader in the concave structure

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	than in the normal one. This suggests that the electric field in the concave MOSFET is less than in the standard MOSFET structure. Since the surface induced avalanche breakdown is initiated at these high-field regions, the breakdown voltage of the concave MOSFET is higher than that of the normal shallow diffusion MOSFET."); *see, e.g., id.* at 452 ("Fig. 9 shows an example of the equipotential line distribution in the triode region of a concave MOSFET. The width of the gate oxide is not correctly illustrated in the figure. The profile of the equipotential line distribution is similar to Fig. 5(c) and the increase of the threshold voltage is seen in this example. The threshold voltage of the concave MOSFET in Fig. 4 is controlled by the high threshold voltage value of the corner MOSFET's in the equivalent circuit model of Fig. 7."); *see, e.g., id.* at 453 ("Fig. 13(a) shows that the pinchoff point is located near the corner on the drain side. The electrostatic potential distribution near the corner on the source side is not so much affected by the drain voltage and the normal device action is not disturbed by the punch-through breakdown of the MOSFET. According to Fig. 13(b), on the other hand, the electrostatic potential distribution near the source of the normal MOSFET is much affected by the drain voltage. The fact that one of the equipotential lines in the figure does not approach the semiconductor surface indicates that the potential barrier between the source and the drain is lowered by the effect of the drain voltage. This figure as well as other calculated data suggest the presence of the punch-through breakdown of the MOSFET. Thus it is concluded that the concave MOSFET structure has the advantage of the higher punch-through breakdown voltage than in the normal MOSFET structure.").

Claim 5

Claim limitation	Natori
5. An insulated-gate field effect transistor according to claim 4 wherein the concave surface portion is curved in a transverse cross-sectional plane extending through the transistor between but not intersecting the first and second sides of the gate so as to provide an effective channel width greater than a width of the channel as projected onto the plane of the main substrate	*See, e.g.,* Natori at Figs. 4, 9, 13, 14; *see, e.g., id.* at 448-49 (List of Symbols); *see, e.g., id.* at 450 ("This paper shows … the concave MOS structure…. The source and drain junction depth is shallower than the channel region. This means that a negative x_J can be realized in the MOSFET."); *see, e.g., id.* at 455 ("As for the optimum structure of the concave MOSFET, two possibilities are pointed out. One of them is the adjustment of the junction depth x_J so that neither the threshold voltage increase nor the lowering takes place. And the other is the adjustment of the corner structure in the channel region of the MOSFET. The two limitting [sic] cases along this line are the V-MOSFET and the cylindrical MOSFET. The value of R in the corner is desired to satisfy the condition $R >> t_{ox}$, or else the decrease of the capacitance of the gate oxide is brought about and the decrease of the conductance of the MOSFET results.").

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surface.	
Claim 6	
Claim limitation	**Natori**
6. An insulated-gate field effect transistor according to claim 5 wherein the concave surface portion is curved both in the transverse cross-sectional plane and in a non-transverse cross-sectional plane, extending between and joining the first and second sides of the gate, so as to provide an effective channel surface area greater than an area of the channel as projected onto the plane of the main substrate surface.	*See, e.g.*, Natori at Figs. 4, 9, 13, 14; *see, e.g.*, *id.* at 448-49 (List of Symbols); *see, e.g.*, *id.* at 450 ("This paper shows … the concave MOS structure…. The source and drain junction depth is shallower than the channel region. This means that a negative x_J can be realized in the MOSFET."); *see, e.g.*, *id.* at 455 ("As for the optimum structure of the concave MOSFET, two possibilities are pointed out. One of them is the adjustment of the junction depth x_J so that neither the threshold voltage increase nor the lowering takes place. And the other is the adjustment of the corner structure in the channel region of the MOSFET. The two limitting [sic] cases along this line are the V-MOSFET and the cylindrical MOSFET. The value of R in the corner is desired to satisfy the condition $R >> t_{ox}$, or else the decrease of the capacitance of the gate oxide is brought about and the decrease of the conductance of the MOSFET results."); *see, e.g.*, *id.* at 454 (discussing isotropic and anisotropic etching).
Claim 7	
Claim limitation	**Natori**
7. An insulated-gate field effect transistor according to claim 6 wherein the concave surface portion is equally curved both in the transverse cross-sectional plane and in the non-transverse cross-sectional plane, so as to provide a sheet-like depletion region having a uniform thickness and a smooth bottom boundary underlying the channel	*See, e.g.*, Natori at 454 ("The concave groove is formed by etching the (111) silicon plane using silicon oxide as a mask. Two sorts of etchants are tried. One of them is the isotropic etchant that contains hydrofluoric acid and nitric acid, and it acts on each crystallographic plane with equal effectiveness.").

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region and the source and drain regions, when the transistor is in a turned-off state.	
Claim 11	
Claim limitation	**Natori**
11. An insulated-gate field effect transistor according to claim 4 wherein the depth of the concave surface portion is set to a value which ranges between one and two times the depth of the source and drain regions.	*See, e.g.*, Natori at Figs. 4, 5, 9, 13; *see, e.g.*, *id.* at 448-49 (List of Symbols); *see, e.g.*, *id.* at 450 ("The cross-sectional view of an ideal concave MOSFET is shown in Fig. 4. The source and drain junction depth is shallower than the channel region."); *see, e.g.*, *id.* ("The profile of the depletion region and the equipotential lines in this situation is illustrated in Fig. 5(a). This condition will be realized by (1) and (2) in the one-sided step junction approximation $x_{sJ} = P - (x_{dS} - x_{dG})$, at source (1) $x_{dJ} = P - (x_{dD} - x_{dG})$, at drain. (2) When x_{sJ} and x_{dJ} are larger than $\{P - (x_{dS} - x_{dG})\}$ and $\{P - (x_{dD} - x_{dG})\}$, respectively, Fig. 5(b) schematically shows the profile of the depletion charge and the equipotential lines. Since the profile of equipotential line distribution is similar to that of Fig. 3, the threshold voltage lowering is brought about. On the other hand, if x_{sJ} and x_{dJ} are smaller than $\{P - (x_{dS} - x_{dG})\}$ and $\{P - (x_{dD} - x_{dG})\}$, respectively, the equipotential lines bend in the opposite direction as shown in Fig. 5(c)."); *see, e.g.*, *id.* at 455 ("As for the optimum structure of the concave MOSFET, two possibilities are pointed out. One of them is the adjustment of the junction depth x_J so that neither the threshold voltage increase nor the lowering takes place."); *see, e.g.*, *id.* at 454 ("The source and the drain diffused with phosphorus has the fixed junction depth of 1.5 µm.... The depth of the groove has a fixed value of 1.5 µm in all cases.").

Appendix C5
Defendants and Counterclaimants' Invalidity Contentions
Advanced Micro Devices, Inc. et al. v. Samsung Electronics Co., Ltd. et al., Case No. CV-08-0986-SI

U.S. Patent No. 5,248,893 Invalidity Chart: Japanese Patent Application 61-239669 ("JPA '669")

All asserted claims are anticipated by the JPA '669 and/or are rendered obvious by it, either alone or in combination with other prior art described below and/or listed in Section I of Defendants' and Counterclaimants' Preliminary Invalidity Contentions and/or through modifications described below. Nothing in this invalidity chart should be construed as signifying or suggesting Defendants and Counterclaimants' adoption of or acquiescence in any claim scope and/or claim construction positions taken by Plaintiffs and Counterdefendants in this litigation.

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Claim 1	
Claim limitation	**JPA '669**
1 An insulated gate field effect device comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, JPA '669 discloses an insulated gate field effect device. *See*, *e.g.*, Figs. 1-2.
a first conductivity type semiconductor substrate having a main surface;	*See*, *e.g.*, JPA '669 at Fig. 1-2; *see*, *e.g.*, JPA '669 translation at 2 ("[A] 2000Å silicon nitride film (21) is formed using the CVD method on a P-type silicon substrate (22) with an impurity concentration of $10^{16}/cm^3$.").
said semiconductor substrate having a concave surface formed on said main surface extending to a prespecified depth below the main surface;	*See*, *e.g.*, JPA '669 at Figs. 1-2; *see*, *e.g.*, JPA '669 translation at 2 ("Figure 1 is a process diagram of the structure of a transistor of this invention and the formation of the LDD along the walls of an indentation that was formed by means of etching."); *see*, *e.g.*, *id.* ("Figure 2 is a process diagram of the structure of another embodiment of this invention and the formation of the LDD along the walls of a hole that was made by means of LOCOS oxidization.").
an insulating film formed on said concave surface;	*See*, *e.g.*, JPA '669 at Figs. 1-2; *see*, *e.g.*, JPA '669 translation at 2 ("Next, in step (e) the gate oxidized film (15) is formed by means of oxidization at 950°C for 110 minutes."); *see also*, *e.g.*, *id.* ("In step (f), the oxide film is removed, after which the gate oxide film (27) is formed by means of oxidization at 950°C for 110 minutes.").
a conductive gate electrode formed above said insulating film, overlying the concave surface;	*See*, *e.g.*, JPA '669 at Figs. 1-2; *see*, *e.g.*, JPA '669 translation at 2 ("Then, the indentation is filled with the polycrystalline silicon (16) that serves as the gate material using the CVD method in step (f)."); *see*, *e.g.*, *id.* ("Then, in step (g), the hole is filled with the polycrystalline silicon (28) that serves as the gate material using the CVD method.").

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first and second impurity regions of a second conductivity type respectively formed in the substrate, in the vicinity of said main surfaces, self-aligned to and positioned at one side and the other side of said gate electrode respectively; and	*See, e.g.*, JPA '669 at Figs. 1-2; *see, e.g.*, JPA '669 translation at 1 ("A widely known countermeasure is provision of a drain that consists of a low-concentration diffusion layer in the area near the gate and a normal high-concentration diffusion layer in the other areas (hereinafter, an 'LDD'), lessening the convergence of electrical fields."); *see, e.g.*, *id.* at 2 ("In (f) the LDD is formed longitudinally along the wall of the groove and part of the channel is formed longitudinally and across the floor of the indentation."); *see, e.g.*, *id.* ("In step (g), the LDD is formed at an angle along the walls of the hole and the channel is formed so as to wrap around the floor of the hole."). One of skill in the art at the time of the '893 patent would have known to implement self-alignment. *See, e.g.*, Natori, et. al., An Analysis of the Concave MOSFET, *IEEE Transactions on Electron. Devices*, Vol. ED-25, No. 4, April 1978 ("Natori") at at Fig. 4; *see, e.g.*, *id.* at 454 ("Then the thick field oxide layer is placed, the transistor region is defined, a polysilicon gate is formed on the gate oxide with t_{ox} = 1000 Å, and the source and the drain regions are diffused.").
a first conductivity type region located in said semiconductor substrate between said first and second impurity regions for defining a channel region and a channel-free region extending conformably under and along said concave surface;	*See, e.g.*, JPA '669 at Figs. 1-2; *see, e.g.*, JPA '669 translation at 1 ("A widely known countermeasure is provision of a drain that consists of a low-concentration diffusion layer in the area near the gate and a normal high-concentration diffusion layer in the other areas (hereinafter, an 'LDD'), lessening the convergence of electrical fields."); *see, e.g.*, *id.* at 2 ("In (f) the LDD is formed longitudinally along the wall of the groove and part of the channel is formed longitudinally and across the floor of the indentation."); *see, e.g.*, *id.* ("In step (g), the LDD is formed at an angle along the walls of the hole and the channel is formed so as to wrap around the floor of the hole.").
wherein the depth of said concave surface is set to a value which ranges between one and two times the depth of said first and second impurity regions, and	*See, e.g.*, JPA '669 at Figs. 1-2; *see, e.g.*, JPA '669 translation at 2 ("In step (a), a P-type silicon substrate (12) with an impurity concentration of $10^{16}/cm^3$ is oxidized to form a buffer oxidized film (11) with a depth of 2000Å. In step (b), ion injection of phosphorous is carried out at an energy of 120 KeV and a dose of 3 X $10^{13}/cm^2$ and dispersed for 120 minutes at 1000°C in order to provide the deep low-concentration diffusion layer (13). Next, in step (c) ion injection of arsenic at 50 KeV and 4 X $10^{13}/cm^2$ is carried out in order to provide the shallow high-concentration diffusion layer (14). In step (d), an indentation (18) with a depth of 8000Å is created by means of anisotropic ion etching using a gas such as CBrF3. Next, in step (e) the gate oxidized film (15) is formed by means of oxidization at 950°C for 110 minutes. Dispersion of both phosphorous and arsenic is carried out. Then, the indentation is filled with the polycrystalline silicon (16) that serves as the gate material using the CVD method in step (f). In (f) the LDD is formed longitudinally along the wall of the groove and part of the channel is formed longitudinally and across the floor of the indentation."); *see, e.g.*, *id.* ("In step (a), a 2000Å silicon nitride film (21) is formed using the CVD method on a P-type silicon

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	substrate (22) with an impurity concentration of $10^{16}/cm^3$. Next, in step (b), the LOCOS oxidized layer (23) is formed using water vapor oxidization at 1000°C for 5 hours. In step (c), the silicon nitride film (21) is removed, after which oxidization is carried out to create a 200Å buffer oxide film (24). Then, in step (d), ion injection of phosphorous is carried out at 100 KeV and 3 X $10^{13}/cm^2$ and dispersed at 1000°C for 90 minutes in order to provide the deep low-concentration diffusion layer. In step (e), ion injection of arsenic is carried out at 50 KeV and 5 X $10^{15}/cm^2$ in order to provide the shallow high-concentration diffusion layer. In step (f), the oxide film is removed, after which the gate oxide film (27) is formed by means of oxidization at 950°C for 110 minutes. Dispersion of both phosphorous and arsenic is carried out. Then, in step (g), the hole is filled with the polycrystalline silicon (28) that serves as the gate material using the CVD method. In step (g), the LDD is formed at an angle along the walls of the hole and the channel is formed so as to wrap around the floor of the hole.").
wherein the concave surface is continuously curved in the vicinity of at least one of the first and second impurity regions to produce smooth merger of a conforming first depletion region formed around the at least one impurity region and a conforming second depletion region formed in the vicinity of the gate electrode so that excessive field concentration will not develop in the vicinity where the first and second depletion regions meet.	*See, e.g.*, JPA '669 at Figs. 1-2; *see, e.g.*, JPA '669 translation at 1 ("A widely known countermeasure is provision of a drain that consists of a low-concentration diffusion layer in the area near the gate and a normal high-concentration diffusion layer in the other areas (hereinafter, an 'LDD'), lessening the convergence of electrical fields."); *see, e.g.*, *id.* at 2 ("In (f) the LDD is formed longitudinally along the wall of the groove and part of the channel is formed longitudinally and across the floor of the indentation."); *see, e.g.*, *id.* ("In step (g), the LDD is formed at an angle along the walls of the hole and the channel is formed so as to wrap around the floor of the hole.").
<u>Claim 2</u>	
Claim limitation	**JPA '669**
2. An insulated gate field effect device according to claim 1, wherein one of said first and second	*See, e.g.*, JPA '669 at Figs. 1-2; *see, e.g.*, JPA '669 translation at 1 ("A widely known countermeasure is provision of a drain that consists of a low-concentration diffusion layer in the area near the gate and a normal high-concentration diffusion layer in the other areas (hereinafter, an 'LDD'), lessening the convergence of

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impurity regions constitutes a drain region of said insulated gate field effect device, the other of said first and second impurity regions constitutes a source region and wherein the concave surface is continuously curved at least in the vicinity of the drain region, where the channel-free region develops during an off state of the device, to produce smooth merger of the conforming first depletion region which develops in the vicinity of the channel-free region and the drain region and the conforming second depletion region formed in the vicinity of the gate electrode so that excessive field concentration will not develop in the vicinity of the channel-free region.	electrical fields."); *see, e.g., id.* at 2 ("In (f) the LDD is formed longitudinally along the wall of the groove and part of the channel is formed longitudinally and across the floor of the indentation."); *see, e.g., id.* ("In step (g), the LDD is formed at an angle along the walls of the hole and the channel is formed so as to wrap around the floor of the hole.").
<u>Claim 3</u>	
Claim limitation	**JPA '669**
3. An insulated gate field effect device according to claim 1, which comprises a metal oxide semiconductor (MOS) transistor, and wherein said insulating film comprises an oxide film.	*See, e.g.*, JPA '669 at Figs. 1-2; *see, e.g.*, JPA '669 translation at 2 ("Below, embodiments of the invention within N-channel MOS transistors are explained in detail using figures.").

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Claim 4

Claim limitation	**JPA '669**
4. An insulated-gate field effect transistor comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, JPA '669 discloses an insulated gate field effect transistor. *See, e.g.*, Figs. 1-2.
a substrate having a substantially planar main surface and a concave surface portion extending continuously from the main surface to a predetermined depth below the main surface;	*See, e.g.*, JPA '669 at Figs. 1-2; *see, e.g.*, JPA '669 translation at 2 ("Figure 1 is a process diagram of the structure of a transistor of this invention and the formation of the LDD along the walls of an indentation that was formed by means of etching."); *see, e.g.*, *id.* ("Figure 2 is a process diagram of the structure of another embodiment of this invention and the formation of the LDD along the walls of a hole that was made by means of LOCOS oxidization.").
an insulating layer conformably disposed on the main surface and the concave surface portion;	*See, e.g.*, JPA '669 at Figs. 1-2; *see, e.g.*, JPA '669 translation at 2 ("Next, in step (e) the gate oxidized film (15) is formed by means of oxidization at 950°C for 110 minutes."); *see, e.g.*, *id.* ("[T]he gate oxide film (27) is formed by means of oxidization at 950°C for 110 minutes.").
a gate conformably disposed on the insulating layer, overlying the concave surface portion, the gate having opposed first and second sides;	*See, e.g.*, JPA '669 at Figs. 1-2; *see, e.g.*, JPA '669 translation at 2 ("Then, the indentation is filled with the polycrystalline silicon (16) that serves as the gate material using the CVD method in step (f)."); *see, e.g.*, *id.* ("Then, in step (g), the hole is filled with the polycrystalline silicon (28) that serves as the gate material using the CVD method.").
implanted source and drain regions disposed within the substrate and self-aligned to the respective first and second opposed sides of the gate; and	*See, e.g.*, JPA '669 at Figs. 1-2; *see, e.g.*, JPA '669 translation at 1 ("A widely known countermeasure is provision of a drain that consists of a low-concentration diffusion layer in the area near the gate and a normal high-concentration diffusion layer in the other areas (hereinafter, an 'LDD'), lessening the convergence of electrical fields."); *see, e.g.*, *id.* at 2 ("In (f) the LDD is formed longitudinally along the wall of the groove and part of the channel is formed longitudinally and across the floor of the indentation."); *see, e.g.*, *id.* ("In step (g), the LDD is formed at an angle along the walls of the hole and the channel is formed so as to wrap around the floor of the hole."). One of skill in the art at the time of the '893 patent would have known to implement self-alignment. *See, e.g.*, Natori at at Fig. 4; *see, e.g.*, *id.* at 454 ("Then the thick field oxide layer is placed, the transistor region is defined, a polysilicon gate is formed on the gate oxide with t_{ox} = 1000 Å, and the source and

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	the drain regions are diffused.").
a channel-region formed between the source and drain regions, for defining a channel that conducts current between the source and drain regions when the transistor is in a turned-on state;	*See, e.g.*, JPA '669 at Figs. 1-2; *see, e.g.*, JPA '669 translation at 1 ("A widely known countermeasure is provision of a drain that consists of a low-concentration diffusion layer in the area near the gate and a normal high-concentration diffusion layer in the other areas (hereinafter, an 'LDD'), lessening the convergence of electrical fields."); *see, e.g.*, *id.* at 2 ("In (f) the LDD is formed longitudinally along the wall of the groove and part of the channel is formed longitudinally and across the floor of the indentation."); *see, e.g.*, *id.* ("In step (g), the LDD is formed at an angle along the walls of the hole and the channel is formed so as to wrap around the floor of the hole.").
wherein a channel-free zone develops in the substrate, under the gate and between the source and drain regions, when the transistor is in a turned-off state; and	*See, e.g.*, JPA '669 at Figs. 1-2; *see, e.g.*, JPA '669 translation at 1 ("A widely known countermeasure is provision of a drain that consists of a low-concentration diffusion layer in the area near the gate and a normal high-concentration diffusion layer in the other areas (hereinafter, an 'LDD'), lessening the convergence of electrical fields."); *see, e.g.*, *id.* at 2 ("In (f) the LDD is formed longitudinally along the wall of the groove and part of the channel is formed longitudinally and across the floor of the indentation."); *see, e.g.*, *id.* ("In step (g), the LDD is formed at an angle along the walls of the hole and the channel is formed so as to wrap around the floor of the hole.").
wherein the gate and concave surface portion are curved at least in the vicinity of the channel-free zone such that a smoothly curved depletion zone boundary will develop in the vicinity of the channel-free zone when the transistor is in the turned-off state.	*See, e.g.*, JPA '669 at Figs. 1-2; *see, e.g.*, JPA '669 translation at 1 ("A widely known countermeasure is provision of a drain that consists of a low-concentration diffusion layer in the area near the gate and a normal high-concentration diffusion layer in the other areas (hereinafter, an 'LDD'), lessening the convergence of electrical fields."); *see, e.g.*, *id.* at 2 ("In (f) the LDD is formed longitudinally along the wall of the groove and part of the channel is formed longitudinally and across the floor of the indentation."); *see, e.g.*, *id.* ("In step (g), the LDD is formed at an angle along the walls of the hole and the channel is formed so as to wrap around the floor of the hole.").
Claim 5	
Claim limitation	**JPA '669**
5. An insulated-gate field effect transistor according to claim 4	*See, e.g.*, JPA '669 at Figs. 1-2; *see, e.g.*, JPA '669 translation at 2 ("Figure 1 is a process diagram of the structure of a transistor of this invention and the formation of the LDD along the walls of an indentation that

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wherein the concave surface portion is curved in a transverse cross-sectional plane extending through the transistor between but not intersecting the first and second sides of the gate so as to provide an effective channel width greater than a width of the channel as projected onto the plane of the main substrate surface.	was formed by means of etching."); *see, e.g., id.* (In (f) the LDD is formed longitudinally along the wall of the groove and part of the channel is formed longitudinally and across the floor of the indentation."); *see, e.g., id.* ("Figure 2 is a process diagram of the structure of another embodiment of this invention and the formation of the LDD along the walls of a hole that was made by means of LOCOS oxidization."); *see, e.g., id.* ("In step (g), the LDD is formed at an angle along the walls of the hole and the channel is formed so as to wrap around the floor of the hole.").
Claim 6	
Claim limitation	**JPA '669**
6. An insulated-gate field effect transistor according to claim 5 wherein the concave surface portion is curved both in the transverse cross-sectional plane and in a non-transverse cross-sectional plane, extending between and joining the first and second sides of the gate, so as to provide an effective channel surface area greater than an area of the channel as projected onto the plane of the main substrate surface.	*See, e.g.*, JPA '669 at Figs. 1-2; *see, e.g.*, JPA '669 translation at 2 ("Figure 1 is a process diagram of the structure of a transistor of this invention and the formation of the LDD along the walls of an indentation that was formed by means of etching."); *see, e.g., id.* (In (f) the LDD is formed longitudinally along the wall of the groove and part of the channel is formed longitudinally and across the floor of the indentation."); *see, e.g., id.* ("Figure 2 is a process diagram of the structure of another embodiment of this invention and the formation of the LDD along the walls of a hole that was made by means of LOCOS oxidization."); *see, e.g., id.* ("In step (g), the LDD is formed at an angle along the walls of the hole and the channel is formed so as to wrap around the floor of the hole.").
Claim 7	
Claim limitation	**JPA '669**

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7. An insulated-gate field effect transistor according to claim 6 wherein the concave surface portion is equally curved both in the transverse cross-sectional plane and in the non-transverse cross-sectional plane, so as to provide a sheet-like depletion region having a uniform thickness and a smooth bottom boundary underlying the channel region and the source and drain regions, when the transistor is in a turned-off state.	*See, e.g.*, JPA '669 at Figs. 1-2; *see, e.g.*, JPA '669 translation at 2 ("Figure 1 is a process diagram of the structure of a transistor of this invention and the formation of the LDD along the walls of an indentation that was formed by means of etching."); *see, e.g.*, *id.* (In (f) the LDD is formed longitudinally along the wall of the groove and part of the channel is formed longitudinally and across the floor of the indentation."); *see, e.g.*, *id.* ("Figure 2 is a process diagram of the structure of another embodiment of this invention and the formation of the LDD along the walls of a hole that was made by means of LOCOS oxidization."); *see, e.g.*, *id.* ("In step (g), the LDD is formed at an angle along the walls of the hole and the channel is formed so as to wrap around the floor of the hole.").
Claim 11	
Claim limitation	**JPA '669**
11. An insulated-gate field effect transistor according to claim 4 wherein the depth of the concave surface portion is set to a value which ranges between one and two times the depth of the source and drain regions.	*See, e.g.*, JPA '669 at Figs. 1-2; *see, e.g.*, JPA '669 translation at 2 ("In step (a), a P-type silicon substrate (12) with an impurity concentration of $10^{16}/cm^3$ is oxidized to form a buffer oxidized film (11) with a depth of 2000Å. In step (b), ion injection of phosphorous is carried out at an energy of 120 KeV and a dose of 3 X $10^{13}/cm^2$ and dispersed for 120 minutes at 1000°C in order to provide the deep low-concentration diffusion layer (13). Next, in step (c) ion injection of arsenic at 50 KeV and 4 X $10^{13}/cm^2$ is carried out in order to provide the shallow high-concentration diffusion layer (14). In step (d), an indentation (18) with a depth of 8000Å is created by means of anisotropic ion etching using a gas such as CBrF3. Next, in step (e) the gate oxidized film (15) is formed by means of oxidization at 950°C for 110 minutes. Dispersion of both phosphorous and arsenic is carried out. Then, the indentation is filled with the polycrystalline silicon (16) that serves as the gate material using the CVD method in step (f). In (f) the LDD is formed longitudinally along the wall of the groove and part of the channel is formed longitudinally and across the floor of the indentation."); *see, e.g.*, *id.* ("In step (a), a 2000Å silicon nitride film (21) is formed using the CVD method on a P-type silicon substrate (22) with an impurity concentration of $10^{16}/cm^3$. Next, in step (b), the LOCOS oxidized layer (23) is formed using water vapor oxidization at 1000°C for 5 hours. In step (c), the silicon nitride film (21) is removed, after which oxidization is carried out to create a 200Å buffer oxide film (24). Then, in step (d), ion

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	injection of phosphorous is carried out at 100 KeV and 3 X $10^{13}/cm^2$ and dispersed at 1000°C for 90 minutes in order to provide the deep low-concentration diffusion layer. In step (e), ion injection of arsenic is carried out at 50 KeV and 5 X $10^{15}/cm^2$ in order to provide the shallow high-concentration diffusion layer. In step (f), the oxide film is removed, after which the gate oxide film (27) is formed by means of oxidization at 950°C for 110 minutes. Dispersion of both phosphorous and arsenic is carried out. Then, in step (g), the hole is filled with the polycrystalline silicon (28) that serves as the gate material using the CVD method. In step (g), the LDD is formed at an angle along the walls of the hole and the channel is formed so as to wrap around the floor of the hole.").