EXHIBIT 1

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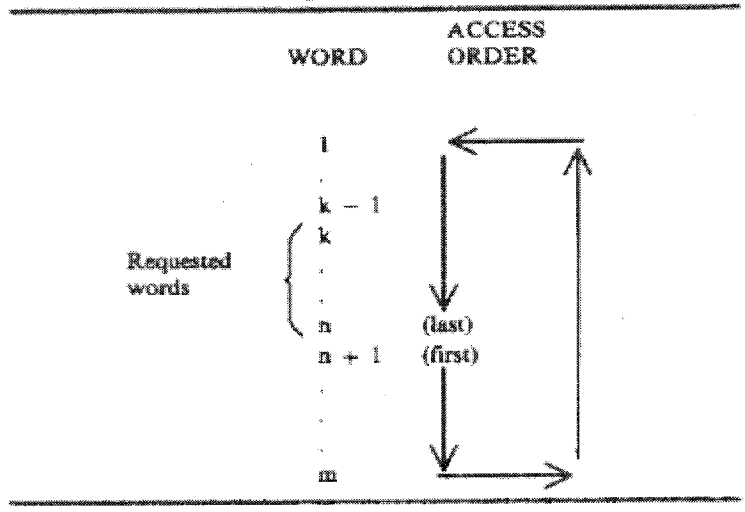
CLAIM	RESPONSE
and	This limitation is met by the '754 Reference in combination with the '494 Reference. The '754 Reference states: "4x2(n-1) (n: a positive integer) memory blocks, each of which includes a plurality of cells substantially arranged in a matrix form, and a plurality of word lines and data lines coupled to said memory cells; ... a plurality of sense amplifying means responsive to a control signal input thereto, for selectively activating one sense amplifying means to sense and amplify data on said selected data lines of one of said two column-selected memory blocks, and for selectively activating at least one other sense amplifying means to refresh data of said each memory cell along said selected word lines ...." ['754 Reference, Page 4:1-10] The '494 Reference states: "The bit lines are each connected to column multiplexing circuitry 37 for each column and coupled to sense amplifier and coupled to sense amplifier and write circuitry 38 for each column. Each sense amplifier and write circuit is connected through a bus driver circuit 39 to the data output 17. Each memory block 14 and 15 has 70 rows each having a word line 25. The word lines are connected to a row decoder 40. The row decoder is coupled to memory block 14 through a latch and word line driver 41 and to the memory block 15 through a latch and word line driver 42. The column multiplex circuitry 37 is controlled by a column counter 44. The row decoder 40 is controlled by a row counter 45. The latch and word line drivers 41 and 42 are controlled by pulse generators 46 and 47 respectively." ['494 Reference, Col. 8:3-17]
in said operation, time tARA does not exceed m * (k-1) * (tOE), wherein: tARA is measured from the time that an address of the first location to be read out in	A person of skill in the art would know that this timing relationship would be used when designing the memory disclosed in claim 1.

CLAIM	RESPONSE
said operation is made available to said memory to the time when said plurality of sense amplifier circuits develops an output signal indicative of the contents of said first location; and tOE is the time to transfer the contents of any one of said locations from said plurality of sense amplifier circuits to said output.	
11. The memory of claim 8 wherein, in said operation, each location to be read out except the first location to be read out is read out to said output in a shorter time than the first location to be read out.	This limitation is met by the '495 Reference alone of in combination with any of the '587 Reference or the '003 Reference or the '199 Reference. Specifically, the '495 Reference states: "Accordingly, read of the memory cells on the digit lines D and [D bar] described in the above becomes feasible without carrying out the activation of the word line. This situation remains valid even if the system recurs to the same word line in a cell array block after access is shifted to another cell array block." ['495 Reference, Col 6: 60-65] The '587 Reference states: "The reduction in the memory access cycle time from a convention memory access operation, generally represented by the first prefetch with a three clock cycle span between event t1 and t2, is clearly evident when the times are compared to those of the consecutive prefetch operation extending for two clock cycles between corresponding time intervals t3 and t4. Time t2 and t4 identify the first clock interval suitable to initiate succeeding memory access operations." ['587 Reference, Col. 5:63-6:3]

CLAIM	RESPONSE
	The '003 Reference states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer. Typically, the access addresses of the 'extra' storage cells differ from the original access address by only one or two bits. However, subsequent accesses to these cells can be accomplished by simply executing additional access cycles without changing the access address. In the art, such memories are referred to as 'nibble mode'. In some other integrated circuit memories, a portion of the original address can be 'assumed' for one (or more) subsequent accesses, so that only the least significant

CLAIM	RESPONSE
	portion of the address needs to be decoded, etc. Thus, once the original access had been completed, subsequent accesses to 'related' storage cells will be significantly quicker." ['199 Reference, Col. 1:13-28]
12. The memory of claim 8 wherein the sequence of locations L1, . . . , Ln is a sequence of increasing order of addresses.	This element is met by the '495 Reference alone or in combination with Reference '196. Specifically, the '495 Reference states: "The RAM is frequently subjected to an access mode in which one address I accessed continuously. Such an access mode is called "page mode" or "static column mode" (represented by "page mode" hereinafter). The continuous address in this case is generally designated by consecutive column addresses for the same row address."['495 Reference, Col 1: 39-45] The '196 Reference states: "Consecutive addresses are mapped sequentially be [sic] columns, so repeated reading or writing effectively marches along the row until the array boundary is reached." ['196 Reference, Col. 1:57-60]
13. The memory of claim 7 wherein in said operation any number of said locations addressed consecutively with wrap around can be read out to said output so that:	This element is met by the '495 Reference in combination with the '885 Reference or the '631 Reference. The '885 Reference states: "After the last memory address is reached, the access automatically rolls over to the first address." ['885 Reference, Col. 3:1-3] "A method as in claim 5 wherein the sequence of incremented addresses wraps around when the address of the Nth register is reached such that all N registers in the array are read." ['885 Reference, Col. 7:45-48]

CLAIM	RESPONSE
	The '631 Reference states that: "The above-described method is accomplished by utilizing two pieces of information, which are placed on the bus (23) by the GDP: the data word's offset and the number of words requested. The data word's offset in the cache line is derived from adress bits 2 and 3 (00=word 1, 01=word 2, 10=word 3, and 11=word 4). The number of words being requested is obtained from the size bits 0 and 1 (00=1word, 01=2 words, 10=3 words, and 11=4words). Using these two pieces of information, the following algorithm is executed: FIRST WORD ACCESSED = PROCESSOR WORD ADDRESS + SIZE +1 The 1 is added to the size in order to yield the correct offset. For example, if the GDP requests two words at offset 01 in a four-word line, it is convereted to a wraparound request of four words to memory starting at word four [offset (01) + word count (01) + 1 = 11]." ['631 Reference, Col. 3:46-65] See, '631 Reference, Table II:

CLAIM	RESPONSE
	TABLE II  See also, '631 Reference, Abstract, Table I, Fig. 3.
the first location to be read out in said operation is read out to said output after time tARA+tOE wherein: tARA is measured from the time that an address of said first location is made available to said memory to the time when said plurality of sense amplifier circuits develops an output signal indicative of the	This element is met by the '196 Reference in combination with any of the '587 Reference or the '003 Reference or the '199 Reference. The '587 Reference states: "The reduction in the memory access cycle time from a convention memory access operation, generally represented by the first prefetch with a three clock cycle span between event t1 and t2, is clearly evident when the times are compared to those of the consecutive prefetch operation extending for two clock cycles between corresponding time intervals t3 and t4. Time t2 and t4 identify the first clock interval suitable to

CLAIM	RESPONSE
contents of said first location; and tOE is the time to transfer the contents of any one of said locations from said plurality of sense amplifier circuits to said output of said memory; and	initiate succeeding memory access operations." ['587 Reference, Col. 5:63-6:3] The '003 Reference states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer. Typically, the access addresses of the 'extra' storage cells differ from the original access address by only one or two bits. However, subsequent accesses to these cells can be accomplished by simply executing additional access cycles without changing the access address. In the art, such memories are referred to as 'nibble mode'. In

CLAIM	RESPONSE
	some other integrated circuit memories, a portion of the original address can be 'assumed' for one (or more) subsequent accesses, so that only the least significant portion of the address needs to be decoded, etc. Thus, once the original access had been completed, subsequent accesses to 'related' storage cells will be significantly quicker." ['199 Reference, Col. 1:13-28]
every other location to be read out in said operation is read out to said output within time tOE.	This element is met by the '196 Reference in combination with any of the '587 Reference or the '003 Reference or the '199 Reference. The '587 Reference states: "The reduction in the memory access cycle time from a convention memory access operation, generally represented by the first prefetch with a three clock cycle span between event t1 and t2, is clearly evident when the times are compared to those of the consecutive prefetch operation extending for two clock cycles between corresponding time intervals t3 and t4. Time t2 and t4 identify the first clock interval suitable to initiate succeeding memory access operations." ['587 Reference, Col. 5:63-6:3] The '003 Reference states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first

CLAIM	RESPONSE
	instruction." ['003 Reference, Col. 10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer. Typically, the access addresses of the 'extra' storage cells differ from the original access address by only one or two bits. However, subsequent accesses to these cells can be accomplished by simply executing additional access cycles without changing the access address. In the art, such memories are referred to as 'nibble mode'. In some other integrated circuit memories, a portion of the original address can be 'assumed' from one (or more) subsequent accesses, so that only the least significant portion of the address needs to be decoded, etc. Thus, once the original access had been completed, subsequent accesses to 'related' storage cells will be significantly quicker." ['199 Reference, Col. 1:13-28]
14. The memory of claim 8 wherein said memory is fabricated in an integrated circuit.	This element is met in the '495 Reference. Specifically, the '495 Reference states that: "Referring to FIG 1, there is shown a block diagram of a conventional dynamic RAM having 4 megabit capacity and being constructed as an integrated circuit device. In particular, this RAM is a 1M×4 dynamic RAM which carries out data write and read operation in the unit of 4 bits. A memory cell array of this dynamic RAM consists of four cell array blocks 10a,10b, 10c, and 10d that are accessed with mutually staggered

CLAIM	RESPONSE
	timings as will be described later. Each of these cell array blocks consists of memory cells arranged in matrix form of 256 rows × 4,096 columns.." ['196 Reference, Col. 2:67-68, 3:1-9; See also FIGS 1, 2]
20. An integrated memory comprising:	Although a preamble is normally not limiting, should this preamble be limiting, this element is met in the '495 Reference. Specifically, the '495 Reference states that: "The present invention relates to a random access memory (RAM) and, more particularly, to a high storage capacity RAM in which a memory cell array consists of a plurality of blocks arranged in the direction of digit lines, each of these blocks being equipped with a row decoder, a column decoder, and a sense amplifier. ['495 Reference, Col. 1:9-14] "Referring to FIG 1, there is shown a block diagram of a conventional dynamic RAM having 4 megabit capacity and being constructed as an integrated circuit device." ['495 Reference, Col. 2:67-68, Col 3, 1: 2]
an array of memory locations, the array comprising a plurality of subarrays, each subarray comprising a predetermined number of groups of columns of the memory locations such that for any given column position in a group, the memory locations in any given row in the columns at said given position in the groups of the subarray have consecutive addresses;	This element is met in the '495 Reference. Specifically, the '495 Reference states that: "Referring to FIG 1, there is shown a block diagram of a conventional dynamic RAM having 4 megabit capacity and being constructed as an integrated circuit device. In particular, this RAM is a 1M×4 dynamic RAM which carries out data write and read operation in the unit of 4 bits. A memory cell array of this dynamic RAM consists of four cell array blocks 10a, 10b, 10c, and 10d that are accessed with mutually staggered timings as will be described later. Each of these cell array blocks consists of memory cells arranged in matrix form of 256 rows × 4,096 columns.." ['196 Reference, Col. 2:67-68, 3:1-9; See also FIGS 1, 2] "The RAM is frequently subjected to an access mode in which one address is accessed continuously. Such an access mode is called "page mode" or "static mode" (represented collectively by "page mode" hereinafter. The continuous address in this

CLAIM	RESPONSE
	case is generally designated by consecutive column addresses for the same row address. Accordingly, redriving of the word lines is not needed so long as the access address remains at an address on the same word line, and in that case it has only to be done to sequentially read data from the memory cell onto the digit lines or to introduce write data to the digit lines from the outside to write the same to the memory cells" ['495 Reference, Col. 1:39-51]
one X-decoder for each subarray;	This element is met in the '495 Reference. Specifically, the '495 Reference states that: "The present invention relates to a random access memory (RAM) and, more particularly, to a high storage RAM in which a memory cell array consists of a plurality of blocks arranged in the direction of digit lines, each of these blocks being equipped with a row decoder, a column decoder, and a sense amplifier" ['495 Reference, Col 1: 5-14]
one X-register for each X-decoder;	This element is met in the '495 Reference. Specifically, the '495 Reference states that: "Preferably, the RAM of the invention includes a register provided for each of the blocks, in addition to the data hold circuit and the block decoder."['495 Reference, Col 2: 21-23] "The register 70a, 70b, 70c, or 70d selected by the block decoder 50 holds 8-bit address codes ARC0-ARC7 supplied in synchronism with the row selection signal RAS. Since the holding of the address codes ARC0-ARC7 will be maintained even after access is shifted to another cell array block, these registers 70a-70d store respectively the address codes ARC0-ARC7 of the last access in the cell array blocks 10a-10d and supply them to the selectors 80a-90d which also receive the address codes ARC0-ARC7 supplied in synchronism with the row selection signal RAS and introduce them to the row decoders 20a to 20d." ['495 Reference, Col 25-37, *See also*

CLAIM	RESPONSE
	FIG 3]
one Y-decoder for each subarray;	This element is met in the '495 Reference. Specifically, the '495 Reference states that: "The present invention relates to a random access memory (RAM) and, more particularly, to a high storage RAM in which a memory cell array consists of a plurality of blocks arranged in the direction of digit lines, each of these blocks being equipped with a row decoder, a column decoder, and a sense amplifier" ['495 Reference, Col 1: 5-14]
one Y-register for each Y-decoder;	This limitation is met by the '495 Reference alone or in combination with the '937 Reference or U.S. Patent No. 5,274,596 ("the '596 Reference"). Specifically, FIG 3 of the '495 Reference shows the 1:1 configuration of the registers with row decoders. Further, it would be obvious to one of ordinary skill in the art concept of using adding an "X register" as taught the '495 Reference would be equally applicable in the "Y" direction. The '937 Reference states: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e. twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. Ina similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e. twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer

CLAIM	RESPONSE
	gate 95." ['937 Reference, Col. 4:29-42] The '596 Reference states that: "Similarly, column address 38 is given as follows. Column address buffer 40 receives an address signal input from the external terminal as an initial value. The initial value is counted up or down by column address counter 42 in response to a serial access control signal input from control circuit 36. Therefore, column address 38 is given." ['596 Reference, Col. 3:41-47] "In addition, a shift register is arranged in the column direction, so that higher-speed serial access can be performed in the column direction." ['596 Reference, Col. 6:15-17] *See also* '596 Reference, Col. 2:55-5:12; Claims 1, 4 and 5.
one Y-select circuit for each subarray, the Y-select circuit being responsive to the Y-decoder of the subarray to select all the columns that occupy a selected position in the groups of the subarray;	This element is met by the '495 Reference in combination with the '596 Reference or the '937 Reference. Specifically, the '596 Reference states: "A column address is input at a trailing edge of [CAS bar] (column address strobe), and a complementary signal is generated by column address buffer 40. The complementary signal is transferred to column address counter 42 and latched. Output 38 from column address counter 42 is transferred to column decoders 16_1, 16_2, ..., 16_n, through a column address bus to select the columns. the readout data is latched by I/O buffer 44. Then, only the data of block 10_1 is output to output terminal D_{OUT}." ['596 Reference, Col. 4:43-52] "At this time, all the memory cells connected to three word lines including two

CLAIM	RESPONSE
	adjacent rows on the logical address plane can be immediately accessed. More specifically, the sense amplifiers are enabled and all the memory cells can be read out and written at any time." ['596 Reference, Col. 4:53-57] The '937 Reference states: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e. twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. Ina similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e. twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42] "Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to a transfer gate 85.... In a similar manner, the transfer gate 95 transfers data read from the second memory cell array 94 to the sense amplifier 96 through an I/O line 103, while transferring data from the write circuit 98 received through the I/O line 103 to the second memory cell array 94." ['937 Reference, Col. 4:33-52]
a plurality of sense amplifier circuits for each subarray, each sense amplifier circuit for amplifying signals from a column selected by the Y-select circuit of the	This element is met by the '495 Reference in combination with the '596 Reference. Specifically, the '495 Reference states: "The present invention relates to a random access memory (RAM) and, more particularly, to a high storage capacity RAM in which a memory cell array consists of

CLAIM	RESPONSE
subarray;	a plurality of blocks arranged in the direction of digit lines, each of these blocks being equipped with a row decoder, a column decoder, and a sense amplifier. ['495 Reference, Col. 1:9-14] "The sense amplifier 30a amplifies the data read out of the 4,096 memory cells connected to the selected word line or transfers data to be written thereto." ['495 Reference, Col 3:20-23] The '596 Reference states: "A column address is input at a trailing edge of [CAS bar] (column address strobe), and a complementary signal is generated by column address buffer 40. The complementary signal is transferred to column address counter 42 and latched. Output 38 from column address counter 42 is transferred to column decoders 16_1, 16_2, ..., 16_n, through a column address bus to select the columns. the readout data is latched by I/O buffer 44. Then, only the data of block 10_1 is output to output terminal D_{OUT}." ['596 Reference, Col. 4:43-52] "At this time, all the memory cells connected to three word lines including two adjacent rows on the logical address plane can be immediately accessed. More specifically, the sense amplifiers are enabled and all the memory cells can be read out and written at any time." ['596 Reference, Col. 4:53-57]
a memory output; and	This element is met in the '495 Reference. Specifically, the '495 Reference states that: "In the time of the read operation, the data read from the four memory cells designated by the work digit lines are amplified by the sense amplifier 30a and the outputted to the outside through I/O0 -I/O3 as 4-bit output data." ['495 Reference, Col 3: 54-57]

CLAIM	RESPONSE
a control circuit for selecting one of the sense amplifier circuits to provide data to the memory output;	This element is met in the '495 Reference in combination with the '754 Reference. Specifically, the '495 Reference states that: "A MOS memory device operating at high speed which is so constructed as to hold the sense amplifier activating signals SAP and SAN at high potential and at low potential, respectively, even after the completion of a memory access, and keep the sense amplifier 30a in activated state to hold read data from memory cells" ['495 Reference, Abstract] Furthermore, FIG 3 shows the connection from the sense amplifiers to the output lines I/O 0-3. It was well known in the art that information in the sense amplifiers could be read out one bit at a time. For example, the '754 Reference discloses this limitation. Specifically, the '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "A semiconductor dynamic memory device comprising: … a plurality of sense amplifying means (18-1 to 18-4; SA1 to SA8) responsive to a control signal input thereto, for selectively activating one sense amplifying means to sense and amplify data on said selected data lines of one of said two column-selected memory blocks, and for selectively activating at least one other sense amplifying means to refresh data to

CLAIM	RESPONSE
	said each memory cell along said selected word lines; ...." ['754 Reference, Page 6:53-7:5] Further, to the extent AMD contends that the accused Samsung devices practice this limitation, this limitation is met by the '495 Reference.
wherein in a burst mode read operation, at least one X-register provides to its respective X-decoder signals identifying a row in one of the subarrays, and at least one Y-register provides to its respective Y-decoder signals identifying a position of columns in the groups of one of the subarrays.	This element is met in the '495 Reference in combination with the '196 Reference or in combination with the '937 Reference or the '754 Reference or U.S. Patent No. 5,036,494 ("the '494 Reference") or admitted prior art disclosed in Figure 2 of the '990 patent. Specifically the '495 Reference states that "Preferably, the RAM of the invention includes a register provided for each of the blocks, in addition to the data hold circuit and the block decoder."['495 Reference, Col 2: 21-23] "The register 70a, 70b, 70c, or 70d selected by the block decoder 50 holds 8-bit address codes ARC0-ARC7 supplied in synchronism with the row selection signal RAS. Since the holding of the address codes ARC0-ARC7 will be maintained even after access is shifted to another cell array block, these registers 70a-70d store respectively the address codes ARC0-ARC7 of the last access in the cell array blocks 10a-10d and supply them to the selectors 80a-90d which also receive the address codes ARC0-ARC7 supplied in synchronism with the row selection signal RAS and introduce them to the row decoders 20a to 20d." ['495 Reference, Col 25-37, See also FIG 3] The '196 Reference states that: "In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit lines in the other array are being precharged. Thus, as

CLAIM	RESPONSE
	data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit lines in that array will already have been initialied." ['196 Reference, Col. 2:60-67] "In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and settling transient signals) in preparation for the next access form such other array. Therefore, precharging times for one array overlap the time for performing read or write operation in the other array, and therefore do not limit operating speed." ['196 Reference, Col. 3:41-47] The '937 patent states that: "The address counter 81 receives the signals $\emptyset_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $\emptyset_{EV}$ (i.e., twice that of the basic clock pulses $\emptyset_S$). Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $\emptyset_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $\emptyset_{OD}$ (i.e., twice that of the basic clock pulses $\emptyset_S$). Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:33-42] The '754 Reference states: "Furthermore, this dynamic memory device has row and column address buffers 20 and 22 for respectively storing row and column address data supplied from an address signal generator (not shown); …." ['754 Reference, Page 4:44-51]

CLAIM	RESPONSE
	"Output data from the row address buffer 20 excluding the most significant bit MSB is supplied to the row decoders 16-1 to 16-4, and the output data from the column address buffer 22 is supplied to the columns decoders 14-1 and 14-2 through the gate circuits 30 and 32, respectively." ['754 Reference, Page 4:52-54] The '494 Reference states: In the example shown in FIG. 1 each memory block 14 and 15 has sixty four columns 35, each column being coupled to equate and precharge circuitry 36. The columns are arranged in groups, each group having eight pairs of bit lines so that when any column is addressed eight pairs of bit lines (one in each group) are simultaneously accessed, permitting transfer of eight bits or one word at a time. The bit lines are each connected to column multiplexing circuitry 37 for each columns and coupled to sense amplifier and write circuitry 38 for each column. Each sense amplifier and write circuit is connected through a bus driver circuit 39 to the data output 17. Each memory block 14 and 15 has 70 rows each having a word line 25. The word lines are connected to a row decoder 40. The row decoder is coupled to memory block 14 through a latch and word line driver 41 and to the memory block 15 through a latch and word line driver 42. The column multiplex circuitry 37 is controlled by a column counter 44. The row decoder 40 is controlled by a row counter 45. The latch and word line drivers 41 and 42 are controlled by pulse generators 46 and 47 respectively. Each of the drivers 41 and 42 is connected by two separate control lines 48 to the respective one of the pulse generators 46 and 47 so that each driver can be operated either to latch the output of the row decoder 40 or to drive all the word lines low. The selection of memory locations forming each cyclic pattern of addressing is controlled by the control until 13. The row counter 45 and columns counter 44 are connected so that unless instructed by the control 13 to do otherwise they count through successive addresses along each row and then row by row." ['494 Reference, Col. 7:44-8:27]

CLAIM	RESPONSE
22. The memory of claim 20 wherein in the burst mode read operation while data from the sense amplifier circuits of one of the subarrays are provided to the memory output, the sense amplifier circuits of another one of the subarrays develop output signals corresponding to data in said other one of the subarrays.	This element is met in the '495 Reference in combination with the '196 Reference. Specifically, the '196 Reference states that: "In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit lines in the other array are being precharged. Thus, as data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit lines in that array will already have been initialized." ['196 Reference, Col. 2:60-67] "In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and settling transient signals) in preparation for the next access form such other array. Therefore, precharging times for one array overlap the time for performing read or write operation in the other array, and therefore do not limit operating speed." ['196 Reference, Col. 3:41-47]
23. The memory of claim 20 wherein in the burst mode read operation, the control circuit enables the sense amplifier circuit selected to provide data to the memory output and at the same time disables one or more sense amplifier circuits not selected to provide data to the memory output.	This limitation is met by the '495 Reference in combination with the '754 Reference or the '788 Reference or the '937 Reference or the '003 Reference or the '178 Reference. The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are

CLAIM	RESPONSE
	activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58] The '788 Reference states: "According to this arrangement, only one plane is selected in accordance with the content of the upper-order two bits of the row address. The selected plane is activated and exhibits the memory operation but the rest of the planes which are under the non-selection state are inoperative. Therefore, the decoders and the sense amplifiers are inoperative in these inoperative planes and the memory is not refreshed. Therefore, power is consumed in only the selected plane and unnecessary power consumption in the other plane can be saved. Thus, the requirement for low power consumption can be satisfied." ['788 Reference, Col. 5:57-68] The '937 Reference states: "The sense amplifier 86 is controlled by the signals SE_{EV} to amplify the read data thereby to supply the same to the data latch 87, which in turn temporarily stores the outputs from the sense amplifiers 86. When the signals SE_{EV} are at low levels, the data latch 87 is electrically cut off from the sense amplifier 86. Data from the data latch 87 are transferred to the output latch 89 when the signals OE_{EV} are at high levels. In a similar manner, the sense amplifier 96 is controlled by the signals SE_{OD} to amplify the read data thereby to supply the same to the data latch 97, which in turn temporarily stores the outputs from the sense amplifier 96. When the signals SE_{OD} are at low levels, the data latch 97 is electrically cut off from the sense amplifier 96." ['937 Reference, Col. 4:52-66] The '003 Reference states:

CLAIM	RESPONSE
	"The flash memory control 88 also selectively enables one of two sets of bi-directional data buffers 90 and 91 which respectively couple the bank data buses 82 and 83 to the processor section data bus 63. The bank data buses 81 and 83 can be coupled to the instruction bus 61 by the flash memory control 88 selectively enabling buffers 92 and 93, respectively." ['003 Reference, Col. 9:21-27] The '178 Reference states: "Referring now to FIG. 2, the circuit of FIG. 1 has been modified to utilize the fact that, when RA10=1, only one half of the ARRAY BANKs 20 are being utilized and that, when RA10=0, the other half of the ARRAY BANKs 20 are being utilized. In particular, the RA 10 address is used to cause only the half of the ARRAY BANKs 20 that are being utilized to draw power from the DRAM energy source during read/write operations, while at the same time permitting the periodic performance of the refresh cycle in the usual manner on all ARRAY BANKs." ['178 Reference, Col. 3:32-42]