EXHIBIT 1

D14-D15

Appendix D14
Defendants and Counterclaimants' Invalidity Contentions
Advanced Micro Devices, Inc., et al., v. Samsung Electronics Co., Ltd., et al., Case No. 3:08-CV-0986-SI

U.S. patent No. 5,559,990 Invalidity Chart: U.S. Patent No. 4,875,596 ("the '596 Reference")

All asserted claims are anticipated by the '596 Reference and/or are rendered obvious by it, either alone or in combination with other prior art described below and/or listed in Section I of Defendants' and Counterclaimants' Preliminary Invalidity Contentions and/or through modifications described below. Nothing in this invalidity chart should be construed as signifying or suggesting Defendants and Counterclaimants' adoption of or acquiescence in any claim scope and/or claim construction positions taken by Plaintiffs and Counterdefendants in this litigation.

CLAIM	RESPONSE
1. A memory comprising:	Although a preamble is normally not limiting, should this preamble be limiting, this element is met by U.S. Patent No. 5,274,596 ("the '596 Reference"). Specifically, the '596 Reference is titled "Dynamic Semiconductor Memory Device Having Simultaneous Operation of Adjacent Blocks."
a plurality of rows of memory locations;	This element is met by the '596 Reference. Specifically, the '596 Reference states: "In such a dRAM according to the embodiment, memory cell arrays of n memory blocks 10_1, 10_2, ..., 10_n selected by corresponding lower row address data, e.g., a lower row address consisting of the LSB to mth bit are divided in a bit line direction. Word lines selected by row addresses adjacent on the logical address plane are distributed to different memory blocks (memory cell array blocks). Memory blocks 10_1, 10_2, ..., 10_n include row decoders 12_1, 12_2, ...,12_n, sense amplifiers 14_1, 14_2, ..., 14_n and column decoders 16_1, 16_2, ..., 16_n,respectively." ['596 Reference, Col. 2:55-65]

a plurality of first registers, each first register for receiving a row address;	This element is met by the '596 Reference alone or in combination with any of U.S. Patent No. 4,875,196 ("the '196 Reference") or U.S. Patent No. 4,849,937 ("the '937 Reference") or U.S. Patent No. 5,367,495 ("the '495 Reference") or U.S. Patent No. 4,759,021 ("the '021 Reference"). Specifically, the '596 Reference states: "Row address buffer 32 receives an address signal input from an external terminal as an initial value. The initial value is counted up or down by row address counter 34 in responseto a serial access control signal input from control circuit 36." ['596 Reference, Col. 3:33-37] To the extent AMD read this limitation on the Samsung devices, the '596 Reference meets this limitation. The '196 Reference states that: "The row and column location in the arrays 31, 33 at which data is accessed is controlled by the counters which, in one embodiment of the invention may be binary counters, or the like, which have an extended counting range that is double the number of address locations in the array to be accessed." ['196 Reference, Col. 4:49-54; See also, FIGS. 2A, 2B] The '937 Reference states: "The address counter 81 receives the signals $\emptyset_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $\emptyset_{EV}$ (i.e., twice that of the basic clock pulses $\emptyset_{S)}$. Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the

	Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e., twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42] The '495 Reference states: "The register 70a, 70b, 70c or 70d selected by the block decoder 50 holds 8-bit address codes ARC0-ARC7 supplied in synchronism with the row selection signal RAS. Since the holding of the address codes ARC0-ARC7 will be maintained even after access is shifted to another cell array block, these registers 70a-70d store respectively the address codes ARC0-ARC7 of the last access in the cell array blocks 10a-10d and supply them to the selectors 80a-80d which also receive the address codes ARC0-ARC7 supplied in synchronism with the row selection signal RAS and introduce them to the row decoders 20a-20d." ['495 Reference, Col. 4:25-37] The '021 Reference states: "Since the low-speed large-capacity memories 11, 12, 13, 14 performing the 4-way interleave operation are shifted in access timing usually by one cycle from each other, the memories 11-14 are provided respectively with registers 23-26 each for holding an address." ['021 Reference, Col. 4:5-9]
a plurality of row decoders, each row decoder for activating a	This elements is met by the '596 Reference. Specifically, the

portion of a row identified by signals from one of said first registers;	'596 Reference states: "Each of memory blocks 10_1, 10_2, ..., 10_n is enabled by corresponding one of block decoders 20_1, 20_2, ..., 20_n on the basis of lower row address 18. Remaining upper row address 22 is input to row decoders 12_1, 12_2, ..., 12_n, and a word line is selected by upper row address 22." ['596 Reference, Col. 2:65-Col. 3:2]
one or more sense amplifiers for amplifying contents of said memory locations in the row portions; and	This element is met by the '596 Reference. Specifically, the '596 Reference states: "Memory blocks 10_1, 10_2, ..., 10_n include row decoders 12_1, 12_2, ...,12_n, sense amplifiers 14_1, 14_2, ..., 14_n and column decoders 16_1, 16_2, ..., 16_n, respectively." ['596 Reference, Col. 2:62-65]
an output for providing output signals from said sense amplifiers,	This element is met by the '596 Reference. Specifically, the '596 Reference states: "Output 38 from column address counter 42 is transferred to column decoders 16_1, 16_2, ..., 16_n, through a column address bus to select the columns. the readout data is latched by I/O buffer 44. Then, only the data of block 10_1 is output to output terminal D_{OUT}." ['596 Reference, Col. 4:47-52]
wherein at least two locations L1 and L2 in different rows having different row addresses in said memory can be read out to said output in burst mode such that the memory receives an address of one of said locations and provides in response contents of a plurality of memory locations, including the locations L1 and L2, in the sequence of consecutive addresses, so that while one of said row decoders is activating a row portion comprising said location L1 and contents of said location L1 are being transferred from one	This element is met by the '596 Reference alone or in combination with the '196 Reference or U.S. Patent No. 5,036,494 ("the '494 Reference"). Specifically, the '596 Reference states: "In other words, according to the "+1" function, when nth block 10_n is selected and enabled, the word line having the larger address by "1" then the address of nth block 10_n in first block

or more of said sense amplifiers to said output, another one of said row decoders is activating a row portion comprising said location L2 and contents of said location L2 are being transferred from said location L2 to one or more of said sense amplifiers.	10_1 is raised." ['596 Reference, Col. 3:17-20] *See also*, Col. 2:55-5:12; Claims 1, 2, 3 and 5. The '196 Reference states that: "In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit lines in the other array are being precharged. Thus, as data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit lines in that array will already have been initialied." ['196 Reference, Col. 2:60-67] "In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and settling transient signals) in preparation for the next access form such other array. Therefore, precharging times for one array overlap the time for performing read or write operation in the other array, and therefore do not limit operating speed." ['196 Reference, Col. 3:41-47] The '494 Reference states: "The selection of memory locations forming each cyclic pattern of addressing is controlled by the control unit 13. The row counter 45 and column counter 44 are connected so that unless instructed by the control 13 to do otherwise they count through successive addresses along each row and then row by row." ['494 Reference, Col. 8:22-27] "Consequently after reaching address 0 the column and row

	counters cycle sequentially along each row for the two memory blocks in turn (starting at column zero of row 0 in array 0) using all memory locations in each row and then moving to the next row and repeating the operation." ['494 Reference, Col. 11:26-31]
2. The memory of claim 1, said memory having a random mode in which the memory receives an address and provides in response the contents of a unique memory location,	It was well-known in the art to retain a random mode while adding the functionality of a sequential read operation. The following are illustrative: EP 9 326 885 A2 ("the '885 Reference") states: "The circuit provides both random and sequential access functions and allows the memory to be used as a shift register of variable length." ['885 Reference, Page 1] U.S. Patent No. 5, 263,003 ("the '003 Reference") states: "In a first mode, the memory circuit responds to an initial request for access and an address signal by reading data from a storage location in one of the memory banks. Subsequent requests for access to continguous storage locations do no require an address signal, instead a control mechanism responds by generating an address to read data alternately from storage locations in the first and second memory banks. In a second mode, the memory circuit responds to every request for access to the memory circuit by enabling access to the first or second memory bank as indicated by an address which accompanied the request." ['003 Reference, Abstract]
wherein, both in burst mode and in random mode, while the	It would be obvious to a person of skill in the art that

contents of said location L1 are being transferred from one or more of said sense amplifiers to said output, the contents of said location L2 are being transferred from said location L2 to one or more of said sense amplifiers.	transferring the contents of a location L1 from one of the sense amplifiers to the output while the contents of a location L2 are transferred from the location L2 to one or more sense amplifiers could be used in either a burst mode or a random mode. *See* claim 1 above. Further, to the extent AMD reads this limitation on the Samsung devices, this limitation is met by numberous prior art references having both a random access mode and a burst mode.
3. The memory of claim 1 wherein when the locations L1 and L2 are read out in burst mode and when the contents of said location L1 are being transferred from one or more of said sense amplifiers to said output and the contents of said location L2 are being transferred from said location L2 to one or more of said sense amplifiers, the sense amplifiers from which the contents of said location L1 are being transferred are enabled and the sense amplifiers to which the contents of said location L2 are being transferred are disabled, but these latter sense amplifiers become enabled subsequently for amplifying the contents of said location L2.	This limitation is met by the '596 Reference alone or in combination with any of EP 0 087 754 B1 ("the '754 Reference") or U.S. Patent No. 4,937,788 ("the '788 Reference") or the '937 Reference or the '003 Reference or U.S. Patent No. 5,251,178 ("the '178 Reference"). The '596 Reference states: "Memory blocks 10_1, 10_2, ..., 10_n include row decoders 12_1, 12_2, ...,12_n, sense amplifiers 14_1, 14_2, ..., 14_n and column decoders 16_1, 16_2, ..., 16_n,respectively. Each of memory blocks 10_1, 10_2, ..., 10_n is enabled by corresponding one of block decoders 20_1, 20_2, ..., 20_n on the basis of lower row address 18. Remaining upper row address 22 is input to row decoders 12_1, 12_2, ..., 12_n, and a word line is selected by upper row address 22." ['596 Reference, Col. 2:62-Col. 3:2] "At the leading edge of a timing pulse, sense amplifiers 14_1, 14_2, and 14_n in the above three blocks are simultaneously enabled." ['596 Reference, Col. 4:39-42] *See also* Claims 1 and 7.

	The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-2 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58] The '788 Reference states: "According to this arrangement, only one plane is selected in accordance with the content of the upper-order two bits of the row address. The selected plane is activated and exhibits the memory operation but the rest of the planes which are under the non-selection state are inoperative. Therefore, the decoders and the sense amplifiers are inoperative in these inoperative planes and the memory is not refreshed. Therefore, power is consumed in only the selected plane and unnecessary power consumption in the other plane can be saved. Thurs, the requirement for low power consumption can be satisfied." ['788 Reference, Col. 5:57-68]

	The '937 Reference states: "The sense amplifier 86 is controlled by the signals SE_{EV} to smplify the read data thereby to supply the same to the data latch 87, which in turn temporarily stores the outputs from the sense amplifiers 86. When the signals SE_{EV} are at low levels, the data latch 87 is electically cut off from the sense amplifier 86. Data from the data latch 87 are transferred to the output latch 89 when the signals OE_{EV} are at high levels. In a similar manner, the sense amplifier 96 is controlled by the signals SEOD to amplify the read data thereby to supply the same to the data latch 97, which in turn temporarily stores the outputs from the sense amplifier 96. When the signals SE_{OD} are at low levels, the data latch 97 is electrically cut off from the sense amplifier 96." ['937 Reference, Col. 4:52-66] The '003 Reference states: "The flash memory control 99 also selectively enables one of tow sets of bi-directional data buffers 90 and 91 which respectively couple th bank data buses 82 and 83 to the processor section data bus 63. The bank data buses 81 and 83 can be coupled to the instruction bus 61 by the flash memory control 88 selectively enabling buffers 92 and 93, respectively." ['003 Reference, Col. 9:21-27] The '178 Reference states: "Referring now to FIG. 2, the circuit of FIG 1 has been modified to utilize the fact that, when RA10=1, only one half of the ARRAY BANKs 20 are being utilized and that, when RA10=0, the other half of the ARRAY BANKs 20 are being utilized. In

	particular, the RA 10 address is used to cause only the half of the ARRAY BANKs 20 that are being utilized to draw power from the DRAM energy source during read/write operations, while at the same time permitting the periodic performance of the refresh cycle in the usual manner on all ARRAY BANKs." ['178 Reference, Col. 3:32-42]
4. The memory of claim 1 wherein:	
said memory comprises k pluralities S-1, . . . , S-k of locations wherein k is a number of said pluralities and is greater than or equal to two; for each plurality S-i, said sense amplifiers can receive simultaneously the contents of number m of locations from said plurality S-i, wherein m is a positive integer; and	This limitation is met by the '596 Reference. Specifically, the '596 Reference states: "In such a dRAM according to the embodiment, memory cell arrays of n memory blocks 10_1, 10_2, ..., 10_n selected by corresponding lower row address data, e.g., a lower row address consisting of the LSB to mth bit are divided in a bit line direction. Word lines selected by row addresses adjacent on the logical address plane are distributed to different memory blocks (memory cell array blocks). Memory blocks 10_1, 10_2, ..., 10_n include row decoders 12_1, 12_2, ...,12_n, sense amplifiers 14_1, 14_2, ..., 14_n and column decoders 16_1, 16_2, ..., 16_n,respectively." ['596 Reference, Col. 2:55-65] "At this time, all the memory cells connected to three word lines including two adjacent rows on the logical address plane can be immediately accessed. More specifically, the sense amplifiers are enabled and all the memory cells can be read out and written at any time." ['596 Reference, Col. 4:53-57]
time tARA does not exceed m * (k-1) * (tOE), wherein: tARA is measured from the time that an address of a location is made available to said memory to the time when one or more of	A person of skill in the art would know that this timing relationship would be used when designing the memory disclosed in claim 1.

said sense amplifiers develop an output signal indicative of the contents of said location; and tOE is the time to transfer an output of any one of said sense amplifiers to said output of said memory.	
5. The memory of claim 1	
wherein, in burst mode, a time in which each location of said plurality except said one of said locations is read out to said output after a previous location has been read out to said output is shorter than a time in which said one of said locations is read out to said output after said address of said one of said locations has been received by said memory.	This element is met for the '596 Reference alone or in combination with the '738 Reference or U.S Patent No. 4,918,587 ("the '587 Reference") or U.S. Patent No. the '003 Reference or U.S. Patent No. 4,799,199 ("the '199 Reference"). Specifically, see Figure 3 of the '596 Reference. The '738 Reference states: "In the sequential mode, the decoders of the memory are used in a conventional manner for decoding the address of the first cell to be accessed in a predetermined sequence of cells and thereafter, the shift registers are used for addressing the remaining cells in the sequence." ['738 Reference, Col. 1:56-61] The '587 Reference states: "The reduction in the memory access cycle time from a conventional memory access operation, generally represented by the first prefetch with a three clock cycle span between event t1 and t2, is clearly evident when the times are compared to those of the consecutive prefetch operation extending for two clock cycles between corresponding time intervals t3 and t4. Time t2 and t4 identify the first clock interval suitable to initiate succeeding memory access operations." ['587 Reference, Col.

	5:63-6:3] U.S. Patent No. 5,263,003 ("the '003 Reference") states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer. Typically, the access

	addresses of the 'extra' storage cells differ from the original access address by only one or two bits. However, subsequent accesses to these cells can be accomplished by simply executing additional access cycles without changing the access address. In the art, such memories are referre to as 'nibble mode'. In some other integrated circuit memories, a portion of the original address can be 'assumed' from one (or more)subsequent accesses, so that only the least significant porition of the address needs to be decoded, etc. Thus, once the original access had been completed, subsequent accesses to 'related' storage cells will be significantly quicker." ['199 Reference, Col. 1:13-28]
6. The memory of claim 1 wherein said memory is fabricated in an integrated circuit.	This element is met by the '596 Reference alone or in combination with any of the '754 Reference or the '199 Reference or U.S. Patent No. 4,899,312 ("the '312 Reference"). Specifically, the '596 Reference is titled "Dynamic Semiconductor Memory Device Having Simultaneous Operation of Adjacent Blocks." The '754 Reference states: "The present invention relates to a semiconductor dynamic memory device. Mass production of 64K bit dynamic type random access memory devices (DRAMs) has been enabled by the recent development of semiconductor memory devices of high packing density. Furthermore, a 256K bit DRAM has been developed." ['754 Reference, Page 2:1-4] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents

	thereof are held temporarily in a buffer." ['199 Reference, Col. 1:13-16] The '312 Reference states: "The individual circuit elements constructing the RAM of the present embodiment are formed on a semiconductor substrate such as a piece of single-crystalline silicon by the known technique for fabricating a CMOS (i.e. Complementary MOS) integreated circuit." ['312 Reference, Col. 2:34-38]
7. The memory of claim 1 further comprising:	
a plurality of second registers, each second register for receiving at least a portion of a column address; and	This limitation is met by the '596 Reference alone or in combination with the '196 Reference or the '937 Reference. Specifically, the '596 Reference states: "Similarly, column address 38 is given as follows. Column address buffer 40 receives an address signal input from the external terminal as an initial value. The initial value is counted up or down by column address counter 42 in response to a serial access control signal input from control circuit 36. Therefore, column address 38 is given." ['596 Reference, Col. 3:41-47] "In addition, a shift register is arranged in the column direction, so that higher-speed serial access can be performed in the column direction." ['596 Reference, Col. 6:15-17] *See also* '596 Reference, Col. 2:55-5:12; Claims 1, 4 and 5. To the extent AMD reads this limitation on the Samsung

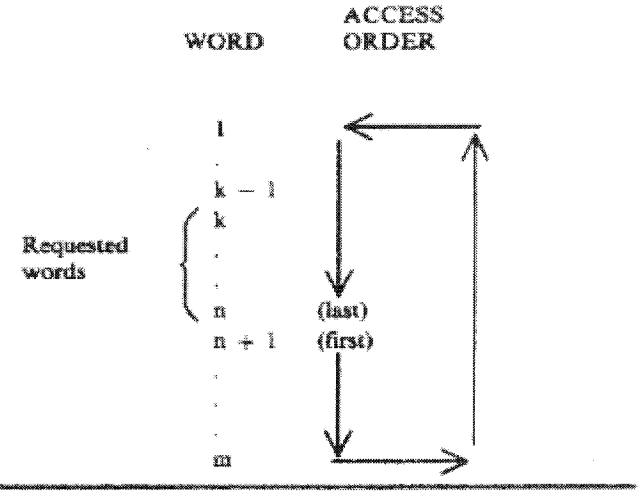
	Devices, this limitation is met by the '596 Reference. The '196 Reference states that: "The row and column location in the arrays 31, 33 at which data is accessed is controlled by the counters which, in one embodiment of the invention may be binary counters, or the like, which have an extended counting range that is double the number of address locations in the array to be accessed." ['196 Reference, Col. 4:49-55; See also, FIGS. 2A, 2B] The '937 Reference states that: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e. twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. Ina similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e. twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42]
a circuitry for each second register for selecting in response to signals from one of the second registers a plurality of columns to be read by the sense amplifiers.	Output 38 from column address counter 42 is transferred to column decoders 16_1, 16_2, ..., 16_n through a column address bus to select the columns. The read out data is latched by I/O buffer 44. Then, only the data of block 10_1 is output to output terminal

	D_{OUT}." " ['596 Reference, Col. 4:47-52] "At this time, all the memory cells connected to three word lines including two adjacent rows on the logical address plane can be immediately accessed. More specifically, the sense amplifiers are enabled and all the memory cells can be read out and written at any time." ['596 Reference, Col. 4:53-57]
8. A memory comprising:	Although a preamble is normally not limiting, should this preamble be limiting, this element is met by the '596 Reference. Specifically, the '596 Reference is titled "Dynamic Semiconductor Memory Device Having Simultaneous Operation of Adjacent Blocks."
a set of consecutively addressed memory locations L1, . . . Ln;	This limitation is met by the '596 Reference. Specifically, the '596 Reference states: "FIG. 2 shows a circuit arrangement of block decoder 20_1 when lower row address 18 is a 3-bit (m=3) address. When lower row address 18 is (0,0,0), the first block is selected. AND gates 52' and 54 detect cases wherein lower row address 18 represents the selected address of the block, the address which is larger than the selected address by "1", and the address which is smaller than the selected address by "1". More specifically, AND gates 52 and 54 detect that addresses (A_{2R}, A_{1R}, A_{0R}) represent (0,0,0), (0,0,1), and (1,1,1). After a block enable signal is output and an output of OR gate 58 is set at "H" level, AND gates 50 and 56 keep enabling the output of OR gate 58 at "H" level during a difference between the data of lower row address 18 and the selected address of the block is less than $\|\pm 3\|$. In other words, even if lower addresses (A_{2R}, A_{1R}, A_{0R}) represent (0,1,0), (1,1,0), (0,0,1), or (1,1,1), the output from OR gate 58 is kept at "H"

	level. By keeping "H" level as described above, even if the memory cell is selected in the reverse direction, the reset time can be sufficiently assured. A forward direction is a direction in which a counter is incremented." ['596 Reference, Col. 3:65-4:18]
a plurality of sense amplifier circuits for amplifying contents of said memory locations; and	This element is met by the '596 Reference. Specifically, the '596 Reference states: "Memory blocks 10_1, 10_2, ..., 10_n include row decoders 12_1, 12_2, ...,12_n, sense amplifiers 14_1, 14_2, ..., 14_n and column decoders 16_1, 16_2, ..., 16_n, respectively." ['596 Reference, Col. 2:62-65]
an output for providing output signals from said plurality of sense amplifier circuits,	This element is met by the '596 Reference. Specifically, the '596 Reference states: "Output 38 from column address counter 42 is transferred to column decoders 16_1, 16_2, ..., 16_n, through a column address bus to select the columns. The readout data is latched by I/O buffer 44. Then, only the data of block 10_1 is output to output terminal D_{OUT}." ['596 Reference, Col. 4:47-52]
wherein said memory has a burst mode operation for receiving an address and reading out to said output, in response to said address, any given number of memory locations in the sequence of consecutive addresses with wrap around so that the next location, if any, to be read out after said location Ln is said location L1, such that during said operation while the contents of any location L to be read out other than the last location to be read out are being transferred from said plurality of sense amplifier circuits to said output, the contents of another location to be read out after said location L are being provided to said plurality of sense amplifier	This element is met by the '596 Reference in combination with the '196 Reference or the '885 Reference or U.S. Patent No. 4,912,631 ("the '631 Reference"). Specifically, the '596 Reference states: "In other words, according to the "+1" function, when nth block 10_n is selected and enabled, the word line having the larger address by "1" then the address of nth block 10_n in first block 10_1 is raised." ['596 Reference, Col. 3:17-20]

circuits for amplification and subsequent transfer to said output, and	*See also*, Col. 2:55-5:12; Claims 1, 2, 3 and 5. The '196 Reference states that: "In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit lines in the other array are being precharged. Thus, as data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit lines in that array will already have been initialied." ['196 Reference, Col. 2:60-67] "In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and settling transient signals) in preparation for the next access form such other array. Therefore, precharging times for one array overlap the time for performing read or write operation in the other array, and therefore do not limit operating speed." ['196 Reference, Col. 3:41-47] The '885 Reference states: "After the last memory address is reached, the access automatically rolls over to the first address." ['885 Reference, page 1; Col. 3:1-3] "A method as in claim 5 wherein the sequence of incremented addresses wraps around when the address of the Nth register is reached such that all N registers in the array are read." ['885 Reference, Col. 7:45-48] The '631 Reference states that:

	"The above-described method is accomplished by utilizing two pieces of information, which are placed on the bus (23) by the GDP: the data word's offset and the number of words requested. The data word's offset in the cache line is derived from adress bits 2 and 3 (00=word 1, 01=word 2, 10=word 3, and 11=word 4). The number of words being requested is obtained from the size bits 0 and 1 (00=1word, 01=2 words, 10=3 words, and 11=4words). Using these two pieces of information, the following algorithm is executed: FIRST WORD ACCESSED = PROCESSOR WORD ADDRESS + SIZE +1 The 1 is added to the size in order to yield the correct offset. For example, if the GDP requests two words at offset 01 in a four-word line, it is convereted to a wraparound request of four words to memory starting at word four [offset (01) + word count (01) + 1 = 11]." ['631 Reference, Col. 3:46-65] See, '631 Reference, Table II:

	TABLE II  See also, '631 Reference, Abstract, Table I, Fig. 3. Further, the '596 Refence could be combined with the admitted prior art shown in Fig. 2 of the '990 patent to form a memory that closely resembles the preferred embodiments of the '990 patent.
wherein said memory further comprises a control circuit for selectively enabling said sense amplifier circuits so that said control circuit enables a sense amplifier circuit whose output signals are being transferred to the output of said memory but said control circuit does not enable all said sense amplifier circuits at the same time.	This limitation is met by the '596 Reference alone or in combination with any of the '754 Reference or the '788 Reference or the '937 Reference or the '003 Reference or the '178 Reference. The '596 Reference states: "Memory blocks 10_1, 10_2, ..., 10_n include row decoders 12_1, 12_2,

	...,12_n, sense amplifiers 14_1, 14_2, ..., 14_n and column decoders 16_1, 16_2, ..., 16_n, respectively. Each of memory blocks 10_1, 10_2, ..., 10_n is enabled by corresponding one of block decoders 20_1, 20_2, ..., 20_n on the basis of lower row address 18. Remaining upper row address 22 is input to row decoders 12_1, 12_2, ..., 12_n, and a word line is selected by upper row address 22." ['596 Reference, Col. 2:62-Col. 3:2] "At the leading edge of a timing pulse, sense amplifiers 14_1, 14_2, and 14_n in the above three blocks are simultaneously enabled." ['596 Reference, Col. 4:39-42] *See also* Claims 1 and 7. The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-2 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58]

	The '788 Reference states: "According to this arrangement, only one plane is selected in accordance with the content of the upper-order two bits of the row address. The selected plane is activated and exhibits the memory operation but the rest of the planes which are under the non-selection state are inoperative. Therefore, the decoders and the sense amplifiers are inoperative in these inoperative planes and the memory is not refreshed. Therefore, power is consumed in only the selected plane and unnecessary power consumption in the other plane can be saved. Thurs, the requirement for low power consumption can be satisfied." ['788 Reference, 5:57-68] The '937 Reference states: "The sense amplifier 86 is controlled by the signals SE_{EV} to smplify the read data thereby to supply the same to the data latch 87, which in turn temporarily stores the outputs from the sense amplifiers 86. When the signals SE_{EV} are at low levels, the data latch 87 is electically cut off from the sense amplifier 86. Data from the data latch 87 are transferred to the output latch 89 when the signals OE_{EV} are at high levels. In a similar manner, the sense amplifier 96 is controlled by the signals SEOD to amplify the read data thereby to supply the same to the data latch 97, which in turn temporarily stores the outputs from the sense amplifier 96. When the signals SE_{OD} are at low levels, the data latch 97 is electrically cut off from the sense amplifier 96." ['937 Reference, 4:52-66] The '003 Reference states: "The flash memory control 99 also selectively enables one of

	two sets of bi-directional data buffers 90 and 91 which respectively couple th bank data buses 82 and 83 to the processor section data bus 63. The bank data buses 81 and 83 can be coupled to the instruction bus 61 by the flash memory control 88 selectively enabling buffers 92 and 93, respectively." ['003 Refrence, 9:21-27] The '178 Reference states: "Referring now to FIG. 2, the circuit of FIG 1 has been modified to utilize the fact that, when RA10=1, only one half of the ARRAY BANKs 20 are being utilized and that, when RA10=0, the other half of the ARRAY BANKs 20 are being utilized. In particular, the RA 10 address is used to cause only the half of the ARRAY BANKs 20 that are being utilized to draw power from the DRAM energy source during read/write operations, while at the same time permitting the periodic performance of the refresh cycle in the usual manner on all ARRAY BANKs." ['178 Reference, 3:32-42]
9. The memory of claim 8 wherein, during said operation, said control circuit enables at the same time only:	
(1) the sense amplifier circuit whose output signals are being transferred to said output of said memory, and	This limitation is met by the '596 Reference alone or in combination with the '754 Reference. Specifically, the '596 Reference states: "When input lower row address 18 represents (0,0,…,0), i.e., the address of first block 10_1, blocks 10_1, 10_2, and 10_n are simultaneously enabled by corresponding block decoders 20_1, 20_2, and 20_n. Therefore, the word lines in these three blocks which are selected by upper row address 22 are enabled. In this

	case, as described above, operation circuit 26 in block 10_n is operated as a subtractor. The word line selected by the address obtained by subtracting "1" from a value represented by upper row address 22 is enabled. At the leading edge of a timing pulse, sense amplifiers 14_1, 14_2, and 14_n in the above three blocks are simultaneously enabled." ['596 Reference, Col. 4:30-42] The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-2 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58] "A semiconductor dynamic memory device comprising: ... a plurality of sense amplifying means (18-1 to 18-2; SA1 to SA8) responsive to a control signal input thereto, for selectively activating one sense amplifying means to sense and amplify data on said selected data lines of one of said two column-selected memory blocks, and for selectively activating at least one other

	sense amplifying means to refresh data to said each memory cell along said selected word lines; ...." ['754 Reference, Page 6:53-Page 7:5]
(2) a predetermined number of other sense amplifier circuits whose output signals will be transferred next to said output of said memory if said operation continues sufficiently long.	This limitation is met by the '596 Reference alone or in combination with the '754 Reference. Specifically, the '596 Reference states: "When input lower row address 18 represents (0,0,...,0), i.e., the address of first block 10_1, blocks 10_1, 10_2, and 10_n are simultaneously enabled by corresponding block decoders 20_1, 20_2, and 20_n. Therefore, the word lines in these three blocks which are selected by upper row address 22 are enabled. In this case, as described above, operation circuit 26 in block 10_n is operated as a subtractor. The word line selected by the address obtained by subtracting "1" from a value represented by upper row address 22 is enabled. At the leading edge of a timing pulse, sense amplifiers 14_1, 14_2, and 14_n in the above three blocks are simultaneously enabled." ['596 Reference, Col. 4:30-42] The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly

	reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-2 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58] "A semiconductor dynamic memory device comprising: ... a plurality of sense amplifying means (18-1 to 18-2; SA1 to SA8) responsive to a control signal input thereto, for selectively activating one sense amplifying means to sense and amplify data on said selected data lines of one of said two column-selected memory blocks, and for selectively activating at least one other sense amplifying means to refresh data to said each memory cell along said selected word lines; ...." ['754 Reference, Page 6:53-Page 7:5]
10. The memory of claim 7 wherein:	
said set of locations comprises k subsets S-1, . . . , S-k wherein k is greater than or equal to two, such that, for a positive integer m and for any subset S-i, the contents of m consecutively addressed locations from said subset S-i can be transferred simultaneously to said plurality of sense amplifier circuits; and	This limitation is met by the '596 Reference. Specifically, the '596 Reference states: "In such a dRAM according to the embodiment, memory cell arrays of n memory blocks 10_1, 10_2, ..., 10_n selected by corresponding lower row address data, e.g., a lower row address consisting of the LSB to mth bit are divided in a bit line direction. Word lines selected by row addresses adjacent on the logical address plane are distributed to different memory blocks (memory cell array blocks). Memory blocks 10_1, 10_2, ..., 10_n include row decoders 12_1, 12_2, ...,12_n, sense amplifiers 14_1, 14_2, ..., 14_n and column decoders 16_1, 16_2, ..., 16_n,respectively."

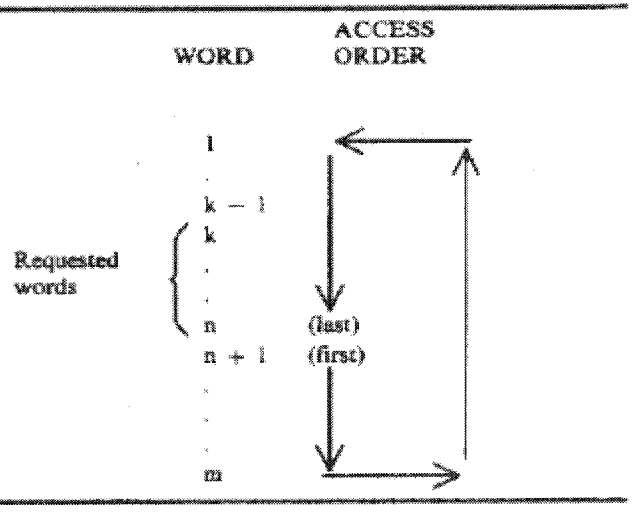
	['596 Reference, Col. 2:55-65] "At this time, all the memory cells connected to three word lines including two adjacent rows on the logical address plane can be immediately accessed. More specifically, the sense amplifiers are enabled and all the memory cells can be read out and written at any time." ['596 Reference, Col. 4:53-57]
in said operation, time tARA does not exceed m * (k-1) * (tOE), wherein: tARA is measured from the time that an address of the first location to be read out in said operation is made available to said memory to the time when said plurality of sense amplifier circuits develops an output signal indicative of the contents of said first location; and tOE is the time to transfer the contents of any one of said locations from said plurality of sense amplifier circuits to said output.	A person of skill in the art would know that this timing relationship would be used when designing the memory disclosed in claim 1.
11. The memory of claim 8 wherein, in said operation, each location to be read out except the first location to be read out is read out to said output in a shorter time than the first location to be read out.	This element is met for the '596 Reference alone or in combination with the '738 Reference or the '587 Reference or the '003 Reference or the '199 Reference. Specifically, see Figure 3 of the '596 Reference. The '738 Reference states: "In the sequential mode, the decoders of the memory are used in a conventional manner for decoding the address of the first cell to be accessed in a predetermined sequence of cells and thereafter, the shift registers are used for addressing the remaining cells in the sequence." ['738 Reference, Col. 1:56-

	61] The '587 Reference states: "The reduction in the memory access cycle time from a conventional memory access operation, generally represented by the first prefetch with a three clock cycle span between event t1 and t2, is clearly evident when the times are compared to those of the consecutive prefetch operation extending for two clock cycles between corresponding time intervals t3 and t4. Time t2 and t4 identify the first clock interval suitable to initiate succeeding memory access operations." ['587 Reference, Col. 5:63-6:3] The '003 Reference states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two

	memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer. Typically, the access addresses of the 'extra' storage cells differ from the original access address by only one or two bits. However, subsequent accesses to these cells can be accomplished by simply executing additional access cycles without changing the access address. In the art, such memories are referre to as 'nibble mode'. In some other integrated circuit memories, a portion of the original address can be 'assumed' from one (or more)subsequent accesses, so that only the least significant porition of the address needs to be decoded, etc. Thus, once the original access had been completed, subsequent accesses to 'related' storage cells will be significantly quicker." ['199 Reference, Col. 1:13-28]
12. The memory of claim 8 wherein the sequence of locations L1, . . . , Ln is a sequence of increasing order of addresses.	This limitation is met by the '596 Reference. Specifically, the '596 Reference states: "FIG. 2 shows a circuit arrangement of block decoder 20_1 when lower row address 18 is a 3-bit (m=3) address. When lower row address 18 is (0,0,0), the first block is selected. AND gates 52' and 54 detect cases wherein lower row address 18 represents the selected address of the block, the address which is larger than

	the selected address by "1", and the address which is smaller than the selected address by "1". More specifically, AND gates 52 and 54 detect that addresses (A_{2R}, A_{1R}, A_{0R}) represent (0,0,0), (0,0,1), and (1,1,1). After a block enable signal is output and an output of OR gate 58 is set at "H" level, AND gates 50 and 56 keep enabling the output of OR gate 58 at "H" level during a difference between the data of lower row address 18 and the selected address of the block is less than $\|\pm 3\|$. In other words, even if lower addresses (A_{2R}, A_{1R}, A_{0R}) represent (0,1,0), (1,1,0), (0,0,1), or (1,1,1), the output from OR gate 58 is kept at "H" level. By keeping "H" level as described above, even if the memory cell is selected in the reverse direction, the reset time can be sufficiently assured. A forward direction is a direction in which a counter is incremented." ['596 Reference, Col. 3:65-4:18]
13. The memory of claim 7 wherein in said operation any number of said locations addressed consecutively with wrap around can be read out to said output so that:	This element is met by the '596 Reference in combination with the '885 Reference or the '631 Reference. Specifically, the '596 Reference states: "In other words, according to the "+1" function, when nth block 10_n is selected and enabled, the word line having the larger address by "1" then the address of nth block 10_n in first block 10_1 is raised." ['596 Reference, Col. 3:17-20] *See also*, Col. 2:55-5:12; Claims 1, 2, 3 and 5. The '885 Reference states: "After the last memory address is reached, the access automatically rolls over to the first address." ['885 Reference,

	page 1; Col. 3:1-3] "A method as in claim 5 wherein the sequence of incremented addresses wraps around when the address of the Nth register is reached such that all N registers in the array are read." ['885 Reference, Col. 7:45-48] The '631 Reference states that: "The above-described method is accomplished by utilizing two pieces of information, which are placed on the bus (23) by the GDP: the data word's offset and the number of words requested. The data word's offset in the cache line is derived from adress bits 2 and 3 (00=word 1, 01=word 2, 10=word 3, and 11=word 4). The number of words being requested is obtained from the size bits 0 and 1 (00=1word, 01=2 words, 10=3 words, and 11=4words). Using these two pieces of information, the following algorithm is executed: FIRST WORD ACCESSED = PROCESSOR WORD ADDRESS + SIZE +1 The 1 is added to the size in order to yield the correct offset. For example, if the GDP requests two words at offset 01 in a four-word line, it is convereted to a wraparound request of four words to memory starting at word four [offset (01) + word count (01) + 1 = 11]." ['631 Reference, Col. 3:46-65] See, '631 Reference, Table II:

	TABLE II  See also, '631 Reference, Abstract, Table I, Fig. 3.
the first location to be read out in said operation is read out to said output after time tARA+tOE wherein: tARA is measured from the time that an address of said first location is made available to said memory to the time when said plurality of sense amplifier circuits develops an output signal indicative of the contents of said first location; and tOE is the time to transfer the contents of any one of said locations from said plurality of sense amplifier circuits to said output of said memory; and	This element is met by the '596 Reference in combination with any of the '587 Reference or the '003 Reference or the '199 Reference. The '587 Reference states: "The reduction in the memory access cycle time from a convention memory access operation, generally represented by the first prefetch with a three clock cycle span between event t1 and t2, is clearly evident when the times are compared to those of the consecutive prefetch operation extending for two clock cycles between corresponding time intervals t3 and t4. Time t2 and t4 identify the first clock interval suitable to initiate

	succeeding memory access operations." ['587 Reference, Col. 5:63-6:3] The '003 Reference states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents

	thereof are held temporarily in a buffer. Typically, the access addresses of the 'extra' storage cells differ from the original access address by only one or two bits. However, subsequent accesses to these cells can be accomplished by simply executing additional access cycles without changing the access address. In the art, such memories are referred to as 'nibble mode'. In some other integrated circuit memories, a portion of the original address can be 'assumed' for one (or more) subsequent accesses, so that only the least significant portion of the address needs to be decoded, etc. Thus, once the original access had been completed, subsequent accesses to 'related' storage cells will be significantly quicker." ['199 Reference, Col. 1:13-28]
every other location to be read out in said operation is read out to said output within time tOE.	This element is met by the '596 Reference in combination with any of the '587 Reference or the '003 Reference or the '199 Reference. The '587 Reference states: "The reduction in the memory access cycle time from a convention memory access operation, generally represented by the first prefetch with a three clock cycle span between event t1 and t2, is clearly evident when the times are compared to those of the consecutive prefetch operation extending for two clock cycles between corresponding time intervals t3 and t4. Time t2 and t4 identify the first clock interval suitable to initiate succeeding memory access operations." ['587 Reference, Col. 5:63-6:3] The '003 Reference states: "The consecutive program instructions are read alternately from

	the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer. Typically, the access addresses of the 'extra' storage cells differ from the original access address by only one or two bits. However, subsequent accesses to these cells can be accomplished by simply executing additional access cycles without changing the access address. In

	the art, such memories are referred to as 'nibble mode'. In some other integrated circuit memories, a portion of the original address can be 'assumed' for one (or more) subsequent accesses, so that only the least significant portion of the address needs to be decoded, etc. Thus, once the original access had been completed, subsequent accesses to 'related' storage cells will be significantly quicker." ['199 Reference, Col. 1:13-28]
14. The memory of claim 8 wherein said memory is fabricated in an integrated circuit.	This element is met by the '596 Reference alone or in combination with any of the '754 Reference or the '199 Reference or the '312 Reference. Specifically, the '596 Reference is titled "Dynamic Semiconductor Memory Device Having Simultaneous Operation of Adjacent Blocks." The '754 Reference states: "The present invention relates to a semiconductor dynamic memory device. Mass production of 64K bit dynamic type random access memory devices (DRAMs) has been enabled by the recent development of semiconductor memory devices of high packing density. Furthermore, a 256K bit DRAM has been developed." ['754 Reference, Page 2:1-4] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer." ['199 Reference, Col. 1:13-16] The '312 Reference states:

	"The individual circuit elements constructing the RAM of the present embodiment are formed on a semiconductor substrate such as a piece of single-crystalline silicon by the known technique for fabricating a CMOS (i.e. Complementary MOS) integreated circuit." ['312 Reference, Col. 2:34-38]
20. An integrated memory comprising:	Although a preamble is normally not limiting, should this preamble be limiting, this element is met by the '596 Reference. Specifically, the '596 Reference is titled "Dynamic Semiconductor Memory Device Having Simultaneous Operation of Adjacent Blocks."
an array of memory locations, the array comprising a plurality of subarrays, each subarray comprising a predetermined number of groups of columns of the memory locations such that for any given column position in a group, the memory locations in any given row in the columns at said given position in the groups of the subarray have consecutive addresses;	This limitation is met by the '596 Reference. Specifically, the '596 Reference states: "In such a dRAM according to the embodiment, memory cell arrays of n memory blocks 10_1, 10_2, ..., 10_n selected by corresponding lower row address data, e.g., a lower row address consisting of the LSB to mth bit are divided in a bit line direction. Word lines selected by row addresses adjacent on the logical address plane are distributed to different memory blocks (memory cell array blocks). Memory blocks 10_1, 10_2, ..., 10_n include row decoders 12_1, 12_2, ...,12_n, sense amplifiers 14_1, 14_2, ..., 14_n and column decoders 16_1, 16_2, ..., 16_n,respectively." ['596 Reference, Col. 2:55-65] "FIG. 2 shows a circuit arrangement of block decoder 20_1 when lower row address 18 is a 3-bit (m=3) address. When lower row address 18 is (0,0,0), the first block is selected. AND gates 52' and 54 detect cases wherein lower row address 18 represents the selected address of the block, the address which is larger than the selected address by "1", and the address which is smaller

	than the selected address by "1". More specifically, AND gates 52 and 54 detect that addresses (A_{2R}, A_{1R}, A_{0R}) represent (0,0,0), (0,0,1), and (1,1,1). After a block enable signal is output and an output of OR gate 58 is set at "H" level, AND gates 50 and 56 keep enabling the output of OR gate 58 at "H" level during a difference between the data of lower row address 18 and the selected address of the block is less than $\|\pm 3\|$. In other words, even if lower addresses (A_{2R}, A_{1R}, A_{0R}) represent (0,1,0), (1,1,0), (0,0,1), or (1,1,1), the output from OR gate 58 is kept at "H" level. By keeping "H" level as described above, even if the memory cell is selected in the reverse direction, the reset time can be sufficiently assured. A forward direction is a direction in which a counter is incremented." ['596 Reference, Col. 3:65-4:18]
one X-decoder for each subarray;	This limitation is met by the '596 Reference. Specifically, the '596 Reference states: "Memory blocks 10_1, 10_2, ..., 10_n include row decoders 12_1, 12_2, ...,12_n, sense amplifiers 14_1, 14_2, ..., 14_n and column decoders 16_1, 16_2, ..., 16_n,respectively." ['596 Reference, Col. 2:62-65]
one X-register for each X-decoder;	This element is met by the '596 Reference alone or in combination with any of U.S. Patent No. 4,875,196 ("the '196 Reference") or U.S. Patent No. 4,849,937 ("the '937 Reference") or U.S. Patent No. 5,367,495 ("the '495 Reference") or U.S. Patent No. 4,759,021 ("the '021 Reference"). Specifically, the '596 Reference states: "Row address buffer 32 receives an address signal input from an external terminal as an initial value. The initial value is counted up or down by row address counter 34 in responseto a serial

	access control signal input from control circuit 36." ['596 Reference, Col. 3:33-37] To the extent AMD read this limitation on the Samsung devices, the '596 Reference meets this limitation. The '196 Reference states that: "The row and column location in the arrays 31, 33 at which data is accessed is controlled by the counters which, in one embodiment of the invention may be binary counters, or the like, which have an extended counting range that is double the number of address locations in the array to be accessed." ['196 Reference, Col. 4:49-54; See also, FIGS. 2A, 2B] The '937 Reference states: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e., twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e., twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42] The '495 Reference states:

	"The register 70a, 70b, 70c or 70d selected by the block decoder 50 holds 8-bit address codes ARC0-ARC7 supplied in synchronism with the row selection signal RAS. Since the holding of the address codes ARC0-ARC7 will be maintained even after access is shifted to another cell array block, these registers 70a-70d store respectively the address codes ARC0-ARC7 of the last access in the cell array blocks 10a-10d and supply them to the selectors 80a-80d which also receive the address codes ARC0-ARC7 supplied in synchronism with the row selection signal RAS and introduce them to the row decoders 20a-20d." ['495 Reference, Col. 4:25-37] The '021 Reference states: "Since the low-speed large-capacity memories 11, 12, 13, 14 performing the 4-way interleave operation are shifted in access timing usually by one cycle from each other, the memories 11-14 are provided respectively with registers 23-26 each for holding an address." ['021 Reference, Col. 4:5-9]
one Y-decoder for each subarray;	This limitation is met by the '596 Reference. Specifically, the '596 Reference states: "Memory blocks 10_1, 10_2, ..., 10_n include row decoders 12_1, 12_2, ...,12_n, sense amplifiers 14_1, 14_2, ..., 14_n and column decoders 16_1, 16_2, ..., 16_n,respectively." ['596 Reference, Col. 2:62-65]
one Y-register for each Y-decoder;	This limitation is met by the '596 Reference alone or in combination with the '196 Reference or the '937 Reference. Specifically, the '596 Reference states: "Similarly, column address 38 is given as follows. Column

	address buffer 40 receives an address signal input from the external terminal as an initial value. The initial value is counted up or down by column address counter 42 in response to a serial access control signal input from control circuit 36. Therefore, column address 38 is given." ['596 Reference, Col. 3:41-47] "In addition, a shift register is arranged in the column direction, so that higher-speed serial access can be performed in the column direction." ['596 Reference, Col. 6:15-17] *See also* '596 Reference, Col. 2:55-5:12; Claims 1, 4 and 5. To the extent AMD reads this limitation on the Samsung Devices, this limitation is met by the '596 Reference. The '196 Reference states that: "The row and column location in the arrays 31, 33 at which data is accessed is controlled by the counters which, in one embodiment of the invention may be binary counters, or the like, which have an extended counting range that is double the number of address locations in the array to be accessed." ['196 Reference, Col. 4:49-55; See also, FIGS. 2A, 2B] The '937 Reference states that: "The address counter 81 receives the signals $\emptyset_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $\emptyset_{EV}$ (i.e. twice that of the basic clock pulses $\emptyset_{S}$). Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. Ina similar

	manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e. twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42]
one Y-select circuit for each subarray, the Y-select circuit being responsive to the Y-decoder of the subarray to select all the columns that occupy a selected position in the groups of the subarray;	This element is met by the '596 Reference alone or in combination with the '937 Reference or the '754 Reference. Specifically, the '596 Reference states: "A column address is input at a trailing edge of [CAS bar] (column address strobe), and a complementary signal is generated by column address buffer 40. The complementary signal is transferred to column address counter 42 and latched. Output 38 from column address counter 42 is transferred to column decoders 16_1, 16_2, ..., 16_n, through a column address bus to select the columns. the readout data is latched by I/O buffer 44. Then, only the data of block 10_1 is output to output terminal D_{OUT}." ['596 Reference, Col. 4:43-52] "At this time, all the memory cells connected to three word lines including two adjacent rows on the logical address plane can be immediately accessed. More specifically, the sense amplifiers are enabled and all the memory cells can be read out and written at any time." ['596 Reference, Col. 4:53-57] The '937 Reference states: "The address counter 81 receives the signals $Ø_{EV}$ to supply even

	X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e. twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. Ina similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e. twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42] "Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to a transfer gate 85.... In a similar manner, the transfer gate 95 transfers data read from the second memory cell array 94 to the sense amplifier 96 through an I/O line 103, while transferring data from the write circuit 98 received through the I/O line 103 to the second memory cell array 94." ['937 Reference, Col. 4:33-52] The '754 Reference states: "Meanwhile, since the randomly selected bit signal RSBS of logic level '0' is supplied to the driver circuit 24, the MOS transistors TR65 and TR68 are turned OFF and the MOS transistors TR66 and 67 are turned ON. Under this condition, the MOS transistors Tr61 and TR63 are turned ON in responses to the timing signal TS3 from the control signal generator 28. The lower level signal [ØS bar] shown in Fig. 7D is supplied to the control lines Cl-1 and Cl-3 of the sense amplifier circuits 18-

	1 and 18-3, respectively. As a result, the sense amplifier circuits 18-1 and 18-3 are activated to discharge one of each pair of data lines of memories 12-1 and 12-3 connected to the sense amplifiers 18-1 and 18-3, respectively, thereby causing a discharging current to flow as shown in Fig. 7E." ['754 Reference, Page 5:33-40]
a plurality of sense amplifier circuits for each subarray, each sense amplifier circuit for amplifying signals from a column selected by the Y-select circuit of the subarray;	This element is met by the '596 Reference. Specifically, the '596 Reference states: "Memory blocks 10_1, 10_2, ..., 10_n include row decoders 12_1, 12_2, ...,12_n, sense amplifiers 14_1, 14_2, ..., 14_n and column decoders 16_1, 16_2, ..., 16_n, respectively." ['596 Reference, Col. 2:62-65]
a memory output; and	This element is met by the '596 Reference. Specifically, the '596 Reference states: "Output 38 from column address counter 42 is transferred to column decoders 16_1, 16_2, ..., 16_n, through a column address bus to select the columns. the readout data is latched by I/O buffer 44. Then, only the data of block 10_1 is output to output terminal D_{OUT}." ['596 Reference, Col. 4:47-52]
a control circuit for selecting one of the sense amplifier circuits to provide data to the memory output;	This limitation is met by the '596 Reference alone or in combination with the '754 Reference or admitted prior art disclosed in Figures 1 and 2 of the '990 patent The '596 Reference states: "Memory blocks 10_1, 10_2, ..., 10_n include row decoders 12_1, 12_2, ...,12_n, sense amplifiers 14_1, 14_2, ..., 14_n and column decoders 16_1, 16_2, ..., 16_n,respectively. Each of memory blocks 10_1, 10_2,

	..., 10_n is enabled by corresponding one of block decoders 20_1, 20_2, ..., 20_n on the basis of lower row address 18. Remaining upper row address 22 is input to row decoders 12_1, 12_2, ..., 12_n, and a word line is selected by upper row address 22." ['596 Reference, Col. 2:62-Col. 3:2] "At the leading edge of a timing pulse, sense amplifiers 14_1, 14_2, and 14_n in the above three blocks are simultaneously enabled." ['596 Reference, Col. 4:39-42] *See also* Claims 1 and 7. The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-2 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58] The '990 patent discloses prior art Figure 2 showing register select circuit 224 for selecting one of the sense amplifier circuits to provide data to the memory output. A person of skill in the

	art would know to use control circuit to select one of the sense amplifier circuits in an embodiment using a plurality of sense amplifier circuits.
wherein in a burst mode read operation, at least one X-register provides to its respective X-decoder signals identifying a row in one of the subarrays, and at least one Y-register provides to its respective Y-decoder signals identifying a position of columns in the groups of one of the subarrays.	This limitation is met by the '596 Reference. Specifically, the '596 Reference states: "A dynamic semiconductor device includes a plurality of dynamic memory cell arrays each having memory cells arranged in a matrix form, row decoders connected to the plurality of memory cell arrays, respectively, sense amplifiers connected to the plurality of memory cell arrays, respectively, a plurality of bit lines connected to the each of the plurality of memory cell arrays, for exchanging data with the memory cells arranged in the matrix form, the plurality of bit lines being connected to a corresponding one of the sense amplifiers, a plurality of word lines, intersecting the plurality of bit lines, for selecting the memory cells, the word lines selected by row addresses adjacent on a logical address plane being located in adjacent ones of the memory cell arrays, the word lines within the each memory cell array being selected by an upper row address of a row address output from a corresponding one of the row decoders, and means for selecting the memory cell arrays by a lower row address of the row address, the selecting means raising a plurality of given word lines selected by the addresses adjacent to a row address corresponding to any word line and enabling corresponding ones of the sense amplifiers of the memory cell arrays including the given word lines when the memory cells on the any word line are to be accessed." ['596 Reference, Abstract]

22. The memory of claim 20 wherein in the burst mode read operation while data from the sense amplifier circuits of one of the subarrays are provided to the memory output, the sense amplifier circuits of another one of the subarrays develop output signals corresponding to data in said other one of the subarrays.	This element is met by the '596 Reference alone or in combination with the '196 Reference or the '494 Reference. Specifically, the '596 Reference states: "In other words, according to the "+1" function, when nth block 10_n is selected and enabled, the word line having the larger address by "1" then the address of nth block 10_n in first block 10_1 is raised." ['596 Reference, Col. 3:17-20] *See also*, Col. 2:55-5:12; Claims 1, 2, 3 and 5. The '196 Reference states that: "In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit lines in the other array are being precharged. Thus, as data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit lines in that array will already have been initialied." ['196 Reference, Col. 2:60-67] "In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and settling transient signals) in preparation for the next access form such other array. Therefore, precharging times for one array overlap the time for performing read or write operation in the other array, and therefore do not limit operating speed." ['196 Reference, Col. 3:41-47] The '494 Reference states: "The selection of memory locations forming each cyclic pattern

	of addressing is controlled by the control unit 13. The row counter 45 and column counter 44 are connected so that unless instructed by the control 13 to do otherwise they count through successive addresses along each row and then row by row." ['494 Reference, Col. 8:22-27] "Consequently after reaching address 0 the column and row counters cycle sequentially along each row for the two memory blocks in turn (starting at column zero of row 0 in array 0) using all memory locations in each row and then moving to the next row and repeating the operation." ['494 Reference, Col. 11:26-31]
23. The memory of claim 20 wherein in the burst mode read operation, the control circuit enables the sense amplifier circuit selected to provide data to the memory output and at the same time disables one or more sense amplifier circuits not selected to provide data to the memory output.	This limitation is met by the '596 Reference alone or in combination with any of the '754 Reference or the '788 Reference or the '937 Reference or the '003 Reference or the '178 Reference. The '596 Reference states: "Memory blocks 10_1, 10_2, ..., 10_n include row decoders 12_1, 12_2, ...,12_n, sense amplifiers 14_1, 14_2, ..., 14_n and column decoders 16_1, 16_2, ..., 16_n, respectively. Each of memory blocks 10_1, 10_2, ..., 10_n is enabled by corresponding one of block decoders 20_1, 20_2, ..., 20_n on the basis of lower row address 18. Remaining upper row address 22 is input to row decoders 12_1, 12_2, ..., 12_n, and a word line is selected by upper row address 22." ['596 Reference, Col. 2:62-Col. 3:2] "At the leading edge of a timing pulse, sense amplifiers 14_1, 14_2, and 14_n in the above three blocks are simultaneously enabled." ['596 Reference, Col. 4:39-42]

	See also Claims 1 and 7. The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-2 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58] The '788 Reference states: "According to this arrangement, only one plane is selected in accordance with the content of the upper-order two bits of the row address. The selected plane is activated and exhibits the memory operation but the rest of the planes which are under the non-selection state are inoperative. Therefore, the decoders and the sense amplifiers are inoperative in these inoperative planes and the memory is not refreshed. Therefore, power is consumed in only the selected plane and unnecessary power consumption in the other plane can be saved. Thurs, the requirement for low power consumption can be satisfied." ['788 Reference, 5:57-68]

	The '937 Reference states: "The sense amplifier 86 is controlled by the signals SE_{EV} to smplify the read data thereby to supply the same to the data latch 87, which in turn temporarily stores the outputs from the sense amplifiers 86. When the signals SE_{EV} are at low levels, the data latch 87 is electically cut off from the sense amplifier 86. Data from the data latch 87 are transferred to the output latch 89 when the signals OE_{EV} are at high levels. In a similar manner, the sense amplifier 96 is controlled by the signals SEOD to amplify the read data thereby to supply the same to the data latch 97, which in turn temporarily stores the outputs from the sense amplifier 96. When the signals SE_{OD} are at low levels, the data latch 97 is electrically cut off from the sense amplifier 96." ['937 Reference, 4:52-66] The '003 Reference states: "The flash memory control 99 also selectively enables one of two sets of bi-directional data buffers 90 and 91 which respectively couple th bank data buses 82 and 83 to the processor section data bus 63. The bank data buses 81 and 83 can be coupled to the instruction bus 61 by the flash memory control 88 selectively enabling buffers 92 and 93, respectively." ['003 Refrence, 9:21-27] The '178 Reference states: "Referring now to FIG. 2, the circuit of FIG 1 has been modified to utilize the fact that, when RA10=1, only one half of the ARRAY BANKs 20 are being utilized and that, when RA10=0, the other half of the ARRAY BANKs 20 are being utilized. In

	particular, the RA 10 address is used to cause only the half of the ARRAY BANKs 20 that are being utilized to draw power from the DRAM energy source during read/write operations, while at the same time permitting the periodic performance of the refresh cycle in the usual manner on all ARRAY BANKs." ['178 Reference, 3:32-42]

U.S. Patent No. 5,559, 990 Invalidity Chart: United States Patent No. 5,276,649 ("'649 Reference")

All asserted claims are anticipated by the '649 Reference and/or are rendered obvious by it, either alone or in combination with other prior art described below and/or listed in Section I of Defendants' and Counterclaimants' Preliminary Invalidity Contentions and/or through modifications described below. Nothing in this invalidity chart should be construed as signifying or suggesting Defendants and Counterclaimants' adoption of or acquiescence in any claim scope and/or claim construction positions taken by Plaintiffs and Counterdefendants in this litigation.

CLAIM	RESPONSE
8. A memory comprising:	Although a preamble is normally not limiting, should this preamble be limiting this element is met by U.S. Patent No. 5,276,649 ("the '649 Reference"). Specifically, the '649 Reference is entitled "Dynamic-Type Semiconductor Memory Device Having Staggered Activation Of Column Groups."
a set of consecutively addressed memory locations L1, . . . Ln;	This limitation is met by the '649 Reference, alone or in combination with one or more of the following references, namely the '738 Reference, or the '196 Reference, or the '885 Reference. Specifically, the '649 Reference states that: "FIG. 6 is a schematic diagram showing an arrangement of the main part of a dynamic type semiconductor memory device according to one embodiment of the present invention, ...Referring to FIG. 6, bit line pairs comprise a first group of bit line pairs comprised of even numbered bit line pairs BL0, BL0(neg), BL2 and BL2(neg) having crossing portions, and a second group of bit line pairs comprised of odd numbered bit line pairs BL1, BL1(neg), . . . , BLm and BLm(neg) of a non-twisted bit line structure having no crossing portion. Bit line pairs belonging to the first group of bit line pairs and bit line pairs belonging to the second

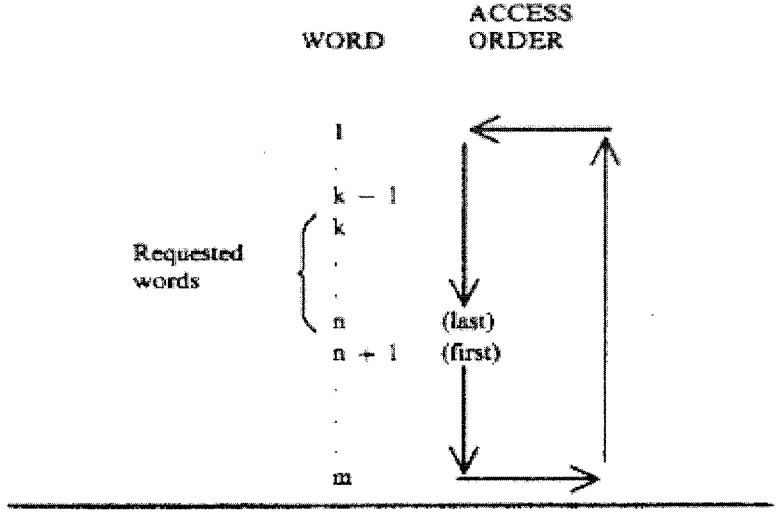
CLAIM	RESPONSE
	group of bit line pairs are alternately disposed." ['649 Reference, Col. 8:17-32]. "Referring to FIG. 2, memory cells MC are arranged in [a] matrix of rows and columns." ['649 Reference, Col. 1:65-66]. "A memory cell MC is disposed at an intersection of each word line and one bit line of a bit line pair." ['649 Reference, Col. 2:24-25]. The '738 Reference states: "A memory comprising a plurality of memory cells, a column decoder, a row decoder, a plurality of shift registers and a multiplexer is provided for addressing the memory cells in a conventional manner or in a high-speed sequential mode." ['738 Reference, Abstract]. The '196 Reference states that: "Referring now to FIGS. 2A and 2B, there is shown a block schematic diagram of a pair of RAM arrays 31, 33, each comprising a plurality of individual memory cells of the type illustrated and described above with reference to FIGS. 1A and 1B. Each of these arrays may be configured to store data in a matrix of rows and columns [sic] that is several columns long and several rows deep (e.g. 72X128). The columns and rows of memory cells in each array are connected to decoders for writing and reading data into and out of selected memory cells in the arrays. Specifically, the write column decoders 35, 37 are connected to the dual arrays to address selected columns of memory cells, and the write row decoders and drivers 39, 41 are connected to the dual arrays to address selected rows of memory cells. Similarly, the read column decoders 45,47 are connected to the dual arrays to address selected columns of memory

CLAIM	RESPONSE
	cells , and the read row decoders and drivers 49, 51 are connected to the dual arrays to address selected rows." ['196 Reference, Col. 3:11-29; See also FIGS 1A, 1B, 2A]. The '885 Reference states: "Fig. 1 shows the basic elements of an electrically erasable programmable read only memory (EEPROM) device. The device includes an EEPROM array 2 which is divided into 256 storage registers of 16 bits each." ['885 Reference, Col. 3:44-48; *see also* Figs. 1 and 2].
a plurality of sense amplifier circuits for amplifying contents of said memory locations; and	This element is met in the '649 Reference. Specifically, the '649 Reference states that: "Sense amplifiers 10-1, 10-3, . . . activated in response to a sense amplifier activating signal .phi..sub.B are provided on bit lines belonging to the first group of bit line pairs. Sense amplifiers 10-2, . . . , 10-n activated in response to a sense amplifier activating signal .phi..sub.A are provided on bit lines belonging to the second group of bit line pairs. A sense amplifier activating signal generating circuit 20 is provided in order to operate a sense amplifier group of the first group and a sense amplifier group of the second group at a different timing. The sense amplifier activating signal generating circuit 20 receives a sense amplifier activating signal .phi.0 and a column address YA0 of 1 bit so as to activate either one of sense amplifier activating signals .phi..sub.A or .phi..sub.B first." ['649 Reference, Col. 8:33-8:46]. See also, '649 Reference, Col 8:47--11:15; FIGs. 6, 8, 14, 17.
an output for providing output signals from said	This element is met in the '649 Reference. Specifically, the '649

CLAIM	RESPONSE
plurality of sense amplifier circuits,	Reference states that: "FIG. 6 is a schematic diagram showing an arrangement of the main part of a dynamic type semiconductor memory device according to one embodiment of the present invention, ...Referring to FIG. 6, bit line pairs comprise a first group of bit line pairs comprised of even numbered bit line pairs BL0, BL0(neg), BL2 and BL2(neg) having crossing portions, and a second group of bit line pairs comprised of odd numbered bit line pairs BL1, BL1, . . . , BLm and BLm of a non-twisted bit line structure having no crossing portion. Bit line pairs belonging to the first group of bit line pairs and bit line pairs belonging to the second group of bit line pairs are alternately disposed." ['649 Reference, Col. 8:17-32]. See also, FIG. 6, "I/O and "I/O(neg)"
wherein said memory has a burst mode operation for receiving an address and reading out to said output, in response to said address, any given number of memory locations in the sequence of consecutive addresses with wrap around so that the next location, if any, to be read out after said location Ln is said location L1, such that during said operation while the contents of any location L to be read out other than the last location to be read out are being transferred from said plurality of sense amplifier circuits to said output, the contents of another location to be read out after said location L are being provided to said plurality of sense amplifier circuits for amplification and subsequent transfer to said output, and	This limitation is met by the '649 Reference, alone or in combination with one or more of the following references: (a) any of the admitted prior art identified in the '990 Patent, or the '738 Reference, or the '196 Reference, and (b) the '885 Reference or the '631 Reference. The '990 patent admits that burst mode is prior art: "When a memory is read sequentially (that is, consecutive read access memory locations at consecutive addresses), the memory access can be made faster by reading from the array several consecutive locations simultaneously. Such a "burst mode" access is provided by memory 202 of FIG. 2." ['990 patent, Background of the Invention, Col. 1:36-41.] The '738 Reference states: "In the sequential mode, the decoders of the memory are used in a

CLAIM	RESPONSE
	conventional manner for decoding the address of the first cell to be accessed in a predetermined sequence of cells and thereafter, the shift registers are used for addressing the remaining cells in the sequence." ['738 Reference, Col. 1:56-61] "At the same time that the column shift register accessing the last column of cells in each of the sets is shifted to access the first column of cells in that set, the row shift register is also shifted to access the cells in another row of the cells in that set." ['738 Reference, Col. 2:14-18] "In response to the first clock pulse CK shown in FIG. 2 at 88, the contents of Cell 10 are transferred from the register 11 to the data output line 98, the flip-flop circuit 10 is activated to switch the multiplexer 9 to couple the second input R to the output line 80 and a clock pulse CKL is generated on the line 95, causing the output Y2 of the shift register 4 to go low and the output Y4 of the shift register 4 to go high, as shown at 100 and 101 of FIG. 2." ['738 Reference, Col. 4:60-68] "When the last cell in a row of the first set, e.g. cell 14, is deselected by the output Y6 of the shift register 4 going from a high to a low as shown at 105 of FIG. 2, a shift pulse is generated on the line 54 for shifting the output of shift register 6 from row X1L to row X2L as shown at 106 and 107 of FIG. 2. Similarly, when cell 15 in row X1R of set 20 is deselected by output line Y7 going low as shown at 107, the transition on line 59 causes the shift register 7 to shift from row X1R to row X2R, as shown at 108 and 109 of FIG. 2." ['738 Reference, Col. 5:15-25] The '196 Reference states that: "In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit lines in the other array are

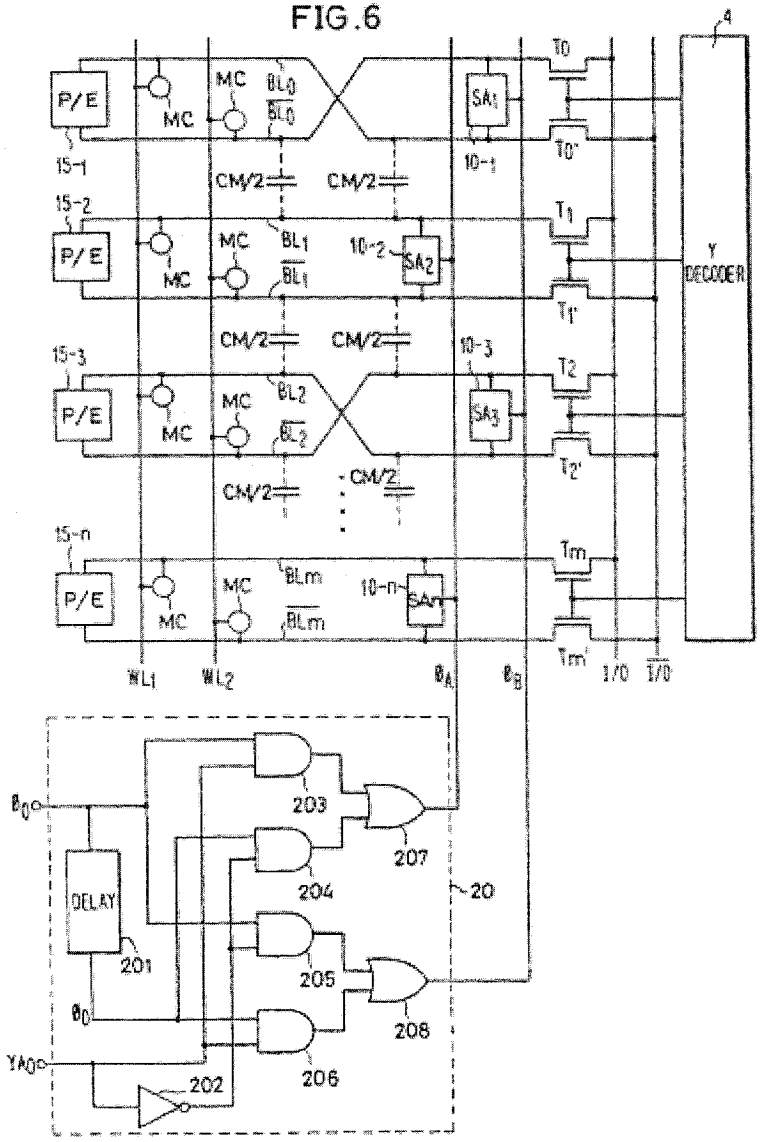
CLAIM	RESPONSE
	being precharged. Thus, as data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit lines in that array will already have been initialized." ['196 Reference, Col. 2:60-67] "In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and settling transient signals) in preparation for the next access form such other array. Therefore, precharging times for one array overlap the time for performing read or write operation in the other array, and therefore do not limit operating speed." ['196 Reference, Col. 3:41-47] The '885 Reference states: "After the last memory address is reached, the access automatically rolls over to the first address." ['885 Reference, Col. 3:1-3] "A method as in claim 5 wherein the sequence of incremented addresses wraps around when the address of the Nth register is reached such that all N registers in the array are read." ['885 Reference, Col. 7:45-48] The '631 Reference states that: "The above-described method is accomplished by utilizing two pieces of information, which are placed on the bus (23) by the GDP: the data word's offset and the number of words requested. The data word's offset in the cache line is derived from address bits 2 and 3 (00=word 1, 01=word 2, 10=word 3, and 11=word 4). The number of words being requested is obtained from the size bits 0 and 1 (00=1 word, 01=2 words, 10=3 words, and 11=4 words).

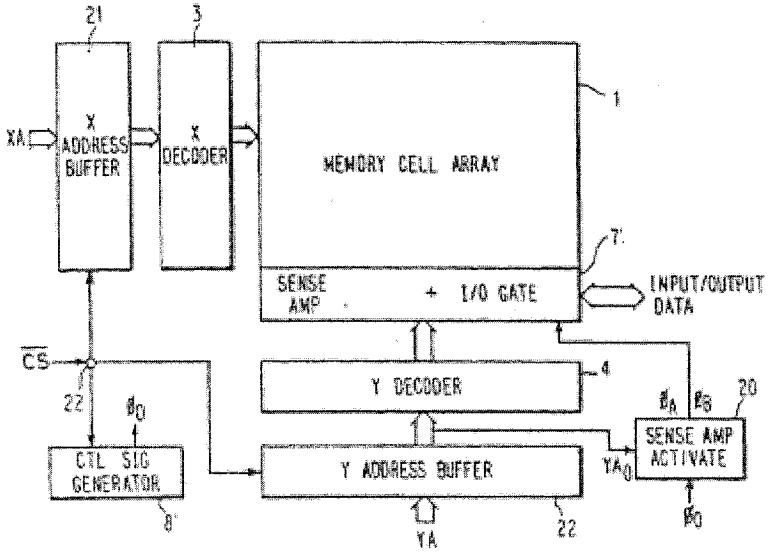
CLAIM	RESPONSE
	Using these two pieces of information, the following algorithm is executed: FIRST WORD ACCESSED = PROCESSOR WORD ADDRESS + SIZE +1 The 1 is added to the size in order to yield the correct offset. For example, if the GDP requests two words at offset 01 in a four-word line, it is converted to a wraparound request of four words to memory starting at word four [offset (01) + word count (01) + 1 = 11]." ['631 Reference, Col. 3:46-65] See, '631 Reference, Table II: **TABLE II** 

CLAIM	RESPONSE
	See also, '631 Reference, Abstract, Table I, Fig. 3.
wherein said memory further comprises a control circuit for selectively enabling said sense amplifier circuits so that said control circuit enables a sense amplifier circuit whose output signals are being transferred to the output of said memory but said control circuit does not enable all said sense amplifier circuits at the same time.	This element is met by the '649 Reference. Specifically, the '649 Reference states: "A dynamic-type semiconductor memory device according to the present invention has bit line pairs of a first group and bit line pairs of a second group. The memory of the invention further includes circuitry for operating at a different timing a first group of sense amplifiers provided on bit line pairs of the first group and a second group of sense amplifiers provided on bit line pairs of the second group. Preferably, a group of sense amplifiers provided on a bit line group to which a bit line pair connected to a selected memory cell by an external address belongs is operated first. A method of driving a sense amplifier comprises the step of activating at a different timing the first group of the sense amplifiers provided on each bit line pair of the first group of bit line pairs, and the second group of the sense amplifiers provided on each bit line pair of the second group of bit line pairs. A sense amplifier of the first sense amplifier group and a sense amplifier of the second amplifier group are arranged alternately. Each bit line pair of the first group of bit line pairs has at least one crossing portion, and each bit line pair of the second group of bit line pairs has no, or one or more crossing portions. A method of driving a sense amplifier according to the present invention further comprise a step of first activating sense amplifiers provided on a bit line group comprised of a bit line pair selected in response to a column address applied from the exterior.

CLAIM	RESPONSE
	Reduction of peak current in the sensing operation without exerting an adverse influence on a read potential becomes possible because bit line pairs are divided into a first group and a second group, so that a first sense amplifier group provided on the first group of bit line pairs and a second sense amplifier group provided on the second group of bit line pairs are activated at different timing." ['649 Reference, Col. 6:47-Col. 7:15]. "Sense amplifiers 10-1, 10-3, . . . activated in response to a sense amplifier activating signal .phi..sub.B are provided on bit lines belonging to the first group of bit line pairs. Sense amplifiers 10-2, . . . , 10-n activated in response to a sense amplifier activating signal .phi..sub.A are provided on bit lines belonging to the second group of bit line pairs. A sense amplifier activating signal generating circuit 20 is provided in order to operate a sense amplifier group of the first group and a sense amplifier group of the second group at a different timing. The sense amplifier activating signal generating circuit 20 receives a sense amplifier activating signal .phi.0 and a column address YA0 of 1 bit so as to activate either one of sense amplifier activating signals .phi..sub.A or .phi..sub.B first." ['649 Reference, Col. 8:33-8:46]. See also, '649 Reference, Col 8:47--11:15.
9. The memory of claim 8 wherein, during said operation, said control circuit enables at the same time only:	
(1) the sense amplifier circuit whose output signals are being transferred to said output of said memory, and	This element is met by the '649 Reference. For example, sense amplifiers circuits with output signals being

CLAIM	RESPONSE
	transferred to said output of said memory is shown in FIGs. 6 and 7, reproduced below.

CLAIM	RESPONSE
	FIG.6  FIG.8

CLAIM	RESPONSE
	FIG.8  Further, the '649 Reference states that: "Sense amplifiers 10-1, 10-3, . . . activated in response to a sense amplifier activating signal .phi.sub.B are provided on bit lines belonging to the first group of bit line pairs." ['649 Reference, Col. 8:33-35]. "A sense amplifier activating signal generating circuit 20 is provided in order to operate a sense amplifier group of the first group and a sense amplifier group of the second group at a different timing. The sense amplifier activating signal generating circuit 20 receives a sense amplifier activating signal .phi.0 and a column address YA0 of 1 bit so as to activate either one of sense amplifier activating signals .phi..sub.A or

CLAIM	RESPONSE
	.phi.sub.B first." ['649 Reference, Col. 8:33-8:46].
(2) a predetermined number of other sense amplifier circuits whose output signals will be transferred next to said output of said memory if said operation continues sufficiently long.	This element is met by the '649 Reference. "Sense amplifiers 10-2, . . ., 10-n activated in response to a sense amplifier activating signal .phi.sub.A are provided on bit lines belonging to the second group of bit line pairs." ['649 Reference, Col. 8:36-38].
14. The memory of claim 8 wherein said memory is fabricated in an integrated circuit.	This element is met by the '649 Reference alone or in combination with any of the '754 Reference or the '199 Reference, or U.S. Patent No. 4,899,312 ("the '312 Reference"). The '649 Reference is titled "Dynamic-Type Semiconductor Memory Device Having Staggered Activation of Column Groups." Further, it was well known in the art to fabricate memories as an integrated circuit and a person of ordinary skill would have know that the memory device shown in the '649 Reference could be fabricated in an integrated circuit. The '754 Reference states: "The present invention relates to a semiconductor dynamic memory device. Mass-production of 64K bit dynamic type random access memory devices (DRAMs) has been enabled by the recent development of semiconductor memory devices of high packing density. Furthermore, a 256K bit DRAM has been developed." ['754 Reference, Page 2:1-4]. The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held

CLAIM	RESPONSE
	temporarily in a buffer." ['199 Reference, Col. 1:13-16]. The '312 Reference states: "The individual circuit elements constructing the RAM of the present embodiment are formed on a semiconductor substrate such as a piece of single-crystalline silicon by the known technique for fabricating a CMOS (i.e., Complementary MOS) integrated circuit." ['312 Reference, Col. 2:34-38].