Goodard v. Google, Inc. Doc. 105 Att. 22

EXHIBIT 1

D16-D17

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Appendix D16

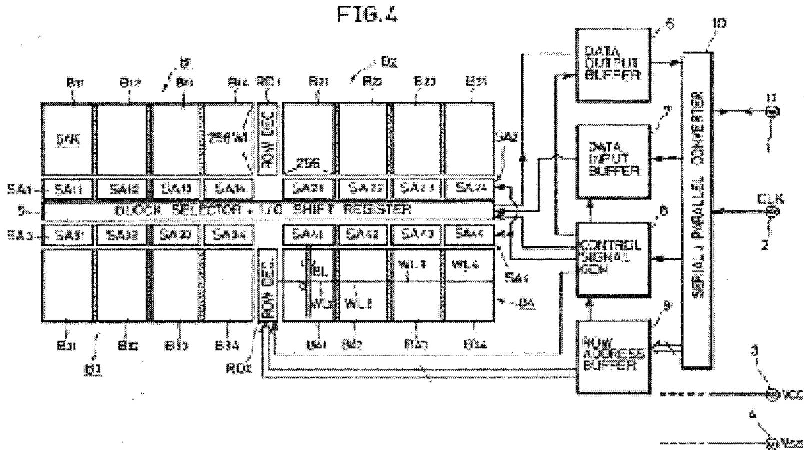
Defendants and Counterclaimants' Invalidity Contentions

Advanced Micro Devices, Inc., et al., v. Samsung Electronics Co., Ltd. et al., Case No. 3:08-CV-0986-SI

U.S. Patent No. 5,559, 990 Invalidity Chart: United States Patent No. 5,222,047 ("'047 Reference")

All asserted claims are anticipated by the '047 Reference and/or are rendered obvious by it, either alone or in combination with other prior art described below and/or listed in Section I of Defendants' and Counterclaimants' Preliminary Invalidity Contentions and/or through modifications described below. Nothing in this invalidity chart should be construed as signifying or suggesting Defendants and Counterclaimants' adoption of or acquiescence in any claim scope and/or claim construction positions taken by Plaintiffs and Counterdefendants in this litigation.

CLAIM	RESPONSE
1. A memory comprising:	Although a preamble is normally not limiting, should this preamble be limiting this element is met by U.S. Patent No. 5,222,047 ("the '047 Reference"). Specifically, the '047 Reference is entitled "Method and Apparatus for Driving Word Line in Block Access Memory."
a plurality of rows of memory locations;	This element is met in the '047 Reference. Specifically, the '047 Reference states that: "Fig. 4 is to illustrate the word line driving method of the block access memory in accordance with one embodiment of the present invention, showing the schematic structure of the block access memory. * * * In Fig. 4, a structure is shown as an example in which one subblock has the capacity of 64K bits and has 256 row X 256 column structure." ['047 Reference, Col. 6, ln. 14-24]; See, Fig. 4:

CLAIM	RESPONSE
	FIG.4 
a plurality of first registers, each first register for receiving a row address;	This limitation is met by the '047 Reference, in combination with any of the '738 Reference or the '885 Reference. The '738 Reference states: "In accordance with the above objects, there are provided a first and a second set of memory cells, a column decoder, a row decoder, a pair of column shift registers for addressing the column address lines, a pair of row shift registers for addressing the row address lines, a multiplexer having a first and a second input coupled to the data output lines of the fist and second sets, respectively, a data register and means for shifting the shift registers and switching the multiplexer between its first and second inputs." ['738 Reference, Col. 1:43-52] The '885 Reference states: "A READ instruction loads the address of the memory register to be read

CLAIM	RESPONSE
	from the instruction register 4 into an 8-bit address register 7. The data from the accessed storage register is then transferred in parallel to data shift register 5 via the sense amplifiers 6 and then clocked out serially to the Data-Out pin DO." ['885 Reference, Col. 4:16-22; *see also*, Figs. 1 and 2] Further, to the extent AMD reads this limitation on the Samsung devices, this limitation is met by the '885 Reference.
a plurality of row decoders, each row decoder for activating a portion of a row identified by signals from one of said first registers;	This element is met in the '047 Reference. Specifically, the '047 Reference states that: "In order to select one word line in response to externally applied address signals, row decoder RD1 is provided for blocks B1 and B2 while a row decoder RD2 is provided for blocks B3 and B4." ['047 Reference, Col. 2:16-19; See FIGs. 1 and 4]. "The external row address applied through the data input/output terminal 1 is applied to the row address buffer 9 through the serial/parallel conversion circuit 10 and is applied to the row decoders RD1 and RD2 under the control of the control signal generation circuit 8." ['047 Reference, Col. 2:57-62].
one or more sense amplifiers for amplifying contents of said memory locations in the row portions; and	This element is met in the '047 Reference. Specifically, the '047 Reference states that: "In the above described conventional block access memory, the memory operation is basically carried out by using one row of memory cells (block unit) as a unit (in the conventional block access memory shown in FIG. 1, 1024 bit serial input/output) and 1024 sense amplifiers are simultaneously activated for the selected one word line . . ." ['047

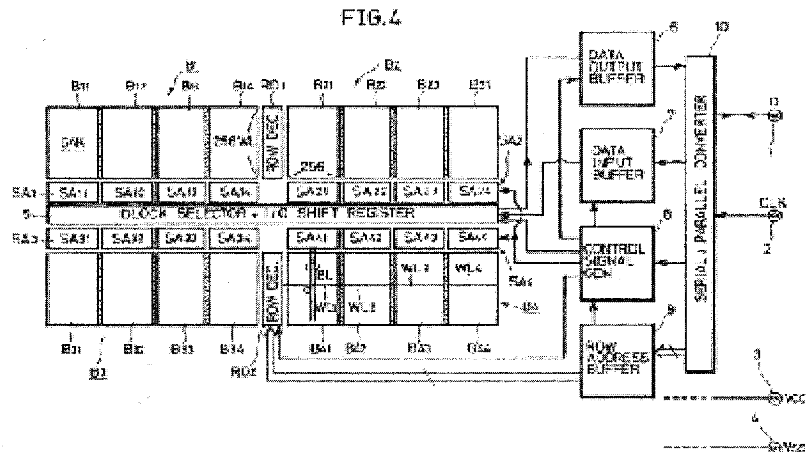
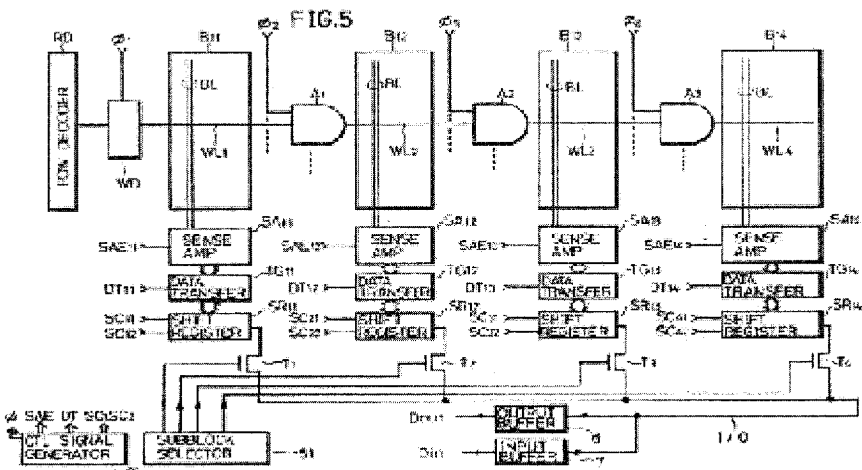
CLAIM	RESPONSE
	Reference, Col. 4:44-49]. In FIG. 4, a structure is shown as an example in which one subblock has the capacity of 64K bits and has 256 row X 256 column structure. Each of the sense amplifiers SA1 to SA4 is divided respectively in correspondence to each subblock. Namely, the sense amplifier SA1 is divided into four sense amplifier groups SA11, SA12, SA13 and SA14." ['047 Reference, Col. 6:22-28; See, FIGs 4 and 5, above].
an output for providing output signals from said sense amplifiers,	This element is met in the '047 Reference. Specifically, the '047 Reference states that: "In reading data, the read data, which are detected and amplified by the sense amplifier of the block to which the selected word line belongs out of the sense amplifiers SA1 to SA4, are transmitted and latched at the shift register provided corresponding to the blocks." ['047 Reference, Col. 3:13-17; See FIGs. 1, 4, 5, and 6.]
wherein at least two locations L1 and L2 in different rows having different row addresses in said memory can be read out to said output in burst mode such that the memory receives an address of one of said locations and provides in response contents of a plurality of memory locations, including the locations L1 and L2, in the sequence of consecutive addresses, so that while one of said row decoders is activating a row portion comprising said location L1 and contents of said location L1 are being transferred from one or more of said sense amplifiers to said output, another one of said row decoders is activating a row portion	This limitation is met by the '047 Reference, alone or in combination with one or more of the following references: any of the admitted prior art identified in the '990 Patent, or the '738 Reference, or the '196 Reference or the '421 Reference. The '990 patent admits that burst mode is prior art: "When a memory is read sequentially (that is, consecutive read access memory locations at consecutive addresses), the memory access can be made faster by reading from the array several consecutive locations simultaneously. Such a "burst mode" access is provided by memory 202 of FIG. 2." ['990 patent, Background of the Invention, Col. 1:36-41.]

CLAIM	RESPONSE
comprising said location L2 and contents of said location L2 are being transferred from said location L2 to one or more of said sense amplifiers.	Specifically, the '738 Reference states: "In the sequential mode, the decoders of the memory are used in a conventional manner for decoding the address of the first cell to be accessed in a predetermined sequence of cells and thereafter, the shift registers are used for addressing the remaining cells in the sequence." ['738 Reference, Col. 1:56-61] "At the same time that the column shift register accessing the last column of cells in each of the sets is shifted to access the first column of cells in that set, the row shift register is also shifted to access the cells in another row of the cells in that set." ['738 Reference, Col. 2:14-18] "In response to the first clock pulse CK shown in FIG. 2 at 88, the contents of Cell 10 are transferred from the register 11 to the data output line 98, the flip-flop circuit 10 is activated to switch the multiplexer 9 to couple the second input R to the output line 80 and a clock pulse CKL is generated on the line 95, causing the output Y2 of the shift register 4 to go low and the output Y4 of the shift register 4 to go high, as shown at 100 and 101 of FIG. 2." ['738 Reference, Col. 4:60-68] "When the last cell in a row of the first set, e.g. cell 14, is deselected by the output Y6 of the shift register 4 going from a high to a low as shown at 105 of FIG. 2, a shift pulse is generated on the line 54 for shifting the output of shift register 6 from row X1L to row X2L as shown at 106 and 107 of FIG. 2. Similarly, when cell 15 in row X1R of set 20 is deselected by output line Y7 going low as shown at 107, the transition on line 59 causes the shift register 7 to shift from row X1R to row X2R, as shown at 108 and 109 of FIG. 2." ['738 Reference, Col. 5:15-25]

CLAIM	RESPONSE
	The ‘196 Reference states that: “In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit lines in the other array are being precharged. Thus, as data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit lines in that array will already have been initialized.” [‘196 Reference, Col. 2:60-67] “In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and settling transient signals) in preparation for the next access form such other array. Therefore, precharging times for one array overlap the time for performing read or write operation in the other array, and therefore do not limit operating speed.” [‘196 Reference, Col. 3:41-47] The ‘421 Reference shows and states:

CLAIM	RESPONSE
	FIGURE 6 "The organization of memory array 503 is shown in FIG. 6. As shown in FIG. 6, the memory array 503 is divided into left and right halves. Word lines WL_{K+1} and WL_K, corresponding to consecutive row addresses are activated simultaneously when signal N+1 is asserted. When signal N+1 is not asserted, activated word lines in both halves have the same row address. * * * As a result of the ability to activate word lines in the left and right halves independently, register banks A and B may be loaded simultaneously upon initial access with data from tow different rows of memory cells, corresponding to two different word lines." ['421 Reference, Col. 4:52-68].
2. The memory of claim 1, said memory having a random mode in which the memory receives an address	Although a preamble is normally not limiting, should this preamble be limiting this element is met by the '047 Reference, either alone or in

CLAIM	RESPONSE
and provides in response the contents of a unique memory location,	combination with the admitted prior art in the '990 patent, the knowledge of one of ordinary skill in the art, or the references cited below.
wherein, both in burst mode and in random mode, while the contents of said location L1 are being transferred from one or more of said sense amplifiers to said output, the contents of said location L2 are being transferred from said location L2 to one or more of said sense amplifiers.	This element is met in the '047 Reference. Specifically, the '047 Reference states that: "In the above described conventional block access memory, the memory operation is basically carried out by using one row of memory cells (block unit) as a unit (in the conventional block access memory shown in FIG. 1, 1024 bit serial input/output) and 1024 sense amplifiers are simultaneously activated for the selected one word line . . ." ['047 Reference, Col. 4:44-49]. In FIG. 4, a structure is shown as an example in which one subblock has the capacity of 64K bits and has 256 row X 256 column structure. Each of the sense amplifiers SA1 to SA4 is divided respectively in correspondence to each subblock. Namely, the sense amplifier SA1 is divided into four sense amplifier groups SA11, SA12, SA13 and SA14." ['047 Reference, Col. 6:22-28]. See '047 Reference, FIGs 4 and 5, above.
3. The memory of claim 1 wherein when the locations L1 and L2 are read out in burst mode and when the contents of said location L1 are being transferred from one or more of said sense amplifiers to said output and the contents of said location L2 are being transferred from said location L2 to one or more of said sense amplifiers, the sense amplifiers from which the contents of said location L1 are being transferred are enabled and the sense amplifiers to which the contents	This limitation is met by the '047 Reference, alone or in combination with one or more of the following references: (a) any of the admitted prior art identified in the '990 Patent, or the '738 Reference, or the '196 Reference. The '047 Reference shows:

CLAIM	RESPONSE
of said location L2 are being transferred are disabled, but these latter sense amplifiers become enabled subsequently for amplifying the contents of said location L2.	FIG.4  FIG.5  See FIGS. 4 & 5. "In the block access memory in accordance with the present invention,

CLAIM	RESPONSE
	each blocks [sic] are further divided into a plurality of subblocks and the timing for activating the word line and the timing for activating sense amplifiers in each subblock in that block selected by the external address are made different from each other. According to the present invention, since the timing for activating the word lines and the timing for activating the sense amplifiers are different from each other in the plurality of subblocks in the selected block, so that the number of sense amplifiers which are activated at one time is reduced, whereby the peak current associated with the charge/discharge of the bit lines at the time of activating sense amplifiers can be suppressed and the errors due to the fluctuation of the substrate potential and so on can be prevented." ['047 Reference, Col. 5:30-45]. "The sense amplifiers and the shift registers are also divided into subblocks so as to correspond to each subblock. Namely, a sense amplifier SA11 which is activated in response to the sense amplifier activating signal SAE11 and a shift register SR11 which latches and shifts the input data in response to the clock signals SC11 and SC12 are provided for the subblock B11. A sense amplifier SA12 which is activated in response to the sense amplifier activating signal SAE12 and a shift register SR12 which latches and shifts the data in response to the clock signals SC21 and SC22 are provided for the subblock B12. A sense amplifier SA13 which is activated in response to the sense amplifier activating signal SAE12 and a shift register SR13 which latches and shifts the data in response to the clock signals SC31 and SC32 are provided for the subblock B13. A sense amplifier SA14 which is activated in response to a sense amplifier activating signal SAE14 and a shift register SR14 which latches and shifts the data in response to the clock signals SC41 and SC42 are provided for the subblock B14." ['047 Reference, Col. 7:30-50].

CLAIM	RESPONSE
	"The sense amplifier activating signal line 70 is connected to the ground potential through a transistor 71 which turns on in response to the sense amplifier activating signal SAE." ['047 Reference, Col. 8:24-29]. "First, in the similar manner as in the conventional case, an external row address is serially applied to the data input/output terminal 1 subsequent to the control designating the row address set. The external row address is simultaneously applied to the row address buffer 9 through the serial/parallel conversion circuit 10. The row address buffer 9 generates a set of internal row addresses (for example complementary address signal pair) corresponding to the applied external row address and applies the same to the row decoders RD1 and RD2. Consequently, one of the 1024 unit row decoders (in the case where one block is constituted by 256 rows, 256 X 4= 1024) included in the row decoders RD1 and RD2 is selected and activated. The subword line WL1 in the subblock B11 is activated by the output of the word driver WD in response to the output of the selected unit row decoder and to the word line driving signal φ1 which is generated from the control signal generator 8' at a prescribed timing, and the potential on the subword line WL1 rises. The data in the memory cells connected to the word line WL1 is read to the bit lines BL and BL and the potentials on the bit lines BL and BL are established, and thereafter the sense amplifier SA11 provided corresponding to the subblock B11 is activated in response to the sense amplifier activating signal SAE11 which is generated under control of the control signal generator 8'." ['047 Reference, Col. 9:3-29]. "When the potential on the bit line is established, the sense amplifier activating signal SAE12 is generated from the control signal generation circuit 8', the sense amplifier SA12 which corresponds to the subblock B12 is established to be high level or low level dependent on the read

CLAIM	RESPONSE
	information." ['047 Reference, Col. 9:55-61]. "Although the timings of the completion of the active state of the word lines in each subblock are the same and the period of the active state of the subword lines in each subblock are different from each other in the above described embodiment, the "H" level period can be made equal to each other for each subword line by directly applying the output of the word driver WD to one input of the AND gates A1 to A3 and by controlling the "H" level period of the subword lines WL1 to WL4 by the clck signal φ1 to φ4." ['047 Reference, Col. 10:47-56 The '990 patent admits that burst mode is prior art: "When a memory is read sequentially (that is, consecutive read access memory locations at consecutive addresses), the memory access can be made faster by reading from the array several consecutive locations simultaneously. Such a "burst mode" access is provided by memory 202 of FIG. 2." ['990 patent, Background of the Invention, Col. 1, Ln. 36-41.] Specifically, the '738 Reference states: "In the sequential mode, the decoders of the memory are used in a conventional manner for decoding the address of the first cell to be accessed in a predetermined sequence of cells and thereafter, the shift registers are used for addressing the remaining cells in the sequence." ['738 Reference, Col. 1:56-61] "At the same time that the column shift register accessing the last column of cells in each of the sets is shifted to access the first column of cells in that set, the row shift register is also shifted to access the cells in another

CLAIM	RESPONSE
	row of the cells in that set." ['738 Reference, Col. 2:14-18] "In response to the first clock pulse CK shown in FIG. 2 at 88, the contents of Cell 10 are transferred from the register 11 to the data output line 98, the flip-flop circuit 10 is activated to switch the multiplexer 9 to couple the second input R to the output line 80 and a clock pulse CKL is generated on the line 95, causing the output Y2 of the shift register 4 to go low and the output Y4 of the shift register 4 to go high, as shown at 100 and 101 of FIG. 2." ['738 Reference, Col. 4:60-68] "When the last cell in a row of the first set, e.g. cell 14, is deselected by the output Y6 of the shift register 4 going from a high to a low as shown at 105 of FIG. 2, a shift pulse is generated on the line 54 for shifting the output of shift register 6 from row X1L to row X2L as shown at 106 and 107 of FIG. 2. Similarly, when cell 15 in row X1R of set 20 is deselected by output line Y7 going low as shown at 107, the transition on line 59 causes the shift register 7 to shift from row X1R to row X2R, as shown at 108 and 109 of FIG. 2." ['738 Reference, Col. 5:15-25] The '196 Reference states that: "In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit lines in the other array are being precharged. Thus, as data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit lines in that array will already have been initialized." ['196 Reference, Col. 2:60-67] "In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and settling transient signals) in preparation for the next access form such other array.

CLAIM	RESPONSE
	Therefore, precharging times for one array overlap the time for performing read or write operation in the other array, and therefore do not limit operating speed." ['196 Reference, Col. 3:41-47]
6. The memory of claim 1 wherein said memory is fabricated in an integrated circuit.	This element is met by the '047 Reference alone or in combination with any of the '754 Reference or the '199 Reference, or U.S. Patent No. 4,899,312 ("the '312 Reference"). It was well known in the art to fabricate memories as an integrated circuit and a person of ordinary skill would have know that the memory device shown in the '047 Reference could be fabricated in an integrated circuit. The '754 Reference states: "The present invention relates to a semiconductor dynamic memory device. Mass-production of 64K bit dynamic type random access memory devices (DRAMs) has been enabled by the recent development of semiconductor memory devices of high packing density. Furthermore, a 256K bit DRAM has been developed." ['754 Reference, Page 2:1-4] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer." ['199 Reference, Col. 1:13-16] The '312 Reference states: "The individual circuit elements constructing the RAM of the present embodiment are formed on a semiconductor substrate such as a piece of single-crystalline silicon by the known technique for fabricating a CMOS

CLAIM	RESPONSE
	(i.e., Complementary MOS) integreated circuit." ['312 Reference, Col. 2:34-38]
8. A memory comprising:	Although a preamble is normally not limiting, should this preamble be limiting this element is met by U.S. Patent No. 5,222,047 ("the '047 Reference"). Specifically, the '047 Reference is entitled "Method and Apparatus for Driving Word Line in Block Access Memory."
a set of consecutively addressed memory locations L1, . . . Ln;	This limitation is met by the '047 Reference, alone or in combination with one or more of the following references, namely the '738 Reference, or the '196 Reference, or the '885 Reference. Specifically, the '047 Reference states that: "The data input/output terminal 1 receives a write data input to the memory cells provided in the device, a read data output from the memory cells, a row address input and a control for designating the operation mode." ['047 Reference, Col. 1:54-57]. "The memory cell array storing the information is divided into a plurality of blocks (four blocks in FIG.1) B1, B2, B3 and B4. In each of the blocks B1 to B4, provided are a plurality of memory cells MC arranged in rows and columns each of which storing information, a plurality of word lines WL for selecting one row of the plurality of memory cells MC and a plurality of bit lines BL to which one column of the plurality of memory cells MC is connected." ['047 Reference, Col. 1:61 -- Col. 2:1]. "In order to select one word line in response to externally applied address signals, a row decoder RD1 is provided for the blocks B1 and B2 while a row decoder RD2 is provided for the blocks B3 and B4." ['047 Reference, Col. 2:16-19].

CLAIM	RESPONSE
	The ‘738 Reference states: “A memory comprising a plurality of memory cells, a column decoder, a row decoder, a plurality of shift registers and a multiplexer is provided for addressing the memory cells in a conventional manner or in a high-speed sequential mode.” [‘738 Reference, Abstract]. The ‘196 Reference states that: “Referring now to FIGS. 2A and 2B, there is shown a block schematic diagram of a pair of RAM arrays 31, 33, each comprising a plurality of individual memory cells of the type illustrated and described above with reference to FIGS. 1A and 1B. Each of these arrays may be configured to store data in a matrix of rows and columns [sic] that is several columns long and several rows deep (e.g. 72X128). The columns and rows of memory cells in each array are connected to decoders for writing and reading data into and out of selected memory cells in the arrays. Specifically, the write column decoders 35, 37 are connected to the dual arrays to address selected columns of memory cells, and the write row decoders and drivers 39, 41 are connected to the dual arrays to address selected rows of memory cells. Similarly, the read column decoders 45,47 are connected to the dual arrays to address selected columns of memory cells , and the read row decoders and drivers 49, 51 are connected to the dual arrays to address selected rows.” [‘196 Reference, Col. 3:11-29; See also FIGS 1A, 1B, 2A] The ‘885 Reference states: “Fig. 1 shows the basic elements of an electrically erasable programmable read only memory (EEPROM) device. The device includes an EEPROM array 2 which is divided into 256 storage registers of 16 bits each.” [‘885

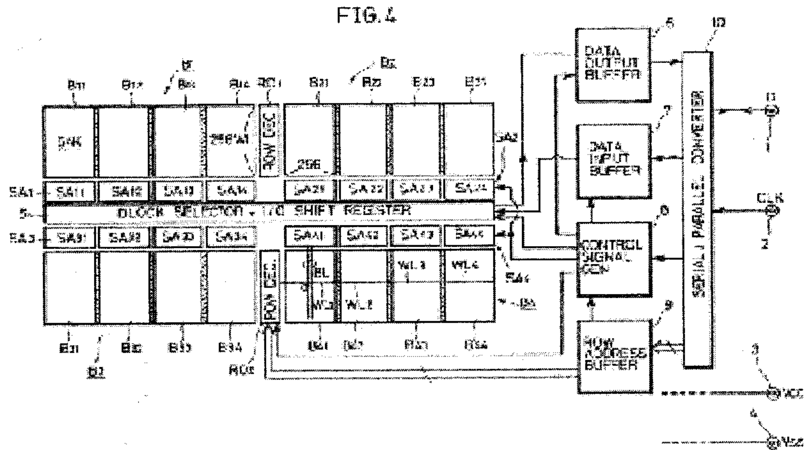
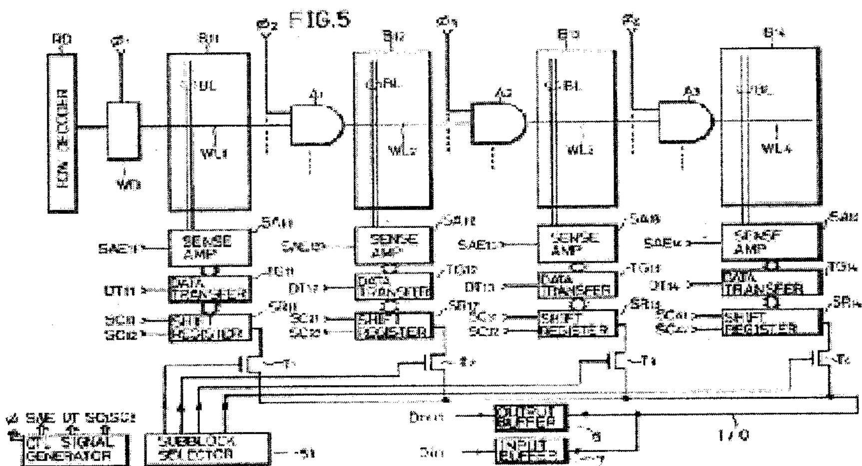
CLAIM	RESPONSE
	Reference, Col. 3:44-48; *see also* Figs. 1 and 2].
a plurality of sense amplifier circuits for amplifying contents of said memory locations; and	This element is met in the '047 Reference. Specifically, the '047 Reference states that: "In the above described conventional block access memory, the memory operation is basically carried out by using one row of memory cells (block unit) as a unity (in the conventional block access memory shown in FIG. 1, 1024 bit serial input/output) and 1024 sense amplifiers are simultaneously activated for the selected one word line . . ." ['047 Reference, Col. 4:44-49]. In FIG. 4, a structure is shown as an example in which one subblock has the capacity of 64K bits and has 256 row X 256 column structure. Each of the sense amplifiers SA1 to SA4 is divided respectively in correspondence to each subblock. Namely, the sense amplifier SA1 is divided into four sense amplifier groups SA11, SA12, SA13 and SA14." ['047 Reference, Col. 6:22-28; See FIGs. 4 and 5, above].
an output for providing output signals from said plurality of sense amplifier circuits,	This element is met in the '047 Reference. Specifically, the '047 Reference states that: "In reading data, the read data, which are detected and amplified by the sense amplifier of the block to which the selected word line belongs out of the sense amplifiers SA1 to SA4, are transmitted and latched at the shift register provided corresponding to the blocks." ['047 Reference, Col. 3:13-17; See FIGs. 1, 4, 5, and 6].
wherein said memory has a burst mode operation for receiving an address and reading out to said output, in response to said address, any given number of memory	This limitation is met by the '047 Reference, alone or in combination with one or more of the following references: (a) any of the admitted prior art identified in the '990 Patent, or the '738 Reference, or the '196 Reference,

CLAIM	RESPONSE
locations in the sequence of consecutive addresses with wrap around so that the next location, if any, to be read out after said location Ln is said location L1, such that during said operation while the contents of any location L to be read out other than the last location to be read out are being transferred from said plurality of sense amplifier circuits to said output, the contents of another location to be read out after said location L are being provided to said plurality of sense amplifier circuits for amplification and subsequent transfer to said output, and	and (b) the ‘885 Reference or the ‘631 Reference. The ‘990 patent admits that burst mode is prior art: “When a memory is read sequentially (that is, consecutive read access memory locations at consecutive addresses), the memory access can be made faster by reading from the array several consecutive locations simultaneously. Such a “burst mode” access is provided by memory 202 of FIG. 2.” [‘990 patent, Background of the Invention, Col. 1:36-41.] Specifically, the ‘738 Reference states: “In the sequential mode, the decoders of the memory are used in a conventional manner for decoding the address of the first cell to be accessed in a predetermined sequence of cells and thereafter, the shift registers are used for addressing the remaining cells in the sequence.” [‘738 Reference, Col. 1:56-61] “At the same time that the column shift register accessing the last column of cells in each of the sets is shifted to access the first column of cells in that set, the row shift register is also shifted to access the cells in another row of the cells in that set.” [‘738 Reference, Col. 2:14-18] “In response to the first clock pulse CK shown in FIG. 2 at 88, the contents of Cell 10 are transferred from the register 11 to the data output line 98, the flip-flop circuit 10 is activated to switch the multiplexer 9 to couple the second input R to the output line 80 and a clock pulse CKL is generated on the line 95, causing the output Y2 of the shift register 4 to go low and the output Y4 of the shift register 4 to go high, as shown at 100 and 101 of FIG. 2.” [‘738 Reference, Col. 4:60-68]

CLAIM	RESPONSE
	"When the last cell in a row of the first set, e.g. cell 14, is deselected by the output Y6 of the shift register 4 going from a high to a low as shown at 105 of FIG. 2, a shift pulse is generated on the line 54 for shifting the output of shift register 6 from row X1L to row X2L as shown at 106 and 107 of FIG. 2. Similarly, when cell 15 in row X1R of set 20 is deselected by output line Y7 going low as shown at 107, the transition on line 59 causes the shift register 7 to shift from row X1R to row X2R, as shown at 108 and 109 of FIG. 2." ['738 Reference, Col. 5:15-25] The '196 Reference states that: "In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit lines in the other array are being precharged. Thus, as data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit lines in that array will already have been initialized." ['196 Reference, Col. 2:60-67] "In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and settling transient signals) in preparation for the next access form such other array. Therefore, precharging times for one array overlap the time for performing read or write operation in the other array, and therefore do not limit operating speed." ['196 Reference, Col. 3:41-47] The '885 Reference states: "After the last memory address is reached, the access automatically rolls over to the first address." ['885 Reference, Col. 3:1-3] "A method as in claim 5 wherein the sequence of incremented addresses

CLAIM	RESPONSE
	wraps around when the address of the Nth register is reached such that all N registers in the array are read." ['885 Reference, Col. 7:45-48] The '631 Reference states that: "The above-described method is accomplished by utilizing two pieces of information, which are placed on the bus (23) by the GDP: the data word's offset and the number of words requested. The data word's offset in the cache line is derived from address bits 2 and 3 (00=word 1, 01=word 2, 10=word 3, and 11=word 4). The number of words being requested is obtained from the size bits 0 and 1 (00=1 word, 01=2 words, 10=3 words, and 11=4 words). Using these two pieces of information, the following algorithm is executed: FIRST WORD ACCESSED = PROCESSOR WORD ADDRESS + SIZE +1 The 1 is added to the size in order to yield the correct offset. For example, if the GDP requests two words at offset 01 in a four-word line, it is converted to a wraparound request of four words to memory starting at word four [offset (01) + word count (01) + 1 = 11]." ['631 Reference, Col. 3:46-65] See, '631 Reference, Table II:

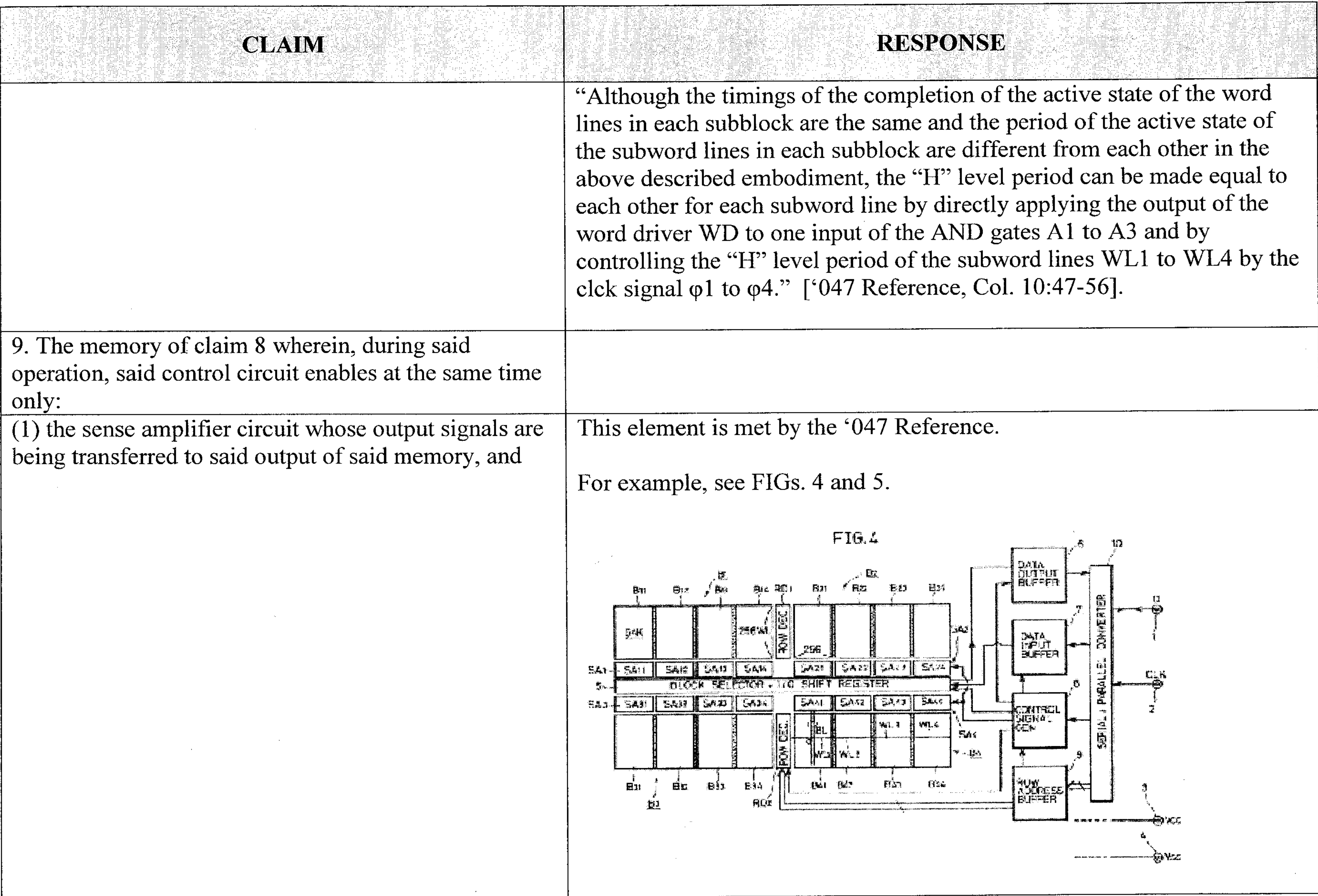
CLAIM	RESPONSE
	TABLE II WORD / ACCESS ORDER 1 . k − 1 Requested words { k . . n (last) n + 1 (first) . . . m See also, ‘631 Reference, Abstract, Table I, Fig. 3.
wherein said memory further comprises a control circuit for selectively enabling said sense amplifier circuits so that said control circuit enables a sense amplifier circuit whose output signals are being transferred to the output of said memory but said control circuit does not enable all said sense amplifier circuits at the same time.	This element is met by the ‘047 Reference. For example, see FIGs. 4 and 5.

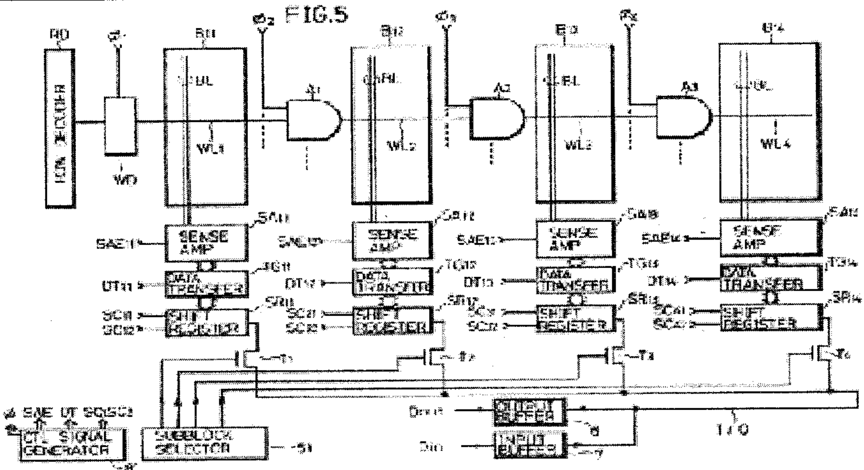
CLAIM	RESPONSE
	  "In the block access memory in accordance with the present invention, each blocks [sic] are further divided into a plurality of subblocks and the timing for activating the word line and the timing for activating sense

CLAIM	RESPONSE
	amplifiers in each subblock in that block selected by the external address are made different from each other. According to the present invention, since the timing for activating the word lines and the timing for activating the sense amplifiers are different from each other in the plurality of subblocks in the selected block, so that the number of sense amplifiers which are activated at one time is reduced, whereby the peak current associated with the charge/discharge of the bit lines at the time of activating sense amplifiers can be suppressed and the errors due to the fluctuation of the substrate potential and so on can be prevented." ['047 Reference, Col. 5:30-45]. "The sense amplifiers and the shift registers are also divided into subblocks so as to correspond to each subblock. Namely, a sense amplifier SA11 which is activated in response to the sense amplifier activating signal SAE11 and a shift register SR11 which latches and shifts the input data in response to the clock signals SC11 and SC12 are provided for the subblock B11. A sense amplifier SA12 which is activated in response to the sense amplifier activating signal SAE12 and a shift register SR12 which latches and shifts the data in response to the clock signals SC21 and SC22 are provided for the subblock B12. A sense amplifier SA13 which is activated in response to the sense amplifier activating signal SAE12 and a shift register SR13 which latches and shifts the data in response to the clock signals SC31 and SC32 are provided for the subblock B13. A sense amplifier SA14 which is activated in response to a sense amplifier activating signal SAE14 and a shift register SR14 which latches and shifts the data in response to the clock signals SC41 and SC42 are provided for the subblock B14." ['047 Reference, Col. 7:30-50]. "The sense amplifier activating signal line 70 is connected to the ground

CLAIM	RESPONSE
	potential through a transistor 71 which turns on in response to the sense amplifier activating signal SAE." ['047 Reference, Col. 8:24-29]. "First, in the similar manner as in the conventional case, an external row address is serially applied to the data input/output terminal 1 subsequent to the control designating the row address set. The external row address is simultaneously applied to the row address buffer 9 through the serial/parallel conversion circuit 10. The row address buffer 9 generates a set of internal row addresses (for example complementary address signal pair) corresponding to the applied external row address and applies the same to the row decoders RD1 and RD2. Consequently, one of the 1024 unit row decoders (in the case where one block is constituted by 256 rows, 256 X 4= 1024) included in the row decoders RD1 and RD2 is selected and activated. The subword line WL1 in the subblock B11 is activated by the output of the word driver WD in response to the output of the selected unit row decoder and to the word line driving signal φ1 which is generated from the control signal generator 8' at a prescribed timing, and the potential on the subword line WL1 rises. The data in the memory cells connected to the word line WL1 is read to the bit lines BL and BL and the potentials on the bit lines BL and BL are established, and thereafter the sense amplifier SA11 provided corresponding to the subblock B11 is activated in response to the sense amplifier activating signal SAE11 which is generated under control of the control signal generator 8'." ['047 Reference, Col. 9:3-29]. "When the potential on the bit line is established, the sense amplifier activating signal SAE12 is generated from the control signal generation circuit 8', the sense amplifier SA12 which corresponds to the subblock B12 is established to be high level or low level dependent on the read information." ['047 Reference, Col. 9:55-61].

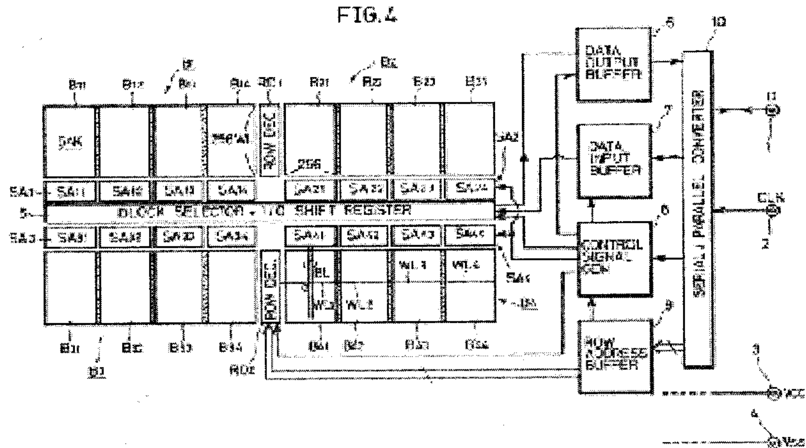
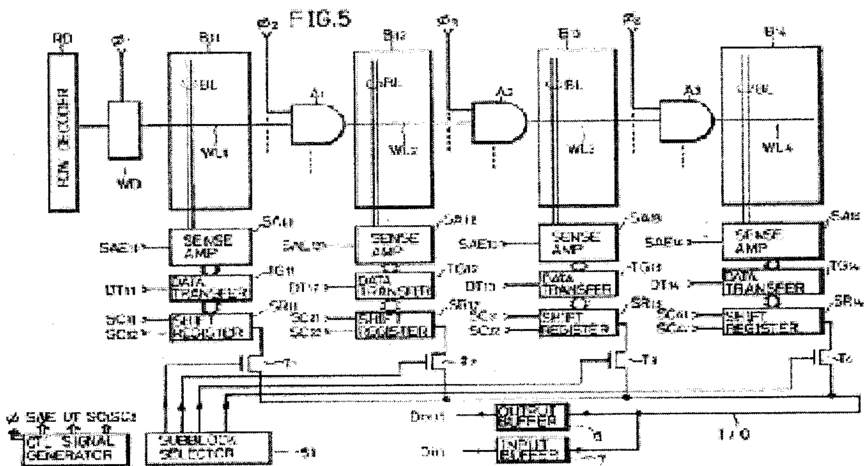
CLAIM	RESPONSE
	"Although the timings of the completion of the active state of the word lines in each subblock are the same and the period of the active state of the subword lines in each subblock are different from each other in the above described embodiment, the "H" level period can be made equal to each other for each subword line by directly applying the output of the word driver WD to one input of the AND gates A1 to A3 and by controlling the "H" level period of the subword lines WL1 to WL4 by the clck signal φ1 to φ4." ['047 Reference, Col. 10:47-56].
9. The memory of claim 8 wherein, during said operation, said control circuit enables at the same time only:	
(1) the sense amplifier circuit whose output signals are being transferred to said output of said memory, and	This element is met by the '047 Reference. For example, see FIGs. 4 and 5.



CLAIM	RESPONSE
	 “In the block access memory in accordance with the present invention, each blocks [sic] are further divided into a plurality of subblocks and the timing for activating the word line and the timing for activating sense amplifiers in each subblock in that block selected by the external address are made different from each other. According to the present invention, since the timing for activating the word lines and the timing for activating the sense amplifiers are different from each other in the plurality of subblocks in the selected block, so that the number of sense amplifiers which are activated at one time is reduced, whereby the peak current associated with the charge/discharge of the bit lines at the time of activating sense amplifiers can be suppressed and the errors due to the fluctuation of the substrate potential and so on can be prevented.” [‘047 Reference, Col. 5:30-45]. “The sense amplifiers and the shift registers are also divided into subblocks so as to correspond to each subblock. Namely, a sense

CLAIM	RESPONSE
	amplifier SA11 which is activated in response to the sense amplifier activating signal SAE11 and a shift register SR11 which latches and shifts the input data in response to the clock signals SC11 and SC12 are provided for the subblock B11. A sense amplifier SA12 which is activated in response to the sense amplifier activating signal SAE12 and a shift register SR12 which latches and shifts the data in respons to the clock signals SC21 and SC22 are provided for the subblock B12. A sense amplifier SA13 which is activated in response to the sense amplifier activating signal SAE12 and a shift register SR13 which latches and shifts the data in response to the clock signals SC31 and SC32 are provided for the subblock B13. A sense amplifier SA14 which is activated in response to a sense amplifier activating signal SAE14 and a shift register SR14 which latches and shifts the data in response to the clock signals SC41 and SC42 are provided for the subblock B14." ['047 Reference, Col. 7:30-50]. "The sense amplifier activating signal line 70 is connected to the ground potential through a transistor 71 which turns on in response to the sense amplifier activating signal SAE." ['047 Reference, Col. 8:24-29]. "First, in the similar manner as in the conventional case, an external row address is serially applied to the data input/output terminal 1 subsequent to the control designating the row address set. The external row address is simultaneously applied to the row address buffer 9 through the serial/parallel conversion circuit 10. The row address buffer 9 generates a set of internal row addresses (for example complementary address signal pair) corresponding to the applied external row address and applies the same to the row decoders RD1 and RD2. Consequently, one of the 1024 unit row decoders (in the case where one block is constituted by 256 rows, 256 X 4= 1024) included in the row decoders RD1 and RD2 is selected and activated. The subword line WL1 in the subblock B11 is

CLAIM	RESPONSE
	activated by the output of the word driver WD in response to the output of the selected unit row decoder and to the word line driving signal φ1 which is generated from the control signal generator 8' at a prescribed timing, and the potential on the subword line WL1 rises. The data in the memory cells connected to the word line WL1 is read to the bit lines BL and BL and the potentials on the bit lines BL and BL are established, and thereafter the sense amplifier SA11 provided corresponding to the subblock B11 is activated in response to the sense amplifier activating signal SAE11 which is generated under control of the control signal generator 8'." ['047 Reference, Col. 9:3-29]. "When the potential on the bit line is established, the sense amplifier activating signal SAE12 is generated from the control signal generation circuit 8', the sense amplifier SA12 which corresponds to the subblock B12 is established to be high level or low level dependent on the read information." ['047 Reference, Col. 9:55-61]. "Although the timings of the completion of the active state of the word lines in each subblock are the same and the period of the active state of the subword lines in each subblock are different from each other in the above described embodiment, the "H" level period can be made equal to each other for each subword line by directly applying the output of the word driver WD to one input of the AND gates A1 to A3 and by controlling the "H" level period of the subword lines WL1 to WL4 by the clck signal φ1 to φ4." ['047 Reference, Col. 10:47-56].
(2) a predetermined number of other sense amplifier circuits whose output signals will be transferred next to said output of said memory if said operation continues sufficiently long.	This element is met by the '047 Reference. For example, see FIGs. 4 and 5.

CLAIM	RESPONSE
	 FIG.4  FIG.5 "In the block access memory in accordance with the present invention, each blocks [sic] are further divided into a plurality of subblocks and the timing for activating the word line and the timing for activating sense

CLAIM	RESPONSE
	amplifiers in each subblock in that block selected by the external address are made different from each other. According to the present invention, since the timing for activating the word lines and the timing for activating the sense amplifiers are different from each other in the plurality of subblocks in the selected block, so that the number of sense amplifiers which are activated at one time is reduced, whereby the peak current associated with the charge/discharge of the bit lines at the time of activating sense amplifiers can be suppressed and the errors due to the fluctuation of the substrate potential and so on can be prevented." ['047 Reference, Col. 5:30-45]. "The sense amplifiers and the shift registers are also divided into subblocks so as to correspond to each subblock. Namely, a sense amplifier SA11 which is activated in response to the sense amplifier activating signal SAE11 and a shift register SR11 which latches and shifts the input data in response to the clock signals SC11 and SC12 are provided for the subblock B11. A sense amplifier SA12 which is activated in response to the sense amplifier activating signal SAE12 and a shift register SR12 which latches and shifts the data in respons to the clock signals SC21 and SC22 are provided for the subblock B12. A sense amplifier SA13 which is activated in response to the sense amplifier activating signal SAE12 and a shift register SR13 which latches and shifts the data in response to the clock signals SC31 and SC32 are provided for the subblock B13. A sense amplifier SA14 which is activated in response to a sense amplifier activating signal SAE14 and a shift register SR14 which latches and shifts the data in response to the clock signals SC41 and SC42 are provided for the subblock B14." ['047 patent, Col. 7:30-50]. "The sense amplifier activating signal line 70 is connected to the ground

CLAIM	RESPONSE
	potential through a transistor 71 which turns on in response to the sense amplifier activating signal SAE." ['047 Reference, Col. 8:24-29]. "First, in the similar manner as in the conventional case, an external row address is serially applied to the data input/output terminal 1 subsequent to the control designating the row address set. The external row address is simultaneously applied to the row address buffer 9 through the serial/parallel conversion circuit 10. The row address buffer 9 generates a set of internal row addresses (for example complementary address signal pair) corresponding to the applied external row address and applies the same to the row decoders RD1 and RD2. Consequently, one of the 1024 unit row decoders (in the case where one block is constituted by 256 rows, 256 X 4= 1024) included in the row decoders RD1 and RD2 is selected and activated. The subword line WL1 in the subblock B11 is activated by the output of the word driver WD in response to the output of the selected unit row decoder and to the word line driving signal φ1 which is generated from the control signal generator 8' at a prescribed timing, and the potential on the subword line WL1 rises. The data in the memory cells connected to the word line WL1 is read to the bit lines BL and BL and the potentials on the bit lines BL and BL are established, and thereafter the sense amplifier SA11 provided corresponding to the subblock B11 is activated in response to the sense amplifier activating signal SAE11 which is generated under control of the control signal generator 8'." ['047 Reference, Col. 9:3-29]. "When the potential on the bit line is established, the sense amplifier activating signal SAE12 is generated from the control signal generation circuit 8', the sense amplifier SA12 which corresponds to the subblock B12 is established to be high level or low level dependent on the read information." ['047 Reference, Col. 9:55-61].

CLAIM	RESPONSE
	"Although the timings of the completion of the active state of the word lines in each subblock are the same and the period of the active state of the subword lines in each subblock are different from each other in the above described embodiment, the "H" level period can be made equal to each other for each subword line by directly applying the output of the word driver WD to one input of the AND gates A1 to A3 and by controlling the "H" level period of the subword lines WL1 to WL4 by the clck signal φ1 to φ4." ['047 Reference, Col. 10:47-56].
14. The memory of claim 8 wherein said memory is fabricated in an integrated circuit.	This element is met by the '047 Reference alone or in combination with any of the '754 Reference or the '199 Reference, or U.S. Patent No. 4,899,312 ("the '312 Reference"). It was well known in the art to fabricate memories as an integrated circuit and a person of ordinary skill would have know that the memory device shown in the '047 Reference could be fabricated in an integrated circuit. The '754 Reference states: "The present invention relates to a semiconductor dynamic memory device. Mass-production of 64K bit dynamic type random access memory devices (DRAMs) has been enabled by the recent development of semiconductor memory devices of high packing density. Furthermore, a 256K bit DRAM has been developed." ['754 Reference, Page 2:1-4] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer." ['199 Reference, Col. 1:13-16]

CLAIM	RESPONSE
	The ‘312 Reference states: “The individual circuit elements constructing the RAM of the present embodiment are formed on a semiconductor substrate such as a piece of single-crystalline silicon by the known technique for fabricating a CMOS (i.e., Complementary MOS) integreated circuit.” [‘312 Reference, Col. 2:34-38]

Appendix D17

Defendants and Counterclaimants' Invalidity Contentions

Advanced Micro Devices, Inc., et al., v. Samsung Electronics Co., Ltd. et al., Case No. 3:08-CV-0986-SI

U.S. Patent No. 5,559, 990 Invalidity Chart: United States Patent No. 4,788,667 ("'667 Reference")

All asserted claims are anticipated by the '667 Reference and/or are rendered obvious by it, either alone or in combination with other prior art described below and/or listed in Section I of Defendants' and Counterclaimants' Preliminary Invalidity Contentions and/or through modifications described below. Nothing in this invalidity chart should be construed as signifying or suggesting Defendants and Counterclaimants' adoption of or acquiescence in any claim scope and/or claim construction positions taken by Plaintiffs and Counterdefendants in this litigation.

CLAIM	RESPONSE
8. A memory comprising:	Although a preamble is normally not limiting, should this preamble be limiting this element is met by U.S. Patent No. 4,788,667 ("the '667 Reference"). Specifically, the '667 Reference is entitled "Semiconductor Memory Device Having Nibble Mode Function."
a set of consecutively addressed memory locations L1, . . . Ln;	This limitation is met by the '667 Reference, alone or in combination with one or more of the following references, namely the '738 Reference, or the '196 Reference, or the '885 Reference. Specifically, the '667 Reference states that: "Referring to FIG. 9, A.sub.0 to A.sub.n-1 represent input address signals, and .phi..sub.R represents a reset signal which has fallen to the "L" level in the same timing as CAS signal." ['667 Reference, Col. 6:54-56] The '738 Reference states: "A memory comprising a plurality of memory cells, a column decoder, a row decoder, a plurality of shift registers and a multiplexer is provided for addressing the memory cells in a conventional manner or in a high-speed sequential mode." ['738 Reference, Abstract].

CLAIM	RESPONSE
	The '196 Reference states that: "Referring now to FIGS. 2A and 2B, there is shown a block schematic diagram of a pair of RAM arrays 31, 33, each comprising a plurality of individual memory cells of the type illustrated and described above with reference to FIGS. 1A and 1B. Each of these arrays may be configured to store data in a matrix of rows and columns [sic] that is several columns long and several rows deep (e.g. 72X128). The columns and rows of memory cells in each array are connected to decoders for writing and reading data into and out of selected memory cells in the arrays. Specifically, the write column decoders 35, 37 are connected to the dual arrays to address selected columns of memory cells, and the write row decoders and drivers 39, 41 are connected to the dual arrays to address selected rows of memory cells. Similarly, the read column decoders 45,47 are connected to the dual arrays to address selected columns of memory cells , and the read row decoders and drivers 49, 51 are connected to the dual arrays to address selected rows." ['196 Reference, Col. 3:11-29; See also FIGS 1A, 1B, 2A] The '885 Reference states: "Fig. 1 shows the basic elements of an electrically erasable programmable read only memory (EEPROM) device. The device includes an EEPROM array 2 which is divided into 256 storage registers of 16 bits each." ['885 Reference, Col. 3:44-48; *see also* Figs. 1 and 2].
a plurality of sense amplifier circuits for amplifying contents of said memory locations; and	This element is met in the '667 Reference. Specifically, the '667 Reference states that: "Referring to FIG. 8, the sense amplifiers SB0 to SB3 are activated by the signals SBA and SBB. The signal SBA activates the sense amplifiers SB0

CLAIM	RESPONSE
	and SB1 in the first cell block CB1, and the signal SBB activates the sense amplifiers SB2 and SB3 in the second cell block CB2. The data in these sense amplifiers is output through the output buffers OB0 and OB1 as the output data DT0 and DT1." ['667 Reference, Col. 6:18-25; Fig. 8]
an output for providing output signals from said plurality of sense amplifier circuits,	This element is met in the '667 Reference. Specifically, the '667 Reference states that: "Referring to FIG. 8, the sense amplifiers SB0 to SB3 are activated by the signals SBA and SBB. The signal SBA activates the sense amplifiers SB0 and SB1 in the first cell block CB1, and the signal SBB activates the sense amplifiers SB2 and SB3 in the second cell block CB2. The data in these sense amplifiers is output through the output buffers OB0 and OB1 as the output data DT0 and DT1." ['667 Reference, Col. 6:18-25; Fig. 8]
wherein said memory has a burst mode operation for receiving an address and reading out to said output, in response to said address, any given number of memory locations in the sequence of consecutive addresses with wrap around so that the next location, if any, to be read out after said location Ln is said location L1, such that during said operation while the contents of any location L to be read out other than the last location to be read out are being transferred from said plurality of sense amplifier circuits to said output, the contents of another location to be read out after said location L are being provided to said plurality of sense amplifier circuits for amplification and subsequent transfer to said output,	This limitation is met by the '667 Reference, alone or in combination with one or more of the following references: (a) any of the admitted prior art identified in the '990 Patent, or the '738 Reference, or the '196 Reference, and (b) the '885 Reference or the '631 Reference. The '990 patent admits that burst mode is prior art: "When a memory is read sequentially (that is, consecutive read access memory locations at consecutive addresses), the memory access can be made faster by reading from the array several consecutive locations simultaneously. Such a "burst mode" access is provided by memory 202 of FIG. 2." ['990 patent, Background of the Invention, Col. 1:36-41.]

CLAIM	RESPONSE
and	The '738 Reference states: "In the sequential mode, the decoders of the memory are used in a conventional manner for decoding the address of the first cell to be accessed in a predetermined sequence of cells and thereafter, the shift registers are used for addressing the remaining cells in the sequence." ['738 Reference, Col. 1:56-61] "At the same time that the column shift register accessing the last column of cells in each of the sets is shifted to access the first column of cells in that set, the row shift register is also shifted to access the cells in another row of the cells in that set." ['738 Reference, Col. 2:14-18] "In response to the first clock pulse CK shown in FIG. 2 at 88, the contents of Cell 10 are transferred from the register 11 to the data output line 98, the flip-flop circuit 10 is activated to switch the multiplexer 9 to couple the second input R to the output line 80 and a clock pulse CKL is generated on the line 95, causing the output Y2 of the shift register 4 to go low and the output Y4 of the shift register 4 to go high, as shown at 100 and 101 of FIG. 2." ['738 Reference, Col. 4:60-68] "When the last cell in a row of the first set, e.g. cell 14, is deselected by the output Y6 of the shift register 4 going from a high to a low as shown at 105 of FIG. 2, a shift pulse is generated on the line 54 for shifting the output of shift register 6 from row X1L to row X2L as shown at 106 and 107 of FIG. 2. Similarly, when cell 15 in row X1R of set 20 is deselected by output line Y7 going low as shown at 107, the transition on line 59 causes the shift register 7 to shift from row X1R to row X2R, as shown at 108 and 109 of FIG. 2." ['738 Reference, Col. 5:15-25] The '196 Reference states that:

CLAIM	RESPONSE
	"In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit lines in the other array are being precharged. Thus, as data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit lines in that array will already have been initialized." ['196 Reference, Col. 2:60-67] "In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and settling transient signals) in preparation for the next access form such other array. Therefore, precharging times for one array overlap the time for performing read or write operation in the other array, and therefore do not limit operating speed." ['196 Reference, Col. 3:41-47] The '885 Reference states: "After the last memory address is reached, the access automatically rolls over to the first address." ['885 Reference, Col. 3:1-3] "A method as in claim 5 wherein the sequence of incremented addresses wraps around when the address of the Nth register is reached such that all N registers in the array are read." ['885 Reference, Col. 7:45-48] The '631 Reference states that: "The above-described method is accomplished by utilizing two pieces of information, which are placed on the bus (23) by the GDP: the data word's offset and the number of words requested. The data word's offset in the cache line is derived from address bits 2 and 3 (00=word 1, 01=word 2, 10=word 3, and 11=word 4). The number of words being

CLAIM	RESPONSE
	requested is obtained from the size bits 0 and 1 (00=1 word, 01=2 words, 10=3 words, and 11=4 words). Using these two pieces of information, the following algorithm is executed: FIRST WORD ACCESSED = PROCESSOR WORD ADDRESS + SIZE +1 The 1 is added to the size in order to yield the correct offset. For example, if the GDP requests two words at offset 01 in a four-word line, it is converted to a wraparound request of four words to memory starting at word four [offset (01) + word count (01) + 1 = 11]." ['631 Reference, Col. 3:46-65] See, '631 Reference, Table II:

CLAIM	RESPONSE
	TABLE II WORD / ACCESS ORDER 1 . k − 1 k (Requested words: k … n) . . n (last) n + 1 (first) . . . m See also, '631 Reference, Abstract, Table I, Fig. 3.
wherein said memory further comprises a control circuit for selectively enabling said sense amplifier circuits so that said control circuit enables a sense amplifier circuit whose output signals are being transferred to the output of said memory but said control circuit does not enable all said sense amplifier circuits at the same time.	This element is met by the '667 Reference. "Referring to FIG. 8, the sense amplifiers SB0 to SB3 are activated by the signals SBA and SBB. The signal SBA activates the sense amplifiers SB0 and SB1 in the first cell block CB1, and the signal SBB activates the sense amplifiers SB2 and SB3 in the second cell block CB2. The data in these sense amplifiers is output through the output buffers OB0 and OB1 as the output data DT0 and DT1." ['667 Reference, Col. 6:18-25; Fig. 8] "Each output of the sense amplifiers SB0 to SB3 is transferred to the common buses CBL and CBL through the transistor TR.sub.a. Accordingly, the data in the first cell block CB1, i.e, the data in the sense

CLAIM	RESPONSE
	amplifiers SB0 and SB1, is output to the data buses CBL and CBL in response to the switching of the signals SBA and SBB. As mentioned above, the signals SBA and SBB are generated from the circuits 4A and 4B through the buffers 6A and 6B, as shown in FIG. 6. The column decoder CD' is explained in detail in FIG. 9." ['667 Reference, Col. 6:44-53] *See also*, claim 1.
9. The memory of claim 8 wherein, during said operation, said control circuit enables at the same time only:	
(1) the sense amplifier circuit whose output signals are being transferred to said output of said memory, and	This element is met by the '667 Reference. "Referring to FIG. 8, the sense amplifiers SB0 to SB3 are activated by the signals SBA and SBB. The signal SBA activates the sense amplifiers SB0 and SB1 in the first cell block CB1, and the signal SBB activates the sense amplifiers SB2 and SB3 in the second cell block CB2. The data in these sense amplifiers is output through the output buffers OB0 and OB1 as the output data DT0 and DT1." [Col. 6:18-25; Fig. 8] "Each output of the sense amplifiers SB0 to SB3 is transferred to the common buses CBL and CBL through the transistor TR.sub.a. Accordingly, the data in the first cell block CB1, i.e, the data in the sense amplifiers SB0 and SB1, is output to the data buses CBL and CBL in response to the switching of the signals SBA and SBB. As mentioned above, the signals SBA and SBB are generated from the circuits 4A and 4B through the buffers 6A and 6B, as shown in FIG. 6. The column decoder CD' is explained in detail in FIG. 9." [Col. 6:44-53]

CLAIM	RESPONSE
	See also, claim 1.
(2) a predetermined number of other sense amplifier circuits whose output signals will be transferred next to said output of said memory if said operation continues sufficiently long.	This element is met by the '667 Reference. "Referring to FIG. 8, the sense amplifiers SB0 to SB3 are activated by the signals SBA and SBB. The signal SBA activates the sense amplifiers SB0 and SB1 in the first cell block CB1, and the signal SBB activates the sense amplifiers SB2 and SB3 in the second cell block CB2. The data in these sense amplifiers is output through the output buffers OB0 and OB1 as the output data DT0 and DT1." [Col. 6:18-25; Fig. 8] "Each output of the sense amplifiers SB0 to SB3 is transferred to the common buses CBL and CBL through the transistor TR.sub.a. Accordingly, the data in the first cell block CB1, i.e, the data in the sense amplifiers SB0 and SB1, is output to the data buses CBL and CBL in response to the switching of the signals SBA and SBB. As mentioned above, the signals SBA and SBB are generated from the circuits 4A and 4B through the buffers 6A and 6B, as shown in FIG. 6. The column decoder CD' is explained in detail in FIG. 9." [Col. 6:44-53] *See also*, claim 1.
14. The memory of claim 8 wherein said memory is fabricated in an integrated circuit.	This element is met by the '667 Reference alone or in combination with any of the '754 Reference or the '199 Reference, or U.S. Patent No. 4,899,312 ("the '312 Reference"). The '667 Reference is titled "Semiconductor Memory Device Having Nibble Mode Function." Further, it was well known in the art to fabricate memories as an integrated circuit and a person of ordinary skill would have know that the memory device shown in the '667 Reference could be

CLAIM	RESPONSE
	fabricated in an integrated circuit. The '754 Reference states: "The present invention relates to a semiconductor dynamic memory device. Mass-production of 64K bit dynamic type random access memory devices (DRAMs) has been enabled by the recent development of semiconductor memory devices of high packing density. Furthermore, a 256K bit DRAM has been developed." ['754 Reference, Page 2:1-4] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer." ['199 Reference, Col. 1:13-16] The '312 Reference states: "The individual circuit elements constructing the RAM of the present embodiment are formed on a semiconductor substrate such as a piece of single-crystalline silicon by the known technique for fabricating a CMOS (i.e., Complementary MOS) integreated circuit." ['312 Reference, Col. 2:34-38]