EXHIBIT 1

E1-E5

Appendix E1
Defendants and Counterclaimants' Invalidity Contentions
Advanced Micro Devices, Inc., et al., v. Samsung Electronics Co., Ltd., et al., Case No. 3:08-CV-0986-SI

U.S. Patent No. 5,377,200 Invalidity Chart: IEEE Standard 1149.1-1990 ("IEEE 1149.1")

All asserted claims are anticipated by IEEE 1149.1 and/or are rendered obvious by it, either alone or in combination with other prior art described below and/or listed in Section I of Defendants' and Counterclaimants' Preliminary Invalidity Contentions and/or through modifications described below. Nothing in this invalidity chart should be construed as signifying or suggesting Defendants and Counterclaimants' adoption of or acquiescence in any claim scope and/or claim construction positions taken by Plaintiffs and Counterdefendants in this litigation.

U.S. Patent No. 5,377,200	
Claim 1	
Claim limitation	**Prior Art**
1. A configuration register for controlling a logic testing circuit, said logic testing circuit being coupled to a logic module for testing the integrity of said logic module, said logic testing circuit having a normal state and a low power state, said configuration register comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, IEEE 1149.1 discloses this limitation. *See, e.g.*, IEEE 1149.1 at Figs. 1-1 and 1-2; *see, e.g., id.* at 3 ("Figure 1-1 illustrates an example implementation for a boundary-scan cell that could be used for an input or output connection to an integrated circuit. Dependent on the control signals applied to the multiplexers, data can either be loaded into the scan register from the Signal-in port (e.g., the input pin), or driven from the register through the Signalout port of the cell (e.g., into the core of the component design)."); *see, e.g., id.* at 4 ("The boundary-scan cells for the pins of a component are interconnected so as to form a shift-register chain around the border of the design, and this path is provided with serial input and output connections and appropriate clock and control signals. Within a product assembled from several integrated circuits the boundary-scan registers for the individual components could be connected in series to form a single path through the complete design, as illustrated in Figure 1-2. Alternatively, a board design could contain several independent boundary-scan paths."); *see, e.g., id.* 5 ("Design-for-test features such as these can be accessed and controlled using the data path between the serial test data pins of the TAP defined by this standard. Instructions that cause internal reconfiguration of the component's system logic such that the test operation is enabled may be shifted into the component through the TAP."); *see, e.g., id.* at Figs. 5-7 and 7-2 (disclosing a state in which the boundary scan cells are disabled, and therefore in a low power state).
a key input disposed to receive a key signal;	*See, e.g., id.* at Fig. 5-1; *see, e.g., id.* at 10 ("The signal received at TMS is decoded by the TAP controller to control test operations."); *see, e.g., id.* at 18 ("The TAP controller is a synchronous finite state machine that responds to changes at the TMS and TCK signals of the TAP and controls the sequence of operations of the circuitry defined by this standard."); *see, e.g., id.* at 18 ("The TAP controller is a synchronous finite state machine that responds to changes at the TMS and TCK signals of the TAP and controls the sequence of

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	operations of the circuitry defined by this standard."); *see, e.g., id.* ("NOTE – The value shown adjacent to each state transition in this figure represents the signal present at TMS at t he time of a rising edge at TCK.")
a reset input disposed to receive a reset signal;	*See, e.g., id.* at 12 ("The optional TRST* input provides for asynchronous initialization of the TAP controller (see 5.3).").
an output coupled to said logic testing circuit;	*See, e.g., id.* at 11 ("TDO is the serial output for test instructions and data from the test logic defined in this standard."); *see, e.g., id.* at Fig. 5-5.
a key logic circuit coupled to said key input, said reset input, and said output, said key logic circuit generating to said logic testing circuit, through said output, a control signal responsive to said key signal and said reset signal;	*See, e.g., id.* at 18 ("The TAP controller is a synchronous finite state machine that responds to changes at the TMS and TCK signals of the TAP and controls the sequence of operations of the circuitry defined by this standard.")
wherein said control signal drives said logic testing circuit to said low power state when said reset input is triggered by said reset signal; and	*See, e.g., id.* at Fig. 5-1 and related text at pp. 18-23; *see, e.g., id.* at 19 ("The test logic is disabled so that normal operation of the on-chip system logic (i.e., in response to stimuli received through the system pins only) can continue unhindered. This is achieved by initializing the instruction register to contain the *IDCODE* instruction or, if the optional device identification register is not provided, the BYPASS instruction (see 6.2). No matter what the original state of the controller, it will enter *Test-Logic-Reset* when TMS is held high for at least five rising edges of TCK. The controller remains in this state while TMS is high."); *see, e.g., id.* ("Note that the TAP controller will also be forced to the Test-Logic-Reset controller state by applying a low logic level at TRST*, if such is provided, or at power-up (see 5.3)."); *see, e.g., id.* at Figs. 5-7 and 7-2.
wherein said control signal drives said logic testing circuit to said normal state when said key signal matches a predetermined data pattern.	See, e.g., id. at Fig. 5-1 and related text at pp. 18-23; *see, e.g., id.* at 20 ("[A]ctivity in selected test logic occurs only when certain instructions are present. For example, the RUNBIST instruction causes a self-test of the on-chip system logic to execute in this state (see 7.9).")

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Claim 2	
Claim limitation	**Prior Art**
2. The configuration register of claim 1 wherein said control signal is a clock signal when said key signal matches said predetermined pattern, and wherein said output is coupled to a clock port of said logic testing circuit.	*See, e.g., id.* at Figs. 5-5 and 10-18; *see, e.g., id.* at 16 ("The TAP controller. This receives TCK and interprets the signals on TMS. The TAP controller generates clock or control signals or both as required for the instruction and test data registers and for other parts of the architecture."); *see, e.g., id.* at 27 ("Note also that, while the ShiftDR and ClockDR signals may be broadcast to all test data registers, distribution of the UpdateDR control signal will be controlled according to the instruction held in the instruction register such that the signal is fed only to the test data register that is selected as the serial path between TDI and TDO."); *see, e.g., id.* at 39 ("Like all the cells shown in this standard, that shown in Figure 7-2 is designed to respond to the ClockDR, ShiftDR, and UpdateDR signals generated by the example TAP controller implementation shown in Figures 5-5 and 5-6.").
Claim 3	
Claim limitation	**Prior Art**
3. The configuration register of claim 2 further comprising a clock input coupled to a clock signal source, said clock signal being generated responsive to a signal generated by said clock signal source.	*See, e.g., id.* at 9 ("The TAP shall include the following connections (defined in 3.3, 3.5, 3.6.2, and 3.7.2): TCK, TMS, TDI, and TDO."); *see, e.g., id.* ("TCK provides the clock for the test logic defined by this standard."). One of skill in the art would know that a circuit arrangement with a clock has a clock signal source coupled to a clock input. IEEE 1149.1 discloses a circuit arrangement with a clock. *See, e.g., id.* at 8 ("TCK: The Test Clock input pin contained in the TAP defined by this standard (see 5.3.2).").
Claim 5	
Claim limitation	**Prior Art**
5. The configuration register of claim 3 further comprising a NOR gate, wherein said key logic circuit and said clock input are coupled to	*See, e.g., id.* at Fig. 5-7 (disclosing that State gates TCK to generate outputs such as ClockDR). One of skill in the art would know to use any particular logic gate appropriate for an application.

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said output through said NOR gate.	
Claim 6	
Claim limitation	**Prior Art**
6. A circuit arrangement comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, IEEE 1149.1 discloses this limitation. *See, e.g.*, IEEE 1149.1 at Figs. 1-1 and 1-2..
a logic component having a logic module and a built-in logic testing circuit, said logic testing circuit being coupled to said logic module for testing the integrity of said logic module and having a normal state and a low power state, wherein said logic testing circuit may be disabled to save power when testing operations are not being performed;	*See, e.g.*, IEEE 1149.1 at Figs. 1-1 and 1-2; *see, e.g., id.* at 3 ("Figure 1-1 illustrates an example implementation for a boundary-scan cell that could be used for an input or output connection to an integrated circuit. Dependent on the control signals applied to the multiplexers, data can either be loaded into the scan register from the Signal-in port (e.g., the input pin), or driven from the register through the Signalout port of the cell (e.g., into the core of the component design)."); *see, e.g., id.* at 4 ("The boundary-scan cells for the pins of a component are interconnected so as to form a shift-register chain around the border of the design, and this path is provided with serial input and output connections and appropriate clock and control signals. Within a product assembled from several integrated circuits the boundary-scan registers for the individual components could be connected in series to form a single path through the complete design, as illustrated in Figure 1-2. Alternatively, a board design could contain several independent boundary-scan paths."); *see, e.g., id.* 5 ("Design-for-test features such as these can be accessed and controlled using the data path between the serial test data pins of the TAP defined by this standard. Instructions that cause internal reconfiguration of the component's system logic such that the test operation is enabled may be shifted into the component through the TAP."); *see, e.g., id.* at Figs. 5-7 and 7-2 (disclosing a state in which the boundary scan cells are disabled, and therefore in a low power state).
a configuration register for controlling said logic testing circuit, said configuration register comprising	see previous limitation
a key input disposed to receive a key signal,	*See, e.g., id.* at Fig. 5-1; *see, e.g., id.* at 10 ("The signal received at TMS is decoded by the TAP controller to control test operations."); *see, e.g., id.* at 18 ("The TAP controller is a synchronous finite state machine that responds to changes at the TMS and TCK signals of the TAP and controls the sequence of operations of the

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	circuitry defined by this standard."); *see, e.g., id.* at 18 ("The TAP controller is a synchronous finite state machine that responds to changes at the TMS and TCK signals of the TAP and controls the sequence of operations of the circuitry defined by this standard."); *see, e.g., id.* ("NOTE – The value shown adjacent to each state transition in this figure represents the signal present at TMS at t he time of a rising edge at TCK.")
a reset input disposed to receive a reset signal,	*See, e.g., id.* at 12 ("The optional TRST* input provides for asynchronous initialization of the TAP controller (see 5.3).").
an output coupled to said logic testing circuit, and	*See, e.g., id.* at 11 ("TDO is the serial output for test instructions and data from the test logic defined in this standard.")
a key logic circuit coupled to said key input, said reset input, and said output, said key logic circuit generating to said logic testing circuit, through said output, a control signal responsive to said key signal and said reset signal;	*See, e.g., id.* at 18 ("The TAP controller is a synchronous finite state machine that responds to changes at the TMS and TCK signals of the TAP and controls the sequence of operations of the circuitry defined by this standard.")
wherein said control signal drives said logic testing circuit to said low power state when said reset input is triggered by said reset signal; and	*See, e.g., id.* at Fig. 5-1 and related text at pp. 18-23; *see, e.g., id.* at 19 ("The test logic is disabled so that normal operation of the on-chip system logic (i.e., in response to stimuli received through the system pins only) can continue unhindered. This is achieved by initializing the instruction register to contain the *IDCODE* instruction or, if the optional device identification register is not provided, the BYPASS instruction (see 6.2). No matter what the original state of the controller, it will enter *Test-Logic-Reset* when TMS is held high for at least five rising edges of TCK. The controller remains in this state while TMS is high."); *see, e.g., id.* ("Note that the TAP controller will also be forced to the Test-Logic-Reset controller state by applying a low logic level at TRST*, if such is provided, or at power-up (see 5.3)."); *see, e.g., id.* at Figs. 5-7 and 7-2.
wherein said control signal drives said logic testing circuit to said normal state when said key signal matches a predetermined data	See, e.g., id. at Fig. 5-1 and related text at pp. 18-23; *see, e.g., id.* at 20 ("[A]ctivity in selected test logic occurs only when certain instructions are present. For example, the RUNBIST instruction causes a self-test of the on-chip system logic to execute in this state (see 7.9).")

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pattern.	
Claim 7	
Claim limitation	**Prior Art**
7. The arrangement of claim 6 wherein said control signal is a clock signal when said key signal matches said predetermined data pattern, and wherein said output is coupled to a clock port of said logic testing circuit.	*See, e.g., id.* at Figs. 5-5 and 10-18; *see, e.g., id.* at 16 ("The TAP controller. This receives TCK and interprets the signals on TMS. The TAP controller generates clock or control signals or both as required for the instruction and test data registers and for other parts of the architecture."); *see, e.g., id.* at 27 ("Note also that, while the ShiftDR and ClockDR signals may be broadcast to all test data registers, distribution of the UpdateDR control signal will be controlled according to the instruction held in the instruction register such that the signal is fed only to the test data register that is selected as the serial path between TDI and TDO."); *see, e.g., id.* at 39 ("Like all the cells shown in this standard, that shown in Figure 7-2 is designed to respond to the ClockDR, ShiftDR, and UpdateDR signals generated by the example TAP controller implementation shown in Figures 5-5 and 5-6.").
Claim 8	
Claim limitation	**Prior Art**
8. The arrangement of claim 7 further comprising a clock signal source, wherein said configuration register further comprises a clock input disposed to receive said clock signal from said clock signal source.	*See, e.g., id.* at 9 ("The TAP shall include the following connections (defined in 3.3, 3.5, 3.6.2, and 3.7.2): TCK, TMS, TDI, and TDO."); *see, e.g., id.* ("TCK provides the clock for the test logic defined by this standard."). One of skill in the art would know that a circuit arrangement with a clock has a clock signal source coupled to a clock input. IEEE 1149.1 discloses a circuit arrangement with a clock. *See, e.g., id.* at 8 ("TCK: The Test Clock input pin contained in the TAP defined by this standard (see 5.3.2).").
Claim 11	
Claim limitation	**Prior Art**
11. The arrangement of claim 6 wherein said logic testing circuit has a clock port and wherein the state of said logic testing circuit is	*See, e.g., id.* at Fig. 1-1; *see, e.g.. id.* at 3 ("Figure 1-1 illustrates an example implementation for a boundary-scan cell that could be used for an input or output connection to an integrated circuit. Dependent on the control signals applied to the multiplexers, data can either be loaded into the scan register from the Signal-in port (e.g., the input pin), or driven from the register through the Signalout port of the cell (e.g., into the core of the

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responsive to a signal at said clock port.	component design). As will be discussed in detail in Chapter 10, the second flip-flop (controlled by input Clock B) is provided to ensure that the signals driven out of the cell in the latter case are held while new data is shifted into the cell using input Clock A. This flip-flop is not required in all cases, but is included in Figure 1-1 to simplify the discussion."); *see, e.g., id.* at Fig. 10-18; *see, e.g., id.* at 39 ("Like all the cells shown in this standard, that shown in Figure 7-2 is designed to respond to the ClockDR, ShiftDR, and UpdateDR signals generated by the example TAP controller implementation shown in Figures 5-5 and 5-6.")..
Claim 12	
Claim limitation	**Prior Art**
12. The arrangement of claim 11 wherein said output is coupled to said clock port, said logic testing circuit is driven to said low power state when a LOW is applied to a clock port, and wherein said control signal is LOW when said reset input is triggered by said reset signal.	*See, e.g., id.* at Fig. 5-1 and related text at pp. 18-23; *see, e.g., id.* at 39 ("Like all the cells shown in this standard, that shown in Figure 7-2 is designed to respond to the ClockDR, ShiftDR, and UpdateDR signals generated by the example TAP controller implementation shown in Figures 5-5 and 5-6."); *see, e.g., id.* at Figs. 5-5 and 10-18. One of skill in the art would know to use any signal polarity appropriate for an application.
Claim 13	
Claim limitation	**Prior Art**
13. The arrangement of claim 11 wherein said output is coupled to said clock port, said logic testing circuit is driven to said normal state when a clock signal is applied to a clock port, and wherein said control signal is a clock signal when said key signal matches said predetermined data pattern.	*See, e.g., id.* at Fig. 5-1 and related text at pp. 18-23; *see, e.g., id.* at 20 ("[A]ctivity in selected test logic occurs only when certain instructions are present. For example, the RUNBIST instruction causes a self-test of the on-chip system logic to execute in this state (see 7.9)."); *see, e.g., id.* at Figs. 5-5 and 10-18; *see, e.g., id.* at 16 ("The TAP controller. This receives TCK and interprets the signals on TMS. The TAP controller generates clock or control signals or both as required for the instruction and test data registers and for other parts of the architecture."); *see, e.g., id.* at 27 ("Note also that, while the ShiftDR and ClockDR signals may be broadcast to all test data registers, distribution of the UpdateDR control signal will be controlled according to the instruction held in the instruction register such that the signal is fed only to the test data register that is selected as the serial path between TDI and TDO."); *see, e.g., id.* at 39 ("Like all the cells shown in this standard, that shown in Figure 7-2 is designed to respond to the ClockDR, ShiftDR, and UpdateDR signals generated by the

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	example TAP controller implementation shown in Figures 5-5 and 5-6.").
Claim 15	
Claim limitation	**Prior Art**
15. A circuit arrangement comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, IEEE 1149.1 discloses this limitation. *See, e.g.*, IEEE 1149.1 at Figs. 1-1 and 1-2..
a logic component having a logic module and a built-in logic testing circuit for testing the integrity of said logic module, said logic testing circuit being coupled to said logic module and having a normal state and a low power state, said logic testing circuit further having a clock port, wherein the state of said logic testing circuit is responsive to a control signal applied at said clock port, wherein said logic testing circuit may be disabled to save power when testing operations are not being performed;	*See, e.g.*, IEEE 1149.1 at Figs. 1-1 and 1-2; *see, e.g., id.* at 3 ("Figure 1-1 illustrates an example implementation for a boundary-scan cell that could be used for an input or output connection to an integrated circuit. Dependent on the control signals applied to the multiplexers, data can either be loaded into the scan register from the Signal-in port (e.g., the input pin), or driven from the register through the Signalout port of the cell (e.g., into the core of the component design)."); *see, e.g., id.* at 4 ("The boundary-scan cells for the pins of a component are interconnected so as to form a shift-register chain around the border of the design, and this path is provided with serial input and output connections and appropriate clock and control signals. Within a product assembled from several integrated circuits the boundary-scan registers for the individual components could be connected in series to form a single path through the complete design, as illustrated in Figure 1-2. Alternatively, a board design could contain several independent boundary-scan paths."); *see, e.g., id.* 5 ("Design-for-test features such as these can be accessed and controlled using the data path between the serial test data pins of the TAP defined by this standard. Instructions that cause internal reconfiguration of the component's system logic such that the test operation is enabled may be shifted into the component through the TAP."); *see, e.g., id.* at Figs. 5-7 and 7-2 (disclosing a state in which the boundary scan cells are disabled, and therefore in a low power state).
a configuration register for controlling said logic testing circuit, said configuration register comprising	*See, e.g.*, IEEE 1149.1 at Figs. 1-1 and 1-2; *see, e.g., id.* at 3 ("Figure 1-1 illustrates an example implementation for a boundary-scan cell that could be used for an input or output connection to an integrated circuit. Dependent on the control signals applied to the multiplexers, data can either be loaded into the scan register from the Signal-in port (e.g., the input pin), or driven from the register through the Signalout port of the cell (e.g., into the core of the component design)."); *see, e.g., id.* at 4 ("The boundary-scan cells for the pins of a component are interconnected so as to form a shift-register chain around the border of the design, and this path is provided with serial input and output connections and appropriate clock and control signals. Within a product assembled from several integrated circuits the boundary-scan registers for the individual components

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	could be connected in series to form a single path through the complete design, as illustrated in Figure 1-2. Alternatively, a board design could contain several independent boundary-scan paths.").
a key input disposed to receive a key signal,	*See, e.g., id.* at Fig. 5-1; *see, e.g., id.* at 10 ("The signal received at TMS is decoded by the TAP controller to control test operations."); *see, e.g., id.* at 18 ("The TAP controller is a synchronous finite state machine that responds to changes at the TMS and TCK signals of the TAP and controls the sequence of operations of the circuitry defined by this standard."); *see, e.g., id.* at 18 ("The TAP controller is a synchronous finite state machine that responds to changes at the TMS and TCK signals of the TAP and controls the sequence of operations of the circuitry defined by this standard."); *see, e.g., id.* ("NOTE – The value shown adjacent to each state transition in this figure represents the signal present at TMS at t he time of a rising edge at TCK.")
a reset input disposed to receive a reset signal,	*See, e.g., id.* at 12 ("The optional TRST* input provides for asynchronous initialization of the TAP controller (see 5.3).").
a clock input disposed to receive a clock signal,	*See, e.g., id.* at 9 ("The TAP shall include the following connections (defined in 3.3, 3.5, 3.6.2, and 3.7.2): TCK, TMS, TDI, and TDO."); *see, e.g., id.* ("TCK provides the clock for the test logic defined by this standard.").
a signal output coupled to the clock port of said logic testing circuit,	*See, e.g., id.* at Figs. 5-5 and 10-18; *see, e.g., id.* at 16 ("The TAP controller. This receives TCK and interprets the signals on TMS. The TAP controller generates clock or control signals or both as required for the instruction and test data registers and for other parts of the architecture."); *see, e.g., id.* at 27 ("Note also that, while the ShiftDR and ClockDR signals may be broadcast to all test data registers, distribution of the UpdateDR control signal will be controlled according to the instruction held in the instruction register such that the signal is fed only to the test data register that is selected as the serial path between TDI and TDO."); *see, e.g., id.* at 39 ("Like all the cells shown in this standard, that shown in Figure 7-2 is designed to respond to the ClockDR, ShiftDR, and UpdateDR signals generated by the example TAP controller implementation shown in Figures 5-5 and 5-6.").
a key logic circuit coupled to said key input and said reset input, wherein said key logic circuit generates a mode signal responsive	*See, e.g., id.* at 18 ("The TAP controller is a synchronous finite state machine that responds to changes at the TMS and TCK signals of the TAP and controls the sequence of operations of the circuitry defined by this standard.").

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to said key signal and said reset signal,	
wherein said mode signal is a disable signal when said reset input is triggered by said reset signal, and wherein said mode signal is an enable signal when said key signal matches a predetermined data pattern, and	*See, e.g., id.* at Fig. 5-1 and related text at pp. 18-23; *see, e.g., id.* at 19 ("The test logic is disabled so that normal operation of the on-chip system logic (i.e., in response to stimuli received through the system pins only) can continue unhindered. This is achieved by initializing the instruction register to contain the *IDCODE* instruction or, if the optional device identification register is not provided, the BYPASS instruction (see 6.2). No matter what the original state of the controller, it will enter *Test-Logic-Reset* when TMS is held high for at least five rising edges of TCK. The controller remains in this state while TMS is high."); *see, e.g., id.* ("Note that the TAP controller will also be forced to the Test-Logic-Reset controller state by applying a low logic level at TRST*, if such is provided, or at power-up (see 5.3)."); *see, e.g., id.* at Figs. 5-7 and 7-2; *see, e.g., id.* at 20 ("[A]ctivity in selected test logic occurs only when certain instructions are present. For example, the RUNBIST instruction causes a self-test of the on-chip system logic to execute in this state (see 7.9).").
a logic gate having inputs coupled to said clock input and said key logic circuit and an output coupled to said signal output, said logic gate generating at said signal output said control signal responsive to said clock signal and said mode signal; and	*See, e.g., id.* at Fig. 5-7.
wherein said control signal drives said logic testing circuit to a low power state when said mode signal is said disable signal, and wherein said control signal drives said logic testing circuit to said normal state when said mode signal is said enable signal.	*See, e.g., id.* at 19 ("Note that the TAP controller will also be forced to the Test-Logic-Reset controller state by applying a low logic level at TRST*, if such is provided, or at power-up (see 5.3)."); *see, e.g., id.* at Figs. 5-7 and 7-2.

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Claim 16	
Claim limitation	**Prior Art**
16. The arrangement of claim 15 wherein said logic gate is a NOR gate, said disable signal is a logical HIGH, and said enable signal is a logic LOW.	*See, e.g., id.* at Fig. 5-7. One of skill in the art would know to use any particular logic gate appropriate for an application.
Claim 17	
Claim limitation	**Prior Art**
17. The arrangement of claim 15 further comprising a clock signal source coupled to said clock input, said clock signal source generating said clock signal.	One of skill in the art would know that a circuit arrangement with a clock has a clock signal source coupled to a clock input. IEEE 1149.1 discloses a circuit arrangement with a clock. *See, e.g., id.* at 8 ("TCK: The Test Clock input pin contained in the TAP defined by this standard (see 5.3.2).").
Claim 19	
Claim limitation	**Prior Art**
19. The arrangement of claim 15 wherein said key input is a multi-bit digital input and wherein said predetermined data pattern is determined by the configuration of the components of said key logic circuit.	One of skill in the art would know that a key input need not be limited to a single bit. *See, e.g.*, IEEE 1149.1 at 110 (disclosing multi-bit arrangements for an identity code); *see, e.g., id.* at 111 (multi-bit part number code); *see, e.g., id.* (multi-bit version code).

Appendix E2
Defendants and Counterclaimants' Invalidity Contentions
Advanced Micro Devices, Inc., et al., v. Samsung Electronics Co., Ltd., et al., Case No. 3:08-CV-0986-SI

U.S. Patent No. 5,377,200 Invalidity Chart: U.S. Patent No. 5,029,166 ("'166 patent")

All asserted claims are anticipated by the '166 patent and/or are rendered obvious by it, either alone or in combination with other prior art described below and/or listed in Section I of Defendants' and Counterclaimants' Preliminary Invalidity Contentions and/or through modifications described below. Nothing in this invalidity chart should be construed as signifying or suggesting Defendants and Counterclaimants' adoption of or acquiescence in any claim scope and/or claim construction positions taken by Plaintiffs and Counterdefendants in this litigation.

To the extent a feature of the claims may not be disclosed or suggested by the '166 patent alone, one of skill in the art would know to consider IEEE Standard 1149.1-1990 ("IEEE 1149.1"), which provides details regarding test access port (TAP) controllers, such as TAP controller 18 in the '166 patent.

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Claim 1	
Claim limitation	**Prior Art**
1. A configuration register for controlling a logic testing circuit, said logic testing circuit being coupled to a logic module for testing the integrity of said logic module, said logic testing circuit having a normal state and a low power state, said configuration register comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, the '166 patent discloses this limitation, either alone or in combination. *See, e.g.*, '166 patent at Fig. 1; *see, e.g., id.* at Abstract ("The test system includes a controller (22) for generating a test signal and for capturing a response signal generated by the associated chain of circuits in response to the test signal. The controller (22) also generates a flow control signal which controls a network (24) that routes the test signals from the controller, or from a first other test system, to the associated chain of circuits (12)."); *see, e.g., id.* at 5:14-18 ("Each active component 12 takes the form of an integrated circuit comprised of an application logic 14 (usually a plurality of interconnected gates (not shown)) which establishes the function of the circuit."); *see, e.g., id.* at 6:5-9 ("The I/O and control BSCs 16 within each integrated circuit 12 are controlled by a test access port (TAP) controller 18 which is responsive to a test mode select (TMS) signal produced by the test system 10 at its TMSi output."); *see also, e.g.*, IEEE 1149.1 at 38 ("When the BYPASS instruction is selected, the operation of the test logic shall have no effect on the operation of the on-chip system logic.").
a key input disposed to receive a key signal;	*See, e.g.*, '166 patent at Fig. 2; *see, e.g., id.* at 9:18-31 ("The interface 42 is coupled to the external test and diagnosis system to receive a chip enable (CE) signal, a register address (RA) signal, a read/write (R/W) signal, a data strobe (DTSB) signal, and a test clock input (TCKIN) signal. The CE signal is comprised of a single binary bit which serves to enable the interface 42 when the bit is at a logic low level. The RA signal comprises a single binary bit which controls the addressing of the latches 44 by the external test and diagnosis

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	system 43. The R/W signal is a single binary bit which indicates whether data is to be written to, or read from, the latch 44. The DTSB signal is a single bit which, when at a logic low level, alerts the interface 42 that valid data is present on the data lines D0-D7.").
a reset input disposed to receive a reset signal;	*See, e.g., id.* at Fig. 2; *see, e.g., id.* at 9:22-24 ("The CE signal is comprised of a single binary bit which serves to enable the interface 42 when the bit is at a logic low level.").
an output coupled to said logic testing circuit;	*See, e.g., id.* at Fig. 2; *see, e.g., id.* at 6:68-7:3 ("Further, the controller 22 generates a test mode (TMS) signal for controlling the TAP controller 18 in each integrated circuit 12"); *see, e.g., id.* at 7:3-7 ("Additionally, the controller 22 generates two other signals, a test clock signal (TCK) for input to each TAP controller 18 to synchronize its operation, and a flow 5 control signal (FC) to control the flow of signals in a reconfigurable network 24.").
a key logic circuit coupled to said key input, said reset input, and said output, said key logic circuit generating to said logic testing circuit, through said output, a control signal responsive to said key signal and said reset signal;	*See, e.g., id.* at Fig. 2 (showing a key logic circuit that outputs TMSi/TCK being a combination of TMS GENERATORS/TCK GENERATOR, coupled via bus 58 to register bank 50, controlled through bus 48 by the interface 42, which has the key input and reset input); *see, e.g., id.* at 13:24-34 ("Referring to FIG. 1, in order for the test system 10 to operate in the multi-ring mode, each of the two bits c1 and c2 of the control signal FC is set by the controller 22 at a logic low level. In this way, the TMS signal and TDo vector produced by the controller 22 pass through the multiplexers 26 and 28, respectively, to the boundary scan chain of circuits 12 while the vector TDi shifted out of the component chain and received at the TDi input of the test system 10 passes to the controller 22.").
wherein said control signal drives said logic testing circuit to said low power state when said reset input is triggered by said reset signal; and	*See, e.g.*, IEEE 1149.1 at 38 ("When the BYPASS instruction is selected, the operation of the test logic shall have no effect on the operation of the on-chip system logic.").
wherein said control signal drives said logic testing circuit to said normal state when said key signal matches a predetermined data	*see, e.g.*, '166 patent at Fig. 2; *see, e.g.*. 9:18-24 ("The interface 42 is coupled to the external test and diagnosis system to receive a chip enable (CE) signal, a register address (RA) signal, a read/write (R/W) signal, a data strobe (DTSB) signal, and a test clock input (TCKIN) signal. The CE signal is comprised of a single binary bit which serves to enable the interface 42 when the bit is at a logic low level.")

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pattern.	
Claim 2	
Claim limitation	**Prior Art**
2. The configuration register of claim 1 wherein said control signal is a clock signal when said key signal matches said predetermined pattern, and wherein said output is coupled to a clock port of said logic testing circuit.	*See, e.g.. id.* at 7:3-6 ("Additionally, the controller 22 generates two other signals, a test clock signal (TCK) for input to each TAP controller 18....").
Claim 3	
Claim limitation	**Prior Art**
3. The configuration register of claim 2 further comprising a clock input coupled to a clock signal source, said clock signal being generated responsive to a signal generated by said clock signal source.	*See, e.g., id.* at Fig. 2; *see, e.g., id.* at 9:18-22 ("The interface 42 is coupled to the external test and diagnosis system to receive a chip enable (CE) signal, a register address (RA) signal, a read/write (R/W) signal, a data strobe (DTSB) signal, and a test clock input (TCKIN) signal."); *see, e.g., id.* at 9:31-33 ("The TCKIN signal is a single binary bit which is time-varying, and it is from this bit that the TCK signal is derived."). One of skill in the art would know that a circuit arrangement with a clock has a clock signal source coupled to a clock input.
Claim 5	
Claim limitation	**Prior Art**
5. The configuration register of claim 3 further comprising a NOR gate, wherein said key logic circuit and said clock input are coupled to	*See, e.g., id.* at 9:66-68 ("The TCK generator 64 takes the form of a programmable divider which divides the TCKIN signal to generate the TCK signal."). One of skill in the art would know to use any particular logic gate appropriate for an application.

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said output through said NOR gate.	
Claim 6	
Claim limitation	**Prior Art**
6. A circuit arrangement comprising:	
a logic component having a logic module and a built-in logic testing circuit, said logic testing circuit being coupled to said logic module for testing the integrity of said logic module and having a normal state and a low power state, wherein said logic testing circuit may be disabled to save power when testing operations are not being performed;	*See, e.g.*, '166 patent at Abstract ("The test system includes a controller (22) for generating a test signal and for capturing a response signal generated by the associated chain of circuits in response to the test signal. The controller (22) also generates a flow control signal which controls a network (24) that routes the test signals from the controller, or from a first other test system, to the associated chain of circuits (12)."); *see, e.g., id.* at 5:14-18 ("Each active component 12 takes the form of an integrated circuit comprised of an application logic 14 (usually a plurality of interconnected gates (not shown)) which establishes the function of the circuit."); *see, e.g., id.* at 6:5-11 ("The I/O and control BSCs 16 within each integrated circuit 12 are controlled by a test access port (TAP) controller 18 which is responsive to a test mode select (TMS) signal produced by the test system 10 at its TMSi output."); *see, e.g., id.* at Fig. 1; *see also, e.g.*, IEEE 1149.1 at 38 ("When the BYPASS instruction is selected, the operation of the test logic shall have no effect on the operation of the on-chip system logic.").
a configuration register for controlling said logic testing circuit, said configuration register comprising	*See* previous limitation.
a key input disposed to receive a key signal,	*See, e.g., id.* at Fig. 2; *see, e.g., id.* at 9:18-31 ("The interface 42 is coupled to the external test and diagnosis system to receive a chip enable (CE) signal, a register address (RA) signal, a read/write (R/W) signal, a data strobe (DTSB) signal, and a test clock input (TCKIN) signal. The CE signal is comprised of a single binary bit which serves to enable the interface 42 when the bit is at a logic low level. The RA signal comprises a single binary bit which controls the addressing of the latches 44 by the external test and diagnosis system 43. The R/W signal is a single binary bit which indicates whether data is to be written to, or read from, the latch 44.

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	The DTSB signal is a single bit which, when at a logic low level, alerts the interface 42 that valid data is present on the data lines D0-D7.").
a reset input disposed to receive a reset signal,	*See, e.g., id.* at Fig. 2; *see, e.g., id.* at 9:22-24 ("The CE signal is comprised of a single binary bit which serves to enable the interface 42 when the bit is at a logic low level.").
an output coupled to said logic testing circuit, and	*See, e.g., id.* at Fig. 2; *see, e.g., id.* at 6:68-7:3 ("Further, the controller 22 generates a test mode (TMS) signal for controlling the TAP controller 18 in each integrated circuit 12"); *see, e.g., id.* at 7:3-7 ("Additionally, the controller 22 generates two other signals, a test clock signal (TCK) for input to each TAP controller 18 to synchronize its operation, and a flow 5 control signal (FC) to control the flow of signals in a reconfigurable network 24.").
a key logic circuit coupled to said key input, said reset input, and said output, said key logic circuit generating to said logic testing circuit, through said output, a control signal responsive to said key signal and said reset signal;	*See, e.g., id.* at Fig. 2 (showing a key logic circuit that outputs TMSi/TCK being a combination of TMS GENERATORS/TCK GENERATOR, coupled via bus 58 to register bank 50, controlled through bus 48 by the interface 42, which has the key input and reset input); *see, e.g., id.* at 13:24-34 ("Referring to FIG. 1, in order for the test system 10 to operate in the multi-ring mode, each of the two bits c1 and c2 of the control signal FC is set by the controller 22 at a logic low level. In this way, the TMS signal and TDo vector produced by the controller 22 pass through the multiplexers 26 and 28, respectively, to the boundary scan chain of circuits 12 while the vector TDi shifted out of the component chain and received at the TDi input of the test system 10 passes to the controller 22.").
wherein said control signal drives said logic testing circuit to said low power state when said reset input is triggered by said reset signal; and	*See also, e.g.*, IEEE 1149.1 at 38 ("When the BYPASS instruction is selected, the operation of the test logic shall have no effect on the operation of the on-chip system logic.").
wherein said control signal drives said logic testing circuit to said normal state when said key signal matches a predetermined data pattern.	*See, e.g.*, '166 patent at Fig. 2; *see, e.g.*. 9:18-24 ("The interface 42 is coupled to the external test and diagnosis system to receive a chip enable (CE) signal, a register address (RA) signal, a read/write (R/W) signal, a data strobe (DTSB) signal, and a test clock input (TCKIN) signal. The CE signal is comprised of a single binary bit which serves to enable the interface 42 when the bit is at a logic low level.")

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Claim 7	
Claim limitation	**Prior Art**
7. The arrangement of claim 6 wherein said control signal is a clock signal when said key signal matches said predetermined data pattern, and wherein said output is coupled to a clock port of said logic testing circuit.	*See, e.g.. id.* at 7:3-6 ("Additionally, the controller 22 generates two other signals, a test clock signal (TCK) for input to each TAP controller 18.").
Claim 8	
Claim limitation	**Prior Art**
8. The arrangement of claim 7 further comprising a clock signal source, wherein said configuration register further comprises a clock input disposed to receive said clock signal from said clock signal source.	*See, e.g., id.* at Fig. 2; *see, e.g., id.* at 9:18-22 ("The interface 42 is coupled to the external test and diagnosis system to receive a chip enable (CE) signal, a register address (RA) signal, a read/write (R/W) signal, a data strobe (DTSB) signal, and a test clock input (TCKIN) signal."); *see, e.g., id.* at 9:31-33 ("The TCKIN signal is a single binary bit which is time-varying, and it is from this bit that the TCK signal is derived."). One of skill in the art would know that a circuit arrangement with a clock has a clock signal source coupled to a clock input
Claim 11	
Claim limitation	**Prior Art**
11. The arrangement of claim 6 wherein said logic testing circuit has a clock port and wherein the state of said logic testing circuit is responsive to a signal at said clock port.	*See, e.g.*, IEEE 1149.1 at 9 ("The TAP shall include the following connections (defined in 3.3, 3.5, 3.6.2, and 3.7.2): TCK, TMS, TDI, and TDO."); *see, e.g., id.* ("TCK provides the clock for the test logic defined by this standard.")

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Claim 12	
Claim limitation	**Prior Art**
12. The arrangement of claim 11 wherein said output is coupled to said clock port, said logic testing circuit is driven to said low power state when a LOW is applied to a clock port, and wherein said control signal is LOW when said reset input is triggered by said reset signal.	*See, e.g.*. '166 patent at 7:3-6 ("Additionally, the controller 22 generates two other signals, a test clock signal (TCK) for input to each TAP controller 18."). One of skill in the art would know to use any signal polarity appropriate for an application.
Claim 13	
Claim limitation	**Prior Art**
13. The arrangement of claim 11 wherein said output is coupled to said clock port, said logic testing circuit is driven to said normal state when a clock signal is applied to a clock port, and wherein said control signal is a clock signal when said key signal matches said predetermined data pattern.	*See, e.g., id.* at Figs. 1-2; *see, e.g., id.* at 7:3-6 ("Additionally, the controller 22 generates two other signals, a test clock signal (TCK) for input to each TAP controller 18...."); *see, e.g.*. 9:18-24 ("The interface 42 is coupled to the external test and diagnosis system to receive a chip enable (CE) signal, a register address (RA) signal, a read/write (R/W) signal, a data strobe (DTSB) signal, and a test clock input (TCKIN) signal. The CE signal is comprised of a single binary bit which serves to enable the interface 42 when the bit is at a logic low level.").
Claim 15	
Claim limitation	**Prior Art**
15. A circuit arrangement comprising:	

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a logic component having a logic module and a built-in logic testing circuit for testing the integrity of said logic module, said logic testing circuit being coupled to said logic module and having a normal state and a low power state, said logic testing circuit further having a clock port, wherein the state of said logic testing circuit is responsive to a control signal applied at said clock port, wherein said logic testing circuit may be disabled to save power when testing operations are not being performed;	*See, e.g.*, '166 patent at Abstract ("The test system includes a controller (22) for generating a test signal and for capturing a response signal generated by the associated chain of circuits in response to the test signal. The controller (22) also generates a flow control signal which controls a network (24) that routes the test signals from the controller, or from a first other test system, to the associated chain of circuits (12)."); *see, e.g., id.* at 5:14-18 ("Each active component 12 takes the form of an integrated circuit comprised of an application logic 14 (usually a plurality of interconnected gates (not shown)) which establishes the function of the circuit."); *see, e.g., id.* at 6:5-11 ("The I/O and control BSCs 16 within each integrated circuit 12 are controlled by a test access port (TAP) controller 18 which is responsive to a test mode select (TMS) signal produced by the test system 10 at its TMSi output."); *see, e.g., id.* at Fig. 1; *see also, e.g.*, IEEE 1149.1 at 38 ("When the BYPASS instruction is selected, the operation of the test logic shall have no effect on the operation of the on-chip system logic.").
a configuration register for controlling said logic testing circuit, said configuration register comprising	*See* previous limitation.
a key input disposed to receive a key signal,	*See, e.g.*, '166 patent at Fig. 2; *see, e.g., id.* at 9:18-31 ("The interface 42 is coupled to the external test and diagnosis system to receive a chip enable (CE) signal, a register address (RA) signal, a read/write (R/W) signal, a data strobe (DTSB) signal, and a test clock input (TCKIN) signal. The CE signal is comprised of a single binary bit which serves to enable the interface 42 when the bit is at a logic low level. The RA signal comprises a single binary bit which controls the addressing of the latches 44 by the external test and diagnosis system 43. The R/W signal is a single binary bit which indicates whether data is to be written to, or read from, the latch 44. The DTSB signal is a single bit which, when at a logic low level, alerts the interface 42 that valid data is present on the data lines D0-D7.").
a reset input disposed to receive a	*See, e.g., id.* at Fig. 2; *see, e.g., id.* at 9:22-24 ("The CE signal is comprised of a single binary bit which serves

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reset signal,	to enable the interface 42 when the bit is at a logic low level.").
a clock input disposed to receive a clock signal,	*See, e.g., id.* at Fig. 2; *see, e.g., id.* at 9:18-22 ("The interface 42 is coupled to the external test and diagnosis system to receive a chip enable (CE) signal, a register address (RA) signal, a read/write (R/W) signal, a data strobe (DTSB) signal, and a test clock input (TCKIN) signal."); *see, e.g., id.* at 9:31-33 ("The TCKIN signal is a single binary bit which is time-varying, and it is from this bit that the TCK signal is derived.").
a signal output coupled to the clock port of said logic testing circuit,	*See, e.g.. id.* at 7:3-6 ("Additionally, the controller 22 generates two other signals, a test clock signal (TCK) for input to each TAP controller 18....").
a key logic circuit coupled to said key input and said reset input, wherein said key logic circuit generates a mode signal responsive to said key signal and said reset signal,	*See, e.g., id.* at Fig. 2 (showing a key logic circuit that outputs TMSi/TCK being a combination of TMS GENERATORS/TCK GENERATOR, coupled via bus 58 to register bank 50, controlled through bus 48 by the interface 42, which has the key input and reset input); *see, e.g., id.* at 13:24-34 ("Referring to FIG. 1, in order for the test system 10 to operate in the multi-ring mode, each of the two bits c1 and c2 of the control signal FC is set by the controller 22 at a logic low level. In this way, the TMS signal and TDo vector produced by the controller 22 pass through the multiplexers 26 and 28, respectively, to the boundary scan chain of circuits 12 while the vector TDi shifted out of the component chain and received at the TDi input of the test system 10 passes to the controller 22.").
wherein said mode signal is a disable signal when said reset input is triggered by said reset signal, and wherein said mode signal is an enable signal when said key signal matches a predetermined data pattern, and	*see, e.g.*, '166 patent at Fig. 2; *see, e.g.*. 9:18-24 ("The interface 42 is coupled to the external test and diagnosis system to receive a chip enable (CE) signal, a register address (RA) signal, a read/write (R/W) signal, a data strobe (DTSB) signal, and a test clock input (TCKIN) signal. The CE signal is comprised of a single binary bit which serves to enable the interface 42 when the bit is at a logic low level.")
a logic gate having inputs coupled to said clock input and said key logic circuit and an output coupled to said signal output, said logic gate generating at said signal output said	*See, e.g., id.* at 9:66-68 ("The TCK generator 64 takes the form of a programmable divider which divides the TCKIN signal to generate the TCK signal."). One of skill in the art would know to use any particular logic gate appropriate for an application.

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control signal responsive to said clock signal and said mode signal; and	
wherein said control signal drives said logic testing circuit to a low power state when said mode signal is said disable signal, and wherein said control signal drives said logic testing circuit to said normal state when said mode signal is said enable signal.	*See, e.g.*, IEEE 1149.1 at 38 ("When the BYPASS instruction is selected, the operation of the test logic shall have no effect on the operation of the on-chip system logic.").
Claim 16	
Claim limitation	**Prior Art**
16. The arrangement of claim 15 wherein said logic gate is a NOR gate, said disable signal is a logical HIGH, and said enable signal is a logic LOW.	*See, e.g., id.* at 9:66-68 ("The TCK generator 64 takes the form of a programmable divider which divides the TCKIN signal to generate the TCK signal."). One of skill in the art would know to use any particular logic gate appropriate for an application. One of skill in the art would know to use any signal polarity appropriate for an application.
Claim 17	
Claim limitation	**Prior Art**
17. The arrangement of claim 15 further comprising a clock signal source coupled to said clock input, said clock signal source generating said clock signal.	*See, e.g., id.* at Fig. 2; *see, e.g., id.* at 9:18-22 ("The interface 42 is coupled to the external test and diagnosis system to receive a chip enable (CE) signal, a register address (RA) signal, a read/write (R/W) signal, a data strobe (DTSB) signal, and a test clock input (TCKIN) signal."); *see, e.g., id.* at 9:31-33 ("The TCKIN signal is a single binary bit which is time-varying, and it is from this bit that the TCK signal is derived."). One of skill in the art would know that a circuit arrangement with a clock has a clock signal source coupled to a clock input.

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Claim 19	
Claim limitation	**Prior Art**
19. The arrangement of claim 15 wherein said key input is a multi-bit digital input and wherein said predetermined data pattern is determined by the configuration of the components of said key logic circuit.	*See, e.g., id.* at Fig. 2; *see, e.g., id.* at 9:18-31 ("The interface 42 is coupled to the external test and diagnosis system to receive a chip enable (CE) signal, a register address (RA) signal, a read/write (R/W) signal, a data strobe (DTSB) signal, and a test clock input (TCKIN) signal. The CE signal is comprised of a single binary bit which serves to enable the interface 42 when the bit is at a logic low level. The RA signal comprises a single binary bit which controls the addressing of the latches 44 by the external test and diagnosis system 43. The R/W signal is a single binary bit which indicates whether data is to be written to, or read from, the latch 44. The DTSB signal is a single bit which, when at a logic low level, alerts the interface 42 that valid data is present on the data lines D0-D7.").

Appendix E3
Defendants and Counterclaimants' Invalidity Contentions
Advanced Micro Devices, Inc. et al. v. Samsung Electronics Co., Ltd. et al., Case No. CV-08-0986-SI

U.S. Patent No. 5,377,200 Invalidity Chart: ARM610, ARM600, ARM60 chips and MEMC2 chip ("ARM610")

All asserted claims are anticipated by the ARM610, ARM600, ARM60, and MEMC2 chip designs ("ARM610") and/or are rendered obvious by them, either alone or in combination with other prior art described below and/or listed in Section I of Defendants' and Counterclaimants' Preliminary Invalidity Contentions and/or through modifications described below. Nothing in this invalidity chart should be construed as signifying or suggesting Defendants and Counterclaimants' adoption of or acquiescence in any claim scope and/or claim construction positions taken by Plaintiffs and Counterdefendants in this litigation.

The boundary scan circuit design referred to in the claim chart below was used in the ARM60, ARM600, and ARM610 chip designs. Any reference to ARM610 in the text below could equivalently be a reference to ARM60 and ARM600. This circuit design is based on a very similar design used in the earlier MEMC2 chip, and references to ARM610 could equivalently be references to MEMC2. Technical features of ARM610 are described below and supported in, *inter alia*, data sheets, schematics, and block diagrams for the ARM610, ARM600, ARM60, and/or MEMC2 chip designs and IEEE Standard 1149.1-1990.

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Claim 1	
Claim limitation	**Prior Art**
1. A configuration register for controlling a logic testing circuit, said logic testing circuit being coupled to a logic module for testing the integrity of said logic module, said logic testing circuit having a normal state and a low power state, said configuration register comprising:	Throughout this document, "JTAG" is used to refer to the Joint Test Action Group standard formalized as IEEE Standard 1149.1-1990 "IEEE Standard Test Access Port and Boundary-Scan Architecture". "TAP" is the Test Access Port of that standard. The "configuration register" is the JTAG TAP controller. The "logic testing circuit" is the JTAG boundary scan chain around the periphery of the ARM610, used for INTEST of ARM610 and EXTEST of connections between ARM610 and other chips. The logic module is the ARM610 processor inside the JTAG boundary scan cell. "a normal state and a low power state" is discussed below.

Appendix E3
Defendants and Counterclaimants' Invalidity Contentions
Advanced Micro Devices, Inc. et al. v. Samsung Electronics Co., Ltd. et al.
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a key input disposed to receive a key signal;	The key input is the IEEE JTAG TAP port inputs TDI and TMS. These signals are sampled on the rising edge of the test clock input TCK.
a reset input disposed to receive a reset signal;	The reset input is the IEEE JTAG nTRST input (the "n" at the start of the signal name indicates an active low signal).
an output coupled to said logic testing circuit;	The output is BSCtl[8] (inverted version of nShClkBS). The signal is also labeled ShClkBS. The BSCtl[8] output is coupled to the scan cells that comprise the JTAG boundary scan chain.
a key logic circuit coupled to said key input, said reset input, and said output, said key logic circuit generating to said logic testing circuit, through said output, a control signal responsive to said key signal and said reset signal;	The key logic circuit is the portions of the JTAG TAP controller which generate the nBTest signal that feeds into the compound NOR/OR gate that drives nShClkBS which drives the BSCtl[8] output.
wherein said control signal drives said logic testing circuit to said low power state when said reset input is triggered by said reset signal; and	A reset initiated by driving nTRST low. Reset loads the instruction register with the value IDCODE = 1110 ([1] section 11.3 "Reset". This can also be inferred from the "Reset" and "NSet" inputs of the instruction register flip flops in the schematic.). This causes the instruction decoder output nBTest to be driven to a 1. nBTest is connected to the top input of the compound NOR/OR gate whose output is nShClkBS. When nBTest is driven high, nShClkBS, which is the OR output of the compound NOR/OR gate, is forced high. This puts the boundary scan cells in a low power state because it disables clock pulses on nShClkDR being passed on to BSctl[8]. Being a static CMOS design, disabling clock pulses leaves the boundary scan cells in a low power state.
wherein said control signal drives said logic testing circuit to said normal state when said key signal matches a predetermined data pattern.	When the TAP controller inputs receive the appropriate serial input sequence to load the INTEST = 1100 instruction into the instruction register, nBTEST goes low, enabling clock pulses on nShClkDR to be passed on to BSctl[8]. This will cause the boundary scan cells to perform shift operations, which is a normal operation state distinct from the low power state described above.

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Claim 2	
Claim limitation	**Prior Art**
2. The configuration register of claim 1 wherein said control signal is a clock signal when said key signal matches said predetermined pattern, and wherein said output is coupled to a clock port of said logic testing circuit.	The control signal BSCtl[8], also labeled ShClkBS, is the "shift clock". It is connected to the Shift Clock port ShClkBS of the boundary scan cells and each clock pulse on BSCtl[8] causes the boundary scan cell to shift by one bit position. It is only a clock when the TAP state machine is driven to the appropriate state by the TAP controller inputs receiving the pre-determined pattern that will drive the state machine into the ShiftDR state.
Claim 3	
Claim limitation	**Prior Art**
3. The configuration register of claim 2 further comprising a clock input coupled to a clock signal source, said clock signal being generated responsive to a signal generated by said clock signal source.	The clock input is TCK and the clock pulses on BSCtl[8] are generated responsive to clock pulses from a clock source coupled to TCK. The clock signal source will be a piece of test equipment designed to drive the ARM610 JTAG test access port, in accordance with the IEEE JTAG specification.
Claim 5	
Claim limitation	**Prior Art**
5. The configuration register of claim 3 further comprising a NOR gate, wherein said key logic circuit and said clock input are coupled to	The circuit diagram [2] shows nShClkBS output from a compound gate which is drawn as a combined OR and NOR gate. As CMOS is fundamentally an inverting logic family, this gate will be implemented as a NOR gate followed by an inverter. The nShClkDR clock signal is derived from TCK, and provides one input to the NOR gate. The nBTest decode signal described earlier is the other input of the NOR gate. The BSctl[8] output is the output of the NOR gate buffered by two inverters (one inside the compound gate).

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said output through said NOR gate.	
Claim 6	
Claim limitation	**Prior Art**
6. A circuit arrangement comprising:	The ARM610 chip is a circuit arrangement
a logic component having a logic module and a built-in logic testing circuit, said logic testing circuit being coupled to said logic module for testing the integrity of said logic module and having a normal state and a low power state, wherein said logic testing circuit may be disabled to save power when testing operations are not being performed;	The ARM610 core and its surrounding JTAG boundary scan cells, and omitting the JTAG TAP controller, is a logic component. The ARM610 core is a logic module. The boundary scan cells are a logic testing circuit. As INTEST is supported on the ARM610 chip, the boundary scan cells are coupled to the ARM610 core for testing the integrity of ARM610 (via INTEST testing). The scan cells have a low-power state when none of their clock inputs are receiving a clock signal (the inputs are held at a steady logic level), and a normal state when the clock inputs are receiving a clock signal. The Shift Clock input is an example of a clock input in the boundary scan cell. The logic circuit is disabled to save power by holding the clock inputs at a steady logic level.
a configuration register for controlling said logic testing circuit, said configuration register comprising	The configuration register is the JTAG TAP controller.
a key input disposed to receive a key signal,	The key input is the IEEE JTAG TAP port inputs TDI and TMS. These signals are sampled on the rising edge of TCK.
a reset input disposed to receive a reset signal,	The reset input is the IEEE JTAG nTRST input

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an output coupled to said logic testing circuit, and	The output is BSCtl[8] (inverted version of nShClkBS). The signal is also labeled ShClkBS. The BSCtl[8] output is coupled to the scan cells that comprise the JTAG boundary scan chain.
a key logic circuit coupled to said key input, said reset input, and said output, said key logic circuit generating to said logic testing circuit, through said output, a control signal responsive to said key signal and said reset signal;	The key logic circuit is the portions of the JTAG TAP controller which generate the nBTest signal that feeds into the compound NOR/OR gate that drives nShClkBS which drives the BSCtl[8] output.
wherein said control signal drives said logic testing circuit to said low power state when said reset input is triggered by said reset signal; and	A reset initiated by driving nTRST low. Reset loads the instruction register with the value IDCODE = 1110 ([1] section 11.3 "Reset". This can also be inferred from the "Reset" and "NSet" inputs of the instruction register flip flops in the schematic.). This causes the instruction decoder output nBTest to be driven to a 1. nBTest is connected to the top input of the compound NOR/OR gate whose output is nShClkBS. When nBTest is driven high, nShClkBS, which is the OR output of the compound NOR/OR gate, is forced high. This puts the boundary scan cells in a low power state because it disables clock pulses on nShClkDR being passed on to BSctl[8]. Being a static CMOS design, disabling clock pulses leaves the boundary scan cells in a low power state.
wherein said control signal drives said logic testing circuit to said normal state when said key signal matches a predetermined data pattern.	When the TAP controller inputs receive the appropriate serial input sequence to load the INTEST = 1100 instruction into the instruction register, nBTEST goes low, enabling clock pulses on nShClkDR to be passed on to BSctl[8]. This will cause the boundary scan cells to perform shift operations, which is a normal operation state distinct from the low power state described above.
Claim 7	
Claim limitation	**Prior Art**
7. The arrangement of claim 6 wherein said control signal is a	The control signal BSCtl[8], also labeled ShClkBS, is the "shift clock". It is connected to the Shift Clock port ShClkBS of the boundary cells and each clock pulse on BSCtl[8] causes the boundary scan cell to shift by one

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clock signal when said key signal matches said predetermined data pattern, and wherein said output is coupled to a clock port of said logic testing circuit.	bit position. It is only a clock when the TAP state machine is driven to the appropriate state by the TAP controller inputs receiving the pre-determined pattern that will drive the state machine into the ShiftDR state.
Claim 8	
Claim limitation	**Prior Art**
8. The arrangement of claim 7 further comprising a clock signal source, wherein said configuration register further comprises a clock input disposed to receive said clock signal from said clock signal source.	The clock input is TCK and the clock pulses on BSCtl[8] are generated responsive to clock pulses from a clock source coupled to TCK. The clock signal source will be a piece of test equipment designed to drive the ARM610 JTAG test access port, in accordance with the IEEE JTAG specification.
Claim 11	
Claim limitation	**Prior Art**
11. The arrangement of claim 6 wherein said logic testing circuit has a clock port and wherein the state of said logic testing circuit is responsive to a signal at said clock port.	The boundary scan chain has a Shift Clock port ShClkBS, also labeled BSCtl[8]. A clock pulse applied to the Shift Clock port causes the state of the scan chain to change by the stored contents of the scan cells shifting by one bit along the scan chain.
Claim 12	
Claim limitation	**Prior Art**
12. The arrangement of claim 11	BSctl[8] is coupled to the Scan Clock input ShClkBS of the boundary scan cells. BSCtl[8] is driven LOW by a

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wherein said output is coupled to said clock port, said logic testing circuit is driven to said low power state when a LOW is applied to a clock port, and wherein said control signal is LOW when said reset input is triggered by said reset signal.	reset signal applied to the nTRST input [As explained above, reset causes nBTest to go HIGH, which forces the NOR gate output nShClkBS HIGH, which forces BSCtl[8] LOW. BSctl[8] is held low by the nBTest decode signal except when appropriate instructions are scanned into the TAP controller that require the boundary scan cells to be shifted. As the boundary scan cells are implemented in static CMOS, holding the clock signal at a steady low level renders the scan cells into a low power state.
Claim 13	
Claim limitation	**Prior Art**
13. The arrangement of claim 11 wherein said output is coupled to said clock port, said logic testing circuit is driven to said normal state when a clock signal is applied to a clock port, and wherein said control signal is a clock signal when said key signal matches said predetermined data pattern.	The BSctl[8] output of the TAP controller is coupled to the ShClkBS input of the scan cells. When the TAP controller inputs receive the appropriate serial input sequence to load the INTEST = 1100 instruction into the instruction register, nBTEST goes low, enabling clock pulses on nShClkDR to be passed on to BSctl[8]. This will cause the boundary scan cells to perform shift operations, which is a normal operation state distinct from the low power state described above. The clock pulses originate in a clock source coupled to the TCK input. The clock source will be a piece of test equipment designed to drive the JTAG Test Access Port in accordance with the IEEE Specification.
Claim 15	
Claim limitation	**Prior Art**
15. A circuit arrangement comprising:	The ARM610 chip is a circuit arrangement.
a logic component having a logic module and a built-in logic testing circuit for testing the integrity of	The ARM610 core and its surrounding JTAG boundary scan cells, and omitting the JTAG TAP controller, is a logic component. The ARM610 core is a logic module.

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said logic module, said logic testing circuit being coupled to said logic module and having a normal state and a low power state, said logic testing circuit further having a clock port, wherein the state of said logic testing circuit is responsive to a control signal applied at said clock port, wherein said logic testing circuit may be disabled to save power when testing operations are not being performed;	The boundary scan cells are a logic testing circuit. As INTEST is supported on the ARM610 chip, the boundary scan cells are coupled to the ARM610 core for testing the integrity of ARM610 (via INTEST testing). The scan cells have a low-power state when none of their clock inputs are receiving a clock signal (the inputs are held at a steady logic level), and a normal state when the clock inputs are receiving a clock signal. The Shift Clock input ShClkBS is an example of a clock input in the boundary scan cell. The logic circuit is disabled to save power by holding the clock inputs at a steady logic level. The ShClkBS input is a clock input of the boundary scan cells. The state of the boundary scan cells is responsive to a control signal applied to the ShClkBS input – it causes the scan chain to perform a shift operation that moves data along the scan chain by one bit per clock pulse applied to ShClkBS.
a configuration register for controlling said logic testing circuit, said configuration register comprising	The configuration register is the ARM610 TAP controller.
a key input disposed to receive a key signal,	The key input is the IEEE JTAG TAP port inputs TDI and TMS. These signals are sampled on the rising edge of TCK.
a reset input disposed to receive a reset signal,	The reset input is the IEEE JTAG nTRST input
a clock input disposed to receive a clock signal,	The clock input is the TCK pin. It is disposed to receive a test clock from a piece of test equipment designed to drive the Test Access Port in accordance with the JTAG specification.
a signal output coupled to the clock	The BSctl[8] output of the ARM610 TAP controller is coupled to the ShClkBS clock port of the boundary scan

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port of said logic testing circuit,	chain.
a key logic circuit coupled to said key input and said reset input, wherein said key logic circuit generates a mode signal responsive to said key signal and said reset signal,	The key logic circuit is the portions of the JTAG TAP controller which generate the nBTest signal. The nBTest signal is the mode signal.
wherein said mode signal is a disable signal when said reset input is triggered by said reset signal, and wherein said mode signal is an enable signal when said key signal matches a predetermined data pattern, and	As explained above, nBTest goes HIGH at Reset, forcing the nShClkBS output of the NOR gate HIGH, and so disabling clock pulses. When the TAP controller TMS and TDI inputs receive the appropriate serial input sequence to load the INTEST = 1100 instruction into the instruction register, nBTEST goes LOW, enabling clock pulses on nShClkDR to be passed on to BSctl[8].
a logic gate having inputs coupled to said clock input and said key logic circuit and an output coupled to said signal output, said logic gate generating at said signal output said control signal responsive to said clock signal and said mode signal; and	The logic gate is the NOR gate within the compound NOR/NAND gate whose output is nShClkBS. As CMOS is fundamentally an inverting logic family, the compound NOR/NAND gate will be implemented as a NAND gate followed by an inverter, with both the output of the NAND gate and the output of the invert available as outputs of the compound gate. The NOR gate has a first input driven by nShClkDR. nShClkDR is driven by a NAND gate which has one input driven by TCK1. TCK1 is generated by a non-overlapping clock generator whose input is the TCK input of the TAP controller circuit. This input is driven by the TCK input pad on the chip. Thus the first input of the NAND gate is coupled to the TCK pin via the circuit elements just described. The second input of the NOR gate is nBTest, which is identified above as the "mode" output of the "key logic circuit".
wherein said control signal drives	The "control signal" BSctl[8] is held LOW when the "mode signal" nBTest is a disable signal, holding the

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said logic testing circuit to a low power state when said mode signal is said disable signal, and wherein said control signal drives said logic testing circuit to said normal state when said mode signal is said enable signal.	boundary scan chain in a static (no clocks) low power state. The "control signal" BSctl[8] carries clock pulses to the boundary scan chain when the "mode signal" nBTest is an enable, causing the boundary scan chain to consume dynamic power with each clock pulse in its "normal state".
Claim 16	
Claim limitation	**Prior Art**
16. The arrangement of claim 15 wherein said logic gate is a NOR gate, said disable signal is a logical HIGH, and said enable signal is a logic LOW.	As described above: • the logic gate is a NOR gate. • nBTest is a logical HIGH when it is operating as a disable signal. • nBTest is a logic LOW when it is operating as an enable signal.
Claim 17	
Claim limitation	**Prior Art**
17. The arrangement of claim 15 further comprising a clock signal source coupled to said clock input, said clock signal source generating said clock signal.	The clock signal source will be a test clock from a piece of test equipment designed to drive the Test Access Port in accordance with the JTAG specification.
Claim 19	

Appendix E3
Defendants and Counterclaimants' Invalidity Contentions
Advanced Micro Devices, Inc. et al. v. Samsung Electronics Co., Ltd. et al.
Case No. CV-08-0986-SI

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Claim limitation	**Prior Art**
19. The arrangement of claim 15 wherein said key input is a multi-bit digital input and wherein said predetermined data pattern is determined by the configuration of the components of said key logic circuit.	Loading the instruction register with the INTEST instruction and driving the TAP controller state machine to the correct state to generate clock pulses on BSCtl[8] requires a multi-bit digital input on the serial inputs TMS and TDI. The required bit sequence is determined by the configuration of the components of the TAP controller circuit elements that generate the nBTest signal.

Appendix E4
Defendants and Counterclaimants' Invalidity Contentions
Advanced Micro Devices, Inc., et al., v. Samsung Electronics Co., Ltd., et al., Case No. 3:08-CV-0986-SI

U.S. Patent No. 5,377,200 Invalidity Chart: Lee Whetsel, *An IEEE 1149.1 Based Logic/Signature Analyzer in a Chip*, Proceedings of International Test Conference, Nashville, TN, October 26-30, 1991 ("Whetsel")

All asserted claims are anticipated by the Whetsel and/or are rendered obvious by it, either alone or in combination with other prior art described below and/or listed in Section I of Defendants' and Counterclaimants' Preliminary Invalidity Contentions and/or through modifications described below. Nothing in this invalidity chart should be construed as signifying or suggesting Defendants and Counterclaimants' adoption of or acquiescence in any claim scope and/or claim construction positions taken by Plaintiffs and Counterdefendants in this litigation.

To the extent a feature of the claims may not be disclosed or suggested by Whetsel alone, one of skill in the art would know to consider the Clock Gating references (defined below). One of skill in the art would know to implement a clock as a control signal using clock gating techniques, especially due to the importance of reducing pin-count. *See, e.g.*, Schnaitter (defined below) at 721. One of skill in the art would know to look at IEEE Standard 1149.1-1990 ("IEEE 1149.1"). *See, e.g.*, Whetsel at 3 ("This paper assumes the reader has a basic understanding of the IEEE 1149.1 standard.") On information and belief, Whetsel describes the TI SN74ACT8994 Digital Bus Monitor chip. Additional information regarding the TI SN74ACT8994 Digital Bus Monitor chip can be found in the following references, which, to avoid repetition, have not been cited in the chart below: Japanese Patent Publication 3-116346; TI SN74ACT8994 Data Sheet; and U.S. Patent No. 5,905,738 and the file history thereto. Further, on information and belief, U.S. Patent No. 5,905,738 and Japanese Patent Publication 3-116346 each comprise prior art in themselves, *i.e.*, apart from being evidence of the features of the TI SN74ACT8994 chip. Although these references have not been separated charted to avoid repetition, Samsung reserves the right to use them to support its invalidity contentions related to the '200 patent.

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Claim 1	
Claim limitation	**Prior Art**
1. A configuration register for controlling a logic testing circuit, said logic testing circuit being coupled to a logic module for testing the integrity of said logic module, said logic testing circuit having a normal state and a low power state, said configuration register comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, Whetsel discloses this limitation. *See, e.g.*, Whetsel at Fig. 8; *see, e.g.*, *id.* at 8 ("While non-testing buffers/transceivers could have been used in this circuit, 1149.1 compliant ones are implemented to provide embedded control and observability of the processors 16-bit data, 16-bit address, and control buses. The 8-bit buffers and transceivers used, like the DBMs, are members of TIs SCOPE family of testability components and are referred to as SCOPE octals."); *see, e.g.*, *id.* at 4 ("The trace memory is a 16-bit by 1024 location static RAM. When disabled the trace memory powers down and requires minimum power to maintain its contents."); *see, e.g.*, *id.* at 3 ("The DBM is a 28 in device designed in compliance with the rules set forth in the IEEE 1149.1 boundary scan standard. The DBM supports all required 1149.1 boundary scan test instructions as well as a rich set of special test instructions supporting its data trace and signature analysis test operations. The data trace and signature

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	analysis operations can operate from control input from the 1149.1 test bus or from control generated internal to the DBM."); *see, e.g.*, IEEE 1149.1 at Figs. 5-7 and 7-2; *see, e.g.*, IEEE 1149.1 at 5 ("Design-for-test features such as these can be accessed and controlled using the data path between the serial test data pins of the TAP defined by this standard. Instructions that cause internal reconfiguration of the component's system logic such that the test operation is enabled may be shifted into the component through the TAP."); *see, e.g., id.* at Figs. 5-7 and 7-2 (disclosing a state in which the boundary scan cells are disabled, and therefore in a low power state).
a key input disposed to receive a key signal;	*See, e.g.*, Whetsel at 6 ("The comparator is used during EQM controlled data trace and compaction test operations to detect patterns input to the DBM via the data bus and output a CTERM signal to the EQM in response to a detection."); *see, e.g., id.* at 10 ("In some monitoring applications it may be desired to trace and/or compact data words transferred between the processor and I/O, RAM, and ROM in response to a single predetermined address and/or data pattern.").
a reset input disposed to receive a reset signal;	*See, e.g.*, IEEE 1149.1 at 12 ("The optional TRST* input provides for asynchronous initialization of the TAP controller (see 5.3).").
an output coupled to said logic testing circuit;	*See, e.g.*, Whetsel at 7 ("Also the test controller outputs test status or internal event signals off chip via the EQO pin. In the status output mode, test status signals can be output from the EQO pin to indicate, among other things: (1) test-in-progress or (2) end-of-test. These status outputs can be monitored by external controllers or testers to determine the state of the test being performed. Alternately, these test status signals can be inspected via 1149.1 instruction register scan operations."); *see, e.g., id.* ("The event signal output from the EQO pin can be used for triggering an external tester, or to input an event to a neighboring ICs EQM to initiate a test protocol operation."); *see, e.g.*, IEEE 1149.1 at Fig. 5-5.
a key logic circuit coupled to said key input, said reset input, and said output, said key logic circuit generating to said logic testing circuit, through said output, a control signal responsive to said key	*See, e.g.*, Whetsel at 6 ("The EQM receives control input from the TAP, clock input from the PCI, external event input from the EQI pin, internal event input from the CTERM signal, serial data input from the TDI pin, and outputs event signals to the EQO pin and serial data to the TDO pin."); *see, e.g., id.* at 7 ("In the event output mode, the CTERM signal from the comparator can be output from the EQO pin to indicate the occurrence of an internal event. The event signal output from the EQO pin can be used for triggering an external tester, or to input an event to a neighboring ICs EQM to initiate a test protocol operation.")

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signal and said reset signal;	
wherein said control signal drives said logic testing circuit to said low power state when said reset input is triggered by said reset signal; and	*See, e.g., id.* at Fig. 8; *see, e.g.,* IEEE 1149.1 at Fig. 5-1 and related text at pp. 18-23; *see, e.g., id.* at 19 ("The test logic is disabled so that normal operation of the on-chip system logic (i.e., in response to stimuli received through the system pins only) can continue unhindered. This is achieved by initializing the instruction register to contain the *IDCODE* instruction or, if the optional device identification register is not provided, the BYPASS instruction (see 6.2). No matter what the original state of the controller, it will enter *Test-Logic-Reset* when TMS is held high for at least five rising edges of TCK. The controller remains in this state while TMS is high."); *see, e.g., id.* ("Note that the TAP controller will also be forced to the Test-Logic-Reset controller state by applying a low logic level at TRST*, if such is provided, or at power-up (see 5.3)."); *see, e.g., id.* at Figs. 5-7 and 7-2.
wherein said control signal drives said logic testing circuit to said normal state when said key signal matches a predetermined data pattern.	*See, e.g.,* Whetsel at 7 ("In the event output mode, the CTERM signal from the comparator can be output from the EQO pin to indicate the occurrence of an internal event. The event signal output from the EQO pin can be used for triggering an external tester, or to input an event to a neighboring ICs EQM to initiate a test protocol operation.")
Claim 2	
Claim limitation	**Prior Art**
2. The configuration register of claim 1 wherein said control signal is a clock signal when said key signal matches said predetermined pattern, and wherein said output is coupled to a clock port of said logic testing circuit.	*See, e.g.,* IEEE 1149.1 at Figs. 5-5 and 10-18; *see, e.g., id.* at 16 ("The TAP controller. This receives TCK and interprets the signals on TMS. The TAP controller generates clock or control signals or both as required for the instruction and test data registers and for other parts of the architecture."); *see, e.g., id.* at 27 ("Note also that, while the ShiftDR and ClockDR signals may be broadcast to all test data registers, distribution of the UpdateDR control signal will be controlled according to the instruction held in the instruction register such that the signal is fed only to the test data register that is selected as the serial path between TDI and TDO."). *See also* the following references (collectively, the "Clock Gating References"): *see, e.g.,* U.S. Patent No. 4,615,005 ("'005 patent") at Abstract ("Disclosed is a method of controlling the supply of a clock signal to a logic circuit, especially, a logic circuit composed of C-MOS gates for further

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	reducing the power consumption. According to the control method, a clock signal supply inhibit instruction is stored, so that, when this instruction is read out, the supply of the clock signal to the logic circuit is inhibited, or its level is fixed at a specific signal level. In response to the application of an interrupt signal, the clock signal having been inhibited to be supplied to the logic circuit starts to be supplied to the logic circuit again. The circuit region or regions for which the supply of the clock signal is to be inhibited can be freely selected for the purpose of control. Thus, the method is especially effective when it is desired to closely control the saving of power consumed by the logic circuit."); *see, e.g.*, Wagner, Kenneth D., *Clock System Design*, IEEE Design & Test of Computers, pp. 9-27, October 1988 ("Wagner") at 23 (two paragraphs under heading, "Clock Gating"); *see, e.g., id.* at Fig. 9; *see, e.g.*, P. Goel and M. T. McMahon, *Electronic Chip-in-Place Test*, 19th Design Automation Conference, Paper 30.1, 1982 ("Goel") at Fig. 4; *see, e.g.*, Schnaitter, William, et al., *A 0.5 GHz CMOS Digital RF Memory Chip*, IEEE Journal of Solid-State Circuits, Vol. SC-21, No. 5, pp. 720-26, October 1986 ("Schnaitter") at Figs. 3 and 4; *see, e.g.*, Bening, Lionel C., et al., *Developments in Logic Network Path Delay Analysis*, 19th Design Automation Conference, Paper 35.1, pp. 605-15, 1982 ("Bening") at Fig. 1; *see, e.g., id.* at 606 ("As an example of clock gating, in Fig. 1 the control input P is used to 'gate' the clock to flip-flop H. This provides a method for conditionally changing H's content.").
Claim 3	
Claim limitation	**Prior Art**
3. The configuration register of claim 2 further comprising a clock input coupled to a clock signal source, said clock signal being generated responsive to a signal generated by said clock signal	*See, e.g.*, Whetsel at Fig. 8; *see, e.g., id.* at 6 ("The PCI receives clock inputs from the CK1, CK2, CK3, and TCK pins...."); *see, e.g., id.* ("The PCI is programmable via input from the control register to couple one of the clock inputs or its complement to the PCI CLK output, or combine the clock inputs using Boolean AND and OR functions and couple the combined clock signal or its complement to the PCI CLK output."). One of skill in the art would know that a circuit arrangement with a clock has a clock signal source coupled to a clock input.

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source.	
Claim 5	
Claim limitation	**Prior Art**
5. The configuration register of claim 3 further comprising a NOR gate, wherein said key logic circuit and said clock input are coupled to said output through said NOR gate.	*See, e.g., id.* at Fig. 1; *see, e.g., id.* at 7 ("The PC1 is programmable via input from the control register to couple one of the clock inputs or its complement to the PC1 CLK output, or combine the clock inputs using Boolean AND and OR functions and couple the combined clock signal or its complement to the PCI CLK output."). One of skill in the art would know to use any particular logic gate appropriate for an application. *See, e.g.*, Schnaitter at Fig. 3 and Bening at Fig. 1.
Claim 6	
Claim limitation	**Prior Art**
6. A circuit arrangement comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, Whetsel discloses this limitation. *See, e.g.*, Whetsel at Fig. 8.
a logic component having a logic module and a built-in logic testing circuit, said logic testing circuit being coupled to said logic module for testing the integrity of said logic module and having a normal state and a low power state, wherein said logic testing circuit may be disabled to save power when testing operations are not being performed;	*See, e.g.*, Whetsel at Fig. 8; *see, e.g., id.* at 8 ("While non-testing buffers/transceivers could have been used in this circuit, 1149.1 compliant ones are implemented to provide embedded control and observability of the processors 16-bit data, 16-bit address, and control buses. The 8-bit buffers and transceivers used, like the DBMs, are members of TIs SCOPE family of testability components and are referred to as SCOPE octals."); *see, e.g., id.* at 4 ("The trace memory is a 16-bit by 1024 location static RAM. When disabled the trace memory powers down and requires minimum power to maintain its contents."); *see also* IEEE 1149.1 at 4 ("The boundary-scan cells for the pins of a component are interconnected so as to form a shift-register chain around the border of the design, and this path is provided with serial input and output connections and appropriate clock and control signals."); *see, e.g., id.* at 3 ("The DBM is a 28 in device designed in compliance with the rules set forth in the IEEE 1149.1 boundary scan standard. The DBM supports all required 1149.1 boundary scan test instructions as well as a rich set of special test instructions supporting its data trace and signature analysis test operations. The data trace and signature analysis operations can operate from control input from the 1149.1 test bus or from control generated internal to the DBM."); *see, e.g.*, IEEE 1149.1 at Figs. 5-7 and 7-2; *see, e.g.*, IEEE 1149.1 at 5 ("Design-for-test features such as these can be accessed and controlled

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	using the data path between the serial test data pins of the TAP defined by this standard. Instructions that cause internal reconfiguration of the component's system logic such that the test operation is enabled may be shifted into the component through the TAP."); *see, e.g., id.* at Figs. 5-7 and 7-2 (disclosing a state in which the boundary scan cells are disabled, and therefore in a low power state)..
a configuration register for controlling said logic testing circuit, said configuration register comprising	*See, e.g.*, Whetsel at Fig. 8; *see, e.g., id.* at 8 ("While non-testing buffers/transceivers could have been used in this circuit, 1149.1 compliant ones are implemented to provide embedded control and observability of the processors 16-bit data, 16-bit address, and control buses. The 8-bit buffers and transceivers used, like the DBMs, are members of TIs SCOPE family of testability components and are referred to as SCOPE octals."); *see, e.g., id.* at 4 ("The trace memory is a 16-bit by 1024 location static RAM. When disabled the trace memory powers down and requires minimum power to maintain its contents.").
a key input disposed to receive a key signal,	*See, e.g., id.* at 6 ("The comparator is used during EQM controlled data trace and compaction test operations to detect patterns input to the DBM via the data bus and output a CTERM signal to the EQM in response to a detection."); *see, e.g., id.* at 10 ("In some monitoring applications it may be desired to trace and/or compact data words transferred between the processor and I/O, RAM, and ROM in response to a single predetermined address and/or data pattern.").
a reset input disposed to receive a reset signal,	*See, e.g.*, IEEE 1149.1 at 12 ("The optional TRST* input provides for asynchronous initialization of the TAP controller (see 5.3).").
an output coupled to said logic testing circuit, and	*See, e.g.*, Whetsel at 7 ("Also the test controller outputs test status or internal event signals off chip via the EQO pin. In the status output mode, test status signals can be output from the EQO pin to indicate, among other things: (1) test-in-progress or (2) end-of-test. These status outputs can be monitored by external controllers or testers to determine the state of the test being performed. Alternately, these test status signals can be inspected via 1149.1 instruction register scan operations."); *see, e.g., id.* ("The event signal output from the EQO pin can be used for triggering an external tester, or to input an event to a neighboring ICs EQM to initiate a test protocol operation."); *see, e.g.*, IEEE 1149.1 at Fig. 5-5.
a key logic circuit coupled to said key input, said reset input, and said output, said key logic circuit	*See, e.g.*, Whetsel at 6 ("The EQM receives control input from the TAP, clock input from the PCI, external event input from the EQI pin, internal event input from the CTERM signal, serial data input from the TDI pin, and outputs event signals to the EQO pin and serial data to the TDO pin."); *see, e.g., id.* at 7 ("In the event

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generating to said logic testing circuit, through said output, a control signal responsive to said key signal and said reset signal;	output mode, the CTERM signal from the comparator can be output from the EQO pin to indicate the occurrence of an internal event. The event signal output from the EQO pin can be used for triggering an external tester, or to input an event to a neighboring ICs EQM to initiate a test protocol operation.")
wherein said control signal drives said logic testing circuit to said low power state when said reset input is triggered by said reset signal; and	*See, e.g., id.* at Fig. 8; *see, e.g.,* IEEE 1149.1 at Fig. 5-1 and related text at pp. 18-23; *see, e.g., id.* at 19 ("The test logic is disabled so that normal operation of the on-chip system logic (i.e., in response to stimuli received through the system pins only) can continue unhindered. This is achieved by initializing the instruction register to contain the *IDCODE* instruction or, if the optional device identification register is not provided, the BYPASS instruction (see 6.2). No matter what the original state of the controller, it will enter *Test-Logic-Reset* when TMS is held high for at least five rising edges of TCK. The controller remains in this state while TMS is high."); *see, e.g., id.* ("Note that the TAP controller will also be forced to the Test-Logic-Reset controller state by applying a low logic level at TRST*, if such is provided, or at power-up (see 5.3)."); *see, e.g., id.* at Figs. 5-7 and 7-2.
wherein said control signal drives said logic testing circuit to said normal state when said key signal matches a predetermined data pattern.	*See, e.g.,* Whetsel at 7 ("In the event output mode, the CTERM signal from the comparator can be output from the EQO pin to indicate the occurrence of an internal event. The event signal output from the EQO pin can be used for triggering an external tester, or to input an event to a neighboring ICs EQM to initiate a test protocol operation.")
Claim 7	
Claim limitation	**Prior Art**
7. The arrangement of claim 6 wherein said control signal is a clock signal when said key signal matches said predetermined data pattern, and wherein said output is coupled to a clock port of said logic testing circuit.	*See, e.g.,* IEEE 1149.1 at Figs. 5-5 and 10-18; *see, e.g., id.* at 16 ("The TAP controller. This receives TCK and interprets the signals on TMS. The TAP controller generates clock or control signals or both as required for the instruction and test data registers and for other parts of the architecture."); *see, e.g., id.* at 27 ("Note also that, while the ShiftDR and ClockDR signals may be broadcast to all test data registers, distribution of the UpdateDR control signal will be controlled according to the instruction held in the instruction register such that the signal is fed only to the test data register that is selected as the serial path between TDI and TDO.").

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	See also Clock Gating References..
Claim 8	
Claim limitation	**Prior Art**
8. The arrangement of claim 7 further comprising a clock signal source, wherein said configuration register further comprises a clock input disposed to receive said clock signal from said clock signal source.	*See, e.g.*, Whetsel at Fig. 8; *see, e.g., id.* at 6 ("The PCI receives clock inputs from the CK1, CK2, CK3, and TCK pins...."); *see, e.g., id.* ("The PCI is programmable via input from the control register to couple one of the clock inputs or its complement to the PCI CLK output, or combine the clock inputs using Boolean AND and OR functions and couple the combined clock signal or its complement to the PCI CLK output."). One of skill in the art would know that a circuit arrangement with a clock has a clock signal source coupled to a clock input.
Claim 11	
Claim limitation	**Prior Art**
11. The arrangement of claim 6 wherein said logic testing circuit has a clock port and wherein the state of said logic testing circuit is responsive to a signal at said clock port.	*See, e.g.*, IEEE 1149.1 at Fig. 1-1; *see, e.g.. id.* at 3 ("Figure 1-1 illustrates an example implementation for a boundary-scan cell that could be used for an input or output connection to an integrated circuit. Dependent on the control signals applied to the multiplexers, data can either be loaded into the scan register from the Signal-in port (e.g., the input pin), or driven from the register through the Signalout port of the cell (e.g., into the core of the component design). As will be discussed in detail in Chapter 10, the second flip-flop (controlled by input Clock B) is provided to ensure that the signals driven out of the cell in the latter case are held while new data is shifted into the cell using input Clock A. This flip-flop is not required in all cases, but is included in Figure 1-1 to simplify the discussion."); *see, e.g., id.* at Fig. 10-18.
Claim 12	
Claim limitation	**Prior Art**
12. The arrangement of claim 11 wherein said output is coupled to said clock port, said logic testing circuit is driven to said low power state when a LOW is applied to a	*See, e.g.*, Whetsel at Fig. 1; *see also* IEEE 1149.1 at Fig. 5-1 and related text at pp. 18-23; *see, e.g., id.* at Figs. 5-5 and 10-18. One of skill in the art would know to use any signal polarity appropriate for an application.

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clock port, and wherein said control signal is LOW when said reset input is triggered by said reset signal.	
Claim 13	
Claim limitation	**Prior Art**
13. The arrangement of claim 11 wherein said output is coupled to said clock port, said logic testing circuit is driven to said normal state when a clock signal is applied to a clock port, and wherein said control signal is a clock signal when said key signal matches said predetermined data pattern.	*See, e.g.*, Whetsel at 7 ("In the event output mode, the CTERM signal from the comparator can be output from the EQO pin to indicate the occurrence of an internal event. The event signal output from the EQO pin can be used for triggering an external tester, or to input an event to a neighboring ICs EQM to initiate a test protocol operation."); *see also* IEEE 1149.1 at Fig. 5-1 and related text at pp. 18-23; *see, e.g., id.* at 20 ("[A]ctivity in selected test logic occurs only when certain instructions are present. For example, the RUNBIST instruction causes a self-test of the on-chip system logic to execute in this state (see 7.9)."); *see, e.g., id.* at Figs. 5-5 and 10-18; *see, e.g., id.* at 16 ("The TAP controller. This receives TCK and interprets the signals on TMS. The TAP controller generates clock or control signals or both as required for the instruction and test data registers and for other parts of the architecture."); *see, e.g., id.* at 27 ("Note also that, while the ShiftDR and ClockDR signals may be broadcast to all test data registers, distribution of the UpdateDR control signal will be controlled according to the instruction held in the instruction register such that the signal is fed only to the test data register that is selected as the serial path between TDI and TDO.").
Claim 15	
Claim limitation	**Prior Art**
15. A circuit arrangement comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, Whetsel discloses this limitation. *See, e.g.*, Whetsel at Fig. 8.
a logic component having a logic module and a built-in logic testing circuit for testing the integrity of said logic module, said logic testing circuit being coupled to said logic module and having a normal state	*See, e.g.*, Whetsel at Fig. 8; *see, e.g., id.* at 8 ("While non-testing buffers/transceivers could have been used in this circuit, 1149.1 compliant ones are implemented to provide embedded control and observability of the processors 16-bit data, 16-bit address, and control buses. The 8-bit buffers and transceivers used, like the DBMs, are members of TIs SCOPE family of testability components and are referred to as SCOPE octals."); *see, e.g., id.* at 4 ("The trace memory is a 16-bit by 1024 location static RAM. When disabled the trace memory powers down and requires minimum power to maintain its contents."); *see also* IEEE 1149.1 at 4

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and a low power state, said logic testing circuit further having a clock port, wherein the state of said logic testing circuit is responsive to a control signal applied at said clock port, wherein said logic testing circuit may be disabled to save power when testing operations are not being performed;	("The boundary-scan cells for the pins of a component are interconnected so as to form a shift-register chain around the border of the design, and this path is provided with serial input and output connections and appropriate clock and control signals."); *see, e.g., id.* at 3 ("The DBM is a 28 in device designed in compliance with the rules set forth in the IEEE 1149.1 boundary scan standard. The DBM supports all required 1149.1 boundary scan test instructions as well as a rich set of special test instructions supporting its data trace and signature analysis test operations. The data trace and signature analysis operations can operate from control input from the 1149.1 test bus or from control generated internal to the DBM."); *see, e.g.*, IEEE 1149.1 at Figs. 5-7 and 7-2; *see, e.g.*, IEEE 1149.1 at 5 ("Design-for-test features such as these can be accessed and controlled using the data path between the serial test data pins of the TAP defined by this standard. Instructions that cause internal reconfiguration of the component's system logic such that the test operation is enabled may be shifted into the component through the TAP."); *see, e.g., id.* at Figs. 5-7 and 7-2 (disclosing a state in which the boundary scan cells are disabled, and therefore in a low power state).
a configuration register for controlling said logic testing circuit, said configuration register comprising	*See, e.g.*, Whetsel at Fig. 8; *see, e.g., id.* at 8 ("While non-testing buffers/transceivers could have been used in this circuit, 1149.1 compliant ones are implemented to provide embedded control and observability of the processors 16-bit data, 16-bit address, and control buses. The 8-bit buffers and transceivers used, like the DBMs, are members of TIs SCOPE family of testability components and are referred to as SCOPE octals."); *see, e.g., id.* at 4 ("The trace memory is a 16-bit by 1024 location static RAM. When disabled the trace memory powers down and requires minimum power to maintain its contents.").
a key input disposed to receive a key signal,	*See, e.g., id.* at 6 ("The comparator is used during EQM controlled data trace and compaction test operations to detect patterns input to the DBM via the data bus and output a CTERM signal to the EQM in response to a detection."); *see, e.g., id.* at 10 ("In some monitoring applications it may be desired to trace and/or compact data words transferred between the processor and I/O, RAM, and ROM in response to a single predetermined address and/or data pattern.").
a reset input disposed to receive a reset signal,	*See, e.g.*, IEEE 1149.1 at 12 ("The optional TRST* input provides for asynchronous initialization of the TAP controller (see 5.3).").
a clock input disposed to receive a clock signal,	*See, e.g.*, Whetsel at Fig. 8; *see, e.g., id.* at 6 ("The PCI receives clock inputs from the CK1, CK2, CK3, and TCK pins...."); *see, e.g., id.* ("The PCI is programmable via input from the control register to couple one of the clock inputs or its complement to the PCI CLK output, or combine the clock inputs using Boolean AND and

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	OR functions and couple the combined clock signal or its complement to the PCI CLK output.")
a signal output coupled to the clock port of said logic testing circuit,	*See, e.g.*, Whetsel at 7 ("Also the test controller outputs test status or internal event signals off chip via the EQO pin. In the status output mode, test status signals can be output from the EQO pin to indicate, among other things: (1) test-in-progress or (2) end-of-test. These status outputs can be monitored by external controllers or testers to determine the state of the test being performed. Alternately, these test status signals can be inspected via 1149.1 instruction register scan operations."); *see, e.g., id.* ("The event signal output from the EQO pin can be used for triggering an external tester, or to input an event to a neighboring ICs EQM to initiate a test protocol operation."); *see, e.g.*, IEEE 1149.1 at Fig. 5-5.
a key logic circuit coupled to said key input and said reset input, wherein said key logic circuit generates a mode signal responsive to said key signal and said reset signal,	*See, e.g.*, Whetsel at 6 ("The EQM receives control input from the TAP, clock input from the PCI, external event input from the EQI pin, internal event input from the CTERM signal, serial data input from the TDI pin, and outputs event signals to the EQO pin and serial data to the TDO pin."); *see, e.g., id.* at 7 ("In the event output mode, the CTERM signal from the comparator can be output from the EQO pin to indicate the occurrence of an internal event. The event signal output from the EQO pin can be used for triggering an external tester, or to input an event to a neighboring ICs EQM to initiate a test protocol operation.")
wherein said mode signal is a disable signal when said reset input is triggered by said reset signal, and wherein said mode signal is an enable signal when said key signal matches a predetermined data pattern, and	*See, e.g., id.* at Fig. 8; *see also* IEEE 1149.1 at Fig. 5-1 and related text at pp. 18-23; *see, e.g., id.* at 19 ("The test logic is disabled so that normal operation of the on-chip system logic (i.e., in response to stimuli received through the system pins only) can continue unhindered. This is achieved by initializing the instruction register to contain the *IDCODE* instruction or, if the optional device identification register is not provided, the BYPASS instruction (see 6.2). No matter what the original state of the controller, it will enter *Test-Logic-Reset* when TMS is held high for at least five rising edges of TCK. The controller remains in this state while TMS is high."); *see, e.g., id.* ("Note that the TAP controller will also be forced to the Test-Logic-Reset controller state by applying a low logic level at TRST*, if such is provided, or at power-up (see 5.3)."); *see, e.g., id.* at Figs. 5-7 and 7-2; *see, e.g., id.* at 20 ("[A]ctivity in selected test logic occurs only when certain instructions are present. For example, the RUNBIST instruction causes a self-test of the on-chip system logic to execute in this state (see 7.9).").
a logic gate having inputs coupled to said clock input and said key logic circuit and an output coupled	*See, e.g.*, Whetsel. at Fig. 1; *see, e.g., id.* at 7 ("The PC1 is programmable via input from the control register to couple one of the clock inputs or its complement to the PC1 CLK output, or combine the clock inputs using Boolean AND and OR functions and couple the combined clock signal or its complement to the PCI CLK

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to said signal output, said logic gate generating at said signal output said control signal responsive to said clock signal and said mode signal; and	output.").
wherein said control signal drives said logic testing circuit to a low power state when said mode signal is said disable signal, and wherein said control signal drives said logic testing circuit to said normal state when said mode signal is said enable signal.	*See, e.g., id.* at 7 ("In the event output mode, the CTERM signal from the comparator can be output from the EQO pin to indicate the occurrence of an internal event. The event signal output from the EQO pin can be used for triggering an external tester, or to input an event to a neighboring ICs EQM to initiate a test protocol operation.")
Claim 16	
Claim limitation	**Prior Art**
16. The arrangement of claim 15 wherein said logic gate is a NOR gate, said disable signal is a logical HIGH, and said enable signal is a logic LOW.	One of skill in the art would know to use any particular logic gate appropriate for an application. *See, e.g.*, Schnaitter at Fig. 3 and Bening at Fig. 1.
Claim 17	
Claim limitation	**Prior Art**
17. The arrangement of claim 15 further comprising a clock signal source coupled to said clock input, said clock signal source generating	*See, e.g., id.* at Fig. 8. *see, e.g., id.* at 6 ("The PCI receives clock inputs from the CK1, CK2, CK3, and TCK pins...."); *see, e.g., id.* ("The PCI is programmable via input from the control register to couple one of the clock inputs or its complement to the PCI CLK output, or combine the clock inputs using Boolean AND and OR functions and couple the combined clock signal or its complement to the PCI CLK output."). One of skill in the art would know that a circuit arrangement with a clock has a clock signal source coupled to a clock

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said clock signal.	input.
Claim 19	
Claim limitation	**Prior Art**
19. The arrangement of claim 15 wherein said key input is a multi-bit digital input and wherein said predetermined data pattern is determined by the configuration of the components of said key logic circuit.	*See, e.g., id.* at 3 ("The DBM IC architecture of Figure 1 has input pins for receiving 16 data inputs (D0-15)...."); *see, e.g., id.* at 6 ("The comparator is used during EQM controlled data trace and compaction test operations to detect patterns input to the DBM via the data bus and output a CTERM signal to the EQM in response to a detection."); *see, e.g., id.* at 10 ("In some monitoring applications it may be desired to trace and/or compact data words transferred between the processor and I/O, RAM, and ROM in response to a single predetermined address and/or data pattern.").

Appendix E5
Defendants and Counterclaimants' Invalidity Contentions
Advanced Micro Devices, Inc., et al., v. Samsung Electronics Co., Ltd., et al., Case No. 3:08-CV-0986-SI

U.S. Patent No. 5,377,200 Invalidity Chart: Japanese Patent Application Publication No. 61-124875 ("JPA '875")

All asserted claims are anticipated by the JPA '875 and/or are rendered obvious by it, either alone or in combination with other prior art described below and/or listed in Section I of Defendants' and Counterclaimants' Preliminary Invalidity Contentions and/or through modifications described below. Nothing in this invalidity chart should be construed as signifying or suggesting Defendants and Counterclaimants' adoption of or acquiescence in any claim scope and/or claim construction positions taken by Plaintiffs and Counterdefendants in this litigation.

To the extent a feature of the claims may not be disclosed or suggested by JPA '875 alone, one of skill in the art would know to consider the Clock Gating references (defined below in connection with claim 2). One of skill in the art would know to implement a clock as a control signal using clock gating techniques, especially due to the importance of reducing pin-count. *See, e.g.*, Schnaitter (defined below) at 721.

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Claim 1	
Claim limitation	**Prior Art**
1. A configuration register for controlling a logic testing circuit, said logic testing circuit being coupled to a logic module for testing the integrity of said logic module, said logic testing circuit having a normal state and a low power state, said configuration register comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, JPA '875 discloses this limitation. *See, e.g.*, JPA '875 translation at 2 ("A test mode generation circuit, characterized by the fact that it comprises a control terminal for input of a control signal, a reset circuit for output of a reset code when the pulse width of the control signal which has been input with said control signal is above a certain predetermined Xμs value, and a code signal detection circuit; wherein when the pulse width of said control signal which is input with said control signal is below Xμs, detection signal is output for test mode in an internal circuit including a code signal, while detection signal is not output when the pulse width is above said Xμs signal."); *see, e.g., id.* at 3 ("In view of the problems described above, the purpose of this invention is to eliminate the deficiencies described above and provide a test mode circuit which enables a changeover to the test mode by using the customary control without increasing the number of terminals, and without causing irregular characteristics during the manufacturing process."). One of skill in the art would know that a test generation circuit would drive a testing circuit. One of skill in the art would know that a circuit that is "off" is in a low-power state. *See, e.g.*, JPA '875 at Figs. 4-5; *see, e.g.*, JPA '875 translation at 5 ("When the control signal VIN is input above the pulse width Xμs to the control register R, the pulse width detection circuit outputs detection signal T. This detection signal T stops the operation of the code signal detection circuit 3."). Figure 4 shows that TEST is the output of circuit 3. *See also* Clock Gating References (defined below in connection with claim 2).

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a key input disposed to receive a key signal;	*See, e.g.*, JPA '875 at Fig 1; *see, e.g.*, JPA '875 translation at 2 ("A test mode generation circuit, characterized by the fact that it comprises a control terminal for input of a control signal, a reset circuit for output of a reset code when the pulse width of the control signal which has been input with said control signal is above a certain predetermined Xμs value, and a code signal detection circuit; wherein when the pulse width of said control signal which is input with said control signal is below Xμs, detection signal is output for test mode in an internal circuit including a code signal, while detection signal is not output when the pulse width is above said Xμs signal."); *see, e.g., id.* at 4 ("Figure 1 shows a construction comprising a control terminal R which inputs a control signal VIN; a reset circuit 1, which outputs a reset signal RESET when the pulse width of control signal VIN input with the control signal VIN is above a predetermined value Xμs; and a code signal detection circuit, which outputs the detection signal TEST for the test mode in an internal circuit containing a code signal when the pulse width of the control signal input with the control signal VIN is less than Xμs, and which does not output the detection signal TEST when the pulse width is more than Xμs."); *see, e.g., id.* at 5 ("At this time, when the code signal is input from the input/output terminal I/O, the signal is detected by the code signal detection circuit 3, detection signal TEST is output and the test mode is implemented.").
a reset input disposed to receive a reset signal;	*See, e.g.*, JPA '875 at Fig 1; *see, e.g.*, JPA '875 translation at 2 ("A test mode generation circuit, characterized by the fact that it comprises a control terminal for input of a control signal, a reset circuit for output of a reset code when the pulse width of the control signal which has been input with said control signal is above a certain predetermined Xμs value, and a code signal detection circuit; wherein when the pulse width of said control signal which is input with said control signal is below Xμs, detection signal is output for test mode in an internal circuit including a code signal, while detection signal is not output when the pulse width is above said Xμs signal."); *see, e.g., id.* at 4 ("Figure 1 shows a construction comprising a control terminal R which inputs a control signal VIN; a reset circuit 1, which outputs a reset signal RESET when the pulse width of control signal VIN input with the control signal VIN is above a predetermined value Xμs; and a code signal detection circuit, which outputs the detection signal TEST for the test mode in an internal circuit containing a code signal when the pulse width of the control signal input with the control signal VIN is less than Xμs, and which does not output the detection signal TEST when the pulse width is more than Xμs.").
an output coupled to said logic testing circuit;	*See, e.g.*, JPA '875 at Fig 1; *see, e.g.*, JPA '875 translation at 2 ("A test mode generation circuit, characterized by the fact that it comprises a control terminal for input of a control signal, a reset circuit for output of a reset code when the pulse width of the control signal which has been input with said control signal is above a certain predetermined Xμs value, and a code signal detection circuit; wherein when the pulse width of said control

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	signal which is input with said control signal is below Xμs, detection signal is output for test mode in an internal circuit including a code signal, while detection signal is not output when the pulse width is above said Xμs signal.")
a key logic circuit coupled to said key input, said reset input, and said output, said key logic circuit generating to said logic testing circuit, through said output, a control signal responsive to said key signal and said reset signal;	*See, e.g., id.* at 5 ("At this time, when the code signal is input from the input/output terminal I/O, the signal is detected by the code signal detection circuit 3, detection signal TEST is output and the test mode is implemented.")
wherein said control signal drives said logic testing circuit to said low power state when said reset input is triggered by said reset signal; and	*See, e.g., id.* at 2 ("A test mode generation circuit, characterized by the fact that it comprises a control terminal for input of a control signal, a reset circuit for output of a reset code when the pulse width of the control signal which has been input with said control signal is above a certain predetermined Xμs value, and a code signal detection circuit; wherein when the pulse width of said control signal which is input with said control signal is below Xμs, detection signal is output for test mode in an internal circuit including a code signal, while detection signal is not output when the pulse width is above said Xμs signal."); *see, e.g., id.* at 3-4 ("The test mode generation circuit of the present invention is provided with a construction comprising a control terminal, which inputs a control signal; a reset circuit, which outputs a reset signal when the pulse width of said control signal input with said control signal is above a predetermined value Xμs; and a code signal detection circuit, which outputs a detection signal when the pulse width of said control signal input with said control signal is less than Xμs, and when the pulse width of the detection signal set for the test mode in an internal circuit containing a code signal is more than said Xμs.").
wherein said control signal drives said logic testing circuit to said normal state when said key signal matches a predetermined data pattern.	*See, e.g., id.* at 2 ("A test mode generation circuit, characterized by the fact that it comprises a control terminal for input of a control signal, a reset circuit for output of a reset code when the pulse width of the control signal which has been input with said control signal is above a certain predetermined Xμs value, and a code signal detection circuit; wherein when the pulse width of said control signal which is input with said control signal is below Xμs, detection signal is output for test mode in an internal circuit including a code signal, while detection signal is not output when the pulse width is above said Xμs signal."); *see, e.g., id.* at 3-4 ("The test mode generation circuit of the present invention is provided with a construction comprising a control terminal,

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	which inputs a control signal; a reset circuit, which outputs a reset signal when the pulse width of said control signal input with said control signal is above a predetermined value Xμs; and a code signal detection circuit, which outputs a detection signal when the pulse width of said control signal input with said control signal is less than Xμs, and when the pulse width of the detection signal set for the test mode in an internal circuit containing a code signal is more than said Xμs.").
Claim 2	
Claim limitation	**Prior Art**
2. The configuration register of claim 1 wherein said control signal is a clock signal when said key signal matches said predetermined pattern, and wherein said output is coupled to a clock port of said logic testing circuit.	*See, e.g.*, JPA '875 at Figs. 4-5; *see, e.g.*, JPA '875 translation at 3 ("In view of the problems described above, the purpose of this invention is to eliminate the deficiencies described above and provide a test mode circuit which enables a changeover to the test mode by using the customary control without increasing the number of terminals, and without causing irregular characteristics during the manufacturing process."). One of skill in the art would know that, in embodiment 1, VIN is a signal with rising and falling edges that is output via the TEST port. *See, e.g., id.* at 3-4 ("...when the pulse width of said control signal input with said control signal is above a predetermined value Xμs; and a code signal detection circuit, which outputs a detection signal when the pulse width of said control signal input with said control signal is less than Xμs, and when the pulse width of the detection signal set for the test mode in an internal circuit containing a code signal is more than said Xμs."); *see, e.g., id.* at 5 ("As was explained, a new terminal for input of test signal is not required in the two embodiments described above. Therefore, the desired effect can be obtained without having to increase the number of terminals so that only an existing terminal is used."). One of skill in the art would know that, in embodiment 2, VIN is a signal with rising and falling edges that is output via the TEST port. *See, e.g., id.* ("When the control signal VIN is input above the pulse width Xμs to the control register R, the pulse width detection circuit outputs detection signal T. This detection signal T stops the operation of the code signal detection circuit 3."). Figure 4 shows that TEST is the output of circuit 3. *See, e.g., id.* at 5 ("At this time, when the code signal is input from the input/output terminal I/O, the signal is detected by the code signal detection circuit 3, detection signal TEST is output and the test mode is implemented."). The code signal is contained in circuit 3. *See also* the following references (collectively, the "Clock Gating References"): *see, e.g.*, U.S. Patent No. 4,615,005 ("'005 patent") at Abstract ("Disclosed is a method of controlling the

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	supply of a clock signal to a logic circuit, especially, a logic circuit composed of C-MOS gates for further reducing the power consumption. According to the control method, a clock signal supply inhibit instruction is stored, so that, when this instruction is read out, the supply of the clock signal to the logic circuit is inhibited, or its level is fixed at a specific signal level. In response to the application of an interrupt signal, the clock signal having been inhibited to be supplied to the logic circuit starts to be supplied to the logic circuit again. The circuit region or regions for which the supply of the clock signal is to be inhibited can be freely selected for the purpose of control. Thus, the method is especially effective when it is desired to closely control the saving of power consumed by the logic circuit."); *see, e.g.*, Wagner, Kenneth D., *Clock System Design*, IEEE Design & Test of Computers, pp. 9-27, October 1988 ("Wagner") at 23 (two paragraphs under heading, "Clock Gating"); *see, e.g., id.* at Fig. 9; *see, e.g.*, P. Goel and M. T. McMahon, *Electronic Chip-in-Place Test*, 19th Design Automation Conference, Paper 30.1, 1982 ("Goel") at Fig. 4; *see, e.g.*, Schnaitter, William, et al., *A 0.5 GHz CMOS Digital RF Memory Chip*, IEEE Journal of Solid-State Circuits, Vol. SC-21, No. 5, pp. 720-26, October 1986 ("Schnaitter") at Figs. 3 and 4; *see, e.g.*, Bening, Lionel C., et al., *Developments in Logic Network Path Delay Analysis*, 19th Design Automation Conference, Paper 35.1, pp. 605-15, 1982 ("Bening") at Fig. 1; *see, e.g., id.* at 606 ("As an example of clock gating, in Fig. 1 the control input P is used to 'gate' the clock to flip-flop H. This provides a method for conditionally changing H's content.").
Claim 3	
Claim limitation	**Prior Art**
3. The configuration register of claim 2 further comprising a clock input coupled to a clock signal source, said clock signal being generated responsive to a signal generated by said clock signal	*See, e.g.*, JPA '875 at Figs. 4-5; *see, e.g.*, JPA '875 translation at 5 ("When the control signal VIN is input above the pulse width Xμs to the control register R, the pulse width detection circuit outputs detection signal T. This detection signal T stops the operation of the code signal detection circuit 3."). Figure 4 shows that TEST is the output of circuit 3; *see also* Clock Gating References. One of skill in the art would know that a clock signal would require the presence of a clock signal source.

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source.	
Claim 5	
Claim limitation	**Prior Art**
5. The configuration register of claim 3 further comprising a NOR gate, wherein said key logic circuit and said clock input are coupled to said output through said NOR gate.	*See* Clock Gating References. One of skill in the art would know to use any particular logic gate appropriate for an application. *See, e.g.*, Schnaitter at Fig. 3 and Bening at Fig. 1.
Claim 6	
Claim limitation	**Prior Art**
6. A circuit arrangement comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, JPA '875 discloses this limitation. *See, e.g.*, JPA '875 at Figs. 1-5.
a logic component having a logic module and a built-in logic testing circuit, said logic testing circuit being coupled to said logic module for testing the integrity of said logic module and having a normal state and a low power state, wherein said logic testing circuit may be disabled to save power when testing operations are not being performed;	*See, e.g.*, JPA '875 translation at 3 ("In view of the advancement achieved in the high integration design of semiconductor integrated circuits in recent years, the number of items that must be tested has grown and since the number of the test patterns has also been increased, this tends to increase the time period required for testing."); *see, e.g., id.* ("In view of the problems described above, the purpose of this invention is to eliminate the deficiencies described above and provide a test mode circuit which enables a changeover to the test mode by using the customary control without increasing the number of terminals, and without causing irregular characteristics during the manufacturing process."). One of skill in the art would know that a test generation circuit would drive a testing circuit. One of skill in the art would know that a circuit that is "off" is in a low-power state. *See, e.g.*, JPA '875 at Figs. 4-5; *see, e.g.*, JPA '875 translation at 5 ("When the control signal VIN is input above the pulse width Xμs to the control register R, the pulse width detection circuit outputs detection signal T. This detection signal T stops the operation of the code signal detection circuit 3."). Figure 4 shows that TEST is the output of circuit 3. *See also* Clock Gating References.
a configuration register for	*See, e.g., id.* at 2 ("A test mode generation circuit, characterized by the fact that it comprises a control terminal

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controlling said logic testing circuit, said configuration register comprising	for input of a control signal, a reset circuit for output of a reset code when the pulse width of the control signal which has been input with said control signal is above a certain predetermined Xμs value, and a code signal detection circuit; wherein when the pulse width of said control signal which is input with said control signal is below Xμs, detection signal is output for test mode in an internal circuit including a code signal, while detection signal is not output when the pulse width is above said Xμs signal."); *see, e.g.*, JPA '875 at Fig. 1.
a key input disposed to receive a key signal,	*See, e.g.*, JPA '875 at Fig 1; *see, e.g.*, JPA '875 translation at 2 ("A test mode generation circuit, characterized by the fact that it comprises a control terminal for input of a control signal, a reset circuit for output of a reset code when the pulse width of the control signal which has been input with said control signal is above a certain predetermined Xμs value, and a code signal detection circuit; wherein when the pulse width of said control signal which is input with said control signal is below Xμs, detection signal is output for test mode in an internal circuit including a code signal, while detection signal is not output when the pulse width is above said Xμs signal."); *see, e.g., id.* at 4 ("Figure 1 shows a construction comprising a control terminal R which inputs a control signal VIN; a reset circuit 1, which outputs a reset signal RESET when the pulse width of control signal VIN input with the control signal VIN is above a predetermined value Xμs; and a code signal detection circuit, which outputs the detection signal TEST for the test mode in an internal circuit containing a code signal when the pulse width of the control signal input with the control signal VIN is less than Xμs, and which does not output the detection signal TEST when the pulse width is more than Xμs."); *see, e.g., id.* at 5 ("At this time, when the code signal is input from the input/output terminal I/O, the signal is detected by the code signal detection circuit 3, detection signal TEST is output and the test mode is implemented.").
a reset input disposed to receive a reset signal,	*See, e.g.*, JPA '875 at Fig 1; *see, e.g.*, JPA '875 translation at 2 ("A test mode generation circuit, characterized by the fact that it comprises a control terminal for input of a control signal, a reset circuit for output of a reset code when the pulse width of the control signal which has been input with said control signal is above a certain predetermined Xμs value, and a code signal detection circuit; wherein when the pulse width of said control signal which is input with said control signal is below Xμs, detection signal is output for test mode in an internal circuit including a code signal, while detection signal is not output when the pulse width is above said Xμs signal."); *see, e.g., id.* at 4 ("Figure 1 shows a construction comprising a control terminal R which inputs a control signal VIN; a reset circuit 1, which outputs a reset signal RESET when the pulse width of control signal VIN input with the control signal VIN is above a predetermined value Xμs; and a code signal detection circuit, which outputs the detection signal TEST for the test mode in an internal circuit containing a code signal when the pulse width of the control signal input with the control signal VIN is less than Xμs, and which

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	does not output the detection signal TEST when the pulse width is more than Xμs.").
an output coupled to said logic testing circuit, and	*See, e.g.*, JPA '875 at Fig 1; *see, e.g.*, JPA '875 translation at 2 ("A test mode generation circuit, characterized by the fact that it comprises a control terminal for input of a control signal, a reset circuit for output of a reset code when the pulse width of the control signal which has been input with said control signal is above a certain predetermined Xμs value, and a code signal detection circuit; wherein when the pulse width of said control signal which is input with said control signal is below Xμs, detection signal is output for test mode in an internal circuit including a code signal, while detection signal is not output when the pulse width is above said Xμs signal.")
a key logic circuit coupled to said key input, said reset input, and said output, said key logic circuit generating to said logic testing circuit, through said output, a control signal responsive to said key signal and said reset signal;	*See, e.g., id.* at 5 ("At this time, when the code signal is input from the input/output terminal I/O, the signal is detected by the code signal detection circuit 3, detection signal TEST is output and the test mode is implemented.")
wherein said control signal drives said logic testing circuit to said low power state when said reset input is triggered by said reset signal; and	*See, e.g., id.* at 2 ("A test mode generation circuit, characterized by the fact that it comprises a control terminal for input of a control signal, a reset circuit for output of a reset code when the pulse width of the control signal which has been input with said control signal is above a certain predetermined Xμs value, and a code signal detection circuit; wherein when the pulse width of said control signal which is input with said control signal is below Xμs, detection signal is output for test mode in an internal circuit including a code signal, while detection signal is not output when the pulse width is above said Xμs signal."); *see, e.g., id.* at 3-4 ("The test mode generation circuit of the present invention is provided with a construction comprising a control terminal, which inputs a control signal; a reset circuit, which outputs a reset signal when the pulse width of said control signal input with said control signal is above a predetermined value Xμs; and a code signal detection circuit, which outputs a detection signal when the pulse width of said control signal input with said control signal is less than Xμs, and when the pulse width of the detection signal set for the test mode in an internal circuit containing a code signal is more than said Xμs.").
wherein said control signal drives	*See, e.g., id.* at 2 ("A test mode generation circuit, characterized by the fact that it comprises a control terminal

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said logic testing circuit to said normal state when said key signal matches a predetermined data pattern.	for input of a control signal, a reset circuit for output of a reset code when the pulse width of the control signal which has been input with said control signal is above a certain predetermined Xμs value, and a code signal detection circuit; wherein when the pulse width of said control signal which is input with said control signal is below Xμs, detection signal is output for test mode in an internal circuit including a code signal, while detection signal is not output when the pulse width is above said Xμs signal."); *see, e.g., id.* at 3-4 ("The test mode generation circuit of the present invention is provided with a construction comprising a control terminal, which inputs a control signal; a reset circuit, which outputs a reset signal when the pulse width of said control signal input with said control signal is above a predetermined value Xμs; and a code signal detection circuit, which outputs a detection signal when the pulse width of said control signal input with said control signal is less than Xμs, and when the pulse width of the detection signal set for the test mode in an internal circuit containing a code signal is more than said Xμs.").
Claim 7	
Claim limitation	**Prior Art**
7. The arrangement of claim 6 wherein said control signal is a clock signal when said key signal matches said predetermined data pattern, and wherein said output is coupled to a clock port of said logic testing circuit.	*See, e.g.*, JPA '875 at Figs. 4-5; *see, e.g.*, JPA '875 translation at 3 ("In view of the problems described above, the purpose of this invention is to eliminate the deficiencies described above and provide a test mode circuit which enables a changeover to the test mode by using the customary control without increasing the number of terminals, and without causing irregular characteristics during the manufacturing process."). One of skill in the art would know that, in embodiment 1, VIN is a signal with rising and falling edges that is output via the TEST port. *See, e.g., id.* at 3-4 ("...when the pulse width of said control signal input with said control signal is above a predetermined value Xμs; and a code signal detection circuit, which outputs a detection signal when the pulse width of said control signal input with said control signal is less than Xμs, and when the pulse width of the detection signal set for the test mode in an internal circuit containing a code signal is more than said Xμs."); *see, e.g., id.* at 5 ("As was explained, a new terminal for input of test signal is not required in the two embodiments described above. Therefore, the desired effect can be obtained without having to increase the number of terminals so that only an existing terminal is used."). One of skill in the art would know that, in embodiment 2, VIN is a signal with rising and falling edges that is output via the TEST port. *See, e.g., id.* ("When the control signal VIN is input above the pulse width Xμs to the control register R, the pulse width detection circuit outputs detection signal T. This detection signal T stops the operation of the code signal detection circuit 3."). Figure 4 shows that TEST is the output of circuit 3. *See, e.g., id.* at 5 ("At this time, when the code signal is input from the input/output terminal I/O, the signal is detected by the code signal

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	detection circuit 3, detection signal TEST is output and the test mode is implemented."). The code signal is contained in circuit 3. *See also* Clock Gating References.
Claim 8	
Claim limitation	**Prior Art**
8. The arrangement of claim 7 further comprising a clock signal source, wherein said configuration register further comprises a clock input disposed to receive said clock signal from said clock signal source.	*See* Clock Gating References.
Claim 11	
Claim limitation	**Prior Art**
11. The arrangement of claim 6 wherein said logic testing circuit has a clock port and wherein the state of said logic testing circuit is responsive to a signal at said clock port.	*See, e.g.*, JPA '875 at Figs. 4-5; *see, e.g.*, JPA '875 translation at 5 ("When the control signal VIN is input above the pulse width Xμs to the control register R, the pulse width detection circuit outputs detection signal T. This detection signal T stops the operation of the code signal detection circuit 3."). Figure 4 shows that TEST is the output of circuit 3; *see also* Clock Gating References.
Claim 12	
Claim limitation	**Prior Art**
12. The arrangement of claim 11 wherein said output is coupled to said clock port, said logic testing circuit is driven to said low power state when a LOW is applied to a clock port, and wherein said control	*See, e.g.*, JPA '875 at Figs. 4-5; *see, e.g.*, JPA '875 translation at 5 ("When the control signal VIN is input above the pulse width Xμs to the control register R, the pulse width detection circuit outputs detection signal T. This detection signal T stops the operation of the code signal detection circuit 3."). Figure 4 shows that TEST is the output of circuit 3.

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signal is LOW when said reset input is triggered by said reset signal.	
Claim 13	
Claim limitation	**Prior Art**
13. The arrangement of claim 11 wherein said output is coupled to said clock port, said logic testing circuit is driven to said normal state when a clock signal is applied to a clock port, and wherein said control signal is a clock signal when said key signal matches said predetermined data pattern.	*See, e.g.*, JPA '875 translation at 2 ("...wherein when the pulse width of said control signal which is input with said control signal is below Xμs, detection signal is output for test mode in an internal circuit including a code signal, while detection signal is not output when the pulse width is above said Xμs signal."); *see, e.g., id.* at 4 ("When the input signal VIN which is input to a control terminal R is above a pulse width Xμs, the reset circuit 1 is operated and reset signal RESET is output. If the signal is below Xμs, the reset circuit 1 is not operated. On the other hand, when the pulse width of the control signal VIN in the code signal detection circuit 5 is less than Xμs and a code signal is contained which generates the test mode in the control signal, this is detected, detection signal TEST is output and the mode in the internal circuit is switched to the test mode. When the pulse width is above Xμs, the code signal detection circuit 5 is not operated. Accordingly, the detection signal is not output. The code signal can be determined within the Xμs time period for instance as '010', although '101' can be also determined, as this can be set at will."); *see, e.g., id.* at 5 ("When the control signal VIN is input above the pulse width Xμs to the control register R, the pulse width detection circuit outputs detection signal T. This detection signal T stops the operation of the code signal detection circuit 3. In addition, the detection signal T is inverted by an inverter 10, an inverted detection signal T is generated and the operation of the input/output circuit 11 is stopped. Since the reset circuit 1 is operated above the pulse width Xμs, the reset signal RESET is output."). Figure 4 shows that TEST is the output of circuit 3. *See also, e.g., id.* ("At this time, when the code signal is input from the input/output terminal I/O, the signal is detected by the code signal detection circuit 3, detection signal TEST is output and the test mode is implemented."). The code signal is contained in circuit 3. *See also, e.g.*, JPA '875 at Figs. 1, 3-5; *see, e.g.*, JPA '875 translation at 3 ("In view of the problems described above, the purpose of this invention is to eliminate the deficiencies described above and provide a test mode circuit which enables a changeover to the test mode by using the customary control without increasing the number of terminals, and without causing irregular characteristics during the manufacturing process."). One of skill in the art would know that, in embodiment 1, VIN is a signal with rising and falling edges that is output via the TEST port. *See, e.g., id.* at 3-4 ("...when the pulse width of said control signal input with said control signal is above a predetermined value Xμs; and a code signal detection circuit, which outputs a detection signal when the pulse width of said control signal input with said control

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	signal is less than Xμs, and when the pulse width of the detection signal set for the test mode in an internal circuit containing a code signal is more than said Xμs."); *see, e.g., id.* at 5 ("As was explained, a new terminal for input of test signal is not required in the two embodiments described above. Therefore, the desired effect can be obtained without having to increase the number of terminals so that only an existing terminal is used."). One of skill in the art would know that, in embodiment 2, VIN is a signal with rising and falling edges that is output via the TEST port. One of skill in the art would know that a special case of a signal with rising and falling edges can be a clock signal. One of skill in the art would know that JPA '875 discloses that when the code signal stored in code signal detection 3 detects the code applied to key input VIN1, the TEST signal is applied, which is VIN passed in some form to the TEST output. One of skill in the art would know that TEST can be a clock signal. *See also* Clock Gating References.
Claim 15	
Claim limitation	**Prior Art**
15. A circuit arrangement comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, JPA '875 discloses this limitation. *See, e.g.*, JPA '875 at Figs. 1-5.
a logic component having a logic module and a built-in logic testing circuit for testing the integrity of said logic module, said logic testing circuit being coupled to said logic module and having a normal state and a low power state, said logic testing circuit further having a clock port, wherein the state of said logic testing circuit is responsive to a control signal applied at said clock port, wherein said logic testing circuit may be disabled to save power when testing operations are	*See, e.g.*, JPA '875 translation at 3 ("In view of the advancement achieved in the high integration design of semiconductor integrated circuits in recent years, the number of items that must be tested has grown and since the number of the test patterns has also been increased, this tends to increase the time period required for testing."); *see, e.g., id.* ("In view of the problems described above, the purpose of this invention is to eliminate the deficiencies described above and provide a test mode circuit which enables a changeover to the test mode by using the customary control without increasing the number of terminals, and without causing irregular characteristics during the manufacturing process."). One of skill in the art would know that a test generation circuit would drive a testing circuit. One of skill in the art would know that a circuit that is "off" is in a low-power state. *See, e.g.*, JPA '875 at Figs. 4-5; *see, e.g.*, JPA '875 translation at 5 ("When the control signal VIN is input above the pulse width Xμs to the control register R, the pulse width detection circuit outputs detection signal T. This detection signal T stops the operation of the code signal detection circuit 3."). Figure 4 shows that TEST is the output of circuit 3. *See also* Clock Gating References.

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not being performed;	
a configuration register for controlling said logic testing circuit, said configuration register comprising	*See, e.g., id.* at 2 ("A test mode generation circuit, characterized by the fact that it comprises a control terminal for input of a control signal, a reset circuit for output of a reset code when the pulse width of the control signal which has been input with said control signal is above a certain predetermined Xμs value, and a code signal detection circuit; wherein when the pulse width of said control signal which is input with said control signal is below Xμs, detection signal is output for test mode in an internal circuit including a code signal, while detection signal is not output when the pulse width is above said Xμs signal."); *see, e.g.*, JPA '875 at Fig. 1.
a key input disposed to receive a key signal,	*See, e.g.*, JPA '875 at Fig 1; *see, e.g.*, JPA '875 translation at 2 ("A test mode generation circuit, characterized by the fact that it comprises a control terminal for input of a control signal, a reset circuit for output of a reset code when the pulse width of the control signal which has been input with said control signal is above a certain predetermined Xμs value, and a code signal detection circuit; wherein when the pulse width of said control signal which is input with said control signal is below Xμs, detection signal is output for test mode in an internal circuit including a code signal, while detection signal is not output when the pulse width is above said Xμs signal."); *see, e.g., id.* at 4 ("Figure 1 shows a construction comprising a control terminal R which inputs a control signal VIN; a reset circuit 1, which outputs a reset signal RESET when the pulse width of control signal VIN input with the control signal VIN is above a predetermined value Xμs; and a code signal detection circuit, which outputs the detection signal TEST for the test mode in an internal circuit containing a code signal when the pulse width of the control signal input with the control signal VIN is less than Xμs, and which does not output the detection signal TEST when the pulse width is more than Xμs."); *see, e.g., id.* at 5 ("At this time, when the code signal is input from the input/output terminal I/O, the signal is detected by the code signal detection circuit 3, detection signal TEST is output and the test mode is implemented.").
a reset input disposed to receive a reset signal,	*See, e.g.*, JPA '875 at Fig 1; *see, e.g.*, JPA '875 translation at 2 ("A test mode generation circuit, characterized by the fact that it comprises a control terminal for input of a control signal, a reset circuit for output of a reset code when the pulse width of the control signal which has been input with said control signal is above a certain predetermined Xμs value, and a code signal detection circuit; wherein when the pulse width of said control signal which is input with said control signal is below Xμs, detection signal is output for test mode in an internal circuit including a code signal, while detection signal is not output when the pulse width is above said Xμs signal."); *see, e.g., id.* at 4 ("Figure 1 shows a construction comprising a control terminal R which inputs a control signal VIN; a reset circuit 1, which outputs a reset signal RESET when the pulse width of control

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	signal VIN input with the control signal VIN is above a predetermined value Xμs; and a code signal detection circuit, which outputs the detection signal TEST for the test mode in an internal circuit containing a code signal when the pulse width of the control signal input with the control signal VIN is less than Xμs, and which does not output the detection signal TEST when the pulse width is more than Xμs.").
a clock input disposed to receive a clock signal,	*See, e.g.*, JPA '875 at Figs. 1 and 4; *see* Clock Gating References.
a signal output coupled to the clock port of said logic testing circuit,	*See, e.g.* JPA '875 at Fig. 4; *see* Clock Gating References.
a key logic circuit coupled to said key input and said reset input, wherein said key logic circuit generates a mode signal responsive to said key signal and said reset signal,	*See, e.g.*, JPA '875 translation at 5 ("At this time, when the code signal is input from the input/output terminal I/O, the signal is detected by the code signal detection circuit 3, detection signal TEST is output and the test mode is implemented.")
wherein said mode signal is a disable signal when said reset input is triggered by said reset signal, and wherein said mode signal is an enable signal when said key signal matches a predetermined data pattern, and	*See, e.g.*, JPA '875 translation at 2 ("A test mode generation circuit, characterized by the fact that it comprises a control terminal for input of a control signal, a reset circuit for output of a reset code when the pulse width of the control signal which has been input with said control signal is above a certain predetermined Xμs value, and a code signal detection circuit; wherein when the pulse width of said control signal which is input with said control signal is below Xμs, detection signal is output for test mode in an internal circuit including a code signal, while detection signal is not output when the pulse width is above said Xμs signal."); *see, e.g., id.* at 4 ("Figure 1 shows a construction comprising a control terminal R which inputs a control signal VIN; a reset circuit 1, which outputs a reset signal RESET when the pulse width of control signal VIN input with the control signal VIN is above a predetermined value Xμs; and a code signal detection circuit, which outputs the detection signal TEST for the test mode in an internal circuit containing a code signal when the pulse width of the control signal input with the control signal VIN is less than Xμs, and which does not output the detection signal TEST when the pulse width is more than Xμs."); *see, e.g.*, JPA '875 at Fig. 1.
a logic gate having inputs coupled	*See, e.g.*, JPA '875 at Figs. 1, 4-5; *see, e.g.*, JPA '875 translation at 3 ("In view of the problems described

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to said clock input and said key logic circuit and an output coupled to said signal output, said logic gate generating at said signal output said control signal responsive to said clock signal and said mode signal; and	above, the purpose of this invention is to eliminate the deficiencies described above and provide a test mode circuit which enables a changeover to the test mode by using the customary control without increasing the number of terminals, and without causing irregular characteristics during the manufacturing process."). One of skill in the art would know that, in embodiment 1, VIN is a signal with rising and falling edges that is output via the TEST port. *See, e.g., id.* at 3-4 ("...when the pulse width of said control signal input with said control signal is above a predetermined value Xμs; and a code signal detection circuit, which outputs a detection signal when the pulse width of said control signal input with said control signal is less than Xμs, and when the pulse width of the detection signal set for the test mode in an internal circuit containing a code signal is more than said Xμs."); *see, e.g., id.* at 5 ("As was explained, a new terminal for input of test signal is not required in the two embodiments described above. Therefore, the desired effect can be obtained without having to increase the number of terminals so that only an existing terminal is used."). One of skill in the art would know that, in embodiment 2, VIN is a signal with rising and falling edges that is output via the TEST port. *See, e.g., id.* ("When the control signal VIN is input above the pulse width Xμs to the control register R, the pulse width detection circuit outputs detection signal T. This detection signal T stops the operation of the code signal detection circuit 3."). Figure 4 shows that TEST is the output of circuit 3. *See, e.g., id.* at 5 ("At this time, when the code signal is input from the input/output terminal I/O, the signal is detected by the code signal detection circuit 3, detection signal TEST is output and the test mode is implemented."). The code signal is contained in circuit 3. *See also* Clock Gating References.
wherein said control signal drives said logic testing circuit to a low power state when said mode signal is said disable signal, and wherein said control signal drives said logic testing circuit to said normal state when said mode signal is said enable signal.	*See, e.g., id.* at 2 ("A test mode generation circuit, characterized by the fact that it comprises a control terminal for input of a control signal, a reset circuit for output of a reset code when the pulse width of the control signal which has been input with said control signal is above a certain predetermined Xμs value, and a code signal detection circuit; wherein when the pulse width of said control signal which is input with said control signal is below Xμs, detection signal is output for test mode in an internal circuit including a code signal, while detection signal is not output when the pulse width is above said Xμs signal."); *see, e.g., id.* at 3-4 ("The test mode generation circuit of the present invention is provided with a construction comprising a control terminal, which inputs a control signal; a reset circuit, which outputs a reset signal when the pulse width of said control signal input with said control signal is above a predetermined value Xμs; and a code signal detection circuit, which outputs a detection signal when the pulse width of said control signal input with said control signal is less than Xμs, and when the pulse width of the detection signal set for the test mode in an internal circuit containing a code signal is more than said Xμs.").

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Claim 16	
Claim limitation	**Prior Art**
16. The arrangement of claim 15 wherein said logic gate is a NOR gate, said disable signal is a logical HIGH, and said enable signal is a logic LOW.	*See* Clock Gating References. One of skill in the art would know to use any particular logic gate appropriate for an application. *See, e.g.*, Schnaitter at Fig. 3 and Bening at Fig. 1.
Claim 17	
Claim limitation	**Prior Art**
17. The arrangement of claim 15 further comprising a clock signal source coupled to said clock input, said clock signal source generating said clock signal.	*See, e.g.*, JPA '875 at Figs. 4-5; *see, e.g.*, JPA '875 translation at 5 ("When the control signal VIN is input above the pulse width Xμs to the control register R, the pulse width detection circuit outputs detection signal T. This detection signal T stops the operation of the code signal detection circuit 3."). Figure 4 shows that TEST is the output of circuit 3; *see also* Clock Gating References. One of skill in the art would know that a clock signal would require the presence of a clock signal source.
Claim 19	
Claim limitation	**Prior Art**
19. The arrangement of claim 15 wherein said key input is a multi-bit digital input and wherein said predetermined data pattern is determined by the configuration of the components of said key logic circuit.	*See, e.g., id.* at 4 ("The code signal can be determined within the Xμs time period for instance as '010', although '101' can be also determined, as this can be set at will."); *see, e.g., id.* at 5 ("At this time, when the code signal is input from the input/output terminal I/O, the signal is detected by the code signal detection circuit 3, detection signal TEST is output and the test mode is implemented."). One of skill in the art would know that a key input need not be limited to a single bit, *e.g.*, one of skill in the art would know that JPA '875 does not limit VIN1 to a single bit and that key logic circuit, block 3, would compare VIN1 to said code signal. *See also* Schnaitter at 721 (in RAM mode, RAM controlled by multiple external pins.).