EXHIBIT 1

F1-F4

Appendix F1
Defendants and Counterclaimants' Invalidity Contentions
Advanced Micro Devices, Inc. et al. v. Samsung Electronics Co., Ltd. et al., Case No. CV-08-0986-SI

U.S. Patent No. 5,623,434 Invalidity Chart: U.S. Patent No. 4,866,652 ("the '652 patent")

All asserted claims are anticipated by U.S. Patent No. 4,866,652 and/or are rendered obvious by it, either alone or in combination with other prior art described below and/or listed in Section I of Defendants and Counterclaimants' Preliminary Invalidity Contentions and/or through modifications described below. Nothing in this invalidity chart should be construed as signifying or suggesting Defendants and Counterclaimants' adoption of or acquiescence in any claim scope and/or claim construction positions taken by Plaintiffs and Counterdefendants in this litigation.

U.S. Patent No. 5,623,434	
Claim 1	
Claim limitation	**'652 Patent**
1. A multiplier for use in a data processing system having an arithmetic and logic unit (ALU), said multiplier comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, the '652 patent discloses this limitation. *See, e.g.*, col. 1, lines 31-37 ("The present invention is a method and apparatus for combining the multiply and ALU functions for floating point numbers to enable the completion of the multiply-accumulate operation in a shorter time. The multiplied fraction is left in sum and carry form and is provided in this form to the ALU, eliminating the carry propagate adder from the multiplier.") col. 2, lines 14-15 ("FIG. 3 is a block diagram of a combined multiplier and ALU according to the present invention.); col. 3, lines 4-10 ("Fraction multiplier 79 contains a pair of registers 80, 81 for receiving the two multiplicand inputs which are then multiplied in an array 82. As can be seen, fraction multiplier 76 does not include CP adder 46 or normalizing circuit 48 of FIG. 2. Instead, the fractional sum and carry are provided to multiplexers 86 and 88 in a fractional ALU circuit 84."); FIG. 3 (reproduced below):

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	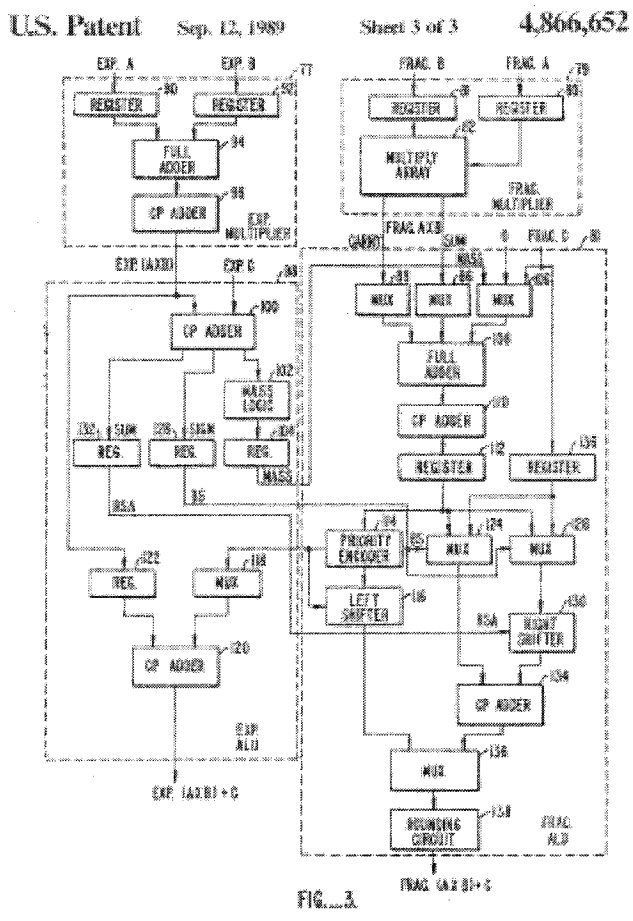 FIG. 3.
a first input terminal for receiving a first data value;	The '652 patent discloses this limitation.

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	See, e.g., FIG. 3 (reproduced above, showing FRAC. A); col. 3, line 4-6 ("Fraction multiplier 79 contains a pair of registers 80, 81 for receiving the two multiplicand inputs . . . .").
a second input terminal for receiving a second data value;	The '652 patent discloses this limitation. *See, e.g.*, FIG. 3 (reproduced above, showing FRAC. B); col. 3, line 4-6 ("Fraction multiplier 79 contains a pair of registers 80, 81 for receiving the two multiplicand inputs . . . .").
a carry save stage coupled to said first and second terminals, wherein said carry save stage generates a carry signal and a sum signal in response to said first and second data values;	The '652 patent discloses this limitation. *See, e.g.*, FIG. 3 (reproduced above, showing FRAC. MULTIPLIER); col. 1, lines 34-35 ("The multiplied fraction is left in sum and carry form . . . ."); col. 3, lines 4-10 ("Fraction multiplier 79 contains a pair of registers 80, 81 for receiving the two multiplicand inputs which are then multiplied in an array 82. As can be seen, fraction multiplier 76 does not include CP adder 46 or normalizing circuit 48 of FIG. 2. Instead, the fractional sum and carry are provided to multiplexers 86 and 88 in a fractional ALU circuit 84.").
a first bus coupling said carry save stage to said ALU, wherein said first bus provides said carry signal to said ALU;	The '652 patent discloses this limitation. *See, e.g.*, FIG. 3 (reproduced above, showing CARRY); col. 3, lines 9-10 ("[T]he fractional sum and carry are provided to multiplexers 86 and 88 in a fractional ALU circuit 84.").
a second bus coupling said carry save stage to said ALU, wherein said second bus	The '652 patent discloses this limitation.

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provides said sum signal to said ALU;	*See, e.g.*, FIG. 3 (reproduced above, showing SUM); col. 3, lines 9-10 ("[T]he fractional sum and carry are provided to multiplexers 86 and 88 in a fractional ALU circuit 84.")
a first multiplexer coupled between said first bus and said ALU; and	The '652 patent discloses this limitation. *See, e.g.*, FIG. 3 (reproduced above, showing MUX 88); col. 3, lines 9-10 ("[T]he fractional sum and carry are provided to multiplexers 86 and 88 in a fractional ALU circuit 84.")
a second multiplexer coupled between said second bus and said ALU,	The '652 patent discloses this limitation. *See, e.g.*, FIG. 3 (reproduced above, showing MUX 86); col. 3, lines 9-10 ("[T]he fractional sum and carry are provided to multiplexers 86 and 88 in a fractional ALU circuit 84.")
whereby said ALU is capable of adding said carry and sum signals to create a third data value equal to the product of said first and second data values.	The '652 patent discloses this limitation. *See, e.g.*, FIG. 3 (reproduced above, showing that output of ALU is the product of FRAC. A and FRAC. B); col. 1, lines 34-37 ("The multiplied fraction is left in sum and carry form and is provided in this form to the ALU, eliminating the carry propagate adder from the multiplier."); col. 3, lines 9-10 ("[T]he fractional sum and carry are provided to multiplexers 86 and 88 in a fractional ALU circuit 84.")
Claim 2	

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2. The multiplier of claim 1, further comprising:	
a third bus coupled between said first terminal and said first multiplexer; and	The '652 patent discloses this limitation. *See, e.g.*, FIG. 3 (reproduced above); col. 1, lines 22-24 ("The arithmetic and logic unit can receive two numbers for addition or subtraction, one of which numbers could be the result of a multiply operation."); col. 3, lines 9-12 ("[T]he fractional sum and carry are provided to multiplexers 86 and 88 in a fractional ALU circuit 84. The other inputs of these multiplexers are unrelated to the present invention and thus are not shown.").
a fourth bus coupled between said second terminal and said second multiplexer.	The '652 patent discloses this limitation. *See, e.g.*, FIG. 3 (reproduced above); col. 1, lines 22-24 ("The arithmetic and logic unit can receive two numbers for addition or subtraction, one of which numbers could be the result of a multiply operation."); col. 3, lines 9-12 ("[T]he fractional sum and carry are provided to multiplexers 86 and 88 in a fractional ALU circuit 84. The other inputs of these multiplexers are unrelated to the present invention and thus are not shown.").
Claim 3	
3. The multiplier of claim 2, further comprising:	
a first register coupled between said first multiplexer and said ALU, wherein said carry signal is stored in said first register;	The '652 patent discloses this limitation. When reading the '652 patent, a person of ordinary skill in the art would understand that a register would be inherent and/or obvious to the design of an ALU in a

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and	system. *See, e.g.*, FIG. 3 (reproduced above, standard industry practice includes a storage element before the ALU).
a second register coupled between said second multiplexer and said ALU, wherein said sum signal is stored in said second register.	The '652 patent discloses this limitation. When reading the '652 patent, a person of ordinary skill in the art would understand that a register would be inherent and/or obvious to the design of an ALU in a system. *See, e.g.*, FIG. 3 (reproduced above, standard industry practice includes a storage element before the ALU).
Claim 4	
4. The multiplier of claim 2, further comprising	
multiplexer select means coupled to said first and second multiplexers,	The '652 patent discloses this limitation. *See, e.g.*, FIG. 3 (reproduced above, MUX 88 and 86 will have select means as a multiplexer by definition has a selector circuit).
said multiplexer select means having a first state and a second state,	The '652 patent discloses this limitation, as it discloses multiplexers and all multiplexers require a select means that has at least two states. *See,* e.g., col. 3, lines 9-12 ("[T]he fractional sum and carry are provided to multiplexers 86 and 88 in a fractional ALU circuit 84. The other inputs of these multiplexers are unrelated to the present invention and thus are not shown.").
wherein said multiplexer select means causes said first multiplexer to route said carry signal to said ALU and causes said second multiplexer to route said sum signal	The '652 patent discloses this limitation. *See, e.g.*, FIG. 3 (reproduced above, showing routing of carry and sum to ALU);

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to said ALU when said multiplexer select means is in said first state, and	col. 1, lines 39-41 ("The ALU can combine the sum and carry of the product fraction simultaneously . . . .")
wherein said multiplexer select means causes said first multiplexer to route said first data value to said ALU and causes said second multiplexer to route said second data value to said ALU when said multiplexer select means is in said second state.	The '652 patent discloses this limitation. *See, e.g.*, col. 3, lines 9-12 ("[T]he fractional sum and carry are provided to multiplexers 86 and 88 in a fractional ALU circuit 84. The other inputs of these multiplexers are unrelated to the present invention and thus are not shown."). FIG. 1 (These other inputs can be the first and second data values as shown in FIG. 1, where the ALU with its multiplexers coupled to A Bus and B Bus can via select means input first and second input values).
Claim 8	
8. A multiplier for use in a system having an arithmetic and logic unit (ALU), said multiplier comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, the '652 patent discloses this limitation. *See, e.g.*, col. 1, lines 31-37 ("The present invention is a method and apparatus for combining the multiply and ALU functions for floating point numbers to enable the completion of the multiply-accumulate operation in a shorter time. The multiplied fraction is left in sum and carry form and is provided in this form to the ALU, eliminating the carry propagate adder from the multiplier.") col. 2, lines 14-15 ("FIG. 3 is a block diagram of a combined multiplier and ALU according to the present invention.); col. 3, lines 4-10 ("Fraction multiplier 79 contains a pair of registers 80, 81 for receiving the two multiplicand inputs which are then multiplied in an array 82. As can be seen, fraction multiplier 76 does not include CP adder 46 or normalizing circuit 48 of FIG. 2. Instead, the fractional sum and carry are provided to multiplexers 86 and 88 in a fractional ALU circuit 84."); FIG. 3 (reproduced above).

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a first input terminal for receiving a first data value;	The '652 patent discloses this limitation. *See, e.g.*, FIG. 3 (reproduced above, showing FRAC. A); col. 3, line 4-6 ("Fraction multiplier 79 contains a pair of registers 80, 81 for receiving the two multiplicand inputs . . . .")
a second input terminal for receiving a second data value;	The '652 patent discloses this limitation. *See, e.g.*, FIG. 3 (reproduced above, showing FRAC. B); col. 3, line 4-6 ("Fraction multiplier 79 contains a pair of registers 80, 81 for receiving the two multiplicand inputs . . . .")
a carry save stage coupled to said first and second terminals, wherein said carry save stage generates a carry signal and a sum signal in response to said first and second data values;	The '652 patent discloses this limitation. *See, e.g.*, FIG. 3 (reproduced above, showing FRAC. MULTIPLIER); col. 3, lines 4-10 ("Fraction multiplier 79 contains a pair of registers 80, 81 for receiving the two multiplicand inputs which are then multiplied in an array 82. As can be seen, fraction multiplier 76 does not include CP adder 46 or normalizing circuit 48 of FIG. 2. Instead, the fractional sum and carry are provided to multiplexers 86 and 88 in a fractional ALU circuit 84.").
means for coupling said carry save stage and said first and second input terminals to said ALU, wherein said carry and sum signals and said first and second data values are transmitted to said ALU, whereby said ALU is capable of adding said carry and sum signals to provide a third data value equal to the product of said first and second data	The '652 patent discloses this limitation, which is subject to 35 U.S.C. § 112, ¶ 6. The claimed function is "coupling said carry save stage and said first and second input terminals to said ALU." The '652 patent implements this function via the multiplier shown in FIG. 3 and the system shown in FIG. 1. *See, e.g.*, FIG. 3 (reproduced above); col. 2, lines 14-15 ("FIG. 3 is a block diagram of a combined multiplier and ALU according to the present invention.);

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values; and	col. 2, lines 10-11 ("FIG. 1 is a block diagram of a three port chip which can incorporate the structure of the present invention"); col. 3, lines 9-10 ("[T]he fractional sum and carry are provided to multiplexers 86 and 88 in a fractional ALU circuit 84."); col. 1, lines 34-37 ("The multiplied fraction is left in sum and carry form and is provided in this form to the ALU, eliminating the carry propagate adder from the multiplier."); col. 1, lines 39-41 ("The ALU can combine the sum and carry of the product fraction simultaneously . . . .")
means for controlling said means for coupling, said means for controlling having a first and a second state, wherein in said first state said means for controlling causes said means for coupling to route said carry and sum signals to said ALU and to prevent said means for coupling from routing said first and second data values to said ALU, and wherein in said second state said means for controlling causes said means for coupling to route said first and second data values to said ALU and to prevent said means for coupling from routing said carry and sum signals to said ALU.	The '652 patent discloses this limitation, which is subject to 35 U.S.C. § 112, ¶ 6. The claimed function is "controlling said means for coupling." The means for controlling is performed by a selector circuit in the '652 patent, which is entailed by the presence of multiplexers. *See, e.g.*, FIG. 3 (reproduced above, MUX 88 and 86 will have select means as a multiplexer by definition has a selector circuit); col. 3, lines 9-12 ("[T]he fractional sum and carry are provided to multiplexers 86 and 88 in a fractional ALU circuit 84. The other inputs of these multiplexers are unrelated to the present invention and thus are not shown.").
Claim 11	
11. A system comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, the '652 patent discloses this limitation.

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	See, e.g., FIG. 1; col. 2, lines 10-11 ("FIG. 1 is a block diagram of a three port chip which can incorporate the structure of the present invention").
a carry save stage coupled to receive a first data value and a second data value, wherein the carry save stage generates a carry signal and a sum signal in response to the first and second data values;	The '652 patent discloses this limitation. *See, e.g.*, FIG. 3 (reproduced above, showing FRAC. A, FRAC. B, and FRAC. MULTIPLIER); col. 3, lines 4-10 ("Fraction multiplier 79 contains a pair of registers 80, 81 for receiving the two multiplicand inputs which are then multiplied in an array 82. As can be seen, fraction multiplier 76 does not include CP adder 46 or normalizing circuit 48 of FIG. 2. Instead, the fractional sum and carry are provided to multiplexers 86 and 88 in a fractional ALU circuit 84.").
a first selector circuit coupled to receive the carry signal and the first data value;	The '652 patent discloses this limitation. *See, e.g.*, FIG. 3 (reproduced above, showing CARRY and MUX 88); col. 3, lines 9-10 ("[T]he fractional sum and carry are provided to multiplexers 86 and 88 in a fractional ALU circuit 84.").
a second selector circuit coupled to receive the sum signal and the second data value;	The '652 patent discloses this limitation. *See, e.g.*, FIG. 3 (reproduced above, showing SUM and MUX 86); col. 3, lines 9-10 ("[T]he fractional sum and carry are provided to multiplexers 86 and 88 in a fractional ALU circuit 84.").
a control signal source coupled to the first and second selector circuits, wherein the control signal source causes the first and second selector circuits to operate in a first mode and a second mode, wherein in the	The '652 patent discloses this limitation. *See, e.g.*, FIG. 3 (reproduced above, showing selector circuits which require a control source);

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first mode, the first selector circuit passes the carry signal and the second selector circuit passes the sum signal, and wherein in the second mode, the first selector circuit passes the first data value and the second selector circuit passes the second data value; and	FIG. 1 (showing existence of control signal source); col. 3, lines 9-12 ("[T]he fractional sum and carry are provided to multiplexers 86 and 88 in a fractional ALU circuit 84. The other inputs of these multiplexers are unrelated to the present invention and thus are not shown.").
an arithmetic and logic unit (ALU) coupled to the first and second selector circuits, wherein the ALU receives the signals passed by the first and second selector circuits, and wherein in the first mode, the ALU adds the carry and sum signals to create a third data value equal to the product of the first and second data values.	The '652 patent discloses this limitation. *See, e.g.*, FIG. 3 (reproduced above); col. 3, lines 9-10 ("[T]he fractional sum and carry are provided to multiplexers 86 and 88 in a fractional ALU circuit 84."); col. 1, lines 34-37 ("The multiplied fraction is left in sum and carry form and is provided in this form to the ALU, eliminating the carry propagate adder from the multiplier."); col. 1, lines 39-41 ("The ALU can combine the sum and carry of the product fraction simultaneously . . . .").

Appendix F2
Defendants and Counterclaimants' Invalidity Contentions
Advanced Micro Devices, Inc. et al. v. Samsung Electronics Co., Ltd. et al., Case No. CV-08-0986-SI

U.S. Patent No. 5,623,434 Invalidity Chart: Japanese Unexamined Patent Publication No. 5-341964 ("Izumikawa '964")

All asserted claims are anticipated by Japanese Unexamined Patent Publication No. 5-341964 and/or are rendered obvious by it, either alone or in combination with other prior art described below and/or listed in Section I of Defendants and Counterclaimants' Preliminary Invalidity Contentions and/or through modifications described below. Nothing in this invalidity chart should be construed as signifying or suggesting Defendants and Counterclaimants' adoption of or acquiescence in any claim scope and/or claim construction positions taken by Plaintiffs and Counterdefendants in this litigation.

To the extent a feature of the claims may not be disclosed or suggested by the Izumikawa '964 alone, one of ordinary skill in the art would have been motivated to combine the disclosed references to arrive at the patented inventions for multiple reasons, including (1) because these references address the subject matter, multiplier circuitry, acknowledged as prior art in the '434 patent; (2) because these references address similar problems to those purportedly addressed by the '434 patent; (3) because there were similar improvements in similar prior art devices, as disclosed in these references and in Defendants and Counterclaimants other claim charts for the '434 patent; (4) because the alleged invention discloses predictable variations of the inventions disclosed in these references; and (5) based on the knowledge or common sense of one of ordinary skill in the art.

U.S. Patent No. 5,623,434	
Claim 1	
Claim limitation	**Izumikawa '964**
1. A multiplier for use in a data processing system having an arithmetic and logic unit (ALU), said multiplier comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, Izumikawa '964 discloses this limitation. *See, e.g.*, translation at 2 ("The invention relates to a multiplication method that is realized on a microprocessor chip."); translation at 3 ("In FIG. 2, 2 is a latch, 3 is a circuit that carries out input-output/bypass control of the I-O data, 7 is a carry save adder (CSA) group, 8 is an ALU, 9 is a shifter, 10 is a bus for source 1 (Src 1), 11 is a bus for source 2 (Src 2), and 12 is a bus for results."); translation at 4 ("(FIG. 2) This is a diagram showing the configuration of the data bus, including the multiplier.");

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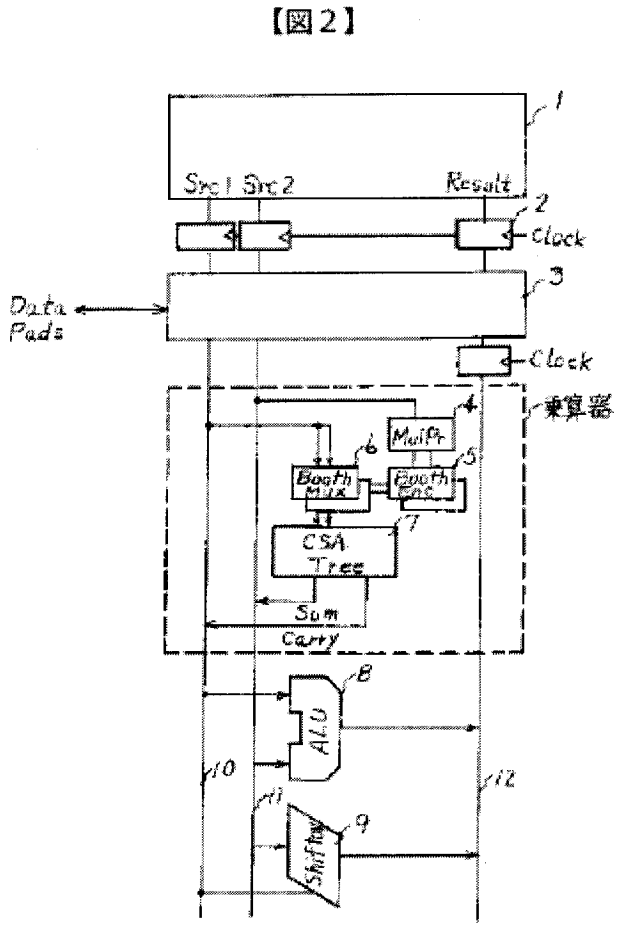
	FIG. 2 (reproduced below): 

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	translation of FIG. 2 ("[three characters at right:] Multiplier").
a first input terminal for receiving a first data value;	Izumikawa '964 discloses this limitation. *See, e.g.*, FIG. 2 (reproduced above); translation at 3 ("In FIG. 2, 2 is a latch, 3 is a circuit that carries out input-output/bypass control of the I-O data, 7 is a carry save adder (CSA) group, 8 is an ALU, 9 is a shifter, 10 is a bus for source 1 (Src 1), 11 is a bus for source 2 (Src 2), and 12 is a bus for results.").
a second input terminal for receiving a second data value;	Izumikawa '964 discloses this limitation. *See, e.g.*, FIG. 2 (reproduced above) ; translation at 3 ("In FIG. 2, 2 is a latch, 3 is a circuit that carries out input-output/bypass control of the I-O data, 7 is a carry save adder (CSA) group, 8 is an ALU, 9 is a shifter, 10 is a bus for source 1 (Src 1), 11 is a bus for source 2 (Src 2), and 12 is a bus for results.").
a carry save stage coupled to said first and second terminals, wherein said carry save stage generates a carry signal and a sum signal in response to said first and second data values;	Izumikawa '964 discloses this limitation. *See, e.g.*, FIG. 2 (reproduced above, showing carry save stage along with sum and carry signals); translation of FIG. 2 ("[three characters at right:] Multiplier"); translation at 3 ("In FIG. 2, 2 is a latch, 3 is a circuit that carries out input-output/bypass control of the I-O data, 7 is a carry save adder (CSA) group, 8 is an ALU, 9 is a shifter, 10 is a bus for source 1 (Src 1), 11 is a bus for source 2 (Src 2), and 12 is a bus for results.").
a first bus coupling said carry save stage to said ALU, wherein said first bus provides	Izumikawa '964 discloses this limitation.

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said carry signal to said ALU;	*See, e.g.*, FIG. 2 (reproduced above, showing carry signal provided to ALU); translation at 3 ("In FIG. 2, 2 is a latch, 3 is a circuit that carries out input-output/bypass control of the I-O data, 7 is a carry save adder (CSA) group, 8 is an ALU, 9 is a shifter, 10 is a bus for source 1 (Src 1), 11 is a bus for source 2 (Src 2), and 12 is a bus for results.").
a second bus coupling said carry save stage to said ALU, wherein said second bus provides said sum signal to said ALU;	Izumikawa '964 discloses this limitation. *See, e.g.*, FIG. 2 (reproduced above, showing sum signal provided to ALU); translation at 3 ("In FIG. 2, 2 is a latch, 3 is a circuit that carries out input-output/bypass control of the I-O data, 7 is a carry save adder (CSA) group, 8 is an ALU, 9 is a shifter, 10 is a bus for source 1 (Src 1), 11 is a bus for source 2 (Src 2), and 12 is a bus for results.").
a first multiplexer coupled between said first bus and said ALU; and	Izumikawa '964 alone or in combination with other prior art discussed below, discloses this limitation. *See, e.g.*, FIG. 2 (reproduced above, showing bus architecture, which multiplexers of '434 emulate). A person of ordinary skill in the art would understand that multiplexers could be substituted for a bus architecture for the purpose of selecting inputs to an ALU in a system. *See, e.g.*, **Computer Systems Architecture**, Jean-Loup Baer, at 392 ("In multiplexors the circuitry is shared among several subchannels. Theoretically a multiplexor could be modeled as in Figure 8.7.a but a more typical configuration is illustrated in Figure 8.7.b where four I/O controllers (or devices) share a channel.").
a second multiplexer coupled between said second bus and said ALU,	Izumikawa '964 alone or in combination with other prior art discussed below, discloses this limitation. *See, e.g.*, FIG. 2 (reproduced above, showing bus architecture, which multiplexers of '434 emulate). A person of ordinary skill in the art would understand that multiplexers could be substituted for a bus architecture for the purpose of selecting inputs to an ALU in a system.

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	See, e.g., **Computer Systems Architecture**, Jean-Loup Baer, at 392 ("In multiplexors the circuitry is shared among several subchannels. Theoretically a multiplexor could be modeled as in Figure 8.7.a but a more typical configuration is illustrated in Figure 8.7.b where four I/O controllers (or devices) share a channel.").
whereby said ALU is capable of adding said carry and sum signals to create a third data value equal to the product of said first and second data values.	Izumikawa '964 discloses this limitation. *See, e.g.*, FIG. 2 (reproduced above, showing ALU which replaces the functionality of the CPA); translation at 3 ("In FIG. 2, 2 is a latch, 3 is a circuit that carries out input-output/bypass control of the I-O data, 7 is a carry save adder (CSA) group, 8 is an ALU, 9 is a shifter, 10 is a bus for source 1 (Src 1), 11 is a bus for source 2 (Src 2), and 12 is a bus for results.").
Claim 2	
2. The multiplier of claim 1, further comprising:	
a third bus coupled between said first terminal and said first multiplexer; and	Izumikawa '964 discloses this limitation. *See, e.g.*, FIG. 2 (reproduced above).
a fourth bus coupled between said second terminal and said second multiplexer.	Izumikawa '964 discloses this limitation. *See, e.g.*, FIG. 2 (reproduced above).
Claim 3	
3. The multiplier of claim 2, further comprising:	
a first register coupled between said first multiplexer and said ALU, wherein said	Izumikawa '964 discloses this limitation. When reading the Izumikawa '964, a person of ordinary skill in the art would understand that a register would be inherent and/or obvious to the design of an

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carry signal is stored in said first register; and	ALU in a system. *See, e.g.*, FIG. 2 (reproduced above, standard industry practice includes a storage element before the ALU).
a second register coupled between said second multiplexer and said ALU, wherein said sum signal is stored in said second register.	Izumikawa '964 discloses this limitation. When reading the Izumikawa '964, a person of ordinary skill in the art would understand that a register would be inherent and/or obvious to the design of an ALU in a system. *See, e.g.*, FIG. 2 (reproduced above, standard industry practice includes a storage element before the ALU).
Claim 4	
4. The multiplier of claim 2, further comprising	
multiplexer select means coupled to said first and second multiplexers,	Izumikawa '964 alone or in combination with other prior art discussed below, discloses this limitation. When reading the Izumikawa '964, a person of ordinary skill in the art would understand that selector means would be inherent and/or obvious to output the correct value onto the bus from the correct block. *See, e.g.*, FIG. 2 (reproduced above, showing bus architecture which requires select means). In addition, **U.S. Patent No. 4,866,652** discloses this limitation. See, e.g., FIG. 3 (MUX 88 and 86 will have select means as a multiplexer by definition has a selector circuit).
said multiplexer select means having a first state and a second state,	Izumikawa '964 alone or in combination with other prior art discussed below, discloses this limitation. When reading the Izumikawa '964, a person of ordinary skill in the art would understand that selector means with a first state and second state would be inherent and/or obvious to the design of the system.

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	See, e.g., FIG. 2 (reproduced above, which contemplates a select means with a first and second state). In addition, **U.S. Patent No. 4,866,652** discloses this limitation, as it discloses multiplexers and all multiplexers require a select means that has at least two states. *See,* e.g., col. 3, lines 9-12 ("[T]he fractional sum and carry are provided to multiplexers 86 and 88 in a fractional ALU circuit 84. The other inputs of these multiplexers are unrelated to the present invention and thus are not shown.").
wherein said multiplexer select means causes said first multiplexer to route said carry signal to said ALU and causes said second multiplexer to route said sum signal to said ALU when said multiplexer select means is in said first state, and	Izumikawa '964 discloses this limitation. *See, e.g.*, FIG. 2 (reproduced above, showing routing of carry and sum to ALU).
wherein said multiplexer select means causes said first multiplexer to route said first data value to said ALU and causes said second multiplexer to route said second data value to said ALU when said multiplexer select means is in said second state.	Izumikawa '964 discloses this limitation. *See, e.g.*, FIG. 2 (reproduced above, showing routing of first and second data values from Block 3 to ALU).
Claim 8	
8. A multiplier for use in a system having an arithmetic and logic unit (ALU), said multiplier comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, Izumikawa '964 discloses this limitation. *See, e.g.*, translation at 2 ("The invention relates to a multiplication method that is realized on a microprocessor chip."); translation at 3 ("In FIG. 2, 2 is a latch, 3 is a circuit that carries out input-output/bypass control of the

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	I-O data, 7 is a carry save adder (CSA) group, 8 is an ALU, 9 is a shifter, 10 is a bus for source 1 (Src 1), 11 is a bus for source 2 (Src 2), and 12 is a bus for results."); translation at 4 ("(FIG. 2) This is a diagram showing the configuration of the data bus, including the multiplier."); translation of FIG. 2 ("[three characters at right:] Multiplier").
a first input terminal for receiving a first data value;	Izumikawa '964 discloses this limitation. *See, e.g.*, FIG. 2 (reproduced above); translation at 3 ("In FIG. 2, 2 is a latch, 3 is a circuit that carries out input-output/bypass control of the I-O data, 7 is a carry save adder (CSA) group, 8 is an ALU, 9 is a shifter, 10 is a bus for source 1 (Src 1), 11 is a bus for source 2 (Src 2), and 12 is a bus for results.").
a second input terminal for receiving a second data value;	Izumikawa '964 discloses this limitation. *See, e.g.*, FIG. 2 (reproduced above) ; translation at 3 ("In FIG. 2, 2 is a latch, 3 is a circuit that carries out input-output/bypass control of the I-O data, 7 is a carry save adder (CSA) group, 8 is an ALU, 9 is a shifter, 10 is a bus for source 1 (Src 1), 11 is a bus for source 2 (Src 2), and 12 is a bus for results.").
a carry save stage coupled to said first and second terminals, wherein said carry save stage generates a carry signal and a sum signal in response to said first and second data values;	Izumikawa '964 discloses this limitation. *See, e.g.*, FIG. 2 (reproduced above, showing carry save stage along with sum and carry signals); translation of FIG. 2 ("[three characters at right:] Multiplier"); translation at 3 ("In FIG. 2, 2 is a latch, 3 is a circuit that carries out input-output/bypass control of the I-O data, 7 is a carry save adder (CSA) group, 8 is an ALU, 9 is a shifter, 10 is a bus for source 1

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	(Src 1), 11 is a bus for source 2 (Src 2), and 12 is a bus for results.").
means for coupling said carry save stage and said first and second input terminals to said ALU, wherein said carry and sum signals and said first and second data values are transmitted to said ALU, whereby said ALU is capable of adding said carry and sum signals to provide a third data value equal to the product of said first and second data values; and	Izumikawa '964 discloses this limitation, which is subject to 35 U.S.C. § 112, ¶ 6. The claimed function is "coupling said carry save stage and said first and second input terminals to said ALU." Izumikawa '964 implements this function via a bus architecture. *See, e.g.*, FIG. 2 (reproduced above, showing bus architecture coupling carry save stage and first and second input terminals to ALU); translation of FIG. 2 ("[three characters at right:] Multiplier"); translation at 3 ("In FIG. 2, 2 is a latch, 3 is a circuit that carries out input-output/bypass control of the I-O data, 7 is a carry save adder (CSA) group, 8 is an ALU, 9 is a shifter, 10 is a bus for source 1 (Src 1), 11 is a bus for source 2 (Src 2), and 12 is a bus for results.").
means for controlling said means for coupling, said means for controlling having a first and a second state, wherein in said first state said means for controlling causes said means for coupling to route said carry and sum signals to said ALU and to prevent said means for coupling from routing said first and second data values to said ALU, and wherein in said second state said means for controlling causes said means for coupling to route said first and second data values to said ALU and to prevent said means for coupling from routing said carry and sum signals to said ALU.	Izumikawa '964 discloses this limitation, which is subject to 35 U.S.C. § 112, ¶ 6. The claimed function is "controlling said means for coupling." The means for controlling is performed by selector means required by the bus architecture. When reading the Izumikawa '964, a person of ordinary skill in the art would understand that selector means would be inherent and/or obvious to output the correct value onto the bus from the correct block. *See, e.g.*, FIG. 2 (reproduced above, showing bus architecture); translation at 3 ("In FIG. 2, 2 is a latch, 3 is a circuit that carries out input-output/bypass control of the I-O data, 7 is a carry save adder (CSA) group, 8 is an ALU, 9 is a shifter, 10 is a bus for source 1 (Src 1), 11 is a bus for source 2 (Src 2), and 12 is a bus for results.").
Claim 11	

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11. A system comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, Izumikawa '964 discloses this limitation. *See, e.g.*, translation at 2 ("The invention relates to a multiplication method that is realized on a microprocessor chip."); translation at 3 ("In FIG. 2, 2 is a latch, 3 is a circuit that carries out input-output/bypass control of the I-O data, 7 is a carry save adder (CSA) group, 8 is an ALU, 9 is a shifter, 10 is a bus for source 1 (Src 1), 11 is a bus for source 2 (Src 2), and 12 is a bus for results."); translation at 4 ("(FIG. 2) This is a diagram showing the configuration of the data bus, including the multiplier."); translation of FIG. 2 ("[three characters at right:] Multiplier").
a carry save stage coupled to receive a first data value and a second data value, wherein the carry save stage generates a carry signal and a sum signal in response to the first and second data values;	Izumikawa '964 discloses this limitation. *See, e.g.*, FIG. 2 (reproduced above, showing carry save stage along with sum and carry signals); translation of FIG. 2 ("[three characters at right:] Multiplier"); translation at 3 ("In FIG. 2, 2 is a latch, 3 is a circuit that carries out input-output/bypass control of the I-O data, 7 is a carry save adder (CSA) group, 8 is an ALU, 9 is a shifter, 10 is a bus for source 1 (Src 1), 11 is a bus for source 2 (Src 2), and 12 is a bus for results.").
a first selector circuit coupled to receive the carry signal and the first data value;	Izumikawa '964 discloses this limitation. *See, e.g.*, FIG. 2 (reproduced above, showing bus architecture).
a second selector circuit coupled to receive the sum signal and the second data value;	Izumikawa '964 discloses this limitation. *See, e.g.*, FIG. 2 (reproduced above, showing bus architecture).

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a control signal source coupled to the first and second selector circuits, wherein the control signal source causes the first and second selector circuits to operate in a first mode and a second mode, wherein in the first mode, the first selector circuit passes the carry signal and the second selector circuit passes the sum signal, and wherein in the second mode, the first selector circuit passes the first data value and the second selector circuit passes the second data value; and	Izumikawa '964 discloses this limitation. *See, e.g.*, translation at 3 ("In FIG. 2, 2 is a latch, 3 is a circuit that carries out input-output/bypass control of the I-O data, 7 is a carry save adder (CSA) group, 8 is an ALU, 9 is a shifter, 10 is a bus for source 1 (Src 1), 11 is a bus for source 2 (Src 2), and 12 is a bus for results.").
an arithmetic and logic unit (ALU) coupled to the first and second selector circuits, wherein the ALU receives the signals passed by the first and second selector circuits, and wherein in the first mode, the ALU adds the carry and sum signals to create a third data value equal to the product of the first and second data values.	Izumikawa '964 discloses this limitation. *See, e.g.*, FIG. 2 (reproduced above, showing ALU which replaces the functionality of the CPA); translation at 3 ("In FIG. 2, 2 is a latch, 3 is a circuit that carries out input-output/bypass control of the I-O data, 7 is a carry save adder (CSA) group, 8 is an ALU, 9 is a shifter, 10 is a bus for source 1 (Src 1), 11 is a bus for source 2 (Src 2), and 12 is a bus for results.").

Appendix F3
Defendants and Counterclaimants' Invalidity Contentions
Advanced Micro Devices, Inc. et al. v. Samsung Electronics Co., Ltd. et al., Case No. CV-08-0986-SI

U.S. Patent No. 5,623,434 Invalidity Chart: U.S. Patent No. 5,457,805 ("the '805 patent")

All asserted claims are anticipated by U.S. Patent No. 5,457,805 and/or are rendered obvious by it, either alone or in combination with other prior art described below and/or listed in Section I of Defendants and Counterclaimants' Preliminary Invalidity Contentions and/or through modifications described below. Nothing in this invalidity chart should be construed as signifying or suggesting Defendants and Counterclaimants' adoption of or acquiescence in any claim scope and/or claim construction positions taken by Plaintiffs and Counterdefendants in this litigation.

To the extent a feature of the claims may not be disclosed or suggested by the '805 patent alone, one of ordinary skill in the art would have been motivated to combine the disclosed references to arrive at the patented inventions for multiple reasons, including (1) because these references address the subject matter, multiplier circuitry, acknowledged as prior art in the '434 patent; (2) because these references address similar problems to those purportedly addressed by the '434 patent; (3) because there were similar improvements in similar prior art devices, as disclosed in these references and in Defendants and Counterclaimants other claim charts for the '434 patent; (4) because the alleged invention discloses predictable variations of the inventions disclosed in these references; and (5) based on the knowledge or common sense of one of ordinary skill in the art.

U.S. Patent No. 5,623,434	
Claim 1	
Claim limitation	**'805 Patent**
1. A multiplier for use in a data processing system having an arithmetic and logic unit (ALU), said multiplier comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, the '805 patent discloses this limitation. *See, e.g.*, col. 1, lines 13-15 ("Referring to FIG. 6, the method to execute a product-sum operation instruction in a conventional microcomputer will be described below."); col. 1, lines 20-21 ("The multiplication is made according to the secondary Booth algorithm and the data have 16 bits."); col. 3, lines 48-49 ("FIG. 6 is a block diagram to show the configuration of a conventional microcomputer."); FIG. 6 (reproduced below):

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	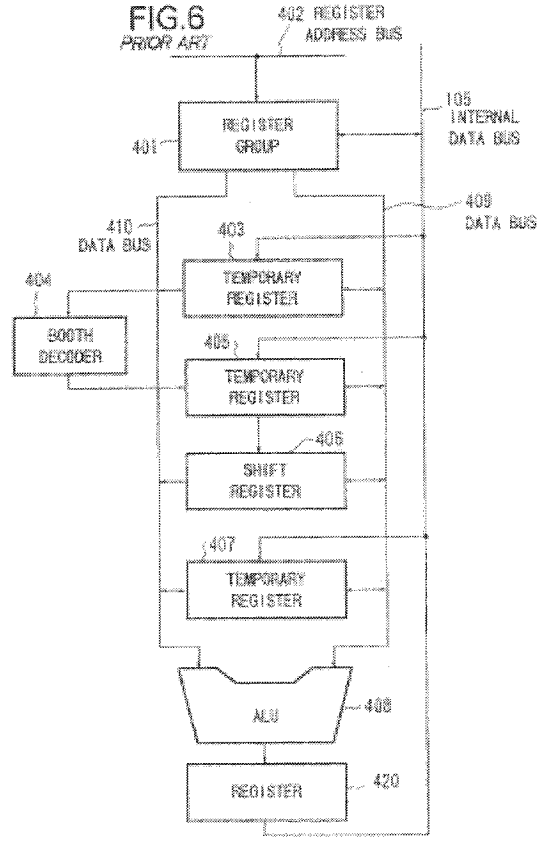
a first input terminal for receiving a first data value;	The '805 patent discloses this limitation.

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	See, e.g., FIG. 6 (reproduced above); col. 1, lines 22-23 ("Firstly, a multiplier data is read from the register group 401[.]").
a second input terminal for receiving a second data value;	The '805 patent discloses this limitation. *See, e.g.*, FIG. 6 (reproduced above); col. 1, lines 25-26 ("A multiplicand data read from the register group 401 . . . .").
a carry save stage coupled to said first and second terminals, wherein said carry save stage generates a carry signal and a sum signal in response to said first and second data values;	The '805 patent discloses this limitation. *See, e.g.*, FIG. 6 (reproduced above); col. 1, lines 28-30 ("In the multiplication of 16-bit data using the secondary Booth algorithm, eight partial products are determined so that they are added with a shift of two bits for each.").
a first bus coupling said carry save stage to said ALU, wherein said first bus provides said carry signal to said ALU;	The '805 patent discloses this limitation. *See, e.g.*, FIG. 6 (reproduced above).
a second bus coupling said carry save stage to said ALU, wherein said second bus provides said sum signal to said ALU;	The '805 patent discloses this limitation. *See, e.g.*, FIG. 6 (reproduced above).
a first multiplexer coupled between said first bus and said ALU; and	The '805 patent alone or in combination with other prior art discussed below discloses this limitation. *See, e.g.*, FIG. 6 (reproduced above, showing bus architecture, which multiplexers of '434 emulate). A person of ordinary skill in the art would understand that multiplexers could be substituted for a bus architecture for the purpose of selecting inputs to an ALU in a system. *See, e.g.*, **Computer Systems Architecture**, Jean-Loup Baer, at 392 ("In multiplexors the circuitry is

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	shared among several subchannels. Theoretically a multiplexor could be modeled as in Figure 8.7.a but a more typical configuration is illustrated in Figure 8.7.b where four I/O controllers (or devices) share a channel.").
a second multiplexer coupled between said second bus and said ALU,	The '805 patent alone or in combination with other prior art discussed below discloses this limitation. *See, e.g.*, FIG. 6 (reproduced above, showing bus architecture, which multiplexers of '434 emulate). A person of ordinary skill in the art would understand that multiplexers could be substituted for a bus architecture for the purpose of selecting inputs to an ALU in a system. *See, e.g.*, **Computer Systems Architecture**, Jean-Loup Baer, at 392 ("In multiplexors the circuitry is shared among several subchannels. Theoretically a multiplexor could be modeled as in Figure 8.7.a but a more typical configuration is illustrated in Figure 8.7.b where four I/O controllers (or devices) share a channel.").
whereby said ALU is capable of adding said carry and sum signals to create a third data value equal to the product of said first and second data values.	The '805 patent discloses this limitation. *See, e.g.*, FIG. 6 (reproduced above); col. 1, lines 46-50 ("The contents of the shift register 406 and the temporary register 407 are added at an ALU 408. The result obtained from the addition at the ALU 408 is written to the temporary register 407."); col. 1, lines 65-66 ("The final product-sum operation result is temporarily held at a register 420[.]").
Claim 2	
2. The multiplier of claim 1, further comprising:	
a third bus coupled between said first	The '805 patent discloses this limitation.

U.S. Patent No. 5,623,434	
terminal and said first multiplexer; and	*See, e.g.*, FIG. 6 (reproduced above).
a fourth bus coupled between said second terminal and said second multiplexer.	The '805 patent discloses this limitation. *See, e.g.*, FIG. 6 (reproduced above).
Claim 3	
3. The multiplier of claim 2, further comprising:	
a first register coupled between said first multiplexer and said ALU, wherein said carry signal is stored in said first register; and	The '805 patent discloses this limitation. When reading the '805 patent, a person of ordinary skill in the art would understand that a register would be inherent and/or obvious to the design of an ALU in a system. *See, e.g.*, FIG. 6 (reproduced above, standard industry practice includes a storage element before the ALU).
a second register coupled between said second multiplexer and said ALU, wherein said sum signal is stored in said second register.	The '805 patent discloses this limitation. When reading the '805 patent, a person of ordinary skill in the art would understand that a register would be inherent and/or obvious to the design of an ALU in a system. *See, e.g.*, FIG. 6 (reproduced above, standard industry practice includes a storage element before the ALU).
Claim 4	
4. The multiplier of claim 2, further comprising	
multiplexer select means coupled to said first and second multiplexers,	The '805 patent alone or in combination with other prior art discussed below, discloses this limitation. When reading the '805 patent, a person of ordinary skill in the art would understand that selector means would be inherent and/or obvious to output the correct value onto the bus from the correct

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	block. *See, e.g.*, FIG. 6 (reproduced above, showing bus architecture which requires select means). In addition, **U.S. Patent No. 4,866,652** discloses this limitation. *See, e.g.*, FIG. 3 (reproduced above, MUX 88 and 86 will have select means as a multiplexer by definition has a selector circuit).
said multiplexer select means having a first state and a second state,	The '805 patent alone or in combination with other prior art discussed below, discloses this limitation. When reading the '805 patent, a person of ordinary skill in the art would understand that selector means with a first state and second state would be inherent and/or obvious to the design of the system. *See, e.g.*, FIG. 6 (reproduced above, which contemplates a select means with a first and second state). In addition, **U.S. Patent No. 4,866,652** discloses this limitation, as it discloses multiplexers and all multiplexers require a select means that has at least two states. *See,* e.g., col. 3, lines 9-12 ("[T]he fractional sum and carry are provided to multiplexers 86 and 88 in a fractional ALU circuit 84. The other inputs of these multiplexers are unrelated to the present invention and thus are not shown.").
wherein said multiplexer select means causes said first multiplexer to route said carry signal to said ALU and causes said second multiplexer to route said sum signal to said ALU when said multiplexer select means is in said first state, and	The '805 patent discloses this limitation. *See, e.g.*, FIG. 6 (reproduced above).
wherein said multiplexer select means causes said first multiplexer to route said first data value to said ALU and causes said second multiplexer to route said second data	The '805 patent discloses this limitation. *See, e.g.*, FIG. 6 (reproduced above).

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value to said ALU when said multiplexer select means is in said second state.	
Claim 8	
8. A multiplier for use in a system having an arithmetic and logic unit (ALU), said multiplier comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, the '805 patent discloses this limitation. *See, e.g.*, col. 1, lines 13-15 ("Referring to FIG. 6, the method to execute a product-sum operation instruction in a conventional microcomputer will be described below."); col. 1, lines 20-21 ("The multiplication is made according to the secondary Booth algorithm and the data have 16 bits."); col. 3, lines 48-49 ("FIG. 6 is a block diagram to show the configuration of a conventional microcomputer."); FIG. 6 (reproduced above).
a first input terminal for receiving a first data value;	The '805 patent discloses this limitation. *See, e.g.*, FIG. 6 (reproduced above); col. 1, lines 22-23 ("Firstly, a multiplier data is read from the register group 401[.]").
a second input terminal for receiving a second data value;	The '805 patent discloses this limitation. *See, e.g.*, FIG. 6 (reproduced above); col. 1, lines 25-26 ("A multiplicand data read from the register group 401 . . . .").
a carry save stage coupled to said first and second terminals, wherein said carry save	The '805 patent discloses this limitation.

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stage generates a carry signal and a sum signal in response to said first and second data values;	*See, e.g.*, FIG. 6 (reproduced above); col. 1, lines 28-30 ("In the multiplication of 16-bit data using the secondary Booth algorithm, eight partial products are determined so that they are added with a shift of two bits for each.").
means for coupling said carry save stage and said first and second input terminals to said ALU, wherein said carry and sum signals and said first and second data values are transmitted to said ALU, whereby said ALU is capable of adding said carry and sum signals to provide a third data value equal to the product of said first and second data values; and	The '805 patent discloses this limitation, which is subject to 35 U.S.C. § 112, ¶ 6. The claimed function is "coupling said carry save stage and said first and second input terminals to said ALU." The '805 patent implements this function via a bus architecture. *See, e.g.*, FIG. 6 (reproduced above); col. 1, lines 46-50 ("The contents of the shift register 406 and the temporary register 407 are added at an ALU 408. The result obtained from the addition at the ALU 408 is written to the temporary register 407."); col. 1, lines 65-66 ("The final product-sum operation result is temporarily held at a register 420[.]").
means for controlling said means for coupling, said means for controlling having a first and a second state, wherein in said first state said means for controlling causes said means for coupling to route said carry and sum signals to said ALU and to prevent said means for coupling from routing said first and second data values to said ALU, and wherein in said second state said means for controlling causes said means for coupling to route said first and second data values to said ALU and to prevent said means for coupling from routing said carry and sum signals to said ALU.	The '805 patent discloses this limitation, which is subject to 35 U.S.C. § 112, ¶ 6. The claimed function is "controlling said means for coupling." The means for controlling is performed by selector means required by the bus architecture. When reading the '805 patent, a person of ordinary skill in the art would understand that selector means would be inherent and/or obvious to output the correct value onto the bus from the correct block. *See, e.g.*, FIG. 6 (reproduced above).

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Claim 11	
11. A system comprising:	Assuming for present purposes (without admitting) that the preamble is a claim limitation, the '805 patent discloses this limitation. *See, e.g.*, col. 1, lines 13-15 ("Referring to FIG. 6, the method to execute a product-sum operation instruction in a conventional microcomputer will be described below."); col. 1, lines 20-21 ("The multiplication is made according to the secondary Booth algorithm and the data have 16 bits."); col. 3, lines 48-49 ("FIG. 6 is a block diagram to show the configuration of a conventional microcomputer."); FIG. 6 (reproduced above).
a carry save stage coupled to receive a first data value and a second data value, wherein the carry save stage generates a carry signal and a sum signal in response to the first and second data values;	The '805 patent discloses this limitation. *See, e.g.*, FIG. 6 (reproduced above); col. 1, lines 28-30 ("In the multiplication of 16-bit data using the secondary Booth algorithm, eight partial products are determined so that they are added with a shift of two bits for each.").
a first selector circuit coupled to receive the carry signal and the first data value;	The '805 patent discloses this limitation. *See, e.g.*, FIG. 6 (reproduced above, showing bus architecture).
a second selector circuit coupled to receive the sum signal and the second data value;	The '805 patent discloses this limitation. *See, e.g.*, FIG. 6 (reproduced above, showing bus architecture).
a control signal source coupled to the first and second selector circuits, wherein the	The '805 patent discloses this limitation.

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control signal source causes the first and second selector circuits to operate in a first mode and a second mode, wherein in the first mode, the first selector circuit passes the carry signal and the second selector circuit passes the sum signal, and wherein in the second mode, the first selector circuit passes the first data value and the second selector circuit passes the second data value; and	*See, e.g.*, FIG. 6 (reproduced above); col. 1, lines 46-50 ("The contents of the shift register 406 and the temporary register 407 are added at an ALU 408. The result obtained from the addition at the ALU 408 is written to the temporary register 407.").
an arithmetic and logic unit (ALU) coupled to the first and second selector circuits, wherein the ALU receives the signals passed by the first and second selector circuits, and wherein in the first mode, the ALU adds the carry and sum signals to create a third data value equal to the product of the first and second data values.	The '805 patent discloses this limitation. *See, e.g.*, FIG. 6 (reproduced above); col. 1, lines 46-50 ("The contents of the shift register 406 and the temporary register 407 are added at an ALU 408. The result obtained from the addition at the ALU 408 is written to the temporary register 407."); col. 1, lines 65-66 ("The final product-sum operation result is temporarily held at a register 420[.]").

Appendix F4

Defendants and Counterclaimants' Invalidity Contentions

Advanced Micro Devices, Inc. et al. v. Samsung Electronics Co., Ltd. et al., Case No. CV-08-0986-SI

U.S. Patent No. 5,623,434 Invalidity Chart: MIPS R4000 and MIPS R3010

All asserted claims are anticipated by MIPS R4000 microprocessor and MIPS R3010 floating point coprocessor and/or are rendered obvious by it, either alone or in combination with other prior art described below and/or listed in Section I of Defendants and Counterclaimants' Preliminary Invalidity Contentions and/or through modifications described below. Nothing in this invalidity chart should be construed as signifying or suggesting Defendants and Counterclaimants' adoption of or acquiescence in any claim scope and/or claim construction positions taken by Plaintiffs and Counterdefendants in this litigation.

References

1. "The MIPS R3010 Floating-Point Coprocessor", Chris Rowen et. al., IEEE Micro, June 1988.
2. "The MIPS R4000 Processor", Sunil Mirapuri, IEEE Micro, April 1992.

To the extent a feature of the claims may not be disclosed or suggested by the MIPS R4000 or MIPS R3010 alone, one of ordinary skill in the art would have been motivated to combine the disclosed references to arrive at the patented inventions for multiple reasons, including (1) because these references address the subject matter, multiplier circuitry, acknowledged as prior art in the '434 patent; (2) because these references address similar problems to those purportedly addressed by the '434 patent; (3) because there were similar improvements in similar prior art devices, as disclosed in these references and in Defendants and Counterclaimants other claim charts for the '434 patent; (4) because the alleged invention discloses predictable variations of the inventions disclosed in these references; and (5) based on the knowledge or common sense of one of ordinary skill in the art.

U.S. Patent No. 5,623,434			
Claim 1			
Claim limitation	**MIPS R4000 Integer Unit** References are to [2]	**MIPS R4000 Floating Point Unit** References are to [2]	**MIPS 3010 Floating Point Coprocessor** References are to [1]
1. A multiplier for use in a data processing system having an arithmetic and logic unit (ALU), said multiplier comprising:	Page 12. "The R4000's 64-bit execution unit includes … multiplier, …"	Figure 6 shows the FP multiplier.	Figure 3 shows the FP multiplier.

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a first input terminal for receiving a first data value; a second input terminal for receiving a second data value;	In Fig 2 the RF stage reads the register file to provide operands for the EX stage ALU operations, which would include multiplications. Page 13 "the register file …[has] two read ports"	Figure 6 shows the Multiplier operand input and the Multiplicand operand input.	Figure 3 shows output busses A and B from the register file to the Multiply unit.
a carry save stage coupled to said first and second terminals, wherein said carry save stage generates a carry signal and a sum signal in response to said first and second data values;	Page 13 describes the multiplier generating multiply results in "sum-and-carry form and must be combined through full carry propagation. The integer ALU performs this operation when the result moves to the general registers"	Figure 6 shows the internal structure of the multiplier. Specifically CSAs 1-4. Inputs are registered in the Multiplier register and the Multiplicand register. Outputs of the multiplier are Sum and Carry.	Page 58 in the second paragraph on the left side, "Results of both the multiplier and divider appear in carry-save form. They are returned to the adder over the two operand busses for final carry propagation…"
a first bus coupling said carry save stage to said ALU, wherein said first bus provides said carry signal to said ALU; a second bus coupling said carry save stage to said ALU, wherein said second bus provides said sum signal to said ALU;	These buses are the means of transferring the carry and sum signals from the multiplier to the ALU to facilitate the sum operation described above.	Figure 7 shows the first and second buses carrying the carry and save inputs to the Adder identified as "Multiply/divide intermediate results path" input to the Adder source multiplexer. These are driven by Sum and Carry outputs shown on Figure 6.	Figure 3 and the above paragraph identify the buses used to input the carry and save signal as operand buses A and B, shown bidirectionally connected to the Add unit.

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a first multiplexer coupled between said first bus and said ALU; and a second multiplexer coupled between said second bus and said ALU,	The use of the ALU adder for both ALU operations and for multiply final product generation necessitates the presence of a multiplexer to select between operands for ALU operations and multiply carry and save signals.	Figure 7 shows the Adder source multiplexer selecting between the Multiply/divide intermediate results and the source operands. This could equivalently be drawn as two multipliexers, one for Carry and first Source operand; and a second for Sum and second Source operand.	The operand buses perform the multiplexer function by enabling multiply drivers.
whereby said ALU is capable of adding said carry and sum signals to create a third data value equal to the product of said first and second data values.	Page 13 describes the multiplier generating multiply results in "sum-and-carry format" which "must be combined through full carry propagation. The integer ALU performs this operation." "Full carry propagation" is a technical description of normal addition, to distinguish it from carry-save addition used in the multiplier.	Page 13: "In the cycle following the last iteration of the multiply, the sum and carry from the multiplier array travel to the floating-point adder to produce the final rounded product." Page 14: "The adder has two data entry paths. One accommodates the normal source operands that go through the unpack stage to form data inputs for all adder-supported operations. The multiplier/divider units send their intermediate results on the other path to the adder's input stage for final computation."	Page 57 in the box labeled "Implementation of the Multiply Unit" states the multiply unit "…produce[s] its double-precision result in carry save form. Another cycle in the add unit produces the final, IEEE rounded result."
Claim 2			
2. The multiplier of claim 1, further comprising:			

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a third bus coupled between said first terminal and said first multiplexer; and a fourth bus coupled between said second terminal and said second multiplexer.	Page 13 describes the multiplier generating multiply results in "sum-and-carry format" which "must be combined through full carry propagation. The integer ALU performs this operation." "Full carry propagation" is a technical description of normal addition, to distinguish it from carry-save addition used in the multiplier.	Page 13: "In the cycle following the last iteration of the multiply, the sum and carry from the multiplier array travel to the floating-point adder to produce the final rounded product." Page 14: "The adder has two data entry paths. One accommodates the normal source operands that go through the unpack stage to form data inputs for all adder-supported operations. The multiplier/divider units send their intermediate results on the other path to the adder's input stage for final computation."	Page 57 in the box labeled "Implementation of the Multiply Unit" states the multiply unit "…produce[s] its double-precision result in carry save form. Another cycle in the add unit produces the final, IEEE rounded result."
Claim 3			
3. The multiplier of claim 2, further comprising:			

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a first register coupled between said first multiplexer and said ALU, wherein said carry signal is stored in said first register; and a second register coupled between said second multiplexer and said ALU, wherein said sum signal is stored in said second register.	P. 13. The multiplier "… breaks each iteration into four stages: …, and product accumulation." The presence of multiple stages necessitates pipeline registers between states.	"Add stage" box is a pipeline register (note text on page 14 explains that addition takes 4 clock cycles and lists the four corresponding stages). This is the first and second register, just as the"adder source multiplexer" is the first and second multiplexer as explained above. Note that the "Add stage" register is coupled between the multiplexer above and the "Mantissa add/subtract" unit below.	P. 57, "…the multiplier unit needs a little less than four cycles to product its double-precision result in carry-save form. Another cycle in the add unit produces the final, IEEE rounded result." Registers are required between stages to ensure proper operation and uncorrupted transfer of data.
Claim 4			
4. The multiplier of claim 2, further comprising			

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multiplexer select means coupled to said first and second multiplexers, said multiplexer select means having a first state and a second state, wherein said multiplexer select means causes said first multiplexer to route said carry signal to said ALU and causes said second multiplexer to route said sum signal to said ALU when said multiplexer select means is in said first state, and wherein said multiplexer select means causes said first multiplexer to route said first data value to said ALU and causes said second multiplexer to route said second data value to said ALU when said multiplexer select means is in said second state.	The presence of a multiplexer requires a multiplexer control signal to produce the multiplexer operation. A multiplexer with two inputs will have a control signal with at least two states, each one operable to produce on the output of the multiplexer the corresponding input to the multiplexer. The two multiplexers will be controlled to pass the sum and carry signals to the ALU in the same cycle (the "first state") so that they may be added to form the product; and the two multiplexers will be controlled to pass the two register file read port values ("first" and "second data value") in the same cycle to the ALU to perform an ALU operation ("second state").	The presence of a multiplexer requires a multiplexer control signal to produce the multiplexer operation. A multiplexer with two inputs will have a control signal with at least two states, each one operable to produce on the output of the multiplexer the corresponding input to the multiplexer. The two multiplexers will be controlled to pass the sum and carry signals to the ALU in the same cycle (the "first state") so that they may be added to form the product; and the two multiplexers will be controlled to pass the two register file read port values ("first" and "second data value") in the same cycle to the ALU to perform an ALU operation ("second state").	The presence of a multiplexer requires a multiplexer control signal to produce the multiplexer operation. A multiplexer with two inputs will have a control signal with at least two states, each one operable to produce on the output of the multiplexer the corresponding input to the multiplexer. The two multiplexers will be controlled to pass the sum and carry signals to the ALU in the same cycle (the "first state") so that they may be added to form the product; and the two multiplexers will be controlled to pass the two register file read port values ("first" and "second data value") in the same cycle to the ALU to perform an ALU operation ("second state").
<u>Claim 8</u>			
8. A multiplier for use in a system having an arithmetic and logic unit (ALU), said multiplier comprising:	Page 12. "The R4000's 64-bit execution unit includes … multiplier, …"	Figure 6 shows the FP multiplier.	Figure 3 shows the FP multiplier.

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a first input terminal for receiving a first data value; a second input terminal for receiving a second data value;	In Fig 2 the RF stage reads the register file to provide operands for the EX stage ALU operations, which would include multiplications. Page 13 "the register file …[has] two read ports"	Figure 6 shows the Multiplier operand input and the Multiplicand operand input.	Figure 3 shows output busses A and B from the register file to the Multiply unit.
a carry save stage coupled to said first and second terminals, wherein said carry save stage generates a carry signal and a sum signal in response to said first and second data values;	Page 13 describes the multiplier generating multiply results in "sum-and-carry format." which are combined in the ALU to form the final product.	Figure 6 shows the internal structure of the multiplier. Specifically CSAs 1-4. Inputs are registered in the Multiplier register and the Multiplicand register. Outputs of the multiplier are Sum and Carry.	Page 58 in the second paragraph on the left side, "Results of both the multiplier and divider appear in carry-save form. They are returned to the adder over the two operand busses for final carry propagation…"
means for coupling said carry save stage and said first and second input terminals to said ALU, wherein said carry and sum signals and said first and second data values are transmitted to said ALU, whereby said ALU is capable of adding said carry and sum signals to provide a third data value equal to the product of said first and second data values; and	The means for coupling are the buses identified in Claim 1 above. Page 13 describes the multiplier generating multiply results in "sum-and-carry format." which are added in the ALU to form the final product.	The means for coupling are the buses shown in Figures 6 and 7 labeled "Sum" and "Carry" in Figure 6 and "Multiply/divide intermediate results path" in Figure 7. Page 13: "In the cycle following the last iteration of the multiply, the sum and carry from the multiplier array travel to the floating-point adder to produce the final rounded product." Page 14: "The adder has two data entry paths. One accommodates the normal source operands that go through the unpack stage to form data	The means for coupling are buses A and B in Figure 3. Page 57 in the box labeled "Implementation of the Multiply Unit" states the multiply unit "…produce[s] its double-precision result in carry save form. Another cycle in the add unit produces the final, IEEE rounded result."

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		inputs for all adder-supported operations. The multiplier/divider units send their intermediate results on the other path to the adder's input stage for final computation."	
means for controlling said means for coupling, said means for controlling having a first and a second state, wherein in said first state said means for controlling causes said means for coupling to route said carry and sum signals to said ALU and to prevent said means for coupling from routing said first and second data values to said ALU, and wherein in said second state said means for controlling causes said means for coupling to route said first and second data values to said ALU and to prevent said means for coupling from routing said carry and sum signals to said ALU.	The presence of a multiplexer requires a multiplexer control signal to produce the multiplexer operation. A multiplexer with two inputs will have a control signal with at least two states, each one operable to produce on the output of the multiplexer the corresponding input to the multiplexer. The sum and carry signals will be passed to the ALU in the same cycle (the "first state") so that they may be added to form the product; and the two register file read port values ("first" and "second data value") will be passed to the ALU in the same cycle an ALU operation ("second state").	The presence of a multiplexer requires a multiplexer control signal to produce the multiplexer operation. A multiplexer with two inputs will have a control signal with at least two states, each one operable to produce on the output of the multiplexer the corresponding input to the multiplexer.	The presence of a multiplexer requires a multiplexer control signal to produce the multiplexer operation. A multiplexer with two inputs will have a control signal with at least two states, each one operable to produce on the output of the multiplexer the corresponding input to the multiplexer.
Claim 11			
11. A system comprising:			
a carry save stage coupled to receive a first data value and a second data value, wherein	Page 13 describes the multiplier generating multiply results in	Figure 6 shows the internal structure of the multiplier.	Page 58 in the second paragraph on the left side, "Results of both

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the carry save stage generates a carry signal and a sum signal in response to the first and second data values;	"sum-and-carry format."	Specifically CSAs 1-4. Inputs are registered in the Multiplier register and the Multiplicand register. Outputs of the multiplier are Sum and Carry.	the multiplier and divider appear in carry-save form. They are returned to the adder over the two operand busses for final carry propagation…"
a first selector circuit coupled to receive the carry signal and the first data value; a second selector circuit coupled to receive the sum signal and the second data value;	The use of the ALU adder for both ALU operations and for multiply final product generation necessitates the presence of a multiplexer to select between operands for ALU operations and multiply carry and save signals.	Figure 7 shows the Adder source multiplexer selecting between the Multiply/divide intermediate results and the source operands.	The operand buses perform the multiplexer function by enabling multiply drivers.
a control signal source coupled to the first and second selector circuits, wherein the control signal source causes the first and second selector circuits to operate in a first mode and a second mode, wherein in the first mode, the first selector circuit passes the carry signal and the second selector circuit passes the sum signal, and wherein in the second mode, the first selector circuit passes the first data value and the second selector circuit passes the second data value; and	The presence of a multiplexer requires a multiplexer control signal to produce the multiplexer operation. A multiplexer with two inputs will have a control signal with at least two states, each one operable to produce on the output of the multiplexer the corresponding input to the multiplexer.	The presence of a multiplexer requires a multiplexer control signal to produce the multiplexer operation. A multiplexer with two inputs will have a control signal with at least two states, each one operable to produce on the output of the multiplexer the corresponding input to the multiplexer.	The presence of a multiplexer requires a multiplexer control signal to produce the multiplexer operation. A multiplexer with two inputs will have a control signal with at least two states, each one operable to produce on the output of the multiplexer the corresponding input to the multiplexer.
an arithmetic and logic unit (ALU) coupled to the first and second selector circuits, wherein the ALU receives the signals passed by the first and second selector circuits, and wherein in the first mode, the ALU adds the	Page 13 describes the multiplier generating multiply results in "sum-and-carry format" which are combined in the ALU to form the final product.	Page 13: "In the cycle following the last iteration of the multiply, the sum and carry from the multiplier array travel to the floating-point adder to produce	Page 57 in the box labeled "Implementation of the Multiply Unit" states the multiply unit "…produce[s] its double-precision result in carry save

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carry and sum signals to create a third data value equal to the product of the first and second data values.		the final rounded product." Page 14: "The adder has two data entry paths. One accommodates the normal source operands that go through the unpack stage to form data inputs for all adder-supported operations. The multiplier/divider units send their intermediate results on the other path to the adder's input stage for final computation."	form. Another cycle in the add unit produces the final, IEEE rounded result."