Goodard v. Google, Inc.
Doc. 105 Att. 3

# EXHIBIT 1

# C6

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**U.S. Patent No. 5,248,893 Invalidity Chart: Nishimatsu, et. al., Grooved Gate MOSFET, *Proceedings of the 8th Conference (1976 International) on Solid State Devices, Japanese Journal of Applied Physics*, Vol. 16 (1977) Supplement 16-1, pp. 179-183 ("Nishimatsu")**

All asserted claims are anticipated by Nishimatsu and/or are rendered obvious by it, either alone or in combination with other prior art described below and/or listed in Section I of Defendants' and Counterclaimants' Preliminary Invalidity Contentions and/or through modifications described below. Nothing in this invalidity chart should be construed as signifying or suggesting Defendants and Counterclaimants' adoption of or acquiescence in any claim scope and/or claim construction positions taken by Plaintiffs and Counterdefendants in this litigation.

To the extent a feature of the claims may not be disclosed or suggested by Nishimatsu alone, one of skill in the art would know to consider Natori, et. al., *An Analysis of the Concave MOSFET*, IEEE Transactions on Electron. Devices, Vol. ED-25, No. 4, April 1978 ("Natori"), especially since Nishimatsu and Natori both discuss the same subject matter, *viz.*, concave transistors.

| **U.S. Patent No. 5,248,893** | |
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| **Claim 1** | |
| **Claim limitation** | **Nishimatsu** |
| 1 An insulated gate field effect device comprising: | Assuming for present purposes (without admitting) that the preamble is a claim limitation, Nishimatsu discloses an insulated gate field effect device. *See, e.g.*, Nishimatsu at Figs. 1, 2, 10. *See, eg.*, '893 Patent at 1:28-30. |
| a first conductivity type semiconductor substrate having a main surface; | *See, e.g.*, Nishimatsu at Figs. 1, 2, 10; *see, e.g., id.* at 179. ("Figure 1 shows a perspective view of structure of the Grooved Gate MOSFET which is characterized by a negative $x_j$. The junction depth from the silicon surface under the gate oxide is defined as $x_j$ (Fig. 2). This structure can be approximated as shown in fig. 2 for two-dimensional MOSFET analyses.").<br><br>*See, e.g., id.* at 181. ("Figure 7 shows a microphotograph of two Grooved Gate MOSFET's [a bar gate type ($L$ = 2 μm, $W$ = 260 μm) and a snake type ($L$ = 2μm, $W$ = 1830μm, gate pitch = 5μm)] fabricated on a *p*-type, (100), 4Ω-cm silicon substrate."). |
| said semiconductor substrate having a concave surface formed on said main surface extending to a prespecified depth below the main | *See, e.g.*, Nishimatsu at Figs. 1-6, 10.<br><br>*See, e.g., id.* at 179. ("Figure 1 shows a perspective view of structure of the Grooved Gate MOSFET which is characterized by a negative $x_j$. The junction depth from the silicon surface under the gate oxide is defined as $x_j$ |

| U.S. Patent No. 5,248,893 | |
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| surface; | (Fig. 2). This structure can be approximated as shown in fig. 2 for two-dimensional MOSFET analyses."). <br><br> *See, e.g., id.* at 180. ("Figure 3(c) shows the relationship between $x_j$ and drain depletion layer width ($W_D$) in the direction to the source as a parameter of drain voltage. The Grooved Gate structure $(x_j \leq 0)$ can reduce the value of $W_D$ by half as compared with conventional MOSFET's. The computer and experimental threshold voltage and channel length ($V_T$ - $L$) relationships as a function of $x_j$ are shown in Fig. 4.[3] As shown in the figure, a device with a shallow $x_j$ has little change in $V_T$ value with channel variation. Therefore, the Grooved Gate structure is expected to show a more improved $V_T$-$L$ relationship, although the $V_T$-$L$ relationship for negative $x_j$ was not calculated."). <br><br> *See, e.g., id.* at 181. ("The fabrication process flow for Grooved Gate MOSFET's is shown in Fig. 5. After LOCOS oxidation, the 1st polycrystaline silicon (poly-Si) layer (3500Å) is deposited and etched by Freon plasma at the gate region. In this case, the silicon substrate is also etched to about 0.2 - 0.3 $\mu$m in depth. Gate oxidation (500 Å) is followed by the 2nd poly-Si (3500 Å) deposition process [Fig.6(a)]. A new photoresist technique (buried gate technique) is used to bury the poly-Si gate in the grooved region without using a photomask. This technique utilizes the photoresist characteristic that photoresist is formed at the grooved region about twice as thick as that of other parts. When a thin photoresist layer is removed by oxygen plasma, the photoresist is left only in the grooved gate region [Fig. 6(b)]. Then the 2nd poly-Si is etched by masking the buried photoresist and the 1st poly-Si layer is etched again to constitute the source and drain regions [Fig. 6(c)]. The other steps are the same as those of conventional silicon-gate technology. The final cross sectional view of Grooved Gate MOSFET is shown in Fig. 6(d)."). |
| an insulating film formed on said concave surface; | *See, e.g.*, Nishimatsu at Figs. 1, 2, 5, 6, 10; *see, e.g. id.* at 181. ("The fabrication process flow for Grooved Gate MOSFET's is shown in Fig. 5. After LOCOS oxidation, the 1st polycrystaline silicon (poly-Si) layer (3500Å) is deposited and etched by Freon plasma at the gate region. In this case, the silicon substrate is also etched to about 0.2 - 0.3 $\mu$m in depth. Gate oxidation (500 Å) is followed by the 2nd poly-Si (3500 Å) deposition process [Fig.6(a)]. A new photoresist technique (buried gate technique) is used to bury the poly-Si gate in the grooved region without using a photomask. This technique utilizes the photoresist characteristic that photoresist is formed at the grooved region about twice as thick as that of other parts. When a thin photoresist layer is removed by oxygen plasma, the photoresist is left only in the grooved gate region [Fig. 6(b)]. Then the 2nd poly-Si is etched by masking the buried photoresist and the 1st poly-Si layer is etched again to constitute the source and drain regions [Fig. 6(c)]. The other steps are the same as those of |

| U.S. Patent No. 5,248,893 | |
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| | conventional silicon-gate technology. The final cross sectional view of Grooved Gate MOSFET is shown in Fig. 6(d)."). |
| a conductive gate electrode formed above said insulating film, overlying the concave surface; | *See, e.g.*, Nishimatsu at Figs. 1, 2, 5-7, 10.<br><br>*See, e.g., id* at 181. ("The fabrication process flow for Grooved Gate MOSFET's is shown in Fig. 5. After LOCOS oxidation, the 1st polycrystaline silicon (poly-Si) layer (3500Å) is deposited and etched by Freon plasma at the gate region. In this case, the silicon substrate is also etched to about 0.2 - 0.3 $\mu$m in depth. Gate oxidation (500 Å) is followed by the 2nd poly-Si (3500 Å) deposition process [Fig.6(a)]. A new photoresist technique (buried gate technique) is used to bury the poly-Si gate in the grooved region without using a photomask. This technique utilizes the photoresist characteristic that photoresist is formed at the grooved region about twice as thick as that of other parts. When a thin photoresist layer is removed by oxygen plasma, the photoresist is left only in the grooved gate region [Fig. 6(b)]. Then the 2nd poly-Si is etched by masking the buried photoresist and the 1st poly-Si layer is etched again to constitute the source and drain regions [Fig. 6(c)]. The other steps are the same as those of conventional silicon-gate technology. The final cross sectional view of Grooved Gate MOSFET is shown in Fig. 6(d).").<br><br>*See, e.g., id.* at 181. ("Figure 7 shows a microphotograph of two Grooved Gate MOSFET's [a bar gate type ($L$ = 2 $\mu$m, $W$ = 260 μm) and a snake type ($L$ = 2$\mu$m, $W$ = 1830$\mu$m, gate pitch = 5$\mu$m)] fabricated on a $p$-type, (100), 4Ω-cm silicon substrate."). |
| first and second impurity regions of a second conductivity type respectively formed in the substrate, in the vicinity of said main surfaces, self-aligned to and positioned at one side and the other side of said gate electrode respectively; and | *See, e.g.*, Nishimatsu at Figs. 1, 2, 5, 6, 7, 10.<br><br>*See, e.g., id.* at 181. ("The fabrication process flow for Grooved Gate MOSFET's is shown in Fig. 5. After LOCOS oxidation, the 1st polycrystaline silicon (poly-Si) layer (3500Å) is deposited and etched by Freon plasma at the gate region. In this case, the silicon substrate is also etched to about 0.2 - 0.3 $\mu$m in depth. Gate oxidation (500 Å) is followed by the 2nd poly-Si (3500 Å) deposition process [Fig.6(a)]. A new photoresist technique (buried gate technique) is used to bury the poly-Si gate in the grooved region without using a photomask. This technique utilizes the photoresist characteristic that photoresist is formed at the grooved region about twice as thick as that of other parts. When a thin photoresist layer is removed by oxygen plasma, the photoresist is left only in the grooved gate region [Fig. 6(b)]. Then the 2nd poly-Si is etched by masking the buried photoresist and the 1st poly-Si layer is etched again to constitute the source and drain regions [Fig. |

| U.S. Patent No. 5,248,893 | |
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| | 6(c)]. The other steps are the same as those of conventional silicon-gate technology. The final cross sectional view of Grooved Gate MOSFET is shown in Fig. 6(d).").<br><br>*See, e.g., id.* at 182. ("The photoresist covering the gate on the field oxide plays the important role of an etching mask in both the 1st and 2nd poly-Si plasma etchings.").<br><br>*See, e.g., id.* at 183. ("A new promising photoresist technique (buried gate technique) was developed to fabricate self-aligned Grooved Gate MOSFET's."). |
| a first conductivity type region located in said semiconductor substrate between said first and second impurity regions for defining a channel region and a channel-free region extending conformably under and along said concave surface; | *See, e.g.,* Nishimatsu at Figs. 1-6, 8-10.<br><br>*See, e.g., id.* at 180. ("The computer results for the drain depletion regions of conventional and Grooved Gate MOSFET's with biased $V_G$=0 V and $V_D$= 10 V are shown in Fig. 3(a) and (b). The results mean that the punch-through voltage of a conventional structure with channel length $L$=2.5 $\mu$m is less than 10 V, whereas that of the Grooved Gate structure with $L$=1.5 $\mu$m is greater than 10V. Also the shorter extension width of the depletion layer implies a lessening of the $V_T$ lowering effect caused by the drain electric field.").<br><br>*See, e.g., id* at 180. ("The computer and experimental threshold voltage and channel length ($V_T$ - $L$) relationships as a function of $x_j$ are shown in Fig. 4.[3] As shown in the figure, a device with a shallow $x_j$ has little change in $V_T$ value with channel variation. Therefore, the Grooved Gate structure is expected to show a more improved $V_T$-$L$ relationship, although the $V_T$-$L$ relationship for negative $x_j$ was not calculated.").<br><br>*See, e.g., id.* at 181. ("From the computer results, it can be concluded that the proposed Grooved Gate MOSFET is an ideal device for shorter channel ($L\approx$ 1µm MOSFET's).").<br><br>*See, e.g., id.* at 181. ("The fabrication process flow for Grooved Gate MOSFET's is shown in Fig. 5. After LOCOS oxidation, the 1st polycrystaline silicon (poly-Si) layer (3500Å) is deposited and etched by Freon plasma at the gate region. In this case, the silicon substrate is also etched to about 0.2 - 0.3 $\mu$m in depth. Gate oxidation (500 Å) is followed by the 2nd poly-Si (3500 Å) deposition process [Fig.6(a)]. A new photoresist technique (buried gate technique) is used to bury the poly-Si gate in the grooved region without using a photomask. This technique utilizes the photoresist characteristic that photoresist is formed at the grooved region about twice as thick as that of other parts. When a thin photoresist layer is removed by oxygen plasma, the photoresist is left only in the grooved gate region [Fig. 6(b)]. Then the 2nd poly-Si is etched by masking |

| **U.S. Patent No. 5,248,893** | |
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| | the buried photoresist and the 1st poly-Si layer is etched again to constitute the source and drain regions [Fig. 6(c)]. The other steps are the same as those of conventional silicon-gate technology. The final cross sectional view of Grooved Gate MOSFET is shown in Fig. 6(d).").<br><br>*See, e.g., id.* at 182. ("The normalized $V_T$ - $L_M$ relationship is also depicted in Fig. 9. Curve A is for somewhat negative $x_j$ devices and curve B is for $x_j$=0.2 $\mu$m devices. Curve B is similar to that shown in Fig. 4. The unique characteristics of curve C in Fig. 9 were obtained due to apparently to [*sic*] a rather high interface state density. Grooved Gate MOSFET's with large negative $x_j$s were not intentionally fabricated, because the channel length is not defined as shown in Fig. 2."). |
| wherein the depth of said concave surface is set to a value which ranges between one and two times the depth of said first and second impurity regions, and | *See, e.g.,* Nishimatsu at Figs. 1-4, 6, 10.<br><br>*See, e.g., id.* at 179. ("Figure 1 shows a perspective view of structure of the Grooved Gate MOSFET which is characterized by a negative $x_j$. The junction depth from the silicon surface under the gate oxide is defined as $x_j$ (Fig. 2). This structure can be approximated as shown in fig. 2 for two-dimensional MOSFET analyses.").<br><br>*See, e.g., id.* at 180. ("The computer results for the drain depletion regions of conventional and Grooved Gate MOSFET's with biased $V_G$=0 V and $V_D$= 10 V are shown in Fig. 3(a) and (b). The results mean that the punch-through voltage of a conventional structure with channel length $L$=2.5 $\mu$m is less than 10 V, whereas that of the Grooved Gate structure with $L$=1.5 $\mu$m is greater than 10V. Also the shorter extension width of the depletion layer implies a lessening of the $V_T$ lowering effect caused by the drain electric field.").<br><br>*See, e.g., id.* at 181. ("From the computer results, it can be concluded that the proposed Grooved Gate MOSFET is an ideal device for shorter channel ($L\approx$ 1µm MOSFET's).").<br><br>*See, e.g., id.* at 181. ("The fabrication process flow for Grooved Gate MOSFET's is shown in Fig. 5. After LOCOS oxidation, the 1st polycrystaline silicon (poly-Si) layer (3500Å) is deposited and etched by Freon plasma at the gate region. In this case, the silicon substrate is also etched to about 0.2 - 0.3 $\mu$m in depth. Gate oxidation (500 Å) is followed by the 2nd poly-Si (3500 Å) deposition process [Fig.6(a)]. A new photoresist technique (buried gate technique) is used to bury the poly-Si gate in the grooved region without using a photomask. This technique utilizes the photoresist characteristic that photoresist is formed at the grooved region about twice as thick as that of other parts. When a thin photoresist layer is removed by oxygen plasma, the photoresist is left only in the grooved gate region [Fig. 6(b)]. Then the 2nd poly-Si is etched by masking |

| U.S. Patent No. 5,248,893 | |
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| | the buried photoresist and the 1st poly-Si layer is etched again to constitute the source and drain regions [Fig. 6(c)]. The other steps are the same as those of conventional silicon-gate technology. The final cross sectional view of Grooved Gate MOSFET is shown in Fig. 6(d).").<br><br>*See, e.g., id.* at 182. ("The normalized $V_T$ - $L_M$ relationship is also depicted in Fig. 9. Curve A is for somewhat negative $x_j$ devices and curve B is for $x_j$=0.2 $\mu$m devices. Curve B is similar to that shown in Fig. 4. The unique characteristics of curve C in Fig. 9 were obtained due to apparently to [*sic*] a rather high interface state density. Grooved Gate MOSFET's with large negative $x_j$s were not intentionally fabricated, because the channel length is not defined as shown in Fig. 2."). |
| wherein the concave surface is continuously curved in the vicinity of at least one of the first and second impurity regions to produce smooth merger of a conforming first depletion region formed around the at least one impurity region and a conforming second depletion region formed in the vicinity of the gate electrode so that excessive field concentration will not develop in the vicinity where the first and second depletion regions meet. | *See, e.g.*, Nishimatsu at Figs. 1-4, 6, 8-10.<br><br>*See, e.g., id.* at 180-81. ("The computer results for the drain depletion regions of conventional and Grooved Gate MOSFET's with biased $V_G$=0 V and $V_D$= 10 V are shown in Fig. 3(a) and (b). The results mean that the punch-through voltage of a conventional structure with channel length $L$=2.5 $\mu$m is less than 10 V, whereas that of the Grooved Gate structure with $L$=1.5 $\mu$m is greater than 10V. Also the shorter extension width of the depletion layer implies a lessening of the $V_T$ lowering effect caused by the drain electric field. Figure 3(c) shows the relationship between $x_j$ and drain depletion layer width ($W_D$) in the direction to the source as a parameter of drain voltage. The Grooved Gate structure $(x_j \lesssim 0)$ can reduce the value of $W_D$ by half as compared with conventional MOSFET's. The computer and experimental threshold voltage and channel length ($V_T$ - $L$) relationships as a function of $x_j$ are shown in Fig. 4.[3] As shown in the figure, a device with a shallow $x_j$ has little change in $V_T$ value with channel variation. Therefore, the Grooved Gate structure is expected to show a more improved $V_T$-$L$ relationship, although the $V_T$-$L$ relationship for negative $x_j$ was not calculated. From the computer results, it can be concluded that the proposed Grooved Gate MOSFET is an ideal device for shorter channel ($L\approx$ 1μm MOSFET's).").<br><br>*See, e.g., id.* at 182. ("The 2 $\mu$m channel devices displayed good punch-through breakdown voltage over 10V as shown in Fig. 8. In the figure, drain current-voltage ($I_D$-$V_D$) characteristics for devices ($L$ = 2, 2.5, 3 and 3.5 $\mu$m) are shown.").<br><br>*See, e.g., id.* at 182. ("The normalized $V_T$ - $L_M$ relationship is also depicted in Fig. 9. Curve A is for somewhat negative $x_j$ devices and curve B is for $x_j$=0.2 $\mu$m devices. Curve B is similar to that shown in Fig. 4. The unique characteristics of curve C in Fig. 9 were obtained due to apparently to [*sic*] a rather high interface state |

| U.S. Patent No. 5,248,893 | |
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| | density. Grooved Gate MOSFET's with large negative $x_j$s were not intentionally fabricated, because the channel length is not defined as shown in Fig. 2."). <br><br> *See, e.g., id.* at 183. ("The fabricated devices show high punch-through characteristics and little threshold voltage fluctuation due to channel length variation as predicted."). |
| **Claim 2** | |
| **Claim limitation** | **Nishimatsu** |
| 2. An insulated gate field effect device according to claim 1, wherein one of said first and second impurity regions constitutes a drain region of said insulated gate field effect device, the other of said first and second impurity regions constitutes a source region and wherein the concave surface is continuously curved at least in the vicinity of the drain region, where the channel-free region develops during an off state of the device, to produce smooth merger of the conforming first depletion region which develops in the vicinity of the channel-free region and the drain region and the conforming second depletion region formed in the vicinity of the gate electrode so that excessive field concentration will not develop in the vicinity of the | *See, e.g.*, Nishimatsu at Figs. 1-10. <br><br> *See, e.g., id.* at 179. ("Figure 1 shows a perspective view of structure of the Grooved Gate MOSFET which is characterized by a negative $x_j$. The junction depth from the silicon surface under the gate oxide is defined as $x_j$ (Fig. 2). This structure can be approximated as shown in fig. 2 for two-dimensional MOSFET analyses."). <br><br> *See, e.g., id.* at 80-81. ("The computer results for the drain depletion regions of conventional and Grooved Gate MOSFET's with biased $V_G$=0 V and $V_D$= 10 V are shown in Fig. 3(a) and (b). The results mean that the punch-through voltage of a conventional structure with channel length $L$=2.5 $\mu$m is less than 10 V, whereas that of the Grooved Gate structure with $L$=1.5 $\mu$m is greater than 10V. Also the shorter extension width of the depletion layer implies a lessening of the $V_T$ lowering effect caused by the drain electric field. Figure 3(c) shows the relationship between $x_j$ and drain depletion layer width ($W_D$) in the direction to the source as a parameter of drain voltage. The Grooved Gate structure $(x_j \leq 0)$ can reduce the value of $W_D$ by half as compared with conventional MOSFET's. The computer and experimental threshold voltage and channel length ($V_T$ - $L$) relationships as a function of $x_j$ are shown in Fig. 4.[3] As shown in the figure, a device with a shallow $x_j$ has little change in $V_T$ value with channel variation. Therefore, the Grooved Gate structure is expected to show a more improved $V_T$-$L$ relationship, although the $V_T$-$L$ relationship for negative $x_j$ was not calculated. From the computer results, it can be concluded that the proposed Grooved Gate MOSFET is an ideal device for shorter channel ($L \approx$ 1µm MOSFET's)."). <br><br> *See, e.g., id.* at 181. ("The fabrication process flow for Grooved Gate MOSFET's is shown in Fig. 5. After LOCOS oxidation, the 1st polycrystaline silicon (poly-Si) layer (3500Å) is deposited and etched by Freon plasma at the gate region. In this case, the silicon substrate is also etched to about 0.2 - 0.3 $\mu$m in depth. Gate |

| U.S. Patent No. 5,248,893 | |
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| channel-free region. | oxidation (500 Å) is followed by the 2nd poly-Si (3500 Å) deposition process [Fig.6(a)]. A new photoresist technique (buried gate technique) is used to bury the poly-Si gate in the grooved region without using a photomask. This technique utilizes the photoresist characteristic that photoresist is formed at the grooved region about twice as thick as that of other parts. When a thin photoresist layer is removed by oxygen plasma, the photoresist is left only in the grooved gate region [Fig. 6(b)]. Then the 2nd poly-Si is etched by masking the buried photoresist and the 1st poly-Si layer is etched again to constitute the source and drain regions [Fig. 6(c)]. The other steps are the same as those of conventional silicon-gate technology. The final cross sectional view of Grooved Gate MOSFET is shown in Fig. 6(d).").<br><br>*See, e.g., id.* at 182. ("The 2 $\mu$m channel devices displayed good punch-through breakdown voltage over 10V as shown in Fig. 8. In the figure, drain current-voltage ($I_D$-$V_D$) characteristics for devices ($L$ = 2, 2.5, 3 and 3.5 $\mu$m) are shown.").<br><br>*See, e.g., id.* at 182. ("The normalized $V_T$ - $L_M$ relationship is also depicted in Fig. 9. Curve A is for somewhat negative $x_j$ devices and curve B is for $x_j$=0.2 $\mu$m devices. Curve B is similar to that shown in Fig. 4. The unique characteristics of curve C in Fig. 9 were obtained due to apparently to [*sic*] a rather high interface state density. Grooved Gate MOSFET's with large negative $x_j$s were not intentionally fabricated, because the channel length is not defined as shown in Fig. 2.").<br><br>*See, e.g., id.* at 183. ("The fabricated devices show high punch-through characteristics and little threshold voltage fluctuation due to channel length variation as predicted."). |
| **<u>Claim 3</u>** | |
| **Claim limitation** | **Nishimatsu** |
| 3. An insulated gate field effect device according to claim 1, which comprises a metal oxide semiconductor (MOS) transistor, and wherein said insulating film | *See, e.g.*, Nishimatsu at Figs. 1, 2, 5, 6, 10.<br><br>*See, e.g., id* at 179. ("Figure 1 shows a perspective view of structure of the Grooved Gate MOSFET which is characterized by a negative $x_j$. The junction depth from the silicon surface under the gate oxide is defined as $x_j$ (Fig. 2). This structure can be approximated as shown in fig. 2 for two-dimensional MOSFET analyses."). |

| U.S. Patent No. 5,248,893 | |
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| comprises an oxide film. | *See, e.g., id.* at 181. ("The fabrication process flow for Grooved Gate MOSFET's is shown in Fig. 5. After LOCOS oxidation, the 1st polycrystaline silicon (poly-Si) layer (3500Å) is deposited and etched by Freon plasma at the gate region. In this case, the silicon substrate is also etched to about 0.2 - 0.3 $\mu$m in depth. Gate oxidation (500 Å) is followed by the 2nd poly-Si (3500 Å) deposition process [Fig.6(a)]. A new photoresist technique (buried gate technique) is used to bury the poly-Si gate in the grooved region without using a photomask. This technique utilizes the photoresist characteristic that photoresist is formed at the grooved region about twice as thick as that of other parts. When a thin photoresist layer is removed by oxygen plasma, the photoresist is left only in the grooved gate region [Fig. 6(b)]. Then the 2nd poly-Si is etched by masking the buried photoresist and the 1st poly-Si layer is etched again to constitute the source and drain regions [Fig. 6(c)]. The other steps are the same as those of conventional silicon-gate technology. The final cross sectional view of Grooved Gate MOSFET is shown in Fig. 6(d)."). |
| **Claim 4** | |
| **Claim limitation** | **Nishimatsu** |
| 4. An insulated-gate field effect transistor comprising: | Assuming for present purposes (without admitting) that the preamble is a claim limitation, Nishimatsu discloses an insulated-gate field effect transistor. *See, e.g.*, Nishimatsu at Figs. 1, 2, 10. *See, e.g.*, '893 Patent at 1:28-30. |
| a substrate having a substantially planar main surface and a concave surface portion extending continuously from the main surface to a predetermined depth below the main surface; | *See, e.g.*, Nishimatsu at Figs. 1, 2, 10; *see, e.g., id.* at 179. ("Figure 1 shows a perspective view of structure of the Grooved Gate MOSFET which is characterized by a negative $x_j$. The junction depth from the silicon surface under the gate oxide is defined as $x_j$ (Fig. 2). This structure can be approximated as shown in fig. 2 for two-dimensional MOSFET analyses."). |
| an insulating layer conformably disposed on the main surface and the concave surface portion; | *See, e.g.*, Nishimatsu at Figs. 1, 2, 5, 6, 10.<br><br>*See, e.g., id.* at 181. ("The fabrication process flow for Grooved Gate MOSFET's is shown in Fig. 5. After LOCOS oxidation, the 1st polycrystaline silicon (poly-Si) layer (3500Å) is deposited and etched by Freon plasma at the gate region. In this case, the silicon substrate is also etched to about 0.2 - 0.3 $\mu$m in depth. Gate oxidation (500 Å) is followed by the 2nd poly-Si (3500 Å) deposition process [Fig.6(a)]. A new photoresist |

| U.S. Patent No. 5,248,893 | |
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| | technique (buried gate technique) is used to bury the poly-Si gate in the grooved region without using a photomask. This technique utilizes the photoresist characteristic that photoresist is formed at the grooved region about twice as thick as that of other parts. When a thin photoresist layer is removed by oxygen plasma, the photoresist is left only in the grooved gate region [Fig. 6(b)]. Then the 2nd poly-Si is etched by masking the buried photoresist and the 1st poly-Si layer is etched again to constitute the source and drain regions [Fig. 6(c)]. The other steps are the same as those of conventional silicon-gate technology. The final cross sectional view of Grooved Gate MOSFET is shown in Fig. 6(d)."). |
| a gate conformably disposed on the insulating layer, overlying the concave surface portion, the gate having opposed first and second sides; | *See, e.g.*, Nishimatsu at Figs. 1, 2, 5-7, 10.<br><br>*See e.g., id.* at 181. ("The fabrication process flow for Grooved Gate MOSFET's is shown in Fig. 5. After LOCOS oxidation, the 1st polycrystaline silicon (poly-Si) layer (3500Å) is deposited and etched by Freon plasma at the gate region. In this case, the silicon substrate is also etched to about 0.2 - 0.3 $\mu$m in depth. Gate oxidation (500 Å) is followed by the 2nd poly-Si (3500 Å) deposition process [Fig.6(a)]. A new photoresist technique (buried gate technique) is used to bury the poly-Si gate in the grooved region without using a photomask. This technique utilizes the photoresist characteristic that photoresist is formed at the grooved region about twice as thick as that of other parts. When a thin photoresist layer is removed by oxygen plasma, the photoresist is left only in the grooved gate region [Fig. 6(b)]. Then the 2nd poly-Si is etched by masking the buried photoresist and the 1st poly-Si layer is etched again to constitute the source and drain regions [Fig. 6(c)]. The other steps are the same as those of conventional silicon-gate technology. The final cross sectional view of Grooved Gate MOSFET is shown in Fig. 6(d).").<br><br>*See, e.g., id.* at 181. ("Figure 7 shows a microphotograph of two Grooved Gate MOSFET's [a bar gate type ($L$ = 2 $\mu$m, $W$ = 260 μm) and a snake type ($L$ = 2$\mu$m, $W$ = 1830$\mu$m, gate pitch = 5$\mu$m)] fabricated on a *p*-type, (100), 4Ω-cm silicon substrate."). |
| implanted source and drain regions disposed within the substrate and self-aligned to the respective first and second opposed sides of the gate; and | *See, e.g.*, Nishimatsu at Figs. 1, 2, 5-7, 10.<br><br>*See, e.g., id.* at 181. ("The fabrication process flow for Grooved Gate MOSFET's is shown in Fig. 5. After LOCOS oxidation, the 1st polycrystaline silicon (poly-Si) layer (3500Å) is deposited and etched by Freon plasma at the gate region. In this case, the silicon substrate is also etched to about 0.2 - 0.3 $\mu$m in depth. Gate oxidation (500 Å) is followed by the 2nd poly-Si (3500 Å) deposition process [Fig.6(a)]. A new photoresist technique (buried gate technique) is used to bury the poly-Si gate in the grooved region without using a |

| U.S. Patent No. 5,248,893 | |
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| | photomask. This technique utilizes the photoresist characteristic that photoresist is formed at the grooved region about twice as thick as that of other parts. When a thin photoresist layer is removed by oxygen plasma, the photoresist is left only in the grooved gate region [Fig. 6(b)]. Then the 2nd poly-Si is etched by masking the buried photoresist and the 1st poly-Si layer is etched again to constitute the source and drain regions [Fig. 6(c)]. The other steps are the same as those of conventional silicon-gate technology. The final cross sectional view of Grooved Gate MOSFET is shown in Fig. 6(d)."). <br><br> *See, e.g., id.* at 182. ("The photoresist covering the gate on the field oxide plays the important role of an etching mask in both the 1st and 2nd poly-Si plasma etchings."). <br><br> *See, e.g., id.* at 183. ("A new promising photoresist technique (buried gate technique) was developed to fabricate self-aligned Grooved Gate MOSFET's."). |
| a channel-region formed between the source and drain regions, for defining a channel that conducts current between the source and drain regions when the transistor is in a turned-on state; | *See, e.g.*, Nishimatsu at Figs. 1-6, 8-10. <br><br> *See, e.g., id.* at 180. ("The computer results for the drain depletion regions of conventional and Grooved Gate MOSFET's with biased $V_G$=0 V and $V_D$= 10 V are shown in Fig. 3(a) and (b). The results mean that the punch-through voltage of a conventional structure with channel length $L$=2.5 $\mu$m is less than 10 V, whereas that of the Grooved Gate structure with $L$=1.5 $\mu$m is greater than 10V. Also the shorter extension width of the depletion layer implies a lessening of the $V_T$ lowering effect caused by the drain electric field."). <br><br> *See, e.g., id.* at 180. ("The computer and experimental threshold voltage and channel length ($V_T$ - $L$) relationships as a function of $x_j$ are shown in Fig. 4.[3) As shown in the figure, a device with a shallow $x_j$ has little change in $V_T$ value with channel variation. Therefore, the Grooved Gate structure is expected to show a more improved $V_T$-$L$ relationship, although the $V_T$-$L$ relationship for negative $x_j$ was not calculated."). <br><br> *See, e.g., id.* at 181. ("From the computer results, it can be concluded that the proposed Grooved Gate MOSFET is an ideal device for shorter channel ($L\approx$ 1µm MOSFET's)."). <br><br> *See, e.g., id.* at 181. ("The fabrication process flow for Grooved Gate MOSFET's is shown in Fig. 5. After LOCOS oxidation, the 1st polycrystaline silicon (poly-Si) layer (3500Å) is deposited and etched by Freon plasma at the gate region. In this case, the silicon substrate is also etched to about 0.2 - 0.3 $\mu$m in depth. Gate oxidation (500 Å) is followed by the 2nd poly-Si (3500 Å) deposition process [Fig.6(a)]. A new photoresist |

| U.S. Patent No. 5,248,893 | |
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| | technique (buried gate technique) is used to bury the poly-Si gate in the grooved region without using a photomask. This technique utilizes the photoresist characteristic that photoresist is formed at the grooved region about twice as thick as that of other parts. When a thin photoresist layer is removed by oxygen plasma, the photoresist is left only in the grooved gate region [Fig. 6(b)]. Then the 2nd poly-Si is etched by masking the buried photoresist and the 1st poly-Si layer is etched again to constitute the source and drain regions [Fig. 6(c)]. The other steps are the same as those of conventional silicon-gate technology. The final cross sectional view of Grooved Gate MOSFET is shown in Fig. 6(d)."). <br><br> *See, e.g., id.* at 182. ("The normalized $V_T$ - $L_M$ relationship is also depicted in Fig. 9. Curve A is for somewhat negative $x_j$ devices and curve B is for $x_j$=0.2 $\mu$m devices. Curve B is similar to that shown in Fig. 4. The unique characteristics of curve C in Fig. 9 were obtained due to apparently to [*sic*] a rather high interface state density. Grooved Gate MOSFET's with large negative $x_j s$ were not intentionally fabricated, because the channel length is not defined as shown in Fig. 2."). |
| wherein a channel-free zone develops in the substrate, under the gate and between the source and drain regions, when the transistor is in a turned-off state; and | *See, e.g.*, Nishimatsu at Figs. 1-6, 8-10. <br><br> *See, e.g., id.* at 180. ("The computer results for the drain depletion regions of conventional and Grooved Gate MOSFET's with biased $V_G$=0 V and $V_D$= 10 V are shown in Fig. 3(a) and (b). The results mean that the punch-through voltage of a conventional structure with channel length $L$=2.5 $\mu$m is less than 10 V, whereas that of the Grooved Gate structure with $L$=1.5 $\mu$m is greater than 10V. Also the shorter extension width of the depletion layer implies a lessening of the $V_T$ lowering effect caused by the drain electric field."). <br><br> *See, e.g., id.* at 180. ("The computer and experimental threshold voltage and channel length ($V_T$ - $L$) relationships as a function of $x_j$ are shown in Fig. 4.[3] As shown in the figure, a device with a shallow $x_j$ has little change in $V_T$ value with channel variation. Therefore, the Grooved Gate structure is expected to show a more improved $V_T$-$L$ relationship, although the $V_T$-$L$ relationship for negative $x_j$ was not calculated."). <br><br> *See, e.g., id.* at 181. ("From the computer results, it can be concluded that the proposed Grooved Gate MOSFET is an ideal device for shorter channel ($L\approx$ 1μm MOSFET's)."). <br><br> *See, e.g., id.* at 181. ("The fabrication process flow for Grooved Gate MOSFET's is shown in Fig. 5. After LOCOS oxidation, the 1st polycrystaline silicon (poly-Si) layer (3500Å) is deposited and etched by Freon plasma at the gate region. In this case, the silicon substrate is also etched to about 0.2 - 0.3 $\mu$m in depth. Gate |

| U.S. Patent No. 5,248,893 | |
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| | oxidation (500 Å) is followed by the 2nd poly-Si (3500 Å) deposition process [Fig.6(a)]. A new photoresist technique (buried gate technique) is used to bury the poly-Si gate in the grooved region without using a photomask. This technique utilizes the photoresist characteristic that photoresist is formed at the grooved region about twice as thick as that of other parts. When a thin photoresist layer is removed by oxygen plasma, the photoresist is left only in the grooved gate region [Fig. 6(b)]. Then the 2nd poly-Si is etched by masking the buried photoresist and the 1st poly-Si layer is etched again to constitute the source and drain regions [Fig. 6(c)]. The other steps are the same as those of conventional silicon-gate technology. The final cross sectional view of Grooved Gate MOSFET is shown in Fig. 6(d)."). <br><br> *See, e.g., id.* at 182. ("The normalized $V_T$ - $L_M$ relationship is also depicted in Fig. 9. Curve A is for somewhat negative $x_j$ devices and curve B is for $x_j$=0.2 $\mu$m devices. Curve B is similar to that shown in Fig. 4. The unique characteristics of curve C in Fig. 9 were obtained due to apparently to [*sic*] a rather high interface state density. Grooved Gate MOSFET's with large negative $x_j$s were not intentionally fabricated, because the channel length is not defined as shown in Fig. 2."). |
| wherein the gate and concave surface portion are curved at least in the vicinity of the channel-free zone such that a smoothly curved depletion zone boundary will develop in the vicinity of the channel-free zone when the transistor is in the turned-off state. | *See, e.g.*, Nishimatsu at Figs. 1-4, 6, 8-10. <br><br> *See, e.g., id.* at 180-81. ("The computer results for the drain depletion regions of conventional and Grooved Gate MOSFET's with biased $V_G$=0 V and $V_D$= 10 V are shown in Fig. 3(a) and (b). The results mean that the punch-through voltage of a conventional structure with channel length $L$=2.5 $\mu$m is less than 10 V, whereas that of the Grooved Gate structure with $L$=1.5 $\mu$m is greater than 10V. Also the shorter extension width of the depletion layer implies a lessening of the $V_T$ lowering effect caused by the drain electric field. Figure 3(c) shows the relationship between $x_j$ and drain depletion layer width ($W_D$) in the direction to the source as a parameter of drain voltage. The Grooved Gate structure ($x_j \lesssim 0$) can reduce the value of $W_D$ by half as compared with conventional MOSFET's. The computer and experimental threshold voltage and channel length ($V_T$ - $L$) relationships as a function of $x_j$ are shown in Fig. 4.[3] As shown in the figure, a device with a shallow $x_j$ has little change in $V_T$ value with channel variation. Therefore, the Grooved Gate structure is expected to show a more improved $V_T$-$L$ relationship, although the $V_T$-$L$ relationship for negative $x_j$ was not calculated. From the computer results, it can be concluded that the proposed Grooved Gate MOSFET is an ideal device for shorter channel ($L \approx$ 1μm MOSFET's)."). <br><br> *See, e.g., id.* at 182. ("The 2 $\mu$m channel devices displayed good punch-through breakdown voltage over 10V |

| U.S. Patent No. 5,248,893 | |
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| | as shown in Fig. 8. In the figure, drain current-voltage ($I_D$-$V_D$) characteristics for devices ($L$ = 2, 2.5, 3 and 3.5 $\mu$m) are shown."). <br><br> *See, e.g., id.* at 182. ("The normalized $V_T$ - $L_M$ relationship is also depicted in Fig. 9. Curve A is for somewhat negative $x_j$ devices and curve B is for $x_j$=0.2 $\mu$m devices. Curve B is similar to that shown in Fig. 4. The unique characteristics of curve C in Fig. 9 were obtained due to apparently to [*sic*] a rather high interface state density. Grooved Gate MOSFET's with large negative $x_j$*s* were not intentionally fabricated, because the channel length is not defined as shown in Fig. 2."). <br><br> *See, e.g., id.* at 183. ("The fabricated devices show high punch-through characteristics and little threshold voltage fluctuation due to channel length variation as predicted."). |
| **Claim 5** | |
| **Claim limitation** | **Nishimatsu** |
| 5. An insulated-gate field effect transistor according to claim 4 wherein the concave surface portion is curved in a transverse cross-sectional plane extending through the transistor between but not intersecting the first and second sides of the gate so as to provide an effective channel width greater than a width of the channel as projected onto the plane of the main substrate surface. | *See, e.g.*, Nishimatsu at Figs. 1, 4, 8-10. <br><br> *See, e.g., id.* at 180. ("The computer results for the drain depletion regions of conventional and Grooved Gate MOSFET's with biased $V_G$=0 V and $V_D$= 10 V are shown in Fig. 3(a) and (b). The results mean that the punch-through voltage of a conventional structure with channel length $L$=2.5 $\mu$m is less than 10 V, whereas that of the Grooved Gate structure with $L$=1.5 $\mu$m is greater than 10V. Also the shorter extension width of the depletion layer implies a lessening of the $V_T$ lowering effect caused by the drain electric field."). <br><br> *See, e.g., id.* at 180-181. ("The computer and experimental threshold voltage and channel length ($V_T$ - $L$) relationships as a function of $x_j$ are shown in Fig. 4.[3] As shown in the figure, a device with a shallow $x_j$ has little change in $V_T$ value with channel variation. Therefore, the Grooved Gate structure is expected to show a more improved $V_T$-$L$ relationship, although the $V_T$-$L$ relationship for negative $x_j$ was not calculated. From the computer results, it can be concluded that the proposed Grooved Gate MOSFET is an ideal device for shorter channel ($L\approx$ 1μm MOSFET's)."). <br><br> *See, e.g., id.* at 182. ("Figure 9 shows the relationship of reciprocal channel conductance and channel length ($1/\beta$-$L_M$), where $L_M$ is the channel length of the photomask design. The unit channel conductance $\beta_0$ of |

| U.S. Patent No. 5,248,893 | |
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| | 58 $\mu℧/V$ for 500 Å gate oxide devices is obtained from the gradient of the straight line in the figure. This value is the same as that for conventional silicon gate MOSFET's. The effective channel length $L_{eff}$ is also obtained as follows. $L_{eff} = L_M + 0.6\ \mu m$. (10).").<br><br>*See, e.g., id.* at 182. ("The normalized $V_T - L_M$ relationship is also depicted in Fig. 9. Curve A is for somewhat negative $x_j$ devices and curve B is for $x_j$=0.2 $\mu$m devices. Curve B is similar to that shown in Fig. 4. The unique characteristics of curve C in Fig. 9 were obtained due to apparently to [*sic*] a rather high interface state density. Grooved Gate MOSFET's with large negative $x_j$s were not intentionally fabricated, because the channel length is not defined as shown in Fig. 2.").<br><br>*See, e.g., id.* at 183. ("The fabricated devices show high punch-through characteristics and little threshold voltage fluctuation due to channel length variation as predicted."). |
| **Claim 6** | |
| **Claim limitation** | **Nishimatsu** |
| 6. An insulated-gate field effect transistor according to claim 5 wherein the concave surface portion is curved both in the transverse cross-sectional plane and in a non-transverse cross-sectional plane, extending between and joining the first and second sides of the gate, so as to provide an effective channel surface area greater than an area of the channel as projected onto the plane of the main substrate surface. | *See, e.g.*, Nishimatsu at Figs. 1, 3, 4, 7-10.<br><br>*See, e.g., id.* at 180-81. ("The computer results for the drain depletion regions of conventional and Grooved Gate MOSFET's with biased $V_G$=0 V and $V_D$= 10 V are shown in Fig. 3(a) and (b). The results mean that the punch-through voltage of a conventional structure with channel length $L$=2.5 $\mu$m is less than 10 V, whereas that of the Grooved Gate structure with $L$=1.5 $\mu$m is greater than 10V. Also the shorter extension width of the depletion layer implies a lessening of the $V_T$ lowering effect caused by the drain electric field. Figure 3(c) shows the relationship between $x_j$ and drain depletion layer width ($W_D$) in the direction to the source as a parameter of drain voltage. The Grooved Gate structure ($x_j \leq 0$) can reduce the value of $W_D$ by half as compared with conventional MOSFET's. The computer and experimental threshold voltage and channel length ($V_T$ - $L$) relationships as a function of $x_j$ are shown in Fig. 4.[3] As shown in the figure, a device with a shallow $x_j$ has little change in $V_T$ value with channel variation. Therefore, the Grooved Gate structure is expected to show a more improved $V_T$-$L$ relationship, although the $V_T$-$L$ relationship for negative $x_j$ was not calculated. From the computer results, it can be concluded that the proposed Grooved Gate MOSFET is an ideal device for shorter channel ($L \approx 1\mu$m MOSFET's)."). |

| | **U.S. Patent No. 5,248,893** |
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| | *See, e.g., id.* at 181. ("Figure 7 shows a microphotograph of two Grooved Gate MOSFET's [a bar gate type ($L$ = 2 $\mu$m, $W$ = 260 μm) and a snake type ($L$ = 2$\mu$m, $W$ = 1830$\mu$m, gate pitch = 5$\mu$m)] fabricated on a *p*-type, (100), 4Ω-cm silicon substrate.").<br><br>*See, e.g., id.* at 182. ("Figure 9 shows the relationship of reciprocal channel conductance and channel length ($1/\beta$-$L_M$), where $L_M$ is the channel length of the photomask design. The unit channel conductance $\beta_0$ of 58 $\mu$℧/V for 500 Å gate oxide devices is obtained from the gradient of the straight line in the figure. This value is the same as that for conventional silicon gate MOSFET's. The effective channel length $L_{eff}$ is also obtained as follows. $L_{eff} = L_M + 0.6$ $\mu$m. (10).").<br><br>*See, e.g., id.* at 182. ("The normalized $V_T$ - $L_M$ relationship is also depicted in Fig. 9. Curve A is for somewhat negative $x_j$ devices and curve B is for $x_j$=0.2 $\mu$m devices. Curve B is similar to that shown in Fig. 4. The unique characteristics of curve C in Fig. 9 were obtained due to apparently to [*sic*] a rather high interface state density. Grooved Gate MOSFET's with large negative $x_j$*s* were not intentionally fabricated, because the channel length is not defined as shown in Fig. 2.").<br><br>*See, e.g., id.* at 183. ("The fabricated devices show high punch-through characteristics and little threshold voltage fluctuation due to channel length variation as predicted."). |

**Claim 7**

| **Claim limitation** | **Nishimatsu** |
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| 7. An insulated-gate field effect transistor according to claim 6 wherein the concave surface portion is equally curved both in the transverse cross-sectional plane and in the non-transverse cross-sectional plane, so as to provide a sheet-like depletion region having a uniform thickness and a smooth bottom boundary underlying the channel | *See, e.g.*, Nishimatsu at Figs. 1, 3, 4, 8-10.<br><br>*See, e.g., id.* at 180-81. ("The computer results for the drain depletion regions of conventional and Grooved Gate MOSFET's with biased $V_G$=0 V and $V_D$= 10 V are shown in Fig. 3(a) and (b). The results mean that the punch-through voltage of a conventional structure with channel length $L$=2.5 $\mu$m is less than 10 V, whereas that of the Grooved Gate structure with $L$=1.5 $\mu$m is greater than 10V. Also the shorter extension width of the depletion layer implies a lessening of the $V_T$ lowering effect caused by the drain electric field. Figure 3(c) shows the relationship between $x_j$ and drain depletion layer width ($W_D$) in the direction to the source as a parameter of drain voltage. The Grooved Gate structure ($x_j \leq 0$) can reduce the value of $W_D$ by half as compared with conventional MOSFET's. The computer and experimental threshold voltage and channel |

| U.S. Patent No. 5,248,893 | |
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| region and the source and drain regions, when the transistor is in a turned-off state. | length ($V_T$ - $L$) relationships as a function of $x_j$ are shown in Fig. 4.[3] As shown in the figure, a device with a shallow $x_j$ has little change in $V_T$ value with channel variation. Therefore, the Grooved Gate structure is expected to show a more improved $V_T$-$L$ relationship, although the $V_T$-$L$ relationship for negative $x_j$ was not calculated. From the computer results, it can be concluded that the proposed Grooved Gate MOSFET is an ideal device for shorter channel ($L \approx$ 1μm MOSFET's).").<br><br>("One of skill in the art would understand that a standard etch technique would result in an equally curved concavity in the transverse and non-transverse planes."). *See also,* Natori at 454 (discussing isotropic etching). |
| **Claim 11** | |
| **Claim limitation** | **Nishimatsu** |
| 11. An insulated-gate field effect transistor according to claim 4 wherein the depth of the concave surface portion is set to a value which ranges between one and two times the depth of the source and drain regions. | *See, e.g.*, Nishimatsu at Figs. 1-4, 6, 10.<br><br>*See, e.g., id.* at 179. ("Figure 1 shows a perspective view of structure of the Grooved Gate MOSFET which is characterized by a negative $x_j$. The junction depth from the silicon surface under the gate oxide is defined as $x_j$ (Fig. 2). This structure can be approximated as shown in fig. 2 for two-dimensional MOSFET analyses.").<br><br>*See, e.g., id.* at 180. ("The computer results for the drain depletion regions of conventional and Grooved Gate MOSFET's with biased $V_G$=0 V and $V_D$= 10 V are shown in Fig. 3(a) and (b). The results mean that the punch-through voltage of a conventional structure with channel length $L$=2.5 $\mu$m is less than 10 V, whereas that of the Grooved Gate structure with $L$=1.5 $\mu$m is greater than 10V. Also the shorter extension width of the depletion layer implies a lessening of the $V_T$ lowering effect caused by the drain electric field.").<br><br>*See, e.g., id.* at 181. ("From the computer results, it can be concluded that the proposed Grooved Gate MOSFET is an ideal device for shorter channel ($L \approx$ 1μm MOSFET's).").<br><br>*See, e.g., id.* at 181. ("The fabrication process flow for Grooved Gate MOSFET's is shown in Fig. 5. After LOCOS oxidation, the 1st polycrystaline silicon (poly-Si) layer (3500Å) is deposited and etched by Freon plasma at the gate region. In this case, the silicon substrate is also etched to about 0.2 - 0.3 $\mu$m in depth. Gate oxidation (500 Å) is followed by the 2nd poly-Si (3500 Å) deposition process [Fig.6(a)]. A new photoresist technique (buried gate technique) is used to bury the poly-Si gate in the grooved region without using a |

| U.S. Patent No. 5,248,893 | |
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| | photomask. This technique utilizes the photoresist characteristic that photoresist is formed at the grooved region about twice as thick as that of other parts. When a thin photoresist layer is removed by oxygen plasma, the photoresist is left only in the grooved gate region [Fig. 6(b)]. Then the 2nd poly-Si is etched by masking the buried photoresist and the 1st poly-Si layer is etched again to constitute the source and drain regions [Fig. 6(c)]. The other steps are the same as those of conventional silicon-gate technology. The final cross sectional view of Grooved Gate MOSFET is shown in Fig. 6(d)."). <br><br> *See, e.g., id.* at 182. ("The normalized $V_T$ - $L_M$ relationship is also depicted in Fig. 9. Curve A is for somewhat negative $x_j$ devices and curve B is for $x_j$=0.2 $\mu$m devices. Curve B is similar to that shown in Fig. 4. The unique characteristics of curve C in Fig. 9 were obtained due to apparently to [*sic*] a rather high interface state density. Grooved Gate MOSFET's with large negative $x_j s$ were not intentionally fabricated, because the channel length is not defined as shown in Fig. 2."). |