EXHIBIT 6

June 9-10, 1992

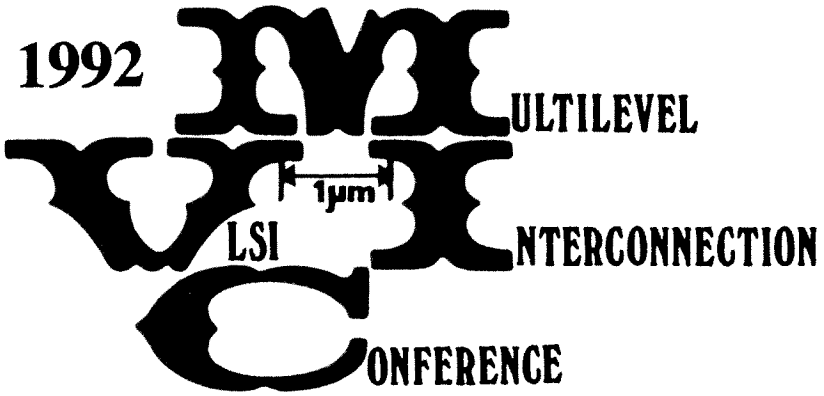
Santa Clara Marriott Hotel
Santa Clara, CA

VMIC Catalog No.
92ISMIC-101

1992 PROCEEDINGS

NINTH INTERNATIONAL

VLSI MULTILEVEL INTERCONNECTION CONFERENCE (VMIC)



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CONFERENCE REGISTRATION

1992 VMIC participants may register either in advance or at the door. **For Advanced Registration,** your application and payment check or money order must be **postmarked** no later than **May 28, 1992.** Those who register in advance may pick up all Conference information (including Proceedings) at the registration desk. Additional registration forms may be obtained by calling the V-MIC Conference Secretary at (813) 978-3552. Applications received without payment **will not be honored as advance registration. Also, no confirmation of advanced registration receipt will be sent.**

Cancellation: Refunds for cancellations of advance registration will be honored provided the requests to cancel are made in writing and are **received** no later than May 30, 1992. All refunds for cancellation will be subject to a $25.00 handling charge.

Registration entitles an attendee admission to all sessions, handouts, coffee breaks, a set of the official Proceedings of the Conference, a box lunch on Tuesday, and an Awards Luncheon Ticket.

Payment at the conference registration desk must be in the form of a check, money order or cash. Credit Cards and purchase orders can not be accepted.

CONFERENCE BADGES

All attendees **must wear** their conference badge for admittance **to all sessions.** Single day registering attendees will have a **different color** badge than regular attendees.

MARRIOTT'S GREAT AMERICA

Marriott's Great America, located adjacent to the hotel, is a 200-acre family entertainment center featuring shows, rides, nd 26 restaurants. Since opening in 1976, Great America has established itself as the largest and most popular Theme ark in the Northwest United States. Architecture, music, costumes, shops, and restaurants combine to create a sense what life was like during parts of our country's colorful past. With six major stage, screen and arena shows, the curtain literally always going up somewhere at Great America.

NINTH INTERNATIONAL VLSI MULTILEVEL INTERCONNECTION CONFERENCE

June 9-10, 1992

ADVANCE PROGRAM

Tuesday, June 9, 1992

OPENING SESSION — 9 A.M.

Welcoming Remarks and General Comments
Dr. Thomas E. Wade
General Chairman
Associate Dean for Research
College of Engineering
University of South Florida

Coffee Break 9:45-10 A.M.

NINTH INTERNATIONAL
VLSI MULTILEVEL INTERCONNECTION
CONFERENCE

Wednesday, June 10, 1992

SESSION V

POSTER PAPER SECTIONS

VLSI MULTILEVEL INTERCONNECTION CONTACT AND VIA FILLING AND NOVEL STRUCTURES

SELF-ALIGNED TIN FORMATION BY N_2 PLASMA BIAS TREATMENT OF $TiSi_x$

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EXECUTIVE SUMMARY

This paper describes the self-aligned TiN formation process at low-temperature and the TiN film characteristics in application to the $TiSi_x$ contact regions of multilevel interconnections in VLSIs. It is found that a thermally stable barrier is achieved without mutual diffusion between $TiSi_x$ and Al.

EXTENDED ABSTRACT

A new TiN formation technology has been developed. A nitrogen (N_2) plasma bias treatment is used in the self-aligning formation of TiN on $TiSi_x$ which has been prepared by selective CVD deposition to form silicide only on the diffused layers [1]. The advantage of N_2 plasma bias treatment over thermal nitriding treatment is that TiN formation can occur at a considerably lower substrate temperature, 350 °C compared to 550 °C - 950 °C [2]-[3].

Figure 1 shows the process flow of contat hole fabrication by the self-aligned TiN formation technology. Nitriding was performed in a N_2 atmosphere by using a multi-gun dc magnetron sputtering system with an RF etching station. There are fewer processing steps involved in $TiN/TiSi_x$ formation than in the thermal annealing method. The N_2 plasma bias treatment of $TiSi_x$ at a substrate temperature of 350 °C and -600V self-bias voltage for 5 min results in superior properties in barrier characteristics. According to SIMS profile measurement, the TiN thickness was about 10 nm.

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Figure 2 shows the leakage current versus annealing temperature of the reverse biased p^+-n and n^+-p junction with the Al-2%Si/TiN/selective CVD $TiSi_x$/Si contact system. The results indicate that leakage current does not change even after annealing up to 500 °C for 30 min, and that it is approximately 1 X 10^{-11} A. For the Al-2%Si/selective CVD $TiSi_x$/Si contact system without N_2 plasma bias treatment, interdiffusion between $TiSi_x$ and Al caused a contact hole edge even after annealing for 30 min at 400 °C. The formed TiN layer is also resistant to wet etch in diluted HF solution. The normalized sheet resistance versus etching time in 1% HF solution at 22 °C is plotted in Fig. 3. The N_2 bias treatment samples showed greater stability improvement than the films produced without the N_2 bias treatment of $TiSi_x$.

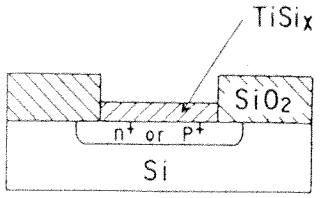
This low-temperature, self-aligned TiN formation technology, combined with selective CVD $TiSi_x$ deposition, makes it possible to form highly stable multilevel interconnections without any deteriorative problems such as interdiffusion reactions of Al to $TiSi_x$ and poor resistance to etching in diluted HF solution. In addition, the number of processing steps can be reduced.

ACKNOWLEDGMENTS

The author would like to thank K. Saito for $TiSi_x$ CVD deposition, E. Arai and K. Minegishi for helpful discussions.

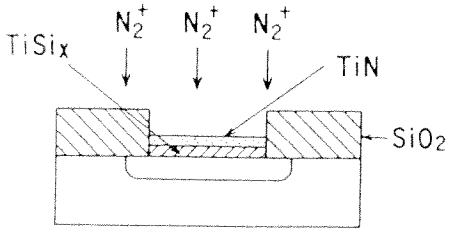
REFERENCES

[1] K. Saito et al., Ext. Abstract 21st Conf. on Solid State Devices and Materials, Tokyo, 541 (1989).
[2] C. Y. Ting, J. Vac. Sci. Technol., vol. 21, 14 (1982)
[3] H. Kaneko et al., IEEE Trans. Electron Devices, vol. ED-33, 1702 (1986)



[Selective CVD deposition of $TiSi_x$]

Thickness: 40 nm

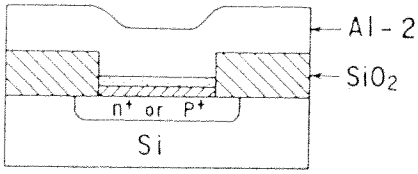


[N_2 plasma bias treatment]

Substrate temperature: 350 °C

Self-bias voltage: -600V

Treatment time: 5 min.



[Al deposition]

Thickness: 1 μm

Fig. 1. Process flow of contact hole fabrication by N_2 plasma bias treatment method.

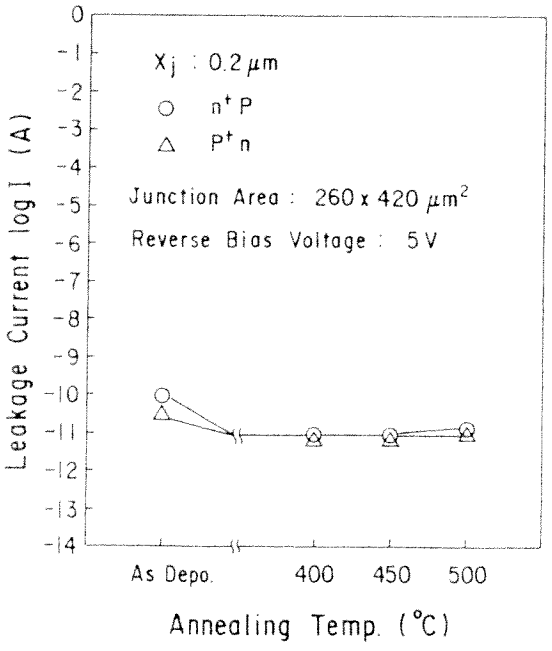


Fig. 2. Leakage current of reverse biased n^+-p and p^+-n junction after 30 min. annealing.

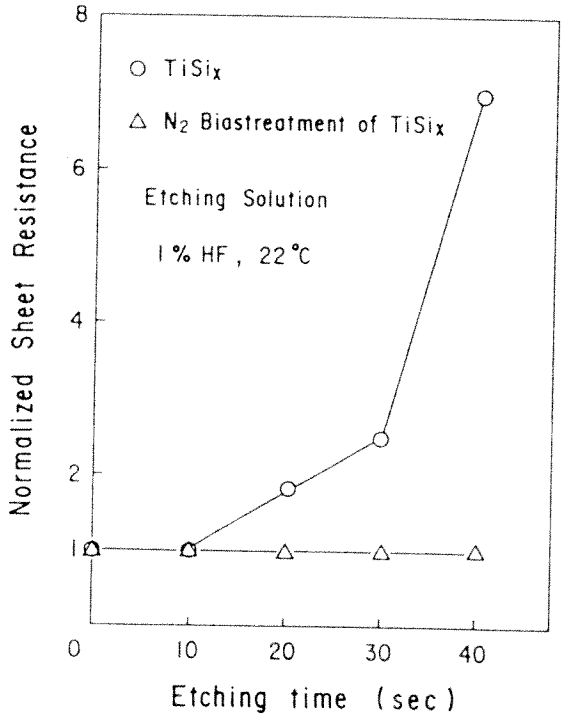


Fig. 3. Sheet resistance vs etching time in 1%HF.