

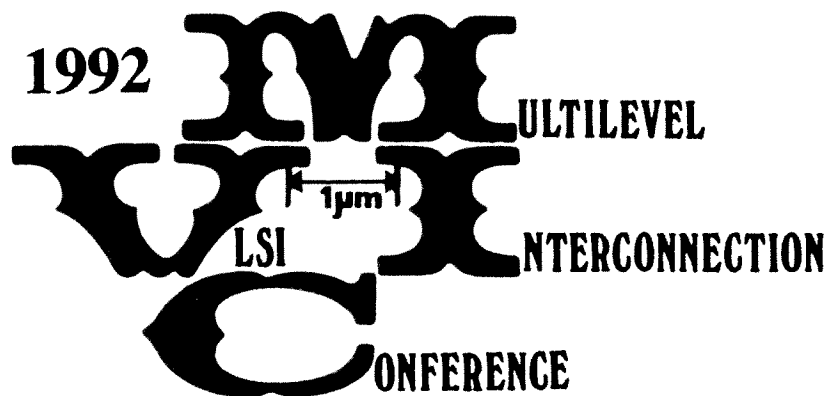
EXHIBIT 6

June 9-10, 1992

VMIC Catalog No.
92ISMIC-101

Santa Clara Marriott Hotel
Santa Clara, CA

1992
PROCEEDINGS
NINTH INTERNATIONAL
VLSI MULTILEVEL
INTERCONNECTION
CONFERENCE
(VMIC)



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Registration entitles an attendee admission to all sessions, handouts, coffee breaks, a set of the official Proceedings of the Conference, a box lunch on Tuesday, and an Awards Luncheon Ticket.

Payment at the conference registration desk must be in the form of a check, money order or cash. Credit Cards and purchase orders can not be accepted.

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**NINTH INTERNATIONAL
VLSI MULTILEVEL INTERCONNECTION
CONFERENCE**

June 9-10, 1992

ADVANCE PROGRAM

Tuesday, June 9, 1992

OPENING SESSION — 9 A.M.

Welcoming Remarks and General Comments
Dr. Thomas E. Wade
General Chairman
Associate Dean for Research
College of Engineering
University of South Florida

SESSION I — 9:15 A.M. 9

KEYNOTE ADDRESS

**“MULTILEVEL METAL PARTNERSHIPS
AND INFRASTRUCTURE”**

Dr. Thomas Seidel
Director, MLM & Etech
SEMATECH
Austin, TX

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Chairman: Dr. Rob Wolters
PHILIPS RESEARCH LABS
The Netherlands

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Colorado Springs, CO

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VLSI MULTILEVEL INTERCONNECTION

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(SRC) — From 1982 to 2002"
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AT&T BELL LABS / SEMATECH
Austin, TX

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**NINTH INTERNATIONAL
VLSI MULTILEVEL INTERCONNECTION
CONFERENCE**

Wednesday, June 10, 1992

SESSION V

POSTER PAPER SECTIONS

**VLSI MULTILEVEL INTERCONNECTION
CONTACT AND VIA FILLING AND NOVEL STRUCTURES**

SELF-ALIGNED TIN FORMATION BY N₂

PLASMA BIAS TREATMENT OF TiSi_x

Kazuyoshi Kamoshida
NTT LSI Laboratories
3-1 Morinosato Wakamiya,
Atsugi-shi, Kanagawa, Japan.

EXECUTIVE SUMMARY

This paper describes the self-aligned TiN formation process at low-temperature and the TiN film characteristics in application to the TiSi_x contact regions of multilevel interconnections in VLSIs. It is found that a thermally stable barrier is achieved without mutual diffusion between TiSi_x and Al.

EXTENDED ABSTRACT

A new TiN formation technology has been developed. A nitrogen (N₂) plasma bias treatment is used in the self-aligning formation of TiN on TiSi_x which has been prepared by selective CVD deposition to form silicide only on the diffused layers [1]. The advantage of N₂ plasma bias treatment over thermal nitriding treatment is that TiN formation can occur at a considerably lower substrate temperature, 350 °C compared to 550 °C - 950 °C [2]-[3].

Figure 1 shows the process flow of contact hole fabrication by the self-aligned TiN formation technology. Nitriding was performed in a N₂ atmosphere by using a multi-gun dc magnetron sputtering system with an RF etching station. There are fewer processing steps involved in TiN/TiSi_x formation than in the thermal annealing method. The N₂ plasma bias treatment of TiSi_x at a substrate temperature of 350 °C and -600V self-bias voltage for 5 min results in superior properties in barrier characteristics. According to SIMS profile measurement, the TiN thickness was about 10 nm.

Figure 2 shows the leakage current versus annealing temperature of the reverse biased p^+-n and n^+-p junction with the Al-2%Si/TiN/selective CVD $TiSi_x$ /Si contact system. The results indicate that leakage current does not change even after annealing up to 500 °C for 30 min, and that it is approximately 1×10^{-11} A. For the Al-2%Si/selective CVD $TiSi_x$ /Si contact system without N_2 plasma bias treatment, interdiffusion between $TiSi_x$ and Al caused a contact hole edge even after annealing for 30 min at 400 °C. The formed TiN layer is also resistant to wet etch in diluted HF solution. The normalized sheet resistance versus etching time in 1% HF solution at 22 °C is plotted in Fig. 3. The N_2 bias treatment samples showed greater stability improvement than the films produced without the N_2 bias treatment of $TiSi_x$.

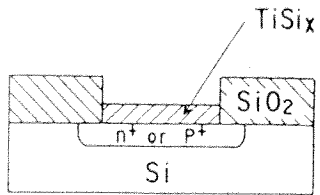
This low-temperature, self-aligned TiN formation technology, combined with selective CVD $TiSi_x$ deposition, makes it possible to form highly stable multilevel interconnections without any deteriorative problems such as interdiffusion reactions of Al to $TiSi_x$ and poor resistance to etching in diluted HF solution. In addition, the number of processing steps can be reduced.

ACKNOWLEDGMENTS

The author would like to thank K. Saito for $TiSi_x$ CVD deposition, E. Arai and K. Minegishi for helpful discussions.

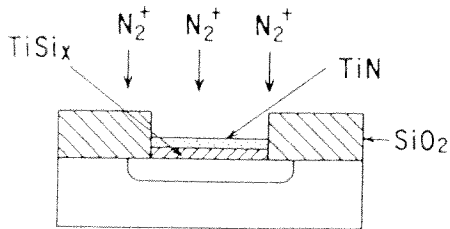
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- [2] C. Y. Ting, J. Vac. Sci. Technol., vol. 21, 14 (1982)
- [3] H. Kaneko et al., IEEE Trans. Electron Devices, vol. ED-33, 1702 (1986)



[Selective CVD deposition of $TiSi_x$]

Thickness: 40 nm

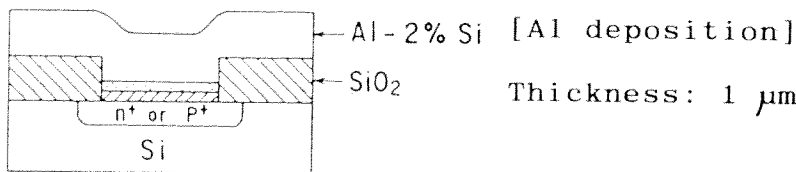


[N_2 plasma bias treatment]

Substrate temperature: $350^\circ C$

Self-bias voltage: $-600V$

Treatment time: 5 min.



Al-2% Si [Al deposition]

Thickness: $1 \mu m$

Fig. 1. Process flow of contact hole fabrication by N_2 plasma bias treatment method.

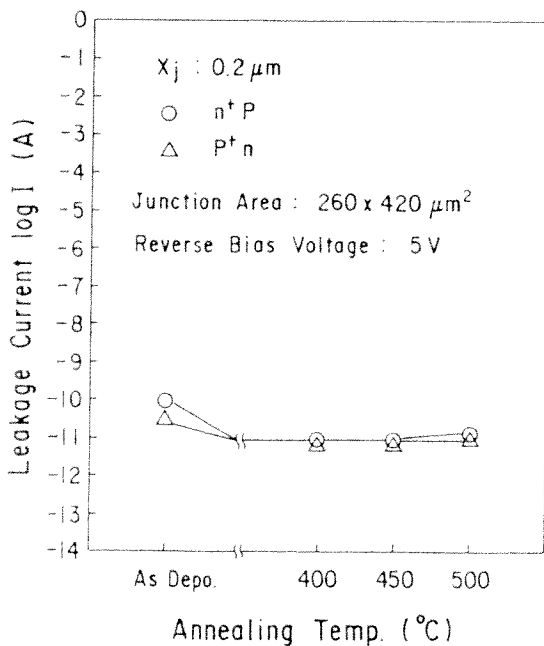


Fig. 2. Leakage current of reverse biased n^+p and p^+n junction after 30 min. annealing.

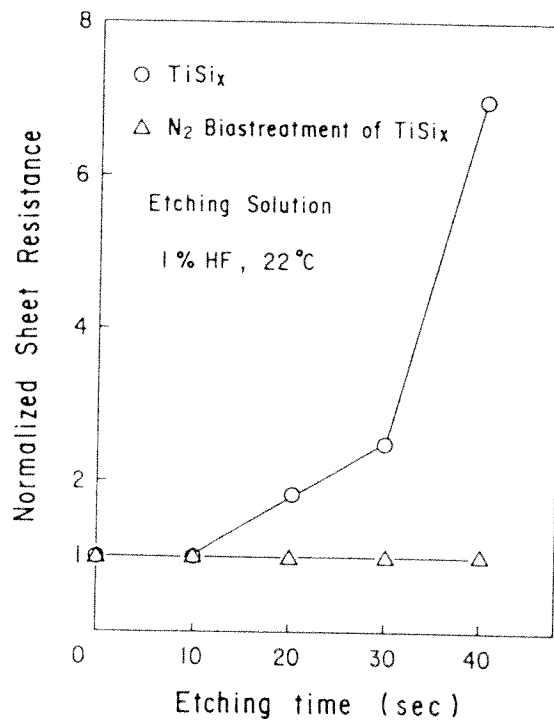


Fig. 3. Sheet resistance vs etching time in 1%HF.