EXHIBIT 1

D1-D2

Appendix D1
Defendants and Counterclaimants' Invalidity Contentions
Advanced Micro Devices, Inc., et al., v. Samsung Electronics Co., Ltd., et al., Case No. 3:08-CV-0986-SI

U.S. patent No. 5,559,990 Invalidity Chart: United States Patent No. 4,849,937 ("'937 Reference")

All asserted claims are anticipated by the '937 Reference and/or are rendered obvious by it, either alone or in combination with other prior art described below and/or listed in Section I of Defendants' and Counterclaimants' Preliminary Invalidity Contentions and/or through modifications described below. Nothing in this invalidity chart should be construed as signifying or suggesting Defendants and Counterclaimants' adoption of or acquiescence in any claim scope and/or claim construction positions taken by Plaintiffs and Counterdefendants in this litigation.

CLAIM	RESPONSE
20. An integrated memory comprising:	
an array of memory locations, the array comprising a plurality of subarrays, each subarray comprising a predetermined number of groups of columns of the memory locations such that for any given column position in a group, the memory locations in any given row in the columns at said given position in the groups of the subarray have consecutive addresses;	This element is met in U.S. Patent No. 4,849,937 ("the '937 Reference"). Specifically, the '937 Reference states that: "Briefly stated, the present invention provides a digital delay unit comprising a memory cell group arrayed in the form of a matrix divided into two address spaces which are alternatively accessed so that data read from the two address spaces are alternately outputted at the clock rate of basic clock pulses and input data received synchronously with the basic clock pulses are alternately written in the two address spaces." ['937 Reference, Col. 3:23-30]
one X-decoder for each subarray;	This element is met in the '937 Reference. Specifically, the '937 Reference states that: "The address counter 81 receives the signals $\emptyset_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $\emptyset_{EV}$ (i.e., twice that of the basic clock pulses $\emptyset_S$). Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are

CLAIM	RESPONSE
	supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42] The '937 Reference could also be combined with U.S. Patent No. 5,280,594 (including the '899 application incorporated by reference and U.S. Patent No. 5,285,421) ("the '594 Reference") or JP-02-282994-A ("the '994 Reference") to meet this limitation.
one X-register for each X-decoder;	This element is met in the '937 Reference. Specifically, the '937 Reference states that: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42]

CLAIM	RESPONSE
	The '937 Reference could also be combined with the '594 Reference or the '994 Reference to meet this limitation.
one Y-decoder for each subarray;	This element is met in the '937 Reference. Specifically, the '937 Reference states that: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42] The '937 Reference could also be combined with the '594 Reference or the '994 Reference to meet this limitation.
one Y-register for each Y-decoder;	This element is met in the '937 Reference. Specifically, the '937 Reference states that: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e. twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 82 are supplied to the

CLAIM	RESPONSE
	first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. Ina similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e. twice that of the basic clock pulses $Ø_{S}$). Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42] The '937 Reference could also be combined with the '594 Reference or the '994 Reference to meet this limitation.
one Y-select circuit for each subarray, the Y-select circuit being responsive to the Y-decoder of the subarray to select all the columns that occupy a selected position in the groups of the subarray;	This element is met in the '937 Reference. Specifically, the '937 Reference states: "Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to a transfer gate 85.... In a similar manner, the transfer gate 95 transfers data read from the second memory cell array 94 to the sense amplifier 96 through an I/O line 103, while transferring data from the write circuit 98 received through the I/O line 103 to the second memory cell array 94." ['937 Reference, Col. 4:33-52] The '937 Reference could also be combined with the '594 Reference or the '994 Reference to meet this limitation.
a plurality of sense amplifier circuits for each subarray, each sense amplifier circuit for amplifying signals from a column	This element by the '937 Reference alone or in combination with any of EP 0 087 754 B1 ("the '754 Reference") or U.S. 5,036,494 ("the '494 Reference") of the admitted prior art disclosed in Figures 1 and

CLAIM	RESPONSE
selected by the Y-select circuit of the subarray;	2 of the '990 patent. Specifically, the '937 patent states that: "The sense amplifier 86 is controlled by the signals SE_{EV} to amplify the read data thereby to supply the same to the date latch 87, which in turn temporarily stores the outputs from the sense amplifier 86." ['937 Reference, Col. 4:52-56] "In a similar manner, the sense amplifier 96 is controlled by the signals SE_{OD} to amplify the read data thereby to supply the same to the data latch 97, which in turn temporarily stores the outputs from the sense amplifier 96." ['937 Reference, Col. 4:60-64] The '754 Reference states: "The present invention involves a semiconductor dynamic memory device comprising [...] a plurality of sense amplifying means responsive to a control signal input thereto, for selectively activating one sense amplifying means to sense and amplify data on said selected data lines of one of said two column-selected memory blocks, and for selectively activating at least one other sense amplifying means to refresh data of said each memory cell along said selected word lines, ..." ['754 Reference, Page 3:65-4:10] The '494 Reference states: "The bit lines are each connected to column multiplexing circuitry 37 for each column and coupled to sense amplifier and coupled to sense

CLAIM	RESPONSE
	amplifier and write circuitry 38 for each column." ['494 Reference, Col. 8:3-6] Further, the '990 patent discloses prior art Figures 1 and 2 showing embodiments using either a single sense amplifier or a plurality of sense amplifiers. A person of skill in the art would know to use a plurality of sense amplifier circuits for each subarray.
a memory output; and	This element by the '937 Reference. Specifically, the '937 patent states that: "Further, data from the data latch 97 are transferred to the output latch 89 during when the signals OE_{OD} are at high levels. The output latch 89 outputs the data delayed by M cycles synchronously with the basic clock pulses $Ø_S$, to supply the same to output terminals 80_1 to 80_n." ['937 Reference, Col. 4:66-5:3]
a control circuit for selecting one of the sense amplifier circuits to provide data to the memory output;	This element by the '937 Reference alone or in combination with the '754 Reference or admitted prior art disclosed in Figures 1 and 2 of the '990 patent. Specifically, the '937 Reference states: "The sense amplifier 86 is controlled by the signals SE_{EV} to amplify the read data thereby to supply the same to the data latch 87, which in turn temporarily stores the outputs from the sense amplifier 86. When the signals SE_{EV} are at low levels, the data latch 87 is electrically cut off from the sense amplifier 86 [....] In a similar manner, the sense amplifier 96 is controlled by the signals SE_{OD} to

CLAIM	RESPONSE
	amplify the read data thereby to supply the same to the data latch 97, which in turn temporarily stores the outputs from the sense amplifier 96. When the signals SE_{OD} are at low levels, the data latch 97 is electrically cut off from the sense amplifier 96." ['937 Reference, Col. 4:52-66] The knowledge of a person of skill in the art regarding the use of a control circuit to select one of the sense amplifier circuits in an embodiment using a plurality of sense amplifier circuits is further established by the '754 Reference. The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "A semiconductor dynamic memory device comprising: ... a plurality of sense amplifying means (18-1 to 18-4; SA1 to SA8) responsive to a control signal input thereto, for selectively activating one sense amplifying means to sense and amplify data on said selected data lines of one of said two column-selected memory blocks, and for selectively activating at least one other sense amplifying means to refresh data to said each memory cell along said selected word lines; ...." ['754 Reference, Page 6:53-Page 6:64]

CLAIM	RESPONSE
	The '990 patent discloses prior art Figure 2 showing register select circuit 224 for selecting one of the sense amplifier circuits to provide data to the memory output. A person of skill in the art would know to use control circuit to select one of the sense amplifier circuits in an embodiment using a plurality of sense amplifier circuits. The '937 Reference could also be combined with the '594 Reference or the '994 Reference to meet this limitation.
wherein in a burst mode read operation, at least one X-register provides to its respective X-decoder signals identifying a row in one of the subarrays, and at least one Y-register provides to its respective Y-decoder signals identifying a position of columns in the groups of one of the subarrays.	This element by the '937 Reference alone or in combination with the '754 Reference or the '494 Reference or U.S. Patent No. 4,875,196 ("the '196 Reference") or admitted prior art disclosed in Figure 2 of the '990 patent. Specifically, the '937 patent states that: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 92 are supplied to an X decoder 92 and add Y address signals to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42]

CLAIM	RESPONSE
	The '754 Reference states: "Furthermore, this dynamic memory device has row and column address buffers 20 and 22 for respectively storing row and column address data supplied from an address signal generator (not shown); ...." ['754 Reference, Page 4:44-51] "Output data from the row address buffer 20 excluding the most significant bit MSB is supplied to the row decoders 16-1 to 16-4, and the output data from the column address buffer 22 is supplied to the columns decoders 14-1 and 14-2 through the gate circuits 30 and 32, respectively." ['754 Reference, Page 4:52-54] The '494 Reference states: In the example shown in FIG. 1 each memory block 14 and 15 has sixty four columns 35, each column being coupled to equate and precharge circuitry 36. The columns are arranged in groups, each group having eight pairs of bit lines so that when any column is addressed eight pairs of bit lines (one in each group) are simultaneously accessed, permitting transfer of eight bits or one word at a time. The bit lines are each connected to column multiplexing circuitry 37 for each columns and coupled to sense amplifier and write circuitry 38 for each column. Each sense amplifier and write circuit is connected through a bus driver circuit 39 to the data output 17. Each memory block 14 and 15 has 70 rows each having a word line 25. The word lines are connected to a row decoder 40. The row decoder is coupled to memory block 14

CLAIM	RESPONSE
	through a latch and word line driver 41 and to the memory block 15 through a latch and word line driver 42. The column multiplex circuitry 37 is controlled by a column counter 44. The row decoder 40 is controlled by a row counter 45. The latch and word line drivers 41 and 42 are controlled by pulse generators 46 and 47 respectively. Each of the drivers 41 and 42 is connected by two separate control lines 48 to the respective one of the pulse generators 46 and 47 so that each driver can be operated either to latch the output of the row decoder 40 or to drive all the word lines low. The selection of memory locations forming each cyclic pattern of addressing is controlled by the control until 13. The row counter 45 and columns counter 44 are connected so that unless instructed by the control 13 to do otherwise they count through successive addresses along each row and then row by row." ['494 Reference, Col. 7:44-8:27] The '196 Reference states that: "In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit lines in the other array are being precharged. Thus, as data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit lines in that array will already have been initialied." '196 Reference, Col. 2:60-67 "In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and settling transient signals) in preparation for the next access form such other array. Therefore, precharging times for one array overlap the

CLAIM	RESPONSE
	time for performing read or write operation in the other array, and therefore do not limit operating speed." ['196 Reference, Col. 3:41-47] The '990 patent discloses prior art Figure 2 showing an embodiment with a burst mode operation. A person of skill in the art would know to implement a burst mode operation with the circuitry of the '937 Reference to provide faster memory access. ['990 Reference, 1:36-44] The '937 Reference could also be combined with the '594 Reference or the '994 Reference to meet this limitation.
22. The memory of claim 20 wherein in the burst mode read operation while data from the sense amplifier circuits of one of the subarrays are provided to the memory output, the sense amplifier circuits of another one of the subarrays develop output signals corresponding to data in said other one of the subarrays.	This element is met by the '937 Reference in combination with the '196 Reference or the '494 Reference. The '196 Reference states that: "In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit lines in the other array are being precharged. Thus, as data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit lines in that array will already have been initialied." ['196 Reference, Col. 2:60-67] "In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and settling transient signals) in preparation for the next access form such

CLAIM	RESPONSE
	other array. Therefore, precharging times for one array overlap the time for performing read or write operation in the other array, and therefore do not limit operating speed." ['196 Reference, Col. 3:41-47] The '494 Reference states: "The selection of memory locations forming each cyclic pattern of addressing is controlled by the control unit 13. The row counter 45 and column counter 44 are connected so that unless instructed by the control 13 to do otherwise they count through successive addresses along each row and then row by row." ['494 Reference, Col. 8:22-27] "Consequently after reaching address 0 the column and row counters cycle sequentially along each row for the two memory blocks in turn (starting at column zero of row 0 in array 0) using all memory locations in each row and then moving to the next row and repeating the operation." ['494 Reference, Col. 11:26-31] "addressing sequentially more than one memory location in said first memory block and effecting a data transfer for each memory location addressed, and at the same time effecting an equate operation on bit lines in said second memory block; and after addressing memory locations in said first memory block, switching said addressing and equate operation so as to address sequentially more than one memory location in said second memory block and effecting a data transfer for each memory location addressed and at the same time equating bit lines in said first memory block." ['494 Reference, Col. 13:36-48]

CLAIM	RESPONSE
23. The memory of claim 20 wherein in the burst mode read operation, the control circuit enables the sense amplifier circuit selected to provide data to the memory output and at the same time disables one or more sense amplifier circuits not selected to provide data to the memory output.	This limitation is met by the '937 Reference in combination with any of the '754 Reference or U.S. Patent No. 4,957,788 ("the '788 Reference") or U.S. Patent No. 5,263,003 or U.S. Patent No. 5,251,178 ("the '178 Reference"). The '937 Reference states: "The sense amplifier 86 is controlled by the signals SE_{EV} to amplify the read data thereby to supply the same to the data latch 87, which in turn temporarily stores the outputs from the sense amplifier 86. When the signals SE_{EV} are at low levels, the data latch 87 is electrically cut off from the sense amplifier 86. Data from the data latch 87 are transferred to the output latch 89 when the signals OE_{EV} are at high levels. In a similar manner, the sense amplifier 96 is controlled by the signals SE_{OD} to amplify the read data thereby to supply the same to the data latch 97, which in turn temporarily stores the outputs from the sense amplifier 96. When the signals SE_{OD} are at low levels, the data latch 97 is electrically cut off from the sense amplifier 96." ['937 Reference, Col. 4:52-66] The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the

CLAIM	RESPONSE
	entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58] The '788 Reference states: "According to this arrangement, only one plane is selected in accordance with the content of the upper-order two bits of the row address. The selected plane is activated and exhibits the memory operation but the rest of the planes which are under the non-selection state are inoperative. Therefore, the decoders and the sense amplifiers are inoperative in these inoperative planes and the memory is not refreshed. Therefore, power is consumed in only the selected plane and unnecessary power consumption in the other plane can be saved. Thus, the requirement for low power consumption can be satisfied." ['788 Reference, Col. 5:57-68] The '003 Reference states: "The flash memory control 88 also selectively enables one of two sets of bi-directional data buffers 90 and 91 which respectively couple the bank data buses 82 and 83 to the processor section data bus 63. The bank data buses 82 and 83 can be coupled to the instruction bus 61 by the flash memory control 88 selectively enabling buffers 92 and 93, respectively." ['003 Reference, Col.

CLAIM	RESPONSE
	9:21-27] The '178 Reference states: "Referring now to FIG. 2, the circuit of FIG. 1 has been modified to utilize the fact that, when RA10=1, only one half of the ARRAY BANKs 20 are being utilized and that, when RA10=0, the other half of the ARRAY BANKs 20 are being utilized. In particular, the RA 10 address is used to cause only the half of the ARRAY BANKs 20 that are being utilized to draw power from the DRAM energy source during read/write operations, while at the same time permitting the periodic performance of the refresh cycle in the usual manner on all ARRAY BANKs." ['178 Reference, Col. 3:32-42]

Appendix D2
Defendants and Counterclaimants' Invalidity Contentions
Advanced Micro Devices, Inc., et al., v. Samsung Electronics Co., Ltd., et al., Case No. 3:08-CV-0986-SI

U.S. patent No. 5,559,990 Invalidity Chart: United States Patent No. 4,759,021 ("'021 Reference")

All asserted claims are anticipated by the '021 Reference and/or are rendered obvious by it, either alone or in combination with other prior art described below and/or listed in Section I of Defendants' and Counterclaimants' Preliminary Invalidity Contentions and/or through modifications described below. Nothing in this invalidity chart should be construed as signifying or suggesting Defendants and Counterclaimants' adoption of or acquiescence in any claim scope and/or claim construction positions taken by Plaintiffs and Counterdefendants in this litigation.

CLAIM	RESPONSE
20. An integrated memory comprising:	Although a preamble is normally not limiting, should this preamble be limiting, this element is met by U.S. Patent No. 4,759,021 ("the '021 Reference"). Specifically, the '021 Reference states: "The test pattern generator in the embodiment comprises four low-speed large-capacity memories 11, 12, 13, 14 and a high-speed small-capacity memory 50 …." ['021 Reference, Col. 2:15-18]
an array of memory locations, the array comprising a plurality of subarrays, each subarray comprising a predetermined number of groups of columns of the memory locations such that for any given column position in a group, the memory locations in any given row in the columns at said given position in the groups of the subarray have consecutive addresses;	This element is met in the '021 Reference. Specifically, the '021 Reference states that: "That is, since the interleave operation is performed in the case of low-speed memories, test patterns corresponding to each address 0, 1, 2, 3 are stored in sequence of the low-speed large-capacity memoriese 11, 12, 13 14." ['021 Reference, Col. 2:47-50]
one X-decoder for each subarray;	This element is met the '021 Reference. Specifically, the '021 Reference states that: "That is, since the interleave operation is performed in the case of low-speed memories, test patterns corresponding to each address 0, 1, 2, 3 are

CLAIM	RESPONSE
	stored in sequence of the low-speed large-capacity memoriese 11, 12, 13 14." ['021 Reference, Col. 2:47-50] Each low-speed memory block includes an x-decoder.
one X-register for each X-decoder;	This element is met the '021 Reference. Specifically, the '021 Reference states that: "Since the low-speed large-capacity memories 11, 12, 13, 14 performing the 4-way interleave operation are shifted in access timing usually by one cycle from each other, the memories 11-14 are provided respectively with registers 23-26 each for holding an address." ['021 Reference, Col. 4:5-9]
one Y-decoder for each subarray;	This element is met by the '021 Reference. Specifically, the '021 Reference states that: "That is, since the interleave operation is performed in the case of low-speed memories, test patterns corresponding to each address 0, 1, 2, 3 are stored in sequence of the low-speed large-capacity memories 11, 12, 13 14." ['021 Reference, Col. 2:47-50] Each low-speed memory block includes a y-decoder.
one Y-register for each Y-decoder;	This element is met by the '021 Reference alone or in combination with U.S. Patent No. 4,849,937 ("the '937 Reference"). Specifically, the '021 Reference states that: "Select signal 129 to the selector 61 is output from the counter 21 delayed by a delay register 27. Count enable control signal 131 to the counter 21 controls the interleave operation of the low-speed memories for the wait state (WAIT cycle)." ['021 Reference, Col. 4:15-19]

CLAIM	RESPONSE
	To the extent AMD reads this limitation on the Samsung devices, the '021 Reference meets this limitation. The '937 Reference states that: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e., twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and Y add address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e. twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42]
one Y-select circuit for each subarray, the Y-select circuit being responsive to the Y-decoder of the subarray to select all the columns that occupy a selected position in the groups of the subarray;	This element is met by the '021 Reference in combination with the '937 Reference or the EP 0 087 754 B1 ("the '754 Reference"). The '937 Reference states: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e. twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to

CLAIM	RESPONSE
	the transfer gate 85. Ina similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e. twice that of the basic clock pulses $Ø_{S)}$ Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42] "Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to a transfer gate 85.... In a similar manner, the transfer gate 95 transfers data read from the second memory cell array 94 to the sense amplifier 96 through an I/O line 103, while transferring data from the write circuit 98 received through the I/O line 103 to the second memory cell array 94." ['937 Reference, Col. 4:33-52] The '754 Reference states: "Meanwhile, since the randomly selected bit signal RSBS of logic level '0' is supplied to the driver circuit 24, the MOS transistors TR65 and TR68 are turned OFF and the MOS transistors TR66 and 67 are turned ON. Under this condition, the MOS transistors Tr61 and TR63 are turned ON in responses to the timing signal TS3 from the control signal generator 28. The lower level signal [ØS bar] shown in Fig. 7D is supplied to the control lines Cl-1 and Cl-3 of the sense amplifier circuits 18-1 and 18-3, respectively. As a result, the sense amplifier circuits 18-1 and 18-3 are activated to discharge one of each pair of data lines of memories 12-1 and 12-3 connected to the sense amplifiers 18-1 and 18-3, respectively, thereby causing a discharging current to flow as shown in

CLAIM	RESPONSE
	Fig. 7E." ['754 Reference, Page 5:33-40]
a plurality of sense amplifier circuits for each subarray, each sense amplifier circuit for amplifying signals from a column selected by the Y-select circuit of the subarray;	This element is met by the '021 Reference alone or in combination with the '754 Reference. Specifically, the '021 Reference states that: "That is, since the interleave operation is performed in the case of low-speed memories, test patterns corresponding to each address 0, 1, 2, 3 are stored in sequence of the low-speed large-capacity memoriese 11, 12, 13 14." ['021 Reference, Col. 2:47-50] Each low-speed memory block includes a sense amplifier circuit. The '754 Reference states: "The present invention involves a semiconductor dynamic memory device comprising ... a plurality of sense amplifying means responsive to a control signal input thereto, for selectively activating one sense amplifying means to sense and amplify data on said selected data lines of one of said two column-selected memory blocks, and for selectively activating at least one other sense amplifying means to refresh data of said each memory cell along said selected word lines, ..." ['754 Reference, Page 3:65-4:15]
a memory output; and	This element is met by the '021 Reference. Specifically, the '021 Reference states: "In FIG. 1, ... numerals 150, 161 indicate output data from the high-speed samll-capacity memory 50 and the selector 61 respectivelyy, and number 162 indicates output data from the selector 62." ['021 Reference, Col. 3:43-68]

CLAIM	RESPONSE
a control circuit for selecting one of the sense amplifier circuits to provide data to the memory output;	This limitation is met by the '021 Reference. Specifically, the '021 Reference states that: "Select signal 129 to the selector 61 is output from the counter 21 delayed by a delay register 27. Count enable control signal 131 to the counter 21 controls the interleave operation of the low-speed memories for the wait state (WAIT cycle)." ['021 Reference, Col. 4:15-19]
wherein in a burst mode read operation, at least one X-register provides to its respective X-decoder signals identifying a row in one of the subarrays, and at least one Y-register provides to its respective Y-decoder signals identifying a position of columns in the groups of one of the subarrays.	This limitation is met by the '021 Reference in combination with the '754 Reference or the '937 Reference or U.S. Patent No. 4,875,196 ("the '196 Reference") or U.S. Patent No. 5,036,494 ("the '494 Reference"). The '754 Reference states: "Furthermore, this dynamic memory device has row and column address buffers 20 and 22 for respectively storing row and column address data supplied from an address signal generator (not shown); …." [Page 4:44-51] "Output data from the row address buffer 20 excluding the most significant bit MSB is supplied to the row decoders 16-1 to 16-4, and the output data from the column address buffer 22 is supplied to the columns decoders 14-1 and 14-2 through the gate circuits 30 and 32, respectively." ['754 Reference, Page 4:52-54] The '937 patent states that: "The address counter 81 receives the signals $Ø_{EV}$ to supply even X

CLAIM	RESPONSE
	address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e., twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e., twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42] The '196 Reference states that: "In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit lines in the other array are being precharged. Thus, as data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit lines in that array will already have been initialied." '196 Reference, Col. 2:60-67 "In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and settling transient signals) in preparation for the next access form such other array. Therefore, precharging times for one array overlap the time for performing read or write operation in the other array, and therefore do not limit operating speed." ['196 Reference, Col. 3:41-47] The '494 Reference states:

CLAIM	RESPONSE
	In the example shown in FIG. 1 each memory block 14 and 15 has sixty four columns 35, each column being coupled to equate and precharge circuitry 36. The columns are arranged in groups, each group having eight pairs of bit lines so that when any column is addressed eight pairs of bit lines (one in each group) are simultaneously accessed, permitting transfer of eight bits or one word at a time. The bit lines are each connected to column multiplexing circuitry 37 for each column and coupled to sense amplifier and write circuitry 38 for each column. Each sense amplifier and write circuit is connected through a bus driver circuit 39 to the data output 17. Each memory block 14 and 15 has 70 rows each having a word line 25. The word lines are connected to a row decoder 40. The row decoder is coupled to memory block 14 through a latch and word line driver 41 and to the memory block 15 through a latch and word line driver 42. The column multiplex circuitry 37 is controlled by a column counter 44. The row decoder 40 is controlled by a row counter 45. The latch and word line drivers 41 and 42 are controlled by pulse generators 46 and 47 respectively. Each of the drivers 41 and 42 is connected by two separate control lines 48 to the respective one of the pulse generators 46 and 47 so that each driver can be operated either to latch the output of the row decoder 40 or to drive all the word lines low. The selection of memory locations forming each cyclic pattern of addressing is controlled by the control until 13. The row counter 45 and columns counter 44 are connected so that unless instructed by the control 13 to do otherwise they count through successive addresses along each row and then row by row." ['494 Reference, Col. 7:44-8:27]
22. The memory of claim 20 wherein in the burst mode read operation while data from the sense amplifier	This element is met by the '021 Reference in combination with the '196

CLAIM	RESPONSE
circuits of one of the subarrays are provided to the memory output, the sense amplifier circuits of another one of the subarrays develop output signals corresponding to data in said other one of the subarrays.	Reference or the '494 Reference. The '196 Reference states that: "In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit lines in the other array are being precharged. Thus, as data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit lines in that array will already have been initialied." ['196 Reference, Col. 2:60-67] "In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and settling transient signals) in preparation for the next access form such other array. Therefore, precharging times for one array overlap the time for performing read or write operation in the other array, and therefore do not limit operating speed." ['196 Reference, Col. 3:41-51] The '494 Reference states: "The selection of memory locations forming each cyclic pattern of addressing is controlled by the control unit 13. The row counter 45 and column counter 44 are connected so that unless instructed by the control 13 to do otherwise they count through successive addresses along each row and then row by row." ['494 Reference, Col. 8:22-27] "Consequently after reaching address 0 the column and row counters cycle sequentially along each row for the two memory blocks in turn (starting at column zero of row 0 in array 0) using all memory locations in each row and then moving to the next row and repeating the operation."

CLAIM	RESPONSE
	['494 Reference, Col. 11:26-31] "addressing sequentially more than one memory location in said first memory block and effecting a data transfer for each memory location addressed, and at the same time effecting an equate operation on bit lines in said second memory block; and after addressing memory locations in said first memory block, switching said addressing and equate operation so as to address sequentially more than one memory location in said second memory block and effecting a data transfer for each memory location addressed and at the same time equating bit lines in said first memory block." ['494 Reference, Col. 13:36-48]
23. The memory of claim 20 wherein in the burst mode read operation, the control circuit enables the sense amplifier circuit selected to provide data to the memory output and at the same time disables one or more sense amplifier circuits not selected to provide data to the memory output.	This limitation is met by the '021 Reference in combination with the '754 Reference or U.S. Patent No. 4,957,788 ("the '788 Reference") or the '937 Reference or U.S. Patent No. 5,263,003 or U.S. Patent No. 5,251,178 ("the '178 Reference"). The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier

CLAIM	RESPONSE
	circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58] "A semiconductor dynamic memory device comprising: ... a plurality of sense amplifying means (18-1 to 18-4; SA1 to SA8) responsive to a control signal input thereto, for selectively activating one sense amplifying means to sense and amplify data on said selected data lines of one of said two column-selected memory blocks, and for selectively activating at least one other sense amplifying means to refresh data to said each memory cell along said selected word lines; ...." ['754 Reference, Page 6:53-7:5] The '788 Reference states: "According to this arrangement, only one plane is selected in accordance with the content of the upper-order two bits of the row address. The selected plane is activated and exhibits the memory operation but the rest of the planes which are under the non-selection state are inoperative. Therefore, the decoders and the sense amplifiers are inoperative in these inoperative planes and the memory is not refreshed. Therefore, power is consumed in only the selected plane and unnecessary power consumption in the other plane can be saved. Thus, the requirement for low power consumption can be satisfied." ['788 Reference, Col. 5:57-68] The '937 Reference states: "The sense amplifier 86 is controlled by the signals SE_{EV} to amplify the read data thereby to supply the same to the data latch 87, which in turn temporarily stores the outputs from the sense amplifier 86. When the signals SE_{EV} are at low levels, the data latch 87 is electrically cut off from

CLAIM	RESPONSE
	the sense amplifier 86. Data from the data latch 87 are transferred to the output latch 89 when the signals OE_{EV} are at high levels. In a similar manner, the sense amplifier 96 is controlled by the signals SE_{OD} to amplify the read data thereby to supply the same to the data latch 97, which in turn temporarily stores the outputs from the sense amplifier 96. When the signals SE_{OD} are at low levels, the data latch 97 is electrically cut off from the sense amplifier 96." ['937 Reference, Col. 4:52-66] The '003 Reference states: "The flash memory control 88 also selectively enables one of two sets of bi-directional data buffers 90 and 91 which respectively couple the bank data buses 82 and 83 to the processor section data bus 63. The bank data buses 82 and 83 can be coupled to the instruction bus 61 by the flash memory control 88 selectively enabling buffers 92 and 93, respectively." ['003 Reference, Col. 9:21-27] The '178 Reference states: "Referring now to FIG. 2, the circuit of FIG. 1 has been modified to utilize the fact that, when RA10=1, only one half of the ARRAY BANKs 20 are being utilized and that, when RA10=0, the other half of the ARRAY BANKs 20 are being utilized. In particular, the RA 10 address is used to cause only the half of the ARRAY BANKs 20 that are being utilized to draw power from the DRAM energy source during read/write operations, while at the same time permitting the periodic performance of the refresh cycle in the usual manner on all ARRAY BANKs." ['178 Reference, Col. 3:32-42]