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Grooved Gate MOSFET

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Grooved Gate type MOS FET's which realize a short channel device with high punch-through breakdown voltage and little threshold voltage (V_T) fluctuation, are fabricated by using a promising photoresist technique.

A proposed, self-aligned gate MOS FET structure (Grooved Gate MOS FET) is based on two-dimensional analyses of short channel devices. A characteristic feature of the device is negative source and drain junction depth.

The fabricated 21 stage ring oscillator displays a high circuit performance for delay and power product of 0.12 pJ.

§1. Introduction

Many attempts[1,2] have been made to realize high speed and high integration MOSLSI's. These attempts focused attention mainly on short channel MOSFET's.

However, these attempts suffer serious limitations especially in (a) poor punch-through breakdown characteristics between source and drain and (b) a large threshold voltage fluctuation caused by channel length modulation effects. The former limitation determines the maximum supply voltage of MOSFET's. The latter reduces the noise margin of the circuits resulting in low reproducibility of the LSI.

Reports have been published on MOSFET's with shallow source and drain junctions (x_j) in addition to short channel devices by the authors and their coworkers[3] and others.[4]

Two-dimensional numerical analyses of MOSFET's are extended quantitatively, and a new MOSFET structure designated Grooved Gate (or buried gate) MOSFET is proposed. This structure enables production of not only a shallow x_j but also a negative x_j which has not been obtained using a conventional silicon gate method.

A similar structure employing an aluminum gate was reported in previous papers.[5,6] However, a negative x_j was not realized and the self-aligned gate method was not effectively utilized.

A new photoresist technique (buried gate technique) which realizes a self-aligned Grooved Gate is presented. The characteristics of fabricated Grooved Gate MOSFET's and 21 stage ring oscillator are also presented.

§2. Two-Dimensional Numerical Analyses of the Device

Figure 1 shows a perspective view of structure of the Grooved Gate MOSFET which is characterized by a negative x_j. The junction depth from the silicon surface under the gate oxide is defined as x_j (Fig. 2). This structure can be approximated as shown in Fig. 2 for two-dimensional MOSFET analyses. The fundamental equations used in the program are as

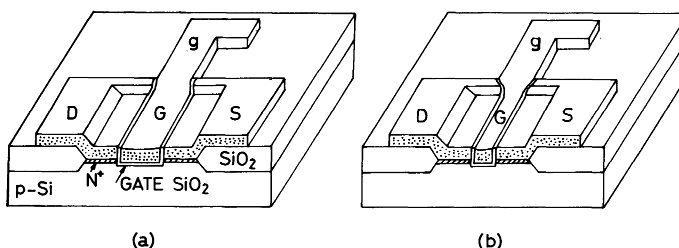

Fig. 1. Perspective view of a Grooved Gate MOS FET's. (a) fabricated structure, (b) proposed structure for short channel ($L<2$ μm). D; Drain, S; Source, G-g; Gate.

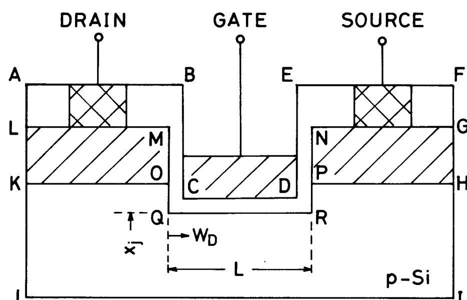

Fig. 2. Approximated cross sectional view of a Grooved Gate MOSFET for two-dimensional analyses.

follows.

ABCDEFGNRQMLA (SiO_2);

$$\nabla^2\phi=0 \tag{1}$$

KOQRPHIJK (Si);

$$\nabla^2\phi=[n-p+N_A(x, y)]/\varepsilon_s \tag{2}$$

$$\nabla(e^{\beta\phi}\nabla n\, e^{-\beta\phi})=0 \tag{3}$$

$$p=N_A\, e^{-\beta\phi}/n_i \tag{4}$$

where $\beta=q/kT$, ϕ is electrical potential, n and p are electron and hole densities respectively, N_A is the impurity concentration in the bulk silicon, k is the Boltzmann constant, T is the absolute temperature and q is the unit charge of the electron. Equations (1) and (2) are expressions of Poisson equations and eq. (3) expresses the current continuity equation. Boundary conditions are determined as follows.

BCDEB,	$\phi=V_G$,	(5)
NGHPN,	$\phi=V_D$,	(6)
LMOKL,	$\phi=V_S$,	(7)
KJ, HI,	$\nabla\phi=0$,	(8)
IJ,	$\phi=0$.	(9)

where V_G, V_D and V_S are gate voltage, drain voltage and source voltage respectively. Calculation was carried out by using a relaxation method of the finite differential equations transformed from partial differential eqs. (1), (2) and (3). For calculating punch-through breakdown voltage, eq. (3) can be eliminated because the drain current should be zero before breakdown. The threshold voltage (V_T) is defined as the gate voltage when the drain current of the unit MOSFET ($W/L=1$) is 0.1 μA. This definition is a reasonable approximation of the physical characteristics of V_T.

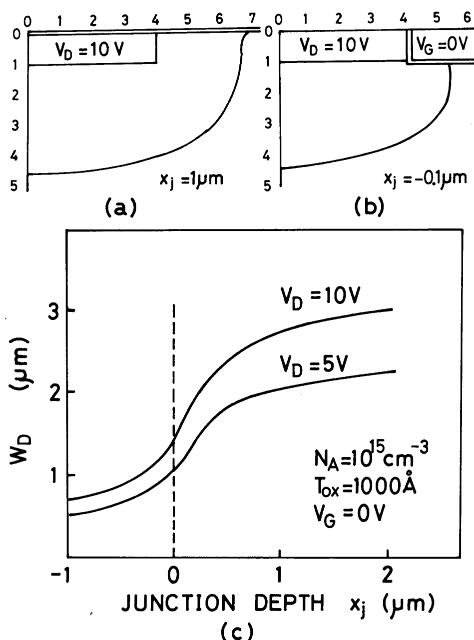

Fig. 3. Calculated drain depletion layer (a) for conventional type MOS FET, (b) for Grooved Gate MOS FET (c) W_D(drain depletion layer width in the direction to the source)$-x_j$ relationship.

The computed results for the drain depletion regions of conventional and Grooved Gate MOSFET's with biased $V_G=0$ V and $V_D=10$ V are shown in Fig. 3(a) and (b). The results mean that the punch-through voltage of a conventional structure with channel length $L=2.5$ μm is less than 10 V, whereas that of the Grooved Gate structure with $L=1.5$ μm is greater than 10 V. Also the shorter extention width of the depletion layer implies a lessening of the V_T lowering effect caused by the drain electric field.

Figure 3(c) shows the relationship between x_j and drain depletion layer width (W_D) in the direction to the source as a parameter of drain voltage. The Grooved Gate structure ($x_j\lesssim 0$) can reduce the value of W_D by half as compared with conventional MOSFET's.

The computed and experimental threshold voltage and channel length (V_T-L) relationships as a function of x_j are shown in Fig. 4.[3] As shown in the figure, a device with a shallow x_j has little change in V_T value with channel variation. Therefore, the Grooved Gate structure is expected to show a more improved V_T-L relationship, although the V_T-L relationship for negative x_j was not calculated.

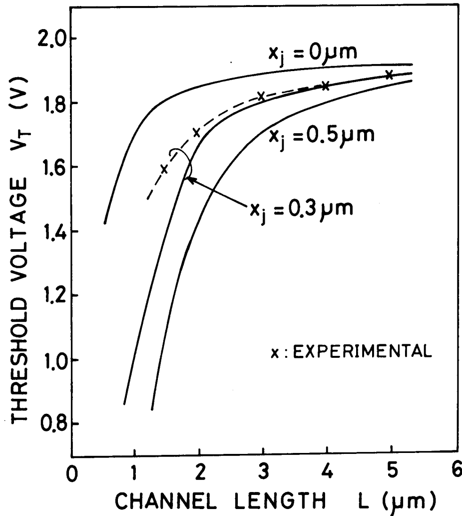

Fig. 4. Calculated and experimental V_T-L relationships. ($N_A=3.5\times10^{15}$ cm^{-3}, $T_{ox}=500$ Å, $V_D=5$ V, $V_{BB}=-5$ V).

From the computed results, it can be concluded that the proposed Grooved Gate MOS FET is an ideal device for shorter channel ($L\approx1$ μm) MOSFET's.

§3. Device Fabrication

The fabrication process flow for Grooved Gate MOSFET's is shown in Fig. 5.

After LOCOS oxidation, the 1st polycrystalline silicon (poly-Si) layer (3500 Å) is deposited and etched by Freon plasma at the gate region. In this case, the silicon substrate is also etched to about 0.2–0.3 μm in depth. Gate oxidation

Si_3N_4 DEPO.
Si_3N_4 ETCHING*
LOCOS OXIDATION.
1st POLY-Si DEPO.
GATE GROOVING*
GATE OXIDATION.
2nd POLY-Si DEPO.
2nd POLY-Si ETCHING* (BURIED GATE TECH.)
1st POLY-Si ETCHING*
N^+ DIFFUSION.
PSG DEPO.
CONTACT ETCHING*
Al DEPO.
Al ETCHING*
HYDROGEN ANNEALING.

Fig. 5. Process flow for fabrication of a Grooved Gate MOSFET (IC), *: photoresist operation.

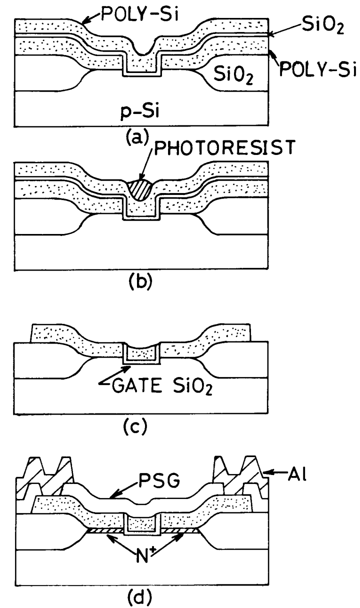

Fig. 6. Cross sectional view of each process steps.

(500 Å) is followed by the 2nd poly-Si (3500 Å) deposition process [Fig. 6(a)].

A new photoresist technique (buried gate technique) is used to bury the poly-Si gate in the grooved region without using a photomask. This technique utilizes the photoresist characteristic that photoresist is formed at the grooved region about twice as thick as that of other parts. When a thin photoresist layer is removed by oxygen plasma, the photoresist is left only in the grooved gate region [Fig. 6(b)].

Then the 2nd poly-Si is etched by masking the buried photoresist and the 1st poly-Si layer is etched again to constitute the source and drain regions [Fig. 6(c)]. The other steps are the same as those of conventional silicon-gate technology. The final cross sectional view of Grooved Gate MOSFET is shown in Fig. 6(d).

§4. Results and Discussions

Figure 7 shows a microphotograph of two Grooved Gate MOSFET's [a bar gate type ($L=2$ μm, $W=260$ μm) and a snake type ($L=2$ μm, $W=1830$ μm, gate pitch $=5$ μm)] fabricated on a p-type, (100), 4 Ω-cm silicon substrate. The pitch of 5 μm is very difficult to realize in aluminum gate structures.[5,6]

The buried gate technique can be applied to devices with channel lengths less than 8 μm, and the gate above 8 μm is missing locally.

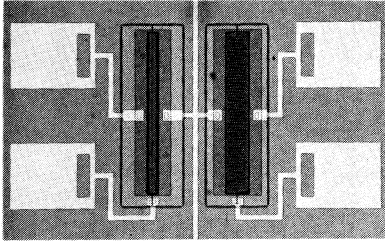

Fig. 7. Microphotograph of two Gıooved Gate MOS FET's, left; a bar type gate ($L=2\ \mu m$, $W=260\ \mu m$), right; a snake type gate ($L=2\ \mu m$, $W=1830\ \mu m$, gate pitch$=5\ \mu m$).

A positive type photoresist AZ1350 was used in all photoresist operations.

The Grooved Gate MOSFET's with 1 μm channels did not operate due to the disappearence of the gate poly-Si on the field oxide during etching process (g in Fig. 1). The photoresist covering the gate on the field oxide plays the important role of an etching mask in both the 1st and 2nd poly-Si plasma etchings. Therefore poly-Si must be spread to at least 2 μm within the drain and source region as shown in Fig. 1(b) for full operation of short channel (less than 2 μm) Grooved Gate MOSFET's.

The 2 μm channel devices displayed good punch-through breakdown voltage over 10 V as shown in Fig. 8. In the figure, drain current-voltage (I_D-V_D) characteristics for devices ($L=2$, 2.5, 3 and 3.5 μm) are shown.

Figure 9 shows the relationship of reciprocal channel conductance and channel length ($1/\beta-L_M$), where L_M is the channel length of the photomask design. The unit channel conductance β_0 of 58 μ℧/V for 500 Å gate oxide devices is obtained from the gradient of the straight

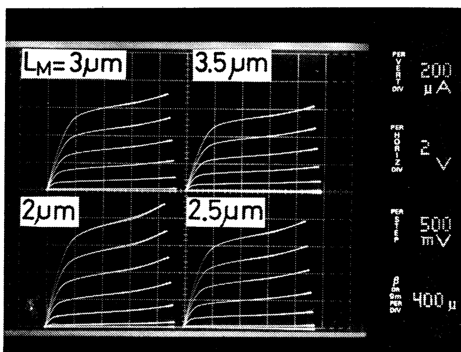

Fig. 8. Experimental I_D-V_D characteristics of the devices, $L_M=2$, 2.5, 3 and 3.5 μm, $W=13\ \mu m$, $x_j\approx 0$, $V_G=0\sim 3$ V, $V_{BB}=0$ V.

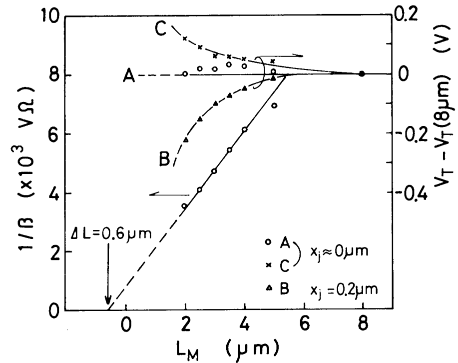

Fig. 9. $1/\beta-L_M$ and normalized V_T-L_M relationships. ($V_D=6$ V, $V_{BB}=-3$ V).

line in the figure. This value is the same as that for conventional silicon gate MOSFET's. The effective channel length L_{eff} is also obtained as follows.

$$L_{eff}=L_M+0.6\ \mu m. \tag{10}$$

In addition, the threshold voltage (V_T) obtained from the square root of the drain current and gate voltage ($\sqrt{I_D}-V_G$) characteristics did not decrease as predicted by numerical analyses of the device. The normalized V_T-L_M relationship is also depicted in Fig. 9. Curve A is for somewhat negative x_j devices and curve B is for $x_j=0.2\ \mu m$ devices. Curve B is similar to that shown in Fig. 4. The unique characteristics of curve C in Fig. 9 were obtained due to apparently to a rather high interface state density. Grooved Gate MOSFET's with large negative $x_j s$ were not intentionally fabricated, because the channel length is not defined as shown in Fig. 2.

A scanning electron micrograph of a cross section of a Grooved Gate MOSFET (device for A in Fig. 9) is shown in Fig. 10. The buried

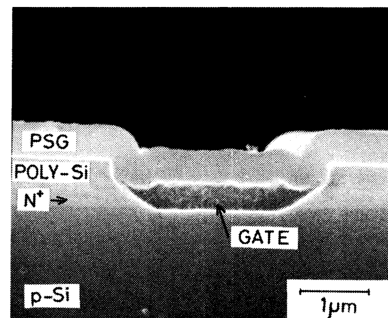

Fig. 10. Scanning electron micrograph of cross sectional view of Grooved Gate MOS FET (device for A in Fig. 9).

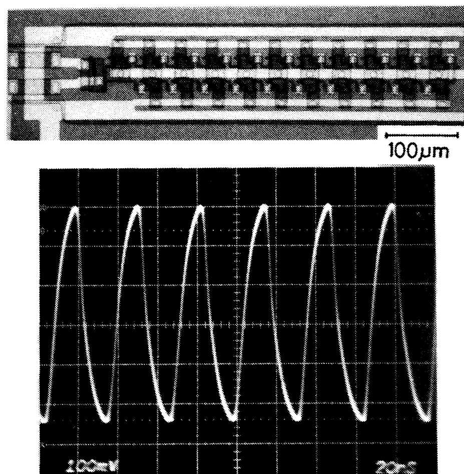

Fig. 11. A microphotograph of 21 stage ring oscillator circuit and the output waveform through an output buffer gate.

gate is clearly shown in the figure.

A 21 stage E/D MOS type ring oscillator IC, composed of 2 μm channel devices, was fabricated and measured. Figure 11 shows a microphotograph of the ring oscillator and the output waveform through an output buffer gate. The following high performance levels were obtained.

Delay time per stage $t_{pd}=0.77$ ns/stage,

Power dissipation per stage

$P_d=0.16$ mW/stage,

Delay and power product

$t_{pd}\cdot P_d=0.12$ pJ.

The Groove Gate MOSFET has characteristic metrits described above, although it has drawbacks such as (1) week breakdown voltage of poly-Si-SiO_2-poly-Si structure (breakdown field $\approx 5\times 10^6$ V/cm) due to asperities of poly-Si surface,[7] and (2) increase of one photomask and process steps comparing with a conventional silicon gate MOSFET.

§5. Summary

A new MOS structure designated Grooved Gate MOSFET was proposed on the basis of two-dimensional analyses of short channel devices. A new promising photoresist technique (buried gate technique) was developed to fabricate self-aligned Grooved Gate MOSFET's.

The fabricated devices show high punch-through characteristics and little threshold voltage fluctuation due to channel length variation as predicted.

A 21 stage ring oscillator composed of E/D Grooved Gate MOSFET's was also constructed. It displayed a high circuit performance for delay and power products of 0.12 pJ.

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