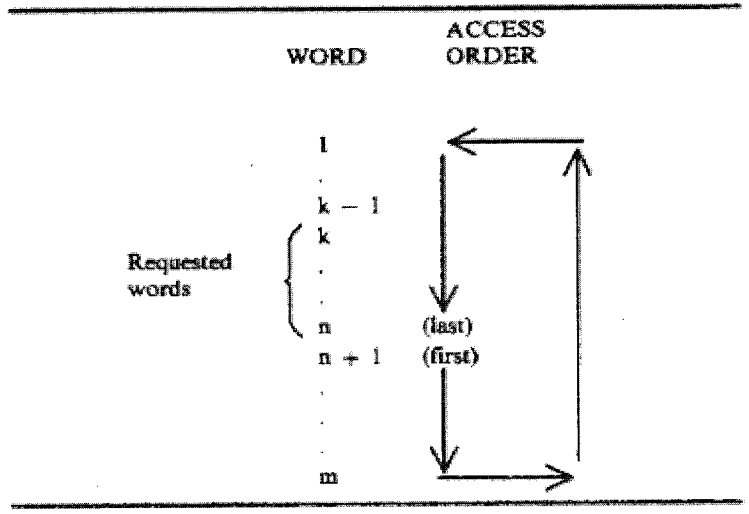
EXHIBIT 1

D5 Pages26-54

CLAIM	RESPONSE
	TABLE II  See also, '631 Reference, Abstract, Table I, Fig. 3. the '297 Reference states that: "That is, in a serial access mode, n rows such as four rows adjacent to a voluntary proposition of the logic bit map plane, are accessed in the sequence of the adjacent row data by the arranging means." ['297 Reference, 2:47-51] "Another object of the present invention is to provide a boundary-free semiconductor memory device in which a voluntary adjacent n-row bit

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	group can be accessed in a serial access mode." ['297 Reference, 1:67-2:2] See also, '297 Reference, 13:1-47 and FIGs. 6, 7, 21 and 22. the '1182 Reference states that: "When the reading has finished to the column address 1023 in response to the above-mentioned address 4, the carrier signals ca for the column-type counter circuit (Y) are produced similarly to what is explained above, and they themselves will be the address 0 and the row-based address will be changed to 6." ['1182 Reference, Page 5, second column] "(5) There is an effect that is obtained whereby high-speed continuous reading is carried out from a random address by incorporating address signals that have been supplied from the external terminal as initial values." ['1182 Reference, Page 6, second column] "(6) Based on (1) to (5) above, there is an effect that is obtained whereby there can be provided a semiconductor memory device that is applicable to a semiconductor memory where picture element data that is large in quantity is repeated to depict high-precision picture images using a display device, such as a CRT, and, therefore, high-speed continuous reading would be presumed to be necessary." ['1182 Reference, Page 6, second column] *See also* Figure 3 and accompanying description on Page 4.
wherein said memory further comprises a control	This element is met in the '994 Reference alone or in combination with

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circuit for selectively enabling said sense amplifier circuits so that said control circuit enables a sense amplifier circuit whose output signals are being transferred to the output of said memory but said control circuit does not enable all said sense amplifier circuits at the same time.	any of the '788 Reference or the '937 Reference or the '003 Reference or the '178 Reference or the '754 Reference. Specifically, the '994 Reference states that: "The invention is not limited to a 2-block memory cell array. In FIG. 5 there is described a cell array that has N number of blocks in general. Here a column address with block 1 has been selected. At this time, the data in the selected row i in block 1 is latched and the data in the selected row i in 1+1=2 is latched at the same time. In this case, the state may be active or disabled for the cell arrays for block 0 and 3 - N - 1; however, the disabled state will tend to make for a better reduction in the amount of energy consumed. After that, access will continue to be executed in the sequential serial direction; however, the row in the i line in the of the instantaneous block N-1 and the row in the i+1 line of the block 0 will be selected and that data will be latched." ['994 Reference, Page 4, Column 2] The '788 Reference states: "According to this arrangement, only one plane is selected in accordance with the content of the upper-order two bits of the row address. The selected plane is activated and exhibits the memory operation but the rest of the planes which are under the non-selection state are inoperative. Therefore, the decoders and the sense amplifiers are inoperative in these inoperative planes and the memory is not refreshed. Therefore, power is consumed in only the selected plane and unnecessary power consumption in the other plane can be saved. Thus, the requirement for low power consumption can be satisfied." ['788 Reference, Col. 5:57-68]

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	The '937 Reference states: "The sense amplifier 86 is controlled by the signals SE_{EV} to simplify the read data thereby to supply the same to the data latch 87, which in turn temporarily stores the outputs from the sense amplifiers 86. When the signals SE_{EV} are at low levels, the data latch 87 is electrically cut off from the sense amplifier 86. Data from the data latch 87 are transferred to the output latch 89 when the signals OE_{EV} are at high levels. In a similar manner, the sense amplifier 96 is controlled by the signals SE_{OD} to amplify the read data thereby to supply the same to the data latch 97, which in turn temporarily stores the outputs from the sense amplifier 96. When the signals SE_{OD} are at low levels, the data latch 97 is electrically cut off from the sense amplifier 96." ['937 Reference, Col. 4:52-66] The '003 Reference states: "The flash memory control 88 also selectively enables one of two sets of bi-directional data buffers 90 and 91 which respectively couple the bank data buses 82 and 83 to the processor section data bus 63. The bank data buses 82 and 83 can be coupled to the instruction bus 61 by the flash memory control 88 selectively enabling buffers 92 and 93, respectively." ['003 Reference, Col. 9:21-27] The '178 Reference states: "Referring now to FIG. 2, the circuit of FIG. 1 has been modified to utilize the fact that, when RA10=1, only one half of the ARRAY BANKs 20 are being utilized and that, when RA10=0, the other half of the ARRAY BANKs 20 are being utilized. In particular, the RA 10 address

CLAIM	RESPONSE
	is used to cause only the half of the ARRAY BANKs 20 that are being utilized to draw power from the DRAM energy source during read/write operations, while at the same time permitting the periodic performance of the refresh cycle in the usual manner on all ARRAY BANKs." ['178 Reference, Col. 3:32-42] The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58]
9. The memory of claim 8 wherein, during said operation, said control circuit enables at the same time only:	
(1) the sense amplifier circuit whose output signals are being transferred to said output of said memory, and	This limitation is met by the '994 Reference in combination with the '754 Reference. The '754 Reference states:

CLAIM	RESPONSE
	"In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58] "A semiconductor dynamic memory device comprising: ... a plurality of sense amplifying means (18-1 to 18-4; SA1 to SA8) responsive to a control signal input thereto, for selectively activating one sense amplifying means to sense and amplify data on said selected data lines of one of said two column-selected memory blocks, and for selectively activating at least one other sense amplifying means to refresh data to said each memory cell along said selected word lines; ...." ['754 Reference, Page 6:53-7:5]
(2) a predetermined number of other sense amplifier circuits whose output signals will be transferred next to said output of said memory if said operation continues sufficiently long.	This limitation is met by the '994 Reference in combination with the '754 Reference. The '754 Reference states: "In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense

CLAIM	RESPONSE
	amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20] "As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58] "A semiconductor dynamic memory device comprising: ... a plurality of sense amplifying means (18-1 to 18-4; SA1 to SA8) responsive to a control signal input thereto, for selectively activating one sense amplifying means to sense and amplify data on said selected data lines of one of said two column-selected memory blocks, and for selectively activating at least one other sense amplifying means to refresh data to said each memory cell along said selected word lines; ...." ['754 Reference, Page 6:53-7:5]
10. The memory of claim 7 wherein:	
said set of locations comprises k subsets S-1, . . . , S-k wherein k is greater than or equal to two, such that, for a positive integer m and for any subset S-i, the contents of m consecutively addressed locations from said subset S-i can be transferred simultaneously to said plurality of sense amplifier circuits; and	This limitation is met by the '994 Reference. Specifically, the '994 Reference states: "Now the address will have been input and the row for the i line and the column for the j row will have been selected (FIG. 1(a)). At that time, the information in the cells that have been connected to the row of the i line in the memory arrays on the left and the right will be read at the same time in the bit linear direction and will undergo sense amplification, and it wll

CLAIM	RESPONSE
	be stored in the latch circuit for the sense amplifiers/latches 7,8. In addition, assuming that the row of the i' line and the column in the j' row (that belong to the block 14 that is on the right side) have been selected, on the right side the information in the cells that have been connected to the row on the i' line will be read and it will be in the sense amplifier/latch 8'." ['994 Reference, Page 3, Columns 1 and 2]
in said operation, time tARA does not exceed m * (k-1) * (tOE), wherein: tARA is measured from the time that an address of the first location to be read out in said operation is made available to said memory to the time when said plurality of sense amplifier circuits develops an output signal indicative of the contents of said first location; and tOE is the time to transfer the contents of any one of said locations from said plurality of sense amplifier circuits to said output.	A person of skill in the art would know that this timing relationship would be used when designing the memory disclosed in claim 1.
11. The memory of claim 8 wherein, in said operation, each location to be read out except the first location to be read out is read out to said output in a shorter time than the first location to be read out.	This element is met for the '994 Reference alone or in combination with the '587 Reference or the '003 Reference or the '199 Reference. The '994 Reference states: "For that reason, even if the address moves serially to the next row and changes, the data itself will be read at high speed t_0. As is evident from the explanation above, as long as serial access continues, the internal data can continue to be read at high speed." ['994 Reference, Page 4,

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	Column 1] "In the specifications, the address access time t_1 is estimated at 150 ns, and t_0 is estimated at the level of 30 ns for simple determination at the number of steps of the gates. In a hypothesis of the worst-case scenario for the current jump command +1 instruction, the jump command would be 3 bytes for the operand +2 data, 1 instruction would be 1 byte. Therefore, the average access time is {150 ns x 1 + 30 ns x 3}/4 = 60 ns. In contrast, the access time is 150 ns when the invention is not used." ['994 Reference, Page 4, Column 2] The '587 Reference states: "The reduction in the memory access cycle time from a convention memory access operation, generally represented by the first prefetch with a three clock cycle span between event t1 and t2, is clearly evident when the times are compared to those of the consecutive prefetch operation extending for two clock cycles between corresponding time intervals t3 and t4. Time t2 and t4 identify the first clock interval suitable to initiate succeeding memory access operations." ['587 Reference, Col. 5:63-6:3] The '003 Reference states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address

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	in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer. Typically, the access addresses of these 'extra' storage cells differ from the original access address by only one or two bits. However, subsequent accesses to these cells can be accomplished by simply executing additional access cycles without changing the access address. In the art, such memories are referred to as 'nibble mode'. In some other integrated circuit memories, a portion of the original address can be 'assumed' for one (or more) subsequent accesses, so that only the least significant portion of the address needs to be decoded, etc. Thus, once the original access had been completed, subsequent accesses to 'related' storage cells will be significantly quicker." ['199 Reference, Col. 1:13-28]

CLAIM	RESPONSE
12. The memory of claim 8 wherein the sequence of locations L1, . . . , Ln is a sequence of increasing order of addresses.	This element is met in the '994 Reference. Specifically, the '994 Reference states that: "The memory cell has been arranged so that the upper left corner 4 will be the 0 address, the upper right corner 5 will be 2m-1, and the upper left 6 will be 2m address." ['994 Reference, Page 3, first column]
13. The memory of claim 7 wherein in said operation any number of said locations addressed consecutively with wrap around can be read out to said output so that:	This element is met by the '994 Reference alone or in combination with the '885 Reference or the '631 Reference. Specifically, the '994 Reference states: "For that reason, even if the address moves serially to the next row and changes, the data itself will be read at high speed t_0. As is evident from the explanation above, as long as serial access continues, the internal data can continue to be read at high speed." ['994 Reference, Page 4, Column 1] "In the specifications, the address access time t_1 is estimated at 150 ns, and t_0 is estimated at the level of 30 ns for simple determination at the number of steps of the gates. In a hypothesis of the worst-case scenario for the current jump command +1 instruction, the jump command would be 3 bytes for the operand +2 data, 1 instruction would be 1 byte. Therefore, the average access time is {150 ns x 1 + 30 ns x 3}/4 = 60 ns. In contrast, the access time is 150 ns when the invention is not used." ['994 Reference, Page 4, Column 2] The '885 Reference states:

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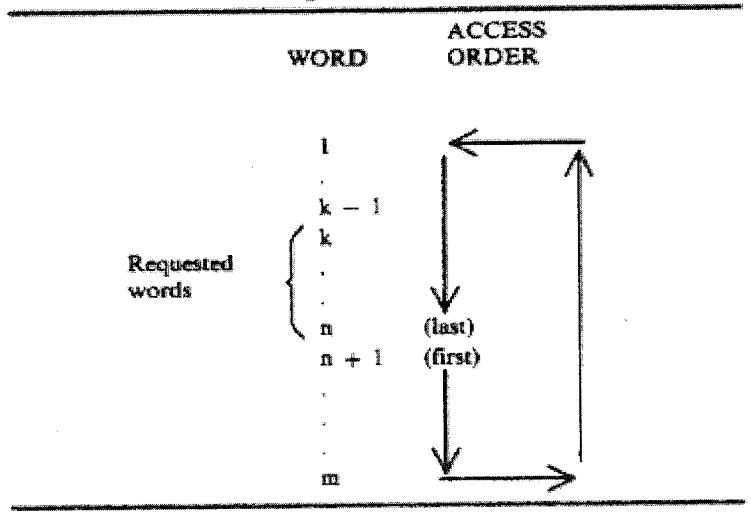
	"After the last memory address is reached, the access automatically rolls over to the first address." ['885 Reference, page 1; Col. 3:1-3] "A method as in claim 5 wherein the sequence of incremented addresses wraps around when the address of the Nth register is reached such that all N registers in the array are read." ['885 Reference, Col. 7:45-48] The '631 Reference states that: "The above-described method is accomplished by utilizing two pieces of information, which are placed on the bus (23) by the GDP: the data word's offset and the number of words requested. The data word's offset in the cache line is derived from adress bits 2 and 3 (00=word 1, 01=word 2, 10=word 3, and 11=word 4). The number of words being requested is obtained from the size bits 0 and 1 (00=1word, 01=2 words, 10=3 words, and 11=4words). Using these two pieces of information, the following algorithm is executed: FIRST WORD ACCESSED = PROCESSOR WORD ADDRESS + SIZE +1 The 1 is added to the size in order to yield the correct offset. For example, if the GDP requests two words at offset 01 in a four-word line, it is convereted to a wraparound request of four words to memory starting at word four [offset (01) + word count (01) + 1 = 11]." ['631 Reference, Col. 3:46-65]

CLAIM	RESPONSE
	See, '631 Reference, Table II: **TABLE II**  See also, '631 Reference, Abstract, Table I, Fig. 3.
the first location to be read out in said operation is read out to said output after time tARA+tOE wherein: tARA is measured from the time that an address of said first location is made available to said memory to the time when said plurality of sense amplifier circuits	This element is met by the '994 Reference alone or in combination with any of the '587 Reference or the '003 Reference or the '199 Reference. Specifically, the '994 Reference states: "For that reason, even if the address moves serially to the next row and changes, the data itself will be read at high speed t_0. As is evident from

CLAIM	RESPONSE
develops an output signal indicative of the contents of said first location; and tOE is the time to transfer the contents of any one of said locations from said plurality of sense amplifier circuits to said output of said memory; and	the explanation above, as long as serial access continues, the internal data can continue to be read at high speed." ['994 Reference, Page 4, Column 1] "In the specifications, the address access time t_1 is estimated at 150 ns, and t_0 is estimated at the level of 30 ns for simple determination at the number of steps of the gates. In a hypothesis of the worst-case scenario for the current jump command +1 instruction, the jump command would be 3 bytes for the operand +2 data, 1 instruction would be 1 byte. Therefore, the average access time is {150 ns x 1 + 30 ns x 3}/4 = 60 ns. In contrast, the access time is 150 ns when the invention is not used." ['994 Reference, Page 4, column 2] The '587 Reference states: "The reduction in the memory access cycle time from a convention memory access operation, generally represented by the first prefetch with a three clock cycle span between event t1 and t2, is clearly evident when the times are compared to those of the consecutive prefetch operation extending for two clock cycles between corresponding time intervals t3 and t4. Time t2 and t4 identify the first clock interval suitable to initiate succeeding memory access operations." ['587 Reference, Col. 5:63-6:3] The '003 Reference states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the

CLAIM	RESPONSE
	instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer. Typically, the access addresses of these 'extra' storage cells differ from the original access address by only one or two bits. However, subsequent accesses to these cells can be accomplished by simply executing additional access cycles without changing the access address. In the art, such memories are referred to as 'nibble mode'. In some other integrated circuit memories, a portion of the original address can be 'assumed' for one (or more) subsequent accesses, so that only the least significant portion of the address needs to be decoded, etc. Thus, once the original access had been completed, subsequent accesses to 'related' storage cells will be significantly quicker." ['199 Reference,

CLAIM	RESPONSE
	Col. 1:13-28]
every other location to be read out in said operation is read out to said output within time tOE.	This element is met by the '994 Reference alone or in combination with any of the '587 Reference or the '003 Reference or the '199 Reference. Specifically, the '994 Reference states: "For that reason, even if the address moves serially to the next row and changes, the data itself will be read at high speed t_0. As is evident from the explanation above, as long as serial access continues, the internal data can continue to be read at high speed." ['994 Reference, Page 4, column 1] "In the specifications, the address access time t_1 is estimated at 150 ns, and t_0 is estimated at the level of 30 ns for simple determination at the number of steps of the gates. In a hypothesis of the worst-case scenario for the current jump command +1 instruction, the jump command would be 3 bytes for the operand +2 data, 1 instruction would be 1 byte. Therefore, the average access time is {150 ns x 1 + 30 ns x 3}/4 = 60 ns. In contrast, the access time is 150 ns when the invention is not used." ['994 Reference, Page 4, Column 2] The '587 Reference states: "The reduction in the memory access cycle time from a convention memory access operation, generally represented by the first prefetch with a three clock cycle span between event t1 and t2, is clearly evident when the times are compared to those of the consecutive prefetch operation extending for two clock cycles between corresponding time intervals t3 and t4. Time t2 and t4 identify the first clock interval suitable to initiate

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	succeeding memory access operations." ['587 Reference, Col. 5:63-6:3] The '003 Reference states: "The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13] "In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41] The '199 Reference states: "However, in some integrated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer. Typically, the access addresses of these 'extra'

CLAIM	RESPONSE
	storage cells differ from the original access address by only one or two bits. However, subsequent accesses to these cells can be accomplished by simply executing additional access cycles without changing the access address. In the art, such memories are referred to as 'nibble mode'. In some other integrated circuit memories, a portion of the original address can be 'assumed' for one (or more) subsequent accesses, so that only the least significant portion of the address needs to be decoded, etc. Thus, once the original access had been completed, subsequent accesses to 'related' storage cells will be significantly quicker." ['199 Reference, Col. 1:13-28]
14. The memory of claim 8 wherein said memory is fabricated in an integrated circuit.	This element is met by the '994 Reference alone or in combination with any of the '754 Reference, the '199 Reference, or the '312 Reference. The '994 Reference is title "Semiconductor Memory Device." Further, it was well known in the art to fabricate memories as an integrated circuit and a person of ordinary skill would have know that the memory device shown in the '994 Reference could be fabricated in an integrated circuit. The '754 Reference states: "The present invention relates to a semiconductor dynamic memory device. Mass-production of 64K bit dynamic type random access memory devices (DRAMs) has been enabled by the recent development of semiconductor memory devices of high packing density. Furthermore, a 256K bit DRAM has been developed." ['754 Reference, Page 2:1-4] The '199 Reference states: "However, in some integrated circuit memory devices, several other

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	storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer." ['199 Reference, Col. 1:13-16] The '312 Reference states: "The individual circuit elements constructing the RAM of the present embodiment are formed on a semiconductor substrate such as a piece of single-crystalline silicon by the known technique for fabricating a CMOS (i.e., Complementary MOS) integreated circuit." ['312 Reference, Col. 2:34-38]
20. An integrated memory comprising:	Although a preamble is normally not limiting, should this preamble be limiting, this element is met by the '994 Reference. Specifically, the '994 Reference is titled "Semiconductor Memory Device."
an array of memory locations, the array comprising a plurality of subarrays, each subarray comprising a predetermined number of groups of columns of the memory locations such that for any given column position in a group, the memory locations in any given row in the columns at said given position in the groups of the subarray have consecutive addresses;	This element is met in the '994 Reference. Specifically, the '994 Reference states that: "In this embodiment, the memory comprises two memory cell arrays that comprise an n numbr of row lines and an m number of (or m pairs) of bit lines. In FIG. 1 (a) they are shown by the memory cell arrays 1_1, 1_2 and in FIG. 1 (b) they are shown by the memory cell array 1_3, 1_4. The memory cell has been arranged so that the upper left corner 4 will be the 0 address, the upper right corner 5 will be 2m-1, and the upper left 6 will be 2m address." ['994 Reference, Page 3, first column]
one X-decoder for each subarray;	This element is met in the '994 Reference alone or in combination with any of the '937 Reference or the '495 Reference or the '021 Reference or

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	the '596 Reference or the '297 Reference or the '1182. Specifically, one of ordinary skill in the art would know to use one X-decoder for each subarray as part of the operation described in the '994 Reference. [*See* Page 3; Page 4, first column; Figs. 1 and 5] Further, the use of a plurality of decoders is well known in the prior art. The following are illustrative: The '937 Reference teaches the use of a plurality of decoders as well as the use of a single decoder for performing the same function. [Figs. 3 and 5] The '937 Reference states: "The address counter 81 receives the signals $\emptyset_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $\emptyset_{EV}$ (i.e., twice that of the basic clock pulses $\emptyset_S$). Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $\emptyset_{OD}$ to supply odd address signals to a Y decoder 93 in the cycle of the signals $\emptyset_{OD}$ (i.e., twice that of the basic clock pulses $\emptyset_S$). Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42] "The latch (see FIG. 6) forming the delay latch circuit 106 fetches the outputs from the X decoder 82 on the leading edges of the clock pulses $\emptyset_L$, and hence the delay latch circuit 106 delays the outputs from the X decoder 82 respectively by one cycle of the basic clock pulses $\emptyset_S$ to

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	transfer the same to the second memory cell array 94. . . . It is to be noted that odd address cycles are always delayed from the even address cycles respectively by one cycle of the basic clock pulses $Ø_S$. Thus, this embodiment is equivalent in operation to that shown in FIG. 3" ['937 Reference, Col. 7:44-63] The '495 Reference states: "The output of the block decoder 50 is supplied in common to the row decoders 20a and 20d and the column decoders 40a and 40d. As a result, one word line is selected in the memory cell array block 10a, for example." ['495 Reference, Col. 3:39-42] The '021 Reference states: "In FIG. 1, numeral 100 designates clock signals to be supplied to the interleave controller 20, the select controller 30 and the high-speed memory access controller 40, numerals 111, 112, 113, 114 designate output data from the low-speed large-capacity memories 11, 12, 13, 14 respectively, numeral 120 designates an address signal to be supplied to the interleave controller 20, numerals 121, 122, 123, 124 designate address signals from the interleave controller 20 to the low-speed large-capacity memories 11, 12, 13, 14 respectively, ..." ['021 Reference, Col. 3:43-68] Each memory 11, 12, 13, and 14 would have a decoder for receiving an address from interleave controller 20. The '596 Reference states: "Memory blocks 10_1, 10_2, ..., 10_n include row decoders 12_1, 12_2, ...,12_n, sense amplifiers 14_1, 14_2, ..., 14_n and column decoders 16_1, 16_2, ...,

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	16_n,respectively." ['596 Reference, Col. 2:62-65] The '297 Reference states: "In FIG. 6, which illustrates a first embodiment of the boundary-free semiconductor memory device, memory cells are divided into n rows x m columns of memory cell blocks B_{00}, B_{01}, . . ., B_{0n-1},; B_{10}, B_{11}, . . ., $B_{1,m-1}$; $B_{n-1,0}$, $B_{n-1,1}$, . . . , $B_{n-1,m-1}$. n number of same row selecting circuits RD0, RD1, . . ., and RD_{n-1} are provided commonly for each row of memory cell blocks, . . ." ['297 Reference, 7:8-15]. the '1182 Reference states that: "The row address decoders R-DCR1 and R-DCR2 decipher the above-mentioned address signals x0-xm and form the selection signals of the word line, are synchronized to the word line selection timing signals Φx1 and Φx2, and perform the selection operation of a one word line of the memory arrays M-ARY 1 and M-ARY 2 and dummy word line. ['1182 Reference, Page 3, first column]
one X-register for each X-decoder;	This element is met in the '994 Reference alone or in combination with any of the '937 Reference or the '495 Reference" or the '021 Reference. Specifically, one of ordinary skill in the art would know to use one X-register for each X-decoder to perform the operation described in the '994 Reference. [*See* Page 3; Page 4, first column; Figs. 1 and 5] The '937 Reference states:

CLAIM	RESPONSE
	"The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42] The '495 Reference states: "The register 70a, 70b, 70c or 70d selected by the block decoder 50 holds 8-bit address codes ARC0-ARC7 supplied in synchronism with the row selection signal RAS. Since the holding of the address codes ARC0-ARC7 will be maintained even after access is shifted to another cell array block, these registers 70a-70d store respectively the address codes ARC0-ARC7 of the last access in the cell array blocks 10a-10d and supply them to the selectors 80a-80d which also receive the address codes ARC0-ARC7 supplied in synchronism with the row selection signal RAS and introduce them to the row decoders 20a-20d." ['495 Reference, Col. 4:25-37] The '021 Reference states: "Since the low-speed large-capacity memories 11, 12, 13, 14 performing the 4-way interleave operation are shifted in access timing usually by one cycle from each other, the memories 11 14 are provided respectively with

CLAIM	RESPONSE
	registers 23 26 each for holding an address." ['021 Reference, Col. 4:5-9]
one Y-decoder for each subarray;	This element is met in the '994 Reference alone or in combination with the '196 Reference or the '937 Reference or the '596 Reference or the '297 Reference or the '1182 Reference. Specifically, one of ordinary skill in the art would know to use one Y-decoder for each subarray to perform the operation described in the '994 Reference. [*See* Page 3; Page 4, first column; Figs. 1 and 5] The '196 Reference states that: "Referring now to FIGS. 2A and 2B, there is shown a block schematic diagram of a pair of RAM arrays 31, 33, each comprising a plurality of individual memory cells of the type illustrated and described above with reference to FIGS. 1A and 1B. Each of these arrays may be configured to store data in a matrix of rows and columsn [sic] that is several columns long and several rows deep (e.g. 72X128). The columns and rows of memory cells in each array are connected to decoders for writing and reading data into and out of selected memory cells in the arrays. Specifically, the write column decoders 35, 37 are connected to the dual arrays to address selected columns of memory cells, and the write row decoders and drivers 39, 41 are connected to the dual arrays to address selected rows of memory cells. Similarly, the read column decoders 45,47 are connected to the dual arrays to address selected columns of memory cells , and the read row decoders and drivers 49, 51 are connected to the dual arrays to address selected rows." ['196 Reference, Col. 3:11-29; See also FIGS 1A, 1B, 2A]

CLAIM	RESPONSE
	"Similarly, the data which is to be read out from the RAM arrays 31, 33 is designated in selected 9-column segments by the column predecoders 61 which, in turn, is selected by the read pointer counters 63. The columns thus addressed may extend over both arrays, where each column is uniquely addressable, and the arrays alternate when the boundary of column addresses for a given array is reached, as previously described." ['196 Reference, Col. 4:5-12] The '937 Reference states: "The address counter 81 receives the signals $\emptyset_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $\emptyset_{EV}$ (i.e., twice that of the basic clock pulses $\emptyset_S$). Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $\emptyset_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $\emptyset_{OD}$ (i.e., twice that of the basic clock pulses $\emptyset_S$). Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42] The '596 Reference states: "Memory blocks 10_1, 10_2, ..., 10_n include row decoders 12_1, 12_2, ...,12_n, sense amplifiers 14_1, 14_2, ..., 14_n and column decoders 16_1, 16_2, ..., 16_n,respectively." ['596 Reference, Col. 2:62-65]

CLAIM	RESPONSE
	the '297 Reference states that: ". . . as illustrated in FIG. 10, memory cells are provided at every other intersection of a pair of bit lines and word lines on one side of each sense amplifier SA. Note that the sense amplifier SA of FIG. 10 is comprised of p-channel transistors between a line PSA and bit lines BL0 and BL0, and N-channel transistors between a line NSA and bit lines BL0 and $\overline{BL0}$, and when the lines PSA and NSA are made high and low, respectively, the sense amplifier SA is operated. Also, in FIG. 9, the row decoder RD_i selects one word line from 256 word lines $WL_{i,0}$, $WL_{i,1}$, . . . , and $WL_{i,225}$, while the column decoder CD_j selects two pairs of bit lines such as BL0 and BL0; and BL1 and $\overline{BL1}$ by the column selection signals $CD_{j,0}$, $CD_{j,1}$, . . . , and $CD_{j,127}$ thereof, and connects them to data buses $DB_{ij,0}$ and $\overline{DB}_{ij,0}$; $DB_{ij,1}$ and $\overline{DB}_{ij,1}$ within the block, and further, one pair of the two paires of the data buses $DB_{ij,0}$ and $\overline{DB}_{ij,0}$; $DB_{ij,1}$ and $\overline{DB}_{ij,1}$ within the block is selected by a switch S_{ij} and is connected to block data buses BDB_{ij} and $\overline{BDB}_{ij}$." ['297 Reference, 8:26-45]. See also, '297 Reference, 13:48-14:14, 14:59-15:7, FIGs. 9, 10, 23. The '1182 Reference states: "In addition, the center is a column decoder C-DCR, and here is one pair of common complementary data lines CD1 and CD2 that run in the vertical direction left and right. As a result, column switching circuits C-SW1 and C-SW2 that connect the complementary data lines connect the

CLAIM	RESPONSE
	complementary data lines and the common data lines that correspond to the addresses." ['1182 Reference, Page 2, second column] "The main amplifiers MA 1, MA 2 are in an operative state in accordance with the timing signals Φ ma1 and Φ ma2, and they perform the operation of amplification of signals that have been read to the common complementary data lines CD1, CD2." ['1182 Reference, Page 3, second column]
one Y-register for each Y-decoder;	This element is met by the '994 Reference alone or in combination with the '196 Reference or the '937 Reference or the '596 Reference. Specifically, one of ordinary skill in the art would know to use one Y-register for each Y-decoder to perform the operation described in the '994 Reference. [*See* Page 3; Page 4, first column; Figs. 1 and 5] The '196 Reference states that: "The row and column location in the arrays 31, 33 at which data is accessed is controlled by the counters which, in one embodiment of the invention may be binary counters, or the like, which have an extended counting range that is double the number of address locations in the array to be accessed." ['196 Reference, Col. 4:49-55; See also, FIGS. 2A, 2B] Further, one of ordinary skill in the art would know that the counters shown are, or can be, implemented through the use of a register. The '937 Reference states that:

CLAIM	RESPONSE
	"The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e. twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. Ina similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e. twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42] the '596 Reference states: "Similarly, column address 38 is given as follows. Column address buffer 40 receives an address signal input from the external terminal as an initial value. The initial value is counted up or down by column address counter 42 in response to a serial access control signal input from control circuit 36. Therefore, column address 38 is given." ['596 Reference, Col. 3:41-47] "In addition, a shift register is arranged in the column direction, so that higher-speed serial access can be performed in the column direction." ['596 Reference, Col. 6:15-17] *See also* '596 Reference, Col. 2:55-5:12; Claims 1, 4 and 5.
one Y-select circuit for each subarray, the Y-select	This element is met in the '994 Reference alone or in combination with

CLAIM	RESPONSE
circuit being responsive to the Y-decoder of the subarray to select all the columns that occupy a selected position in the groups of the subarray;	the '196 Reference or the '937 Reference or the '596 Reference or the '297 Reference or the '1182 Reference. Specifically, one of ordinary skill in the art would know to use one Y-select circuit for each subarray was used to select all the columns that occupy a selected position in the groups of subarrays to perform the operation described in the '994 Reference. [*See* Page 3; Page 4, First Column; Figs. 1 and 5] The '196 Reference states that: "Referring now to FIGS. 2A and 2B, there is shown a block schematic diagram of a pair of RAM arrays 31, 33, each comprising a plurality of individual memory cells of the type illustrated and described above with reference to FIGS. 1A and 1B. Each of these arrays may be configured to store data in a matrix of rows and columsn [sic] that is several columns long and several rows deep (e.g. 72X128). The columns and rows of memory cells in each array are connected to decoders for writing and reading data into and out of selected memory cells in the arrays. Specifically, the write column decoders 35, 37 are connected to the dual arrays to address selected columns of memory cells, and the write row decoders and drivers 39, 41 are connected to the dual arrays to address selected rows of memory cells. Similarly, the read column decoders 45,47 are connected to the dual arrays to address selected columns of memory cells , and the read row decoders and drivers 49, 51 are connected to the dual arrays to address selected rows." ['196 Reference, Col. 3:11-29; See also FIGS 1A, 1B, 2A] "Similarly, the data which is to be read out from the RAM arrays 31, 33 is